APPLICATION NOTE PRD-06933

CAPACITANCE RATIO AND PARASITIC TURN-ON

This application note describes the impact of capacitance ratio on parasitic turn-on for Wolfspeed Gen 3 MOSFETs. It provides the guidance for users to evaluate the influence that capacitance ratio and other application variables will have on safe operation.

CONTENTS

1. INTRODUCTION

SiC MOSFET technology advances the capabilities of many power electronics applications by offering a faster switching solution than conventional power semiconductors. Faster switching can lead to higher efficiency through lower switching losses. It can also allow for smaller converter sizes as it can utilize smaller magnetics when switching at higher frequencies.

An important consideration when introducing fast switching into an application is the impact of switching transients on system stray parasitics. An example of this, which will be covered in this application note, is when the fast voltage gradients of SiC MOSFETs interact with the device input capacitances which can lead to parasitic turn-on events.

2. PARASITIC TURN-ON (PTO)

Parasitic turn-on is an event that occurs when a fast dv/dt causes a power transistor to turn on despite the commanded off state. The voltage switching transient (dv/dt) induces a current through the input and reverse transfer capacitances of the device and causes the gate voltage to increase. If this gate voltage increases above the threshold voltage of the device, there is risk of the device turning on, which is a "parasitic turn-on." When in half-bridge configuration, if a PTO occurs with substantially high gate voltage, both devices end up conducting which can lead to a shoot-through failure. Therefore, it is recommended to avoid parasitic turn-on.

PTO is not isolated to SiC MOSFETs but they are particularly susceptible due to their ability to switch at fast speeds. The faster the dv/dt, the larger the increase in gate voltage. Figure 1 shows more information about the mechanism for PTO occurring in an application when the devices are oriented in a half-bridge configuration.

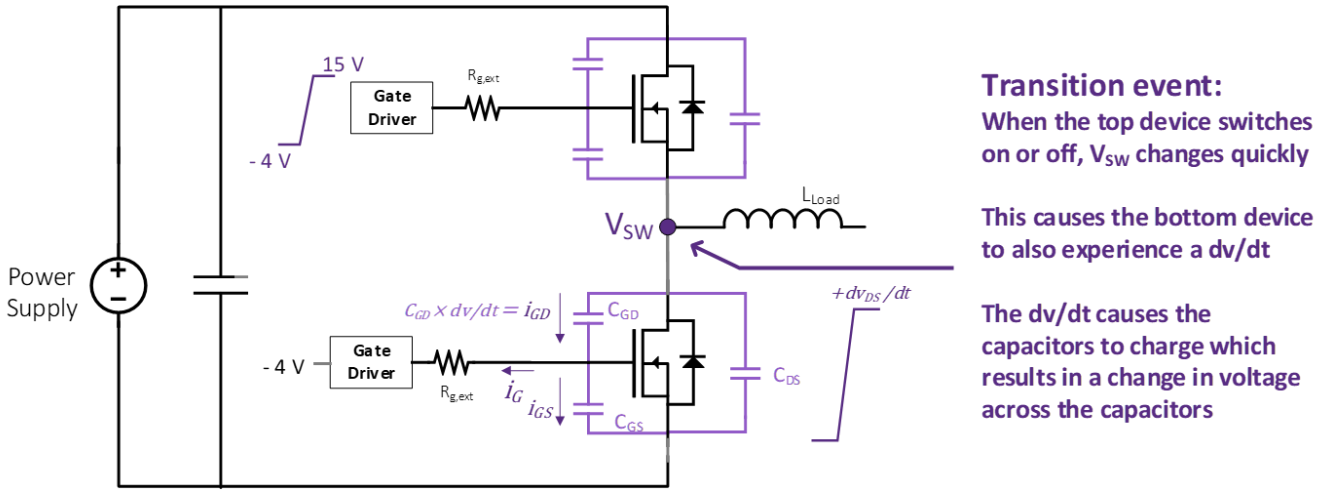


Figure 1: Example circuit showing how a parasitic turn-on can occur

When the top device in the figure switches on, its drain-source voltage quickly decreases which causes a large negative dv/dt as the top device switches from blocking to conducting. Even though the bottom device is being held off, it still experiences a positive dv/dt from the top device and a current flows through the Miller capacitor of the bottom device (C_{GD}). This current then charges up the gate to source capacitor of the bottom device (C_{GS}) and causes a voltage increase on the gate of the bottom device.

A similar effect occurs when the top device is turned off (both situations are summarized in Figure 2). A fast negative dv/dt causes a current to flow in the opposite direction in the device capacitances. In this case, a negative voltage spike is seen on the gate of the bottom device. This negative gate voltage peak can violate the absolute maximum datasheet limits and cause unexpected stresses on the gate oxide of the device. This application note will focus on the positive gate increase and its impact on the parasitic turn-on of the device.

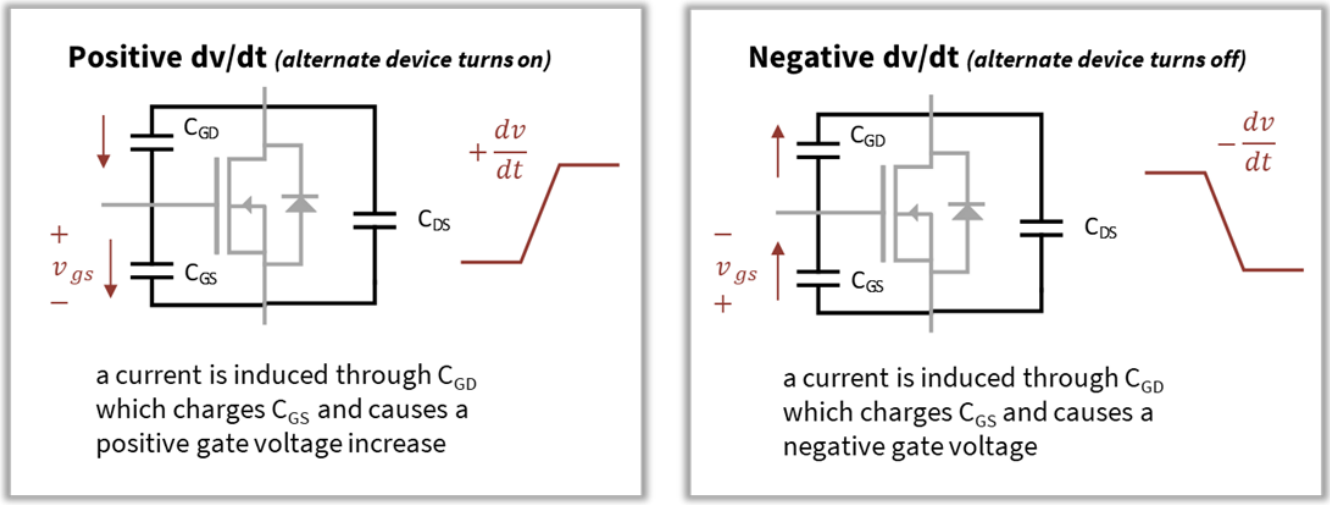


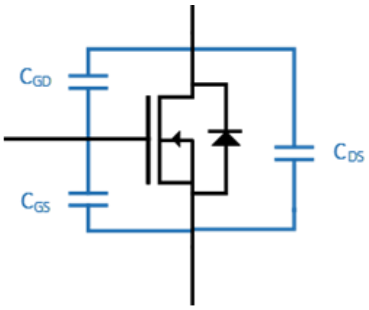
Figure 2: Impact of positive and negative dv/dt

There are some common considerations for reducing the chances of parasitic turn-on events due to fast voltage switching transients. One option is to choose a device with a higher threshold voltage. This would provide additional margin for gate voltage peaks to increase without exceeding the threshold voltage. Another option is to decrease the switching speed (reduce drain-source dv/dt), which would decrease the voltage peak seen at the gate. While these methods have both been shown to work in decreasing the occurrence of parasitic turn-on, they can also lead to higher switching losses in the system.

Evaluating a device's capacitance ratio is one way to determine how susceptible the device is to a parasitic turn-on event, as shown in the next section. Other application methods can also be used to mitigate the risk of parasitic turn-on events, which will be discussed in Section 4.

3. CAPACITANCE RATIO

The capacitance ratio, as shown in
Figure 3, is the ratio between C_{GS} and C_{GD}. The equation can also be defined in terms of C_{iss} and C_{rss} which are the input capacitance (C_{GS} + C_{GD}) and the Miller capacitance (C_{GD}) respectively. C_{iss} and C_{rss} are common measurements performed on SiC MOSFETs and can be found on most device datasheets. Figure 4 shows how Wolfspeed reports the device capacitance information on the datasheet in both the datasheet parameter list and in the figures section. [1]



$$Capacitance\ Ratio = \frac{C_{GS}}{C_{GD}} = \frac{C_{iss}}{C_{rss}} - 1$$

Figure 3: Description of the capacitance ratio

The table shown in Figure 4 gives the capacitance values of the device at a single drain-source voltage level. As seen in the graph, the capacitances are not linear. This is due to the depletion region of the device getting wider when a larger voltage potential is across it, which causes the capacitance to decrease. While the capacitance ratio is a quick check to verify the susceptibility of the device to parasitic turn-on, it is also important to account for the impact of the non-linearity of the capacitances. This is described in more detail below.

C_{iss}	Input Capacitance		6200		pF	V_{GS} = 0 V, V_{DS} = 1000 V f = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		220				
C_{rss}	Reverse Transfer Capacitance		13				
E_{oss}	C_{oss} Stored Energy		126		µJ		Fig. 16

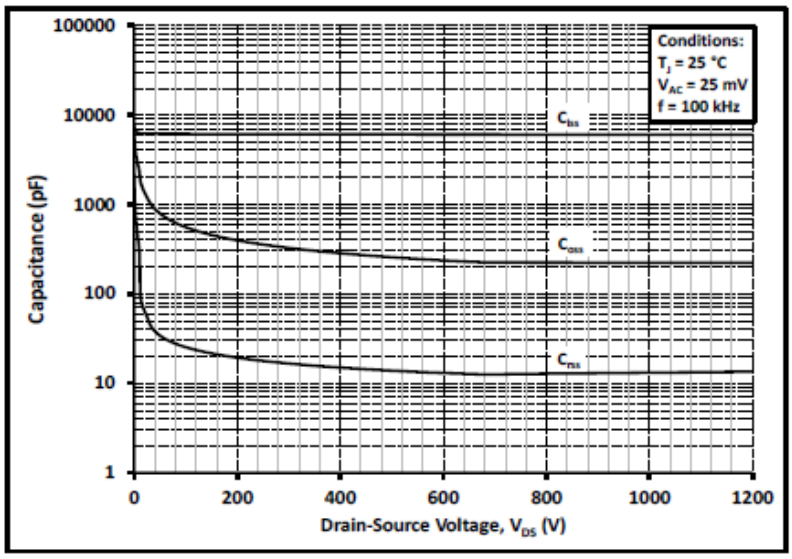


Figure 4: Wolfspeed device capacitances on the datasheet for the EPM3-1200-0017D

As described in the previous section, when the device experiences a large dv/dt, a current flows through the $C_{GD.}$ This current then flows to the C_{GS}, which starts to charge up. The larger the capacitance of $C_{GD,}$ the more current which is flowing ($I_{GD} = C_{GD} \cdot \frac{dv}{dt}$). If C_{GS} is also large, then more charge is needed to increase the gate voltage of the device. Therefore, the capacitance ratio is an important metric for determining how susceptible a device will be to parasitic turn-on. Having a device with a higher capacitance ratio (larger C_{GS} in comparison to the C_{GD}) is preferred.

A method for estimating the potential V_{GS} peak voltage for a device that accounts for the non-linearity of the device capacitances (by looking at the capacitance ratio at each voltage level) can be approximated by using the equation:

$$dv_{GS} = \frac{C_{GD}}{C_{GS}} \cdot dv_{DS}$$

This equation is derived using the current flow through the input capacitances and by assuming the gate driver is not sinking any current. This equation expresses the expected increase in the gate voltage over the same time that the drain-to-source voltage is changing. This is a worst-case scenario assumption, because in actual applications some of the current will also flow to the gate driver which decreases the current going to the $C_{GS.}$ [2]

Figure 5 shows the estimated V_{GS} peak voltages for three different Wolfspeed devices with different capacitance ratios. The equation described above was used along with the capacitance curves (see Figure 4 as an example of the capacitance curves) of the devices to calculate these values. The V_{GS} does not rise as much for the device with the higher capacitance ratio. These curves are based on the recommended V_{GS} of -4 V for Generation 3 devices. Since the device capacitances are not linear, the largest increase in gate voltage occurs at the lower ΔV_{DS}. As the ΔV_{DS} increases, the increase in gate voltage becomes more consistent.

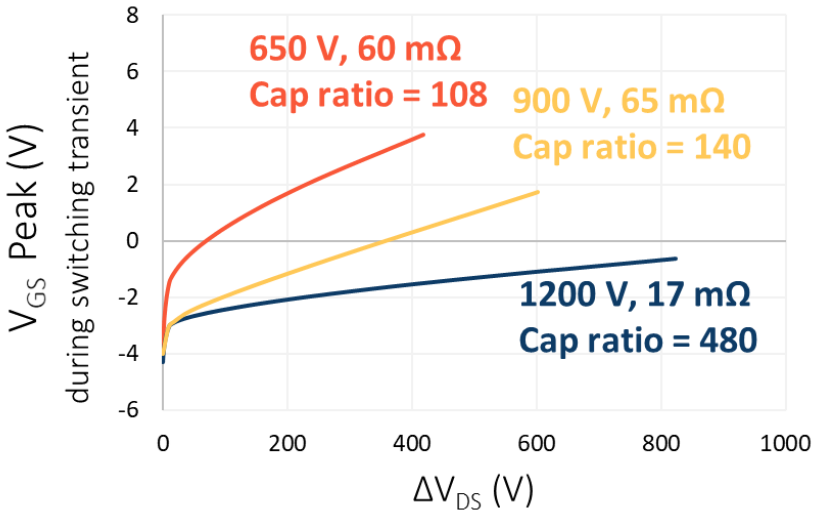


Figure 5: Graph showing the impact of different capacitance ratios on the peak VGS during switching events for Wolfspeed Generation 3 devices

The gate voltage increase of the devices with a higher capacitance ratio does not surpass the threshold voltage of the device (≈ 2.5 V). By using a device with a higher capacitance ratio, there is a lower chance of causing a parasitic turn-on without having to compromise the fast switching capability of the device.
The estimations in Figure 5 were verified by testing packaged devices in a half-bridge configuration. The device under test was switched at different V_{DS} levels and the resulting increase in gate voltage was measured and plotted. Figure 6 shows the results from these tests. To get the largest increase in V_{GS}, the devices in this test were also subjected to aggressive dv/dt's which ranged from 30 V/ns at the lower voltage level to 120 V/ns at the 400 V point.

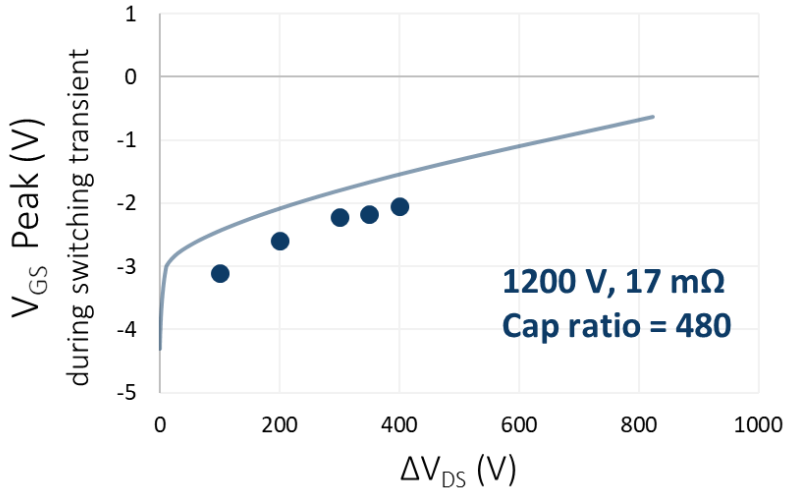


Figure 6: Switching tests results at different V_{DS} levels with the resulting VGS peak for the EPM3-1200-0017 die

4. OTHER FACTORS THAT INFLUENCE PARASITIC TURN-ON

There are other factors in an application that can influence the probability and severity of parasitic turn-on. These factors will be discussed in the following section using simulated examples.

The simulations are run using a simulation model for the 1200 V, 17 mΩ device, which was also featured in the previous sections of this paper. These simulations are run in LTSpice using Wolfspeed's LTspice models. The circuit used is a clamped inductive load half-bridge circuit with a dual gate driver set-up. The simulation circuit also includes typical parasitics (ex. stray inductances, resistance values) extracted from Wolfspeed's test setup to allow the simulation to closely follow typical operation of the device in actual applications.

Gate resistance

As discussed before, slowing down the switching of the device can also decrease the negative gate voltage peaks. This happens because the dv/dt decreases as the switching is slowed. The most common way to slow down the switching speed is by increasing the gate resistance. Figure 7 shows the impact of the V_{GS} peak value when tested with different gate resistances (for both the device under test and the complementary switch) which confirms the decrease in peak V_{GS} when the switching is slowed. Although increasing the gate resistance decreases the amount of gate voltage peak, it also increases the switching losses, which is less desirable.

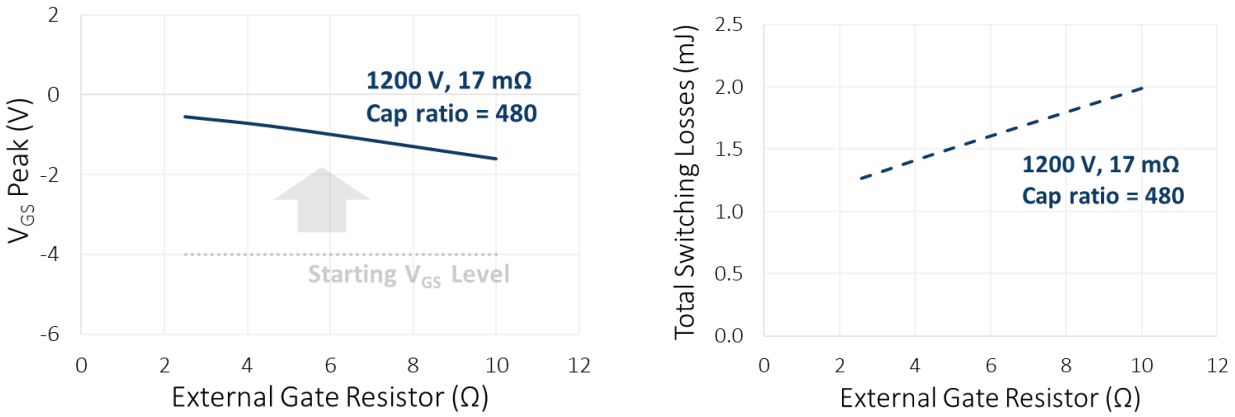


Figure 7: Impact of Gate Resistance on negative gate voltage peak (solid line) and switching losses (dotted line)

One factor to remember is that if the gate resistance is increased, the gate current from the gate driver could decrease, which would make the C_{GS} discharge time take longer. This longer discharge of the gate capacitance can lead to the device being more susceptible to PTO. Other gate driver parameters that can have a similar impact are the gate driver current capability/impedance and gate loop inductance.

Temperature

Threshold voltage has a negative temperature coefficient, so it is important to verify the impact that temperature has on the gate voltage increase during switching transitions. As can be seen in Figure 8, as the temperature increases, the V_{GS} peak decreases. This relationship occurs because as the temperature increases, the dv/dt decreases under the same test conditions. When revisiting the following equation: $I_{GD} =$

$C_{GD} \cdot \frac{dv}{dt}$, the lower the dv/dt at the higher temperatures causes the current and the V_{GS} peak to be lower as well. Therefore, even though the threshold voltage will be slightly lower at higher temperatures, the decrease in dv/dt should help counteract this.

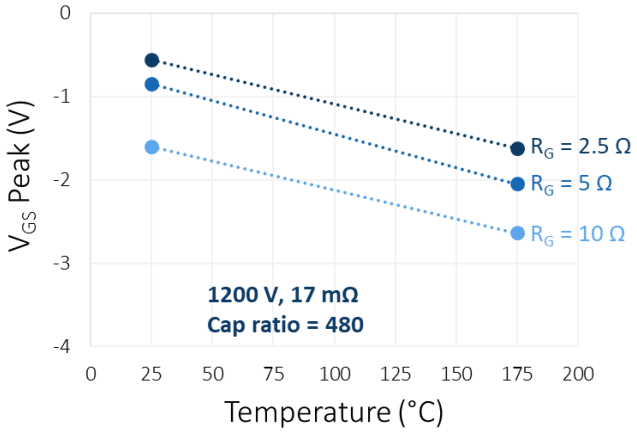


Figure 8: V_{GS} peak for different temperatures and gate resistances

Negative gate drive voltage

Figure 9 shows the results where the device is held at a few different gate voltage levels. As expected, lower gate voltages produce a lower peak. Because of the fast switching of SiC MOSFETs, most applications use a negative gate drive voltage to lower the risk of parasitic turn-on.

For the 0 V gate voltage case, the peak gate voltage gets up to slightly over 2 V which is still under the threshold voltage of the device of 2.5 V. As shown in the transfer characteristics curve below, there is still some leniency if the gate voltage gets above the threshold voltage. Even though there is some current flowing, the specified threshold voltage for a device is usually reported at the mA level so the device doesn't get into a high current conduction mode until the gate voltage is a few volts higher than that.

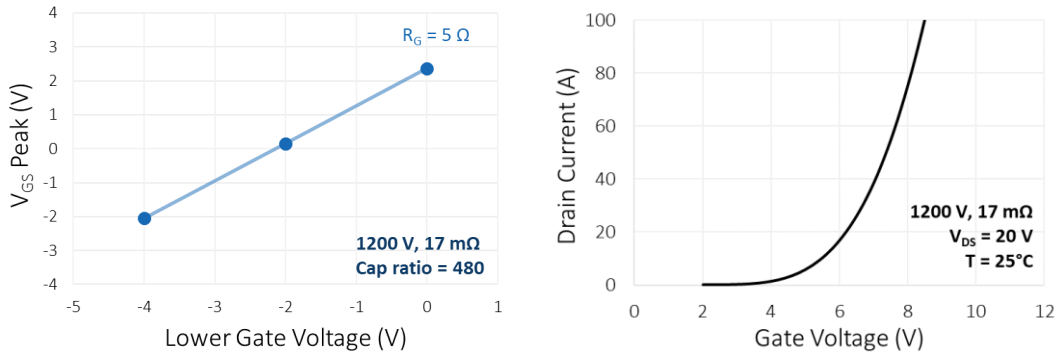


Figure 9: Impact of the negative gate voltage on the maximum peak V_{GS} voltage and the transfer characteristic curve

Gate capacitance

In Section 3, it is discussed that the change in V_{GS} is determined by the capacitance ratio of the MOSFET as given by the below equation. In addition to internal C_{GS}, if an external C_{GS} is added, the equivalent C_{GS} would be higher (artificially increasing the capacitance ratio) and hence the gate voltage increase (dv_{GS}) will be lower.

$$dv_{GS} = \frac{C_{GD}}{C_{GS}} \cdot dv_{DS}$$

It is important to note that this condition is applicable when the time it takes for V_{DS} to switch (dv/dt time) is much smaller than the time constant due to gate resistance and capacitance forming an RC circuit. The graphs in Figure 10 below show that by adding the external C_{GS}, the dV_{GS} is lower as the equation suggests, however the time duration of dv_{GS} rise is higher. With adding external C_{GS}, if the V_{GS} peak value is still greater than the threshold voltage, the system is more susceptible to parasitic turn-on since the time duration for dV_{GS} rise is also higher.

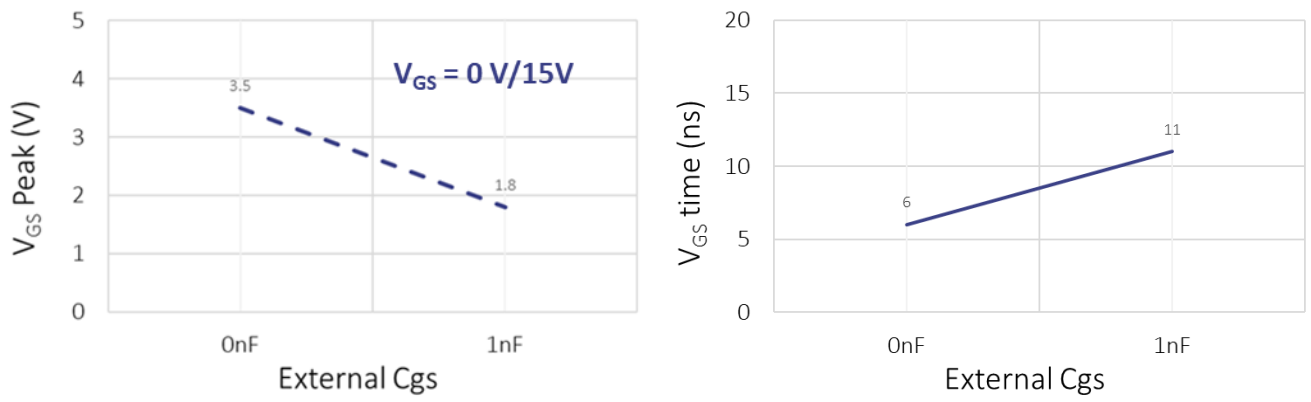


Figure 10: Comparison of the external C_{GS} on the V_{GS} peak voltage and time for the C3M0032120K device with 0 V negative gate voltage

Miller clamp

The addition of a Miller clamp in the gate driver circuitry helps to prevent parasitic turn-on by creating a low-inductance path to hold the device to the negative gate voltage level. Normally, the current from C_{GD} would charge C_{GS} and cause a gate voltage spike; instead, the Miller clamp mitigates this by sinking that current through the gate driver circuitry. Figure 11 shows a comparison of the same simulation configuration except one includes a Miller clamp and the other does not. There is a clear improvement when using a Miller clamp to help reduce the gate peak voltage. The Miller clamp results also show that there is not a large dependence on the external gate resistor because the Miller clamp bypasses the external gate resistance during the off state.

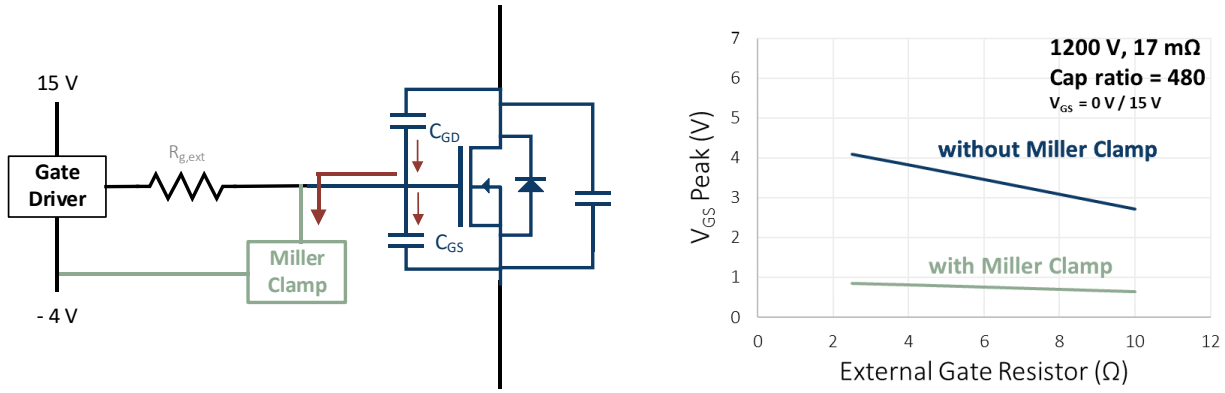


Figure 11: Comparison of the Miller clamp on the V_{GS} peak voltage

The main challenge with using a Miller clamp is that its success hinges on having a low-inductance path to the die, which becomes difficult at the power module level. The longer the path to the Miller clamp is, the less effective it becomes at diverting the current which can make it impractical to use for power modules without special considerations. [3]

The figure below shows some additional testing beyond the simulations on a discrete packaged device (C3M0032120K). The measurements are taken under two conditions - all parameters are the same except one is with an active Miller clamp and the other is without an active Miller clamp. It is confirmed that the gate voltage increases above the threshold voltage in the case without an active Miller clamp, however it is not trivial to determine whether any parasitic turn-on occurs.

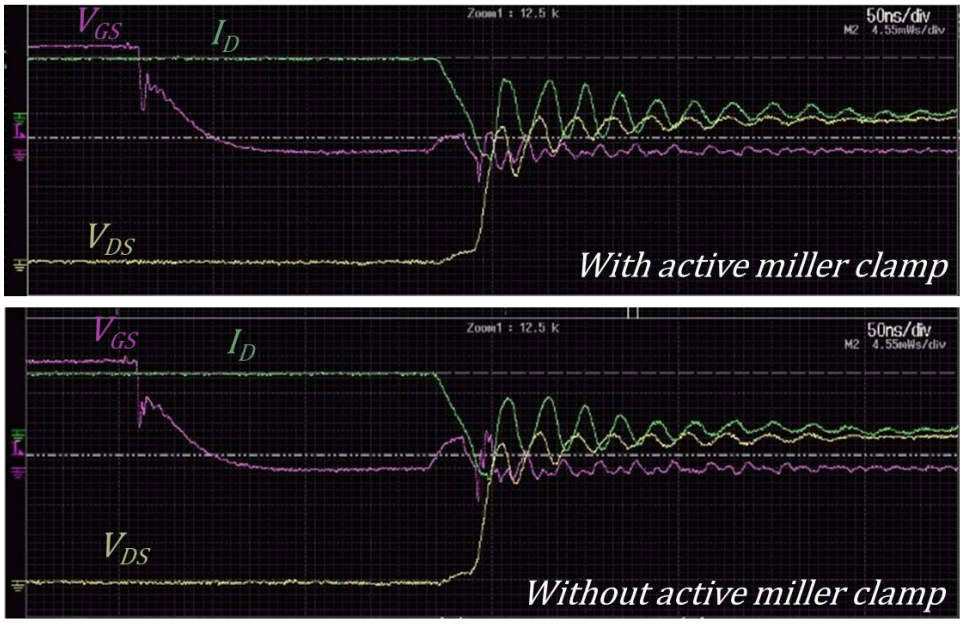


Figure 12: a) With active Miller clamp, b) Without active Miller clamp

5. METHOD TO IDENTIFY PARASITIC TURN-ON

In the actual application it can be difficult to differentiate parasitic turn-on current from body diode reverse recovery current. If parasitic turn-on current occurs, it is superimposed on the body diode reverse recovery current. One way to differentiate and estimate the PTO current from the MOSFET current waveform is by comparing the device currents to a known reference condition in which no PTO occurs. If the current waveforms in these conditions overlap each other except when PTO occurs, the difference provides an estimate of PTO current.

Figure 13 below shows another example of test measurement under two conditions - all parameters are the same except one is taken with a Miller clamp and the other is taken without a Miller clamp.

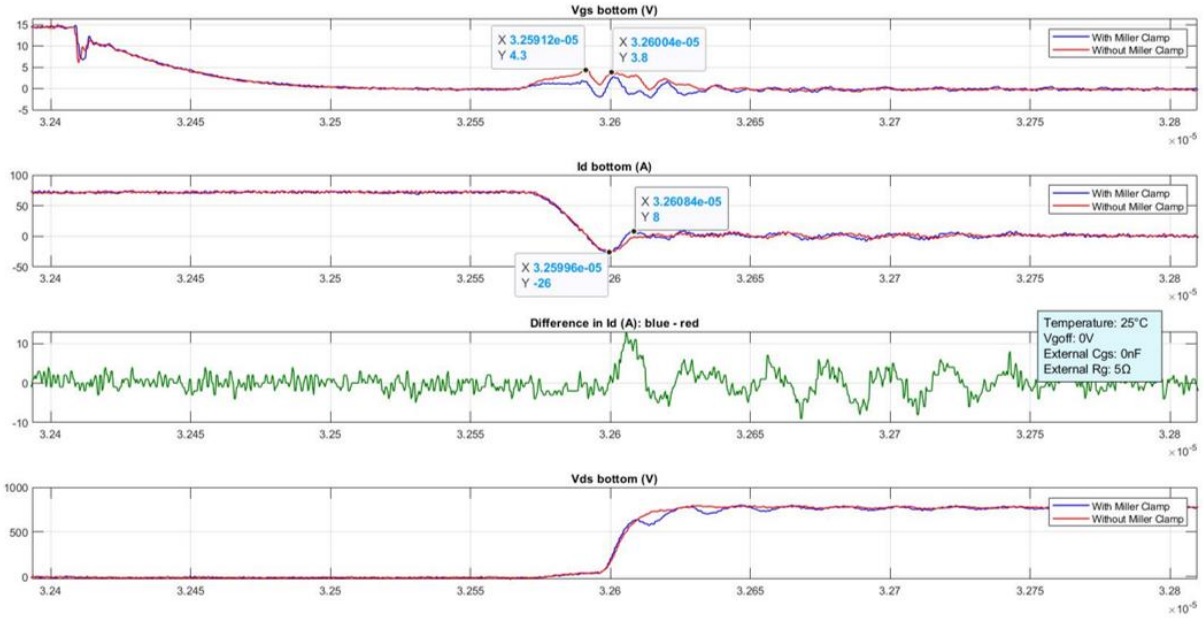


Figure 13: Test measurements and waveforms to analyze PTO current

By comparing the device current waveforms without a Miller clamp (red) and with a Miller clamp (blue), it is seen that they perfectly overlap except during PTO. Thus, the difference in current values (in green) provides an estimate of PTO current when not using a Miller clamp under these test conditions. This method can also be used to understand the impact of a certain design parameters on PTO.

6. CONCLUSION

This app note has summarized what causes a parasitic turn-on event and how to use the capacitances of a device to determine how well a device can withstand large voltage transients without risk of a false turn-on. The impact of gate resistance, temperature, negative gate drive voltage and Miller clamp on the V_{GS} peak was also investigated. Although there were different application parameters that could be changed to decrease the negative peak gate voltage, the most significant parameter is the capacitance ratio of the device. This is a parameter that can easily be calculated using the device datasheet.

REFERENCES

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[2] K. Sobe, T. Basler and B. Klobucar, "Characterization of the parasitic turn-on behavior of discrete CoolSiC™ MOSFETs," *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2019, pp. 1-7.

[3] D. Martin, W. A. Curbow and T. McNutt, "Performance analysis of a SiC MOSFET half bridge power module with a Miller clamp," *2017 IEEE International Workshop On Integrated Power Packaging (IWIPP)*, 2017, pp. 1-5, doi: 10.1109/IWIPP.2017.7936765.

[4] MOSFET Self-Turn-On Phenomenon, Application Note: 2017 – 2018 Toshiba Electronic Devices & Storage Corporation.