Wolfspeed

APPLICATION NOTE PRD-06752

PCB LAYOUT TECHNIQUES FOR DISCRETE SiC MOSFETs

APPLICATION NOTE

ABSTRACT

With the ongoing advancement of power electronic systems, the demand for higher efficiency and power density in applications like solar power inverters, energy storage systems (ESS), uninterruptible power supplies (UPS) and electric vehicles (EV) is on the rise. Silicon carbide (SiC)-based systems leverage SiC's superior switching characteristics coupled with low conduction losses to enable higher switching frequency than possible with silicon (Si), meeting demands of more efficient and power-dense systems with simpler thermal management solutions.

However, the high voltage slew rates (dv/dt) and current slew rates (di/dt) inherent to SiC power devices make these circuits more sensitive to crosstalk, false turn-on, parasitic resonances, and electromagnetic interference (EMI) than their silicon counterparts. This document discusses these challenges and presents general layout guidelines to handle them while designing a PCB for SiC-based systems. In addition to that, this document also discusses coordination of insulation with practical examples, an essential knowledge for engineers dealing with PCB design of power electronics systems.

This document is structured in three sections as follows:

- Device level: Discussion about discrete SiC MOSFET packages and how to ensure creepage/ clearance at a device level
- Sub-circuit level: Challenges of a SiC gate drive and instructions on the layout of an optimized SiC gate drive and switching cell
- System level: Guidelines for PCB layer stack, importance of component placement, impact of layout on cooling, and common thermal solutions for SMDs

CONTENTS

SECTION 1: DEVICE LEVEL

This section introduces Wolfspeed's discrete SiC MOSFET packages and briefly discusses benefits of packages with a Kelvin source pin. In addition, this section discusses creepage and clearance distance at the device level with some practical examples to ensure sufficient creepage.

1.1 Introduction to Discrete SiC MOSFET Packages

Discrete SiC MOSFET packages offered by Wolfspeed are shown in Figure 1. As mentioned previously, higher slew rates (dv/dt and di/dt) are inherent to SiC MOSFETs. In Figure 2 , it can be seen that the high-side switch is a TO-247-3 package and the low-side switch is a TO-247-4 package with Kelvin source (KS) pin. For the high side, source inductance (L_{S1}) in the gate driver loop will limit the switching speed; in the low side, a separate KS pin for gate driver loop is present. $V_{G,KS}$ is not affected by the voltage drop in the source inductance (L_{S2}) introduced by the di/dt of the drain-source current. Hence, for SiC MOSFET packages with KS pin, switching speed is not limited by source inductance resulting in lower switching losses. Refer to the test results as shown in Figure 3, with the same die at the same test conditions, showing the switching loss of the devices in different packages.

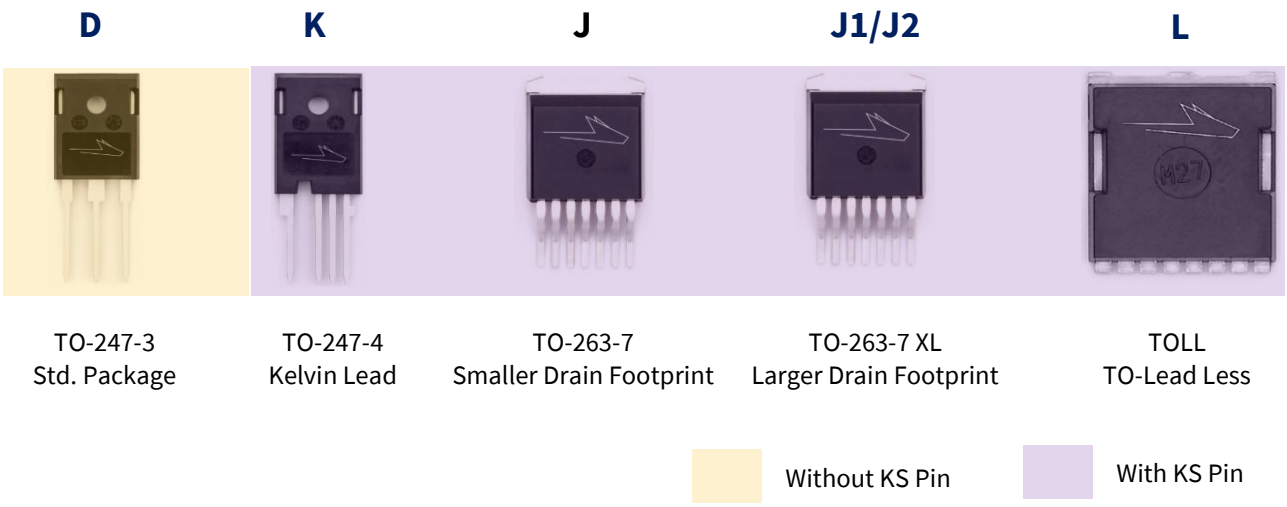


Figure 1 : Discrete SiC MOSFET packages

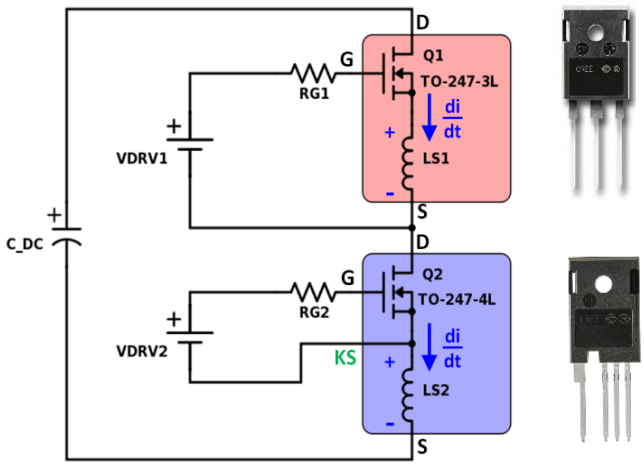


Figure 2 : Half-bridge circuit with TO-247-3 package in high side and TO-247-4 package in low side

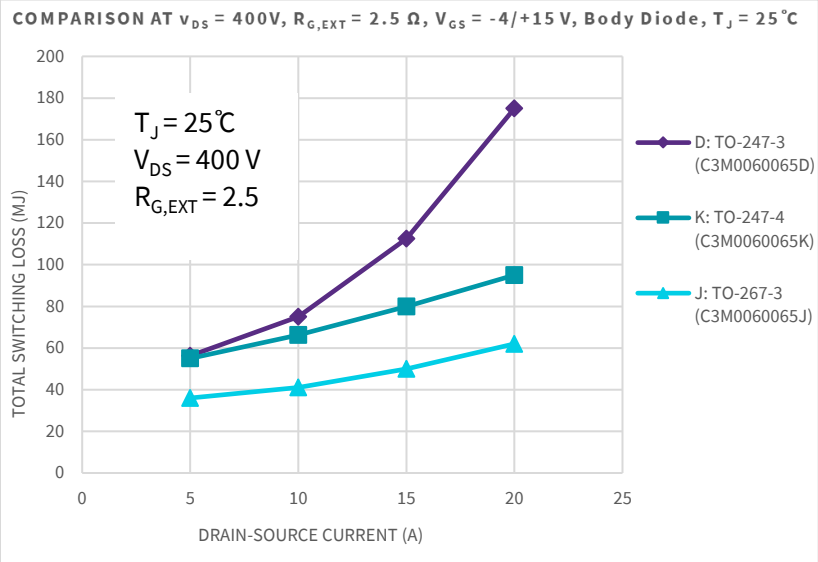


Figure 3 : Comparison at VDS = 400V, RG, EXT = 2.5 Ω, VGS = -4/+15 V, Body Diode, TJ = 25 ℃

1.2 Introduction to Creepage and Clearance Distances

The distance between components that is required to withstand a certain voltage is specified in terms of clearance and creepage. A visual representation of the distinction between these terms is shown in Figure 4.

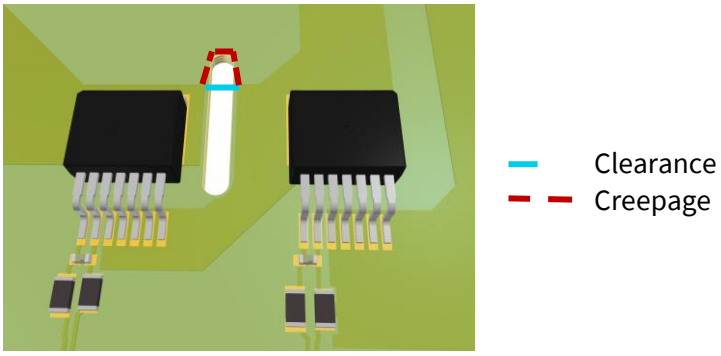


Figure 4 : Distinction between creepage and clearance

Clearance is distance in air between two conductive parts. The determining factors for this are the highest peak voltage present and the dielectric strength of the ambient air. Main factors affecting clearance:

- Temporary over voltages or recurring peak voltages
- Degree of pollution (humidity, dust deposition)
- Type of isolation
- Installation altitude (affects dielectric strength of surrounding air due to decreasing air pressure)

Creepage distance is the shortest distance between two conductors along the surface of a solid insulating material. The damaging effect of creepage currents is a long process and hence, effective value of applied

voltage is critical (and not its peak value). The minimum creepage should at least equal the clearance. Main factors affecting creepage:

- Working voltage
- Degree of pollution (humidity, dust deposition)
- Material properties (CTI)
- Type of isolation

1.3 Introduction to PCB Spacing Requirements

A proper clearance and creepage distance between MOSFET legs/ PCB traces is important to avoid flashover or tracking between them. As will be seen in section 4, a variety of safety standards prescribe different spacing requirements depending on the voltage, application and other factors. But besides safety standards, IPC standards can also be used as a guideline whose aim is to standardize the assembly and production requirements of electronic equipment/assemblies. It is to be noted that all IPC documents are voluntarily rather than mandatory [1]. The following standards can be applied:

- IPC- 2221 Generic Standard on Printed Board Design
- IPC 9592 Performance Parameters for Power Conversion Devices

The image below shows Table 6-1 from the IPC-2221 standards. These values list minimum conductor spacing as a function of the voltage between the two conductors [1]. For example, as per IPC 2221, for a DC-link voltage of 850 V, the minimum spacing between drain and source PCB traces of the MOSFET is 2.6 mm (considering category B4).

Table 6-1 Electrical Conductor Spacing

Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]
16-30	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.25 mm [0.00984 in]	0.13 mm [0.00512 in]
31-50	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	0.6 mm [0.024 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.4 mm [0.016 in]	0.13 mm [0.00512 in]
51-100	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	1.5 mm [0.0591 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.5 mm [0.020 in]	0.13 mm [0.00512 in]
101-150	0.2 mm [0.0079 in]	0.6 mm [0.024 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
151-170	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
171-250	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	6.4 mm [0.252 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
251-300	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	12.5 mm [0.4921 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]
301-500	0.25 mm [0.00984 in]	2.5 mm [0.0984 in]	12.5 mm [0.4921 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]	1.5 mm [0.0591 in]	0.8 mm [0.031 in]
> 500 See para. 6.3 for calc.	0.0025 mm /volt	0.005 mm /volt	0.025 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt

B1 - Internal Conductors
B2 - External Conductors, uncoated, sea level to 3050 m [10,007 feet]
B3 - External Conductors, uncoated, over 3050 m [10,007 feet]
B4 - External Conductors, with permanent polymer coating (any elevation)
A5 - External Conductors, with conformal coating over assembly (any elevation)
A6 - External Component lead/termination, uncoated, sea level to 3050 m [10,007 feet]
A7 - External Component lead termination, with conformal coating (any elevation)

Figure 5 : Electrical conductor spacing as per IPC 2221

IPC-9592 provides a standard spacing requirement for power conversion equipment used in the computer and telecom industries. For spacing between PCB traces (uninsulated conductors/ external PCB layers), IPC-9592 recommends

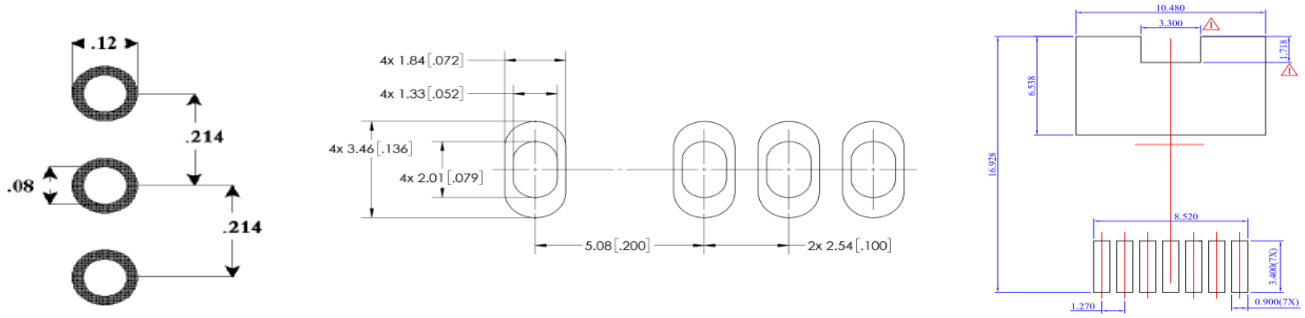
- 0.13 mm for V<15V,
- 0.25 mm for 15 V≤V<30 V and
- 0.1+Vpeak×0.01 for 30 V ≤ V < 100 V
- SPACING (mm) = 0.6 + Vpeak x .005 for V ≥ 100 V

For example, for a DC-link voltage of 850 V, the minimum spacing between the drain and source PCB traces of the MOSFET is 4.85 mm. In addition, a thumb rule of 10 mils for 50 V can also be used as a general guideline to estimate minimum spacing between conductors on a PCB.

1.4 Designing for Sufficient Creepage

1.4.1 Creepage on PCB

Figure 6 shows the recommended solder pad layout for different Wolfspeed discrete SiC MOSFET packages. TO-247-4 and TO-267-7 offer larger creepage compared to the TO-247-3 package. As recommended in Wolfspeed's datasheets, design pads with an elliptical shape are preferred. This increases creepage distance as compared to circular solder pads and also reduces the possibility of solder bridging between pads (source-source pads or gate-source pads) during soldering process. Rectangular shapes should be avoided so as not to introduce the electrical field edge effect on the pad corners. Designers should also be careful not to reduce the pad area too much and leave part of the metallization pad uncovered.



TO-247-3 TO-247-4 TO-267-7

Figure 6 : Recommended solder pad layout for Wolfspeed's discrete SiC MOSFETs

Creepage distance between drain and source pads can be estimated as discussed above and slots can be added in the PCB to attain required creepage if required (see Figure 7). As per IEC 60664-1, minimum slot width is 0.25 mm (pollution degree 1) and 1 mm (pollution degree 2). In addition to ensuring sufficient creepage between drain and source solder pads/pins of the MOSFET, care should be taken to ensure sufficient creepage between circuits/ components connected to drain and source pads with a similar high potential (e.g., snubber circuits).

Electrical breakdowns between the plated through hole and the inner ground layer can occur [2]. Hence, care should also be taken to increase the distance between the inner ground layer and the plated through hole. In addition, the power components can be moved to areas where they are not located above the mass inner layer.

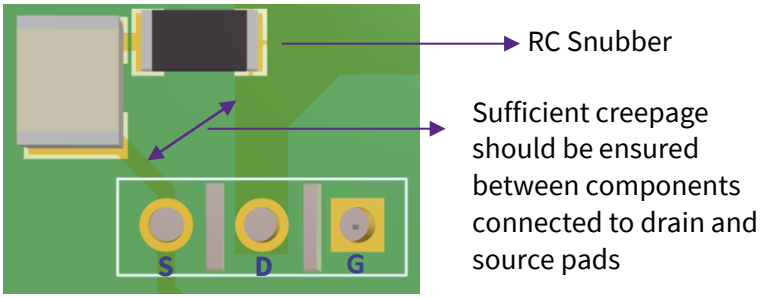


Figure 7 : Ensuring sufficient creepage distance between circuits connected to drain and source pads of MOSFET

1.4.2 Creepage between MOSFET and Heatsink

For the through-hole packages, depending how they are mounted on the heatsink, special care should be taken to ensure that there is sufficient space between drain/ source terminal and the heatsink as shown in Figure 8.

For vertical mounting shown in (a), clearance and creepage distances can be increased by extending the isolation foil size. In a solar application, heatsinks are large and mechanically fixed to chassis, and therefore horizontal mounting shown in (b) is quite common in these applications. Extending the isolation pad slightly over the bent of the terminals can increase creepage in this case. Sometimes, owing to different shapes of chassis, the terminals must be bent at an angle as shown in (c). Here, the isolation pad can be extended to increase spacing between terminals and heatsink. Subfigure (d) shows a situation where the terminals must be bent in the lower direction; in this situation, cutting the heatsink as shown can increase the distance between terminals and heatsink. While doing so, it should be kept in mind that the heatsink should be cut few mm after the copper frame on the device backside, otherwise the edge of the heatsink might cut the Sil-Pad. For SMD packages, solder pads should be designed as per the applicable datasheet's recommendation.

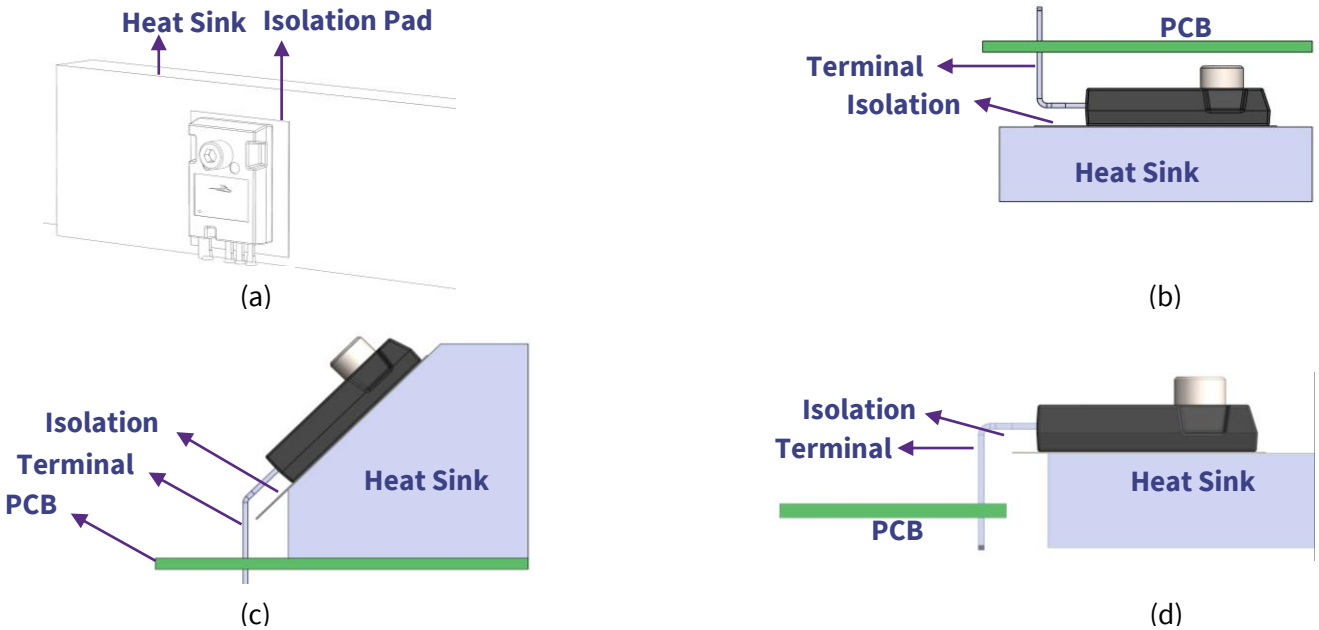


Figure 8 : Examples of increased spacing between MOSFET terminals and heatsink

SECTION 2: SUB-CIRCUIT LEVEL

This section discusses specific layout challenges that a SiC gate drive entails and provides guidelines to overcome these challenges with practical examples. This section also discusses the effect of parasitics of a switching cell and presents PCB design guidelines for an optimized switching cell.

2.1 Gate Drive

Gate drive is used to turn a power semiconductor ON and OFF. As can be seen in Figure 9, a gate loop is a switched resonant circuit with gate voltage (V_G), gate resistance (R), gate loop inductance (L) and, gate capacitance (C_{GS}). As can be noted from Equation 1, the characteristic equation of a gate loop is a second order equation and hence, depending on different elements, oscillations and overshoots might occur at gate. Oscillations at gate can be controlled with a higher damping, and damping is directly proportional to gate resistance and inversely proportional to gate loop inductance (Equation 2). Hence, it can be seen that a low inductive gate loop enables higher damping without compromising on the slew rates.

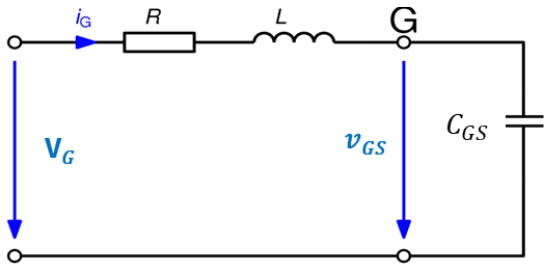


Figure 9 : Switched resonant circuit of a gate drive

$$\frac{d^2 v_{GS}}{dt^2} + 2 \cdot \delta \frac{dv_{GS}}{dt} + \omega_o^2 \cdot v_{GS} = \frac{1}{C_{GS} \cdot L} \cdot V_G$$ *Equation 1, Characteristic equation of a gate loop*

$$\delta = \frac{R}{2L}$$ *Equation 2, Damping Coefficient*

$$\omega_o = \frac{1}{\sqrt{(C_{GS} \cdot L)}}$$ *Equation 3, Resonant Frequency*

Further, to show the importance of low inductive gate loop, a simulation of gate loop as a RLC circuit applied to Wolfspeed's C3M0021120K is provided. Gate capacitance (C_{iss}) is taken as 4.8 nF and high inductive gate loop is assumed with an estimated inductance of 30 nH (estimated for ~2 inches of trace). The simulation is performed with a varied gate resistor as shown in Figure 10. It can be clearly seen that a high inductive gate loop can only be controlled by sacrificing switching speed and efficiency by increasing gate resistor.

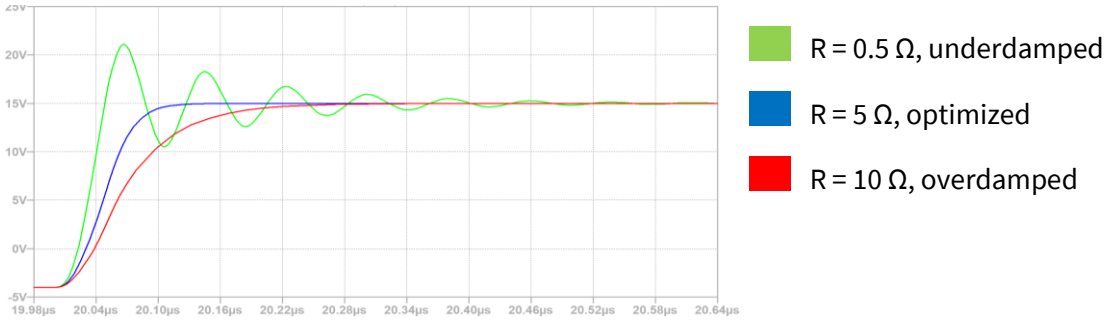


Figure 10 : Simulation of gate loop

2.2 Challenges of SiC Gate Drive

As mentioned before, higher slew rates (dv/dt and di/dt) are inherent to SiC MOSFETs. Higher slew rates coupled with parasitic capacitances (C_{GD}, C_{GS}) and loop inductance (power and gate loop) make circuits more sensitive to crosstalk, false turn-on, voltage overshoots, ringing and potential EMI issues. While designing PCB layout for a SiC gate drive, it is important to ensure following:

- Compact gate loop: 'Compact' means a low-inductive gate loop, and as previously discussed, this can result in increased damping for same gate resistance and hence, less oscillatory gate voltage. In addition, a compact gate loop means a smaller gate loop area, which makes gate drive less susceptible to external magnetic fields (e.g., high magnetic fields of power magnetics).
- Minimize parasitic capacitances: Parasitic capacitances coupled with high dv/dt can result in crosstalk, false turn-on and increasing switching losses. It is important to ensure that one does not add external parasitic capacitances while designing the PCB layout.
- Minimize effects of higher slew rates: Higher slew rates are inevitable in SiC systems. So, in addition to ensuring an optimized gate loop from the point of view of loop inductance and parasitic capacitance, certain countermeasures can be taken in PCB layout to minimize the impacts of high electric and magnetic fields.

2.3 An Optimized Gate Drive

As discussed above, while designing PCB layout for a SiC gate drive, there are certain challenges that should be dealt with utmost care. Some of these critical points and guidelines to handle them are discussed here.

2.3.1 Compact Gate Loop

An example of an optimized gate loop is shown in Figure 11. It can be seen that a compact gate loop is achieved by having the gate driver IC as close to the SiC MOSFET as possible. In addition, the loop of active miller clamp is minimized by connecting the AMC pin of the driver IC and the gate terminal of the SiC MOSFET with a short trace. In addition, it is recommended to place an external gate-source capacitor and resistor as close to the SiC MOSFET as possible. But it is to be noted here that a gate-source capacitor is only applicable for packages with KS pin and Wolfspeed does not recommend an external gate-source capacitor for TO-247-3. Gate-source resistor (typically 10 kΩ) is critical to discharge the gate in case the MOSFET is disconnected from driver. Without this, false turn-on may occur to the MOSFET.

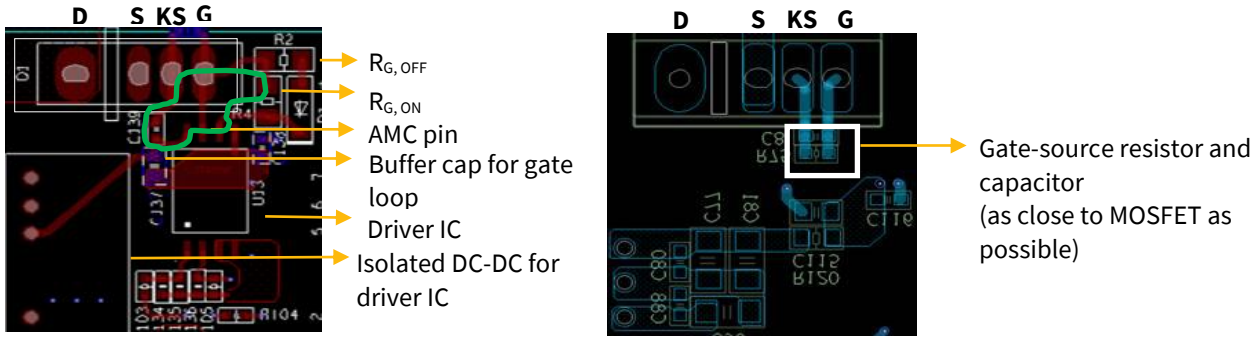
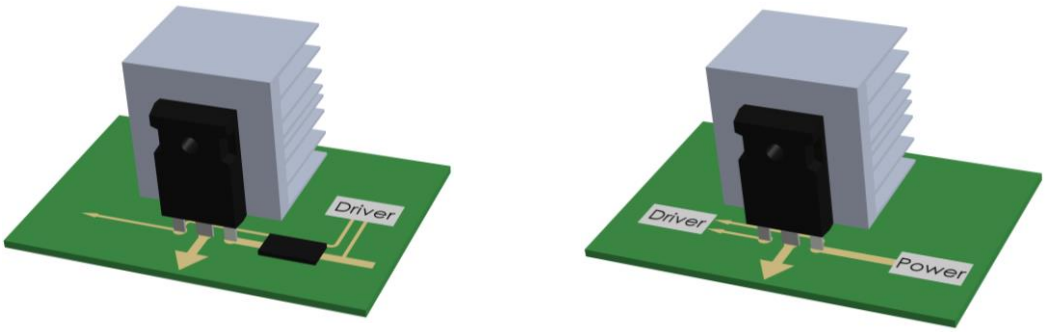


Figure 11 : Practical example of a compact gate loop, top layer (left) and bottom layer (right)

2.3.2 Separate Routing of Gate Drive Return and Power Source (Critical for TO-247-3)

Another point that is critical, especially for the TO-247-3 package, is to ensure that the gate drive return and power source are separated as shown in Figure 12 (b). As shown in Figure 12(a), the high current slope in the power source introduces a voltage across parasitic inductance which may reduce effective gate voltage, reducing switching speed and increasing switching losses. E.g., 15 mm long, 3 mm wide shared trace has an inductance of 8 nH. So, if for a di/dt slope of 250 A/us, the slope can induce a voltage drop of 2 V *(V = L*di/dt = 8 nH * 250 A/us = 2 V)* across shared parasitic inductance. This will reduce effective gate voltage by 2 V and slow down switching. Hence, packages with a KS pin are a better choice.



(a) Gate drive return and power source share common return

(b) Gate drive and power source return separated

Figure 12 : Routing of gate drive return and power source for TO-247-3

2.3.3 Shielding of Gate Loop

In addition to a low inductive gate loop, steps should be taken to minimize the impact of higher slew rates. Shielding of sensitive gate signals from high magnetic fields (caused due to high di/dt) is important to ensure proper operation of the gate drive. As an example, if signals and gate drive circuit are routed on the top layer (as shown in Figure 13), then mid layer-1 underneath this area should be a ground plane connected to the source of the corresponding device. This ground plane ensures:

- Shielding for sensitive signals of gate drive circuit, and
- Shortest possible return paths for gate drive signals to reduce loop area and parasitic loop inductance

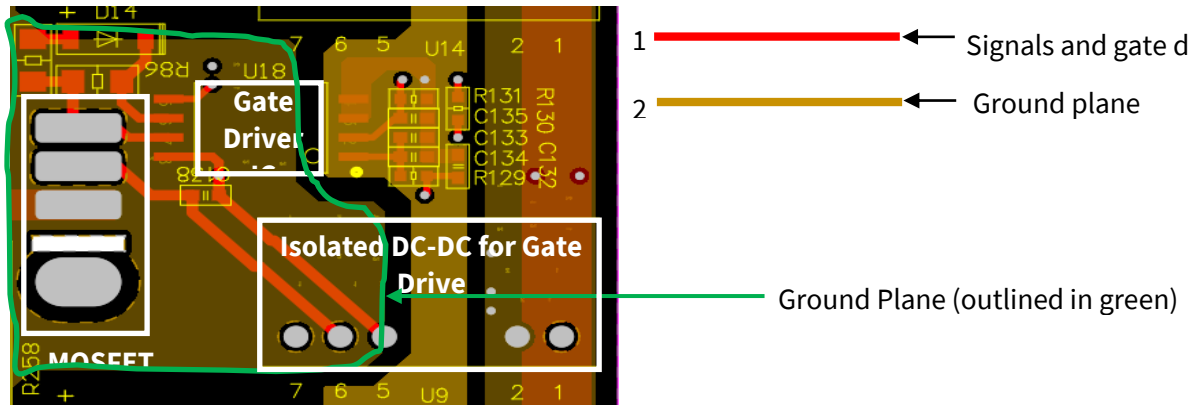


Figure 13 : Shielding of gate loop

2.3.4 Minimize Overlapping of Gate Loop and Power Loop

Overlapping of gate loop and power loop can add external parasitic capacitance (C_{GD}) to the gate loop. This external parasitic capacitance can lead to increased Q_{GD} and hence, higher switching losses. Figure 14 shows the effects of external parasitic capacitance on the system. It is extremely important to lay out gate loop (as well as the power loop) in a way to minimize this overlapping.

Increased Switching Losses	• External parasitic capacitance can lead to increased Q_{GD} • This can result in higher switching losses
Enhanced Cross Talk	• External parasitic capacitance results in larger ratio between C_{GD} and C_{GS} • This can enhance cross talk and result in a shoot through
Potential EMI Issues	• External parasitic capacitance couples with gate loop inductance, results in gate voltage ringing • This could create potential radiated EMI issues
Impact Reliability	• Such ringing can cause MOSFET to switch several times at high frequency instead of one clean transition, causing device failure at high voltage/currents
Impacts Maximum Efficiency	• For an 800 V, hard switching application at 100 kHz, 0.01 sq.mm (d = 0.1m, FR4 PCB) drain and gate trace overlap, C = 38 pF and power loss, $P_C = C \cdot V^2 \cdot f$ = 1.2W

Figure 14 : Impact of external parasitic capacitance

Overlap between the gate loop and power loop can be minimized with proper component placement as shown in Figure 15. In addition, high dv/dt traces (e.g., switching node) should be kept small and only wide enough to carry the required current. This will minimize capacitance between adjacent conductive planes at critical switching nodes.

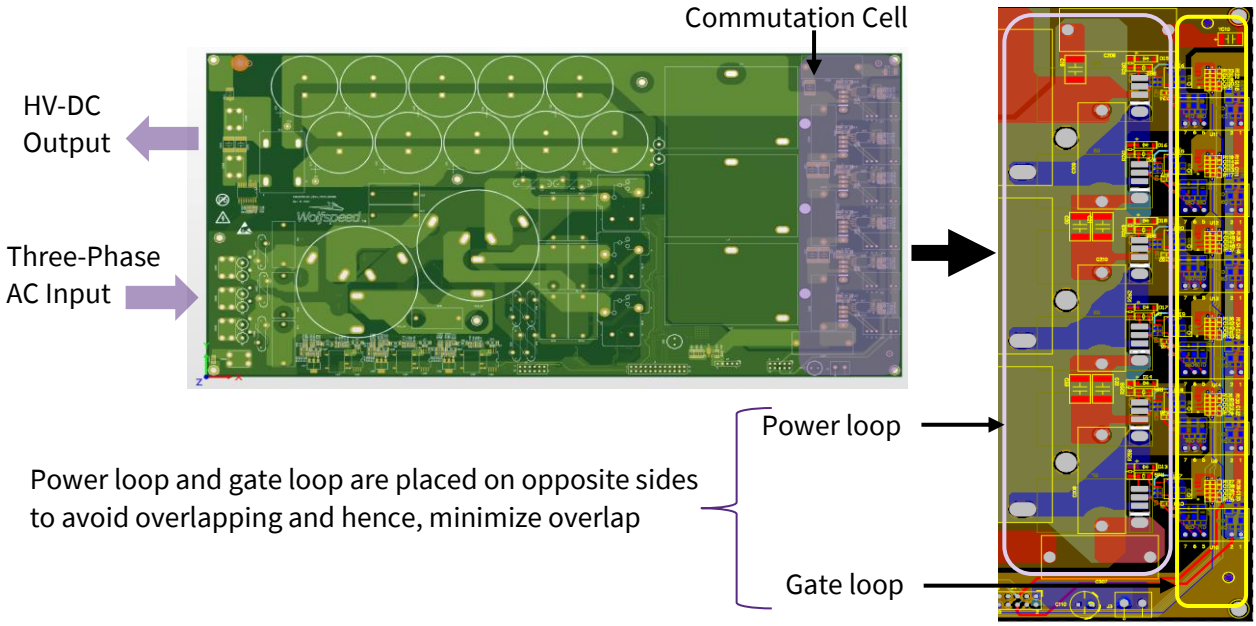
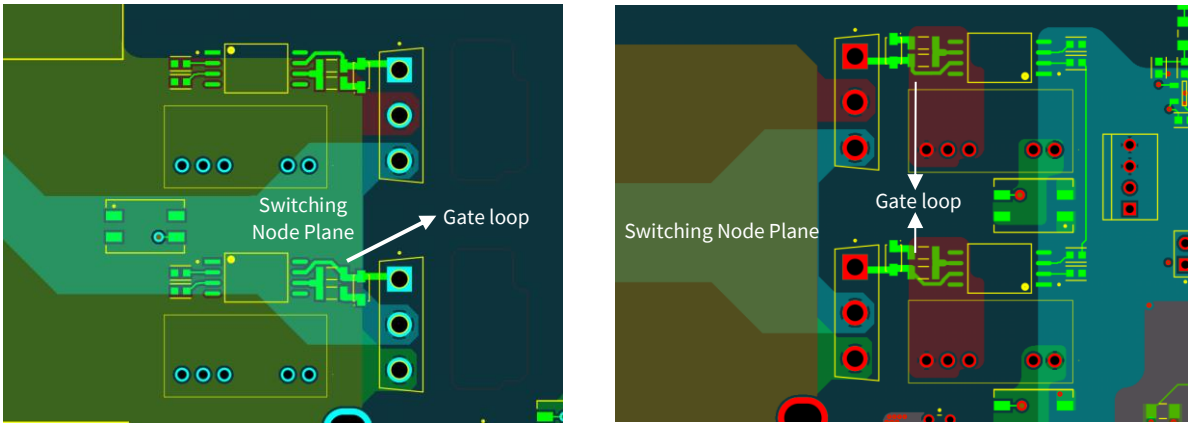


Figure 15 : 'Good' layout example to minimize overlap between power and gate loop (Wolfspeed's Active Front End Reference Design)



(a) (b)

Figure 16 : (a)'Bad' layout example with overlap between power and gate loop (b)'Good' layout example with no overlap between power and gate loop

Figure 16 (a) and (b) shows a PCB layout example of a half-bridge based on a TO-247-3 MOSFET. Figure 16 (a) shows a 'bad' layout practice wherein there is extensive overlap between the gate loop of low side MOSFET and switching node plane. This can lead to issues like cross talk, gate ringing, and potential EMI problems. Figure 16 (b) shows a 'good' layout practice wherein, overlap between power loop and gate loop is avoided by routing them on different sides of MOSFET.

2.3.5 Gate Loop Considerations with Parallel MOSFETs

In many applications, a single MOSFET might not be enough to carry the required current, which poses a demand for paralleling of MOSFETs in order to reduce the conduction losses as well as reduce the operating temperature and improve the efficiency of a power converter.

To ensure good current sharing among paralleled MOSFETs, it is critical to ensure symmetrical gate voltages. This can be achieved if the gate and source return paths from gate driver IC to each MOSFET is symmetrical. To achieve this, place the gate driver IC at the center of both gate terminals and not in the middle of both MOSFETs. The length of the gate and kelvin source traces (as shown in Figure 17) for both MOSFETs should be same. In addition to the gate resistor, it is highly recommended to have resistors in the source return path as well. This limits current arising due to unidentical source inductances.

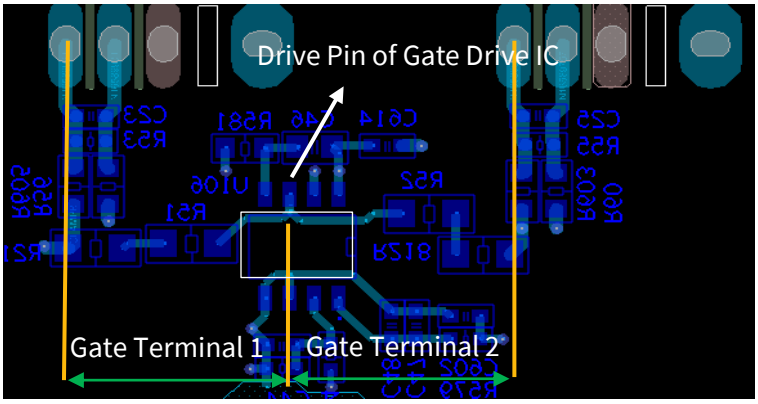


Figure 17 : Gate drive layout of two parallel MOSFETs

From the perspective of the power loop, in order to ensure good current sharing among paralleled MOSFETs, it is critical to ensure that the power current path through each MOSFET is similar in length. For this, minimize and balance stray inductance at the drain and source.

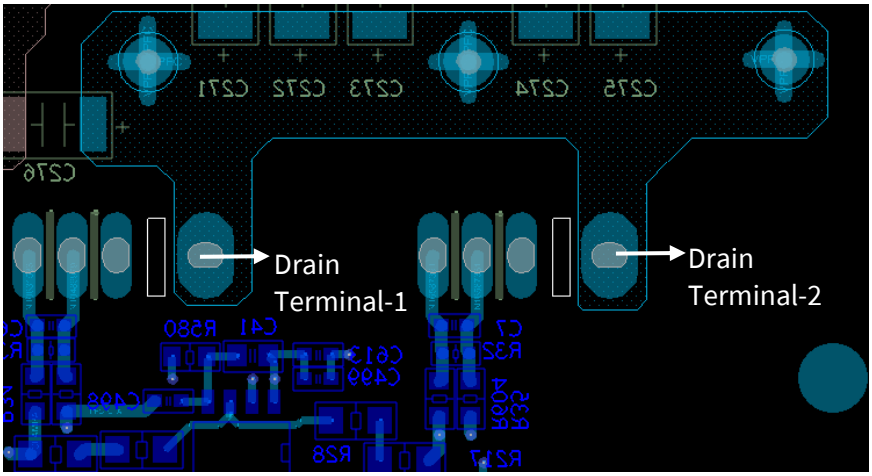


Figure 18: Power loop layout of two parallel MOSFETs

2.4 Switching Cell

2.4.1 Design Goals of an Optimized Switching Cell

Figure 19 shows a SiC MOSFET switching cell. A switching cell is characterized by high frequency di/dt and hence, is a source of strong magnetic field. DC-link inductance of switching cell results in voltage overshoots at turn-off. It also couples with output capacitance of SiC MOSFET, resulting in ringing and potential EMI issues.

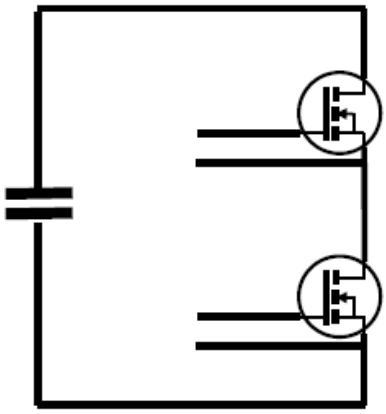


Figure 19 : SiC MOSFET switching cell

Design goals of a switching cell can be listed as follows:

- Small current loop
- Low DC-link inductance

Design goals of a switching cell can be achieved by:

- Placing ceramic or film capacitors as close as possible to the SiC MOSFET
- Proper PCB layout of the power components to minimize commutation loop
- Overlap power planes (DC+ and DC-) in switching cell
- Distribute power planes (DC+ and DC-) on multiple layers of PCB
- No overlap between drain and gate/source traces (as discussed in Section 2.3.4)

Figure 20 shows a practical example of an optimized switching cell with Wolfspeed's TO-263-7 MOSFET. It can be seen that DC-link inductance and high frequency di/dt loop of the switching cell is minimized with an optimized component placement, placing ceramic capacitors close to MOSFETs, and by overlapping DC+ (blue colored plane) and DC- (red colored plane) power planes in the switching cell.

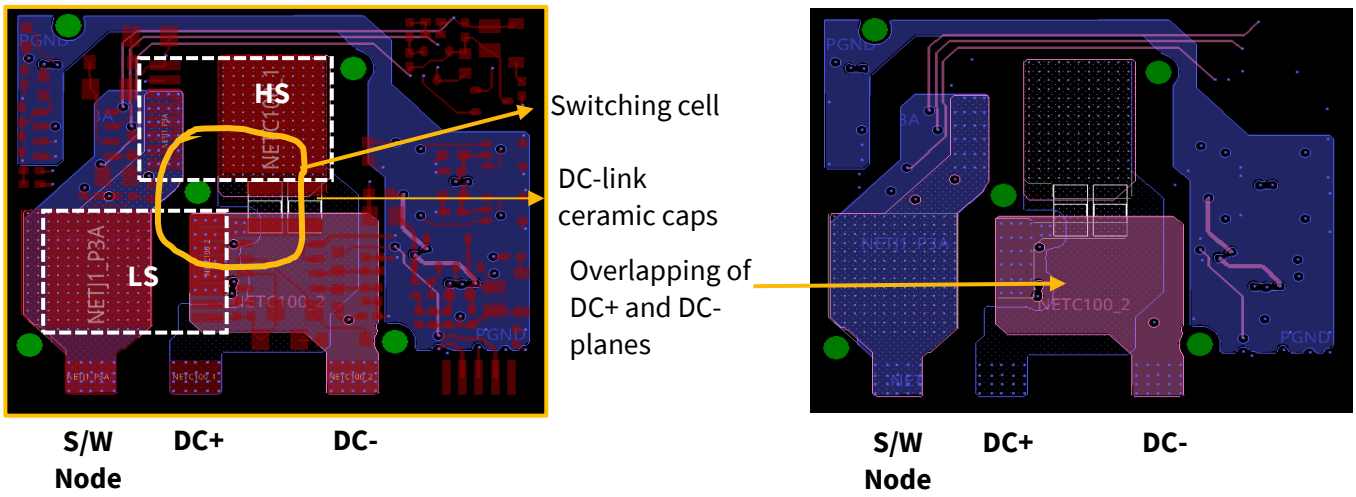


Figure 20 : An optimized switching cell

2.4.2 Impact of Parasitic Inductance (Critical for TO-247-3)

Inductance of the switching cell results in a drain-source overvoltage at turn-off. If this overvoltage is not minimized, it can result in damage to the MOSFET. Inductance of a PCB trace is calculated as follows, where thickness of trace 't' is ignored; 'l' is Length (mm) and 'w' is width (mm). For a PCB trace with 50 mm

$$L = 0.2 \cdot l \cdot \left(\ln \frac{2l}{w} + 0.2235 \cdot \frac{w}{l} + 0.5 \right) nH$$ *Equation 4, Inductance of a PCB trace*

length and 10 mm trace width, the trace inductance is 28.5 nH. Voltage spike in drain-source voltage at turn-off is 71.25 V ($\Delta V = L \cdot \frac{di}{dt}$ = 28.5 nH * 50 A/20 ns = 71.25 V). Hence, short traces/leads reduce voltage spike due to parasitic inductance at turn-off. In addition, it is worth noting that long leads/trace also introduce gate voltage oscillation in the circuit.

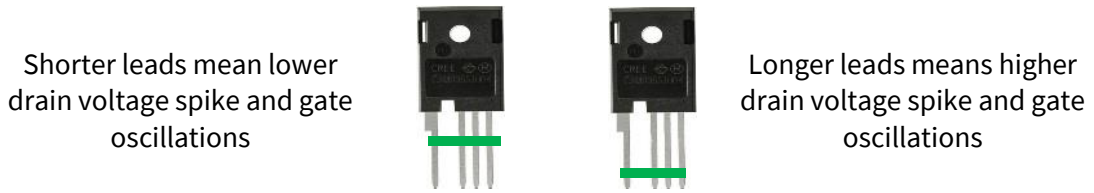


Figure 21 : Impact of MOSFET lead length on drain-source overvoltage and gate oscillations

SECTION 3: SYSTEM LEVEL

Building on the discussion, this section presents design guidelines for PCB layer stacks and discusses the importance of component placement. In addition, this section discusses the impact of PCB layout on cooling and presents a brief introduction to common thermal solutions.

3.1 PCB Layer Stack

Good practice for a 6-layer PCB (can also be adapted for 4-layer PCB) as shown in Figure 22 could be 1st, 2nd and 3rd layers for power loop and 4th layer for GND. The ground layer acts as a shield to cover the sensitive signals at the 5th and 6th layers and SMD components at the 6th layer.

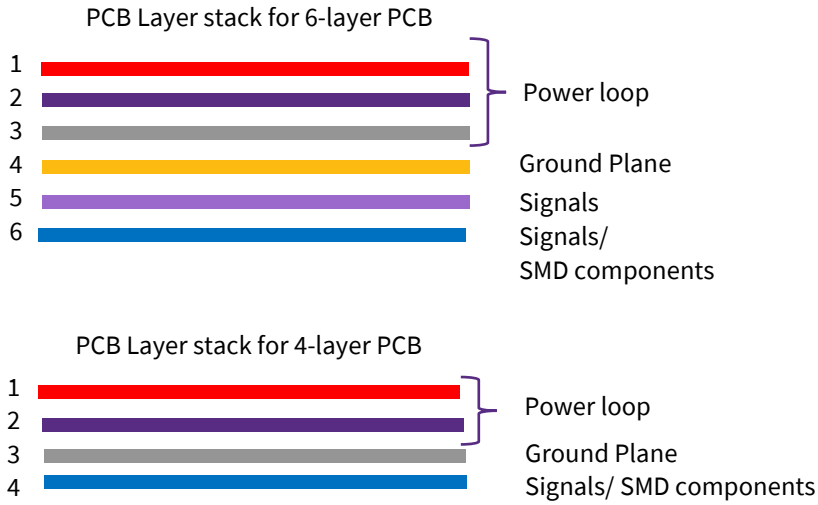


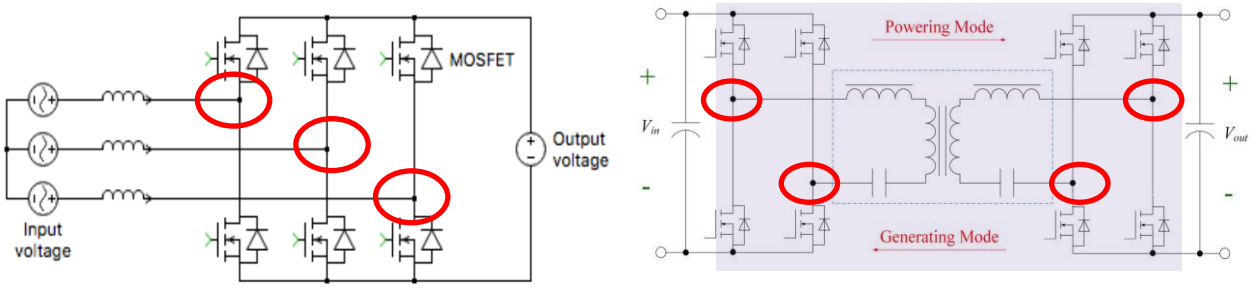
Figure 22 : Layer distribution for 6-yer and 4-layer PCB

3.2 Component Placement

Careful component placement aids in an optimized switching cell. In addition, it is critical to minimize EMI and shield sensitive signals from high magnetic and electric fields. Design goals for component placement can be listed as follows:

- Preferably, input and output connectors should be placed on opposite sides of the board to avoid noise coupling. This is critical for EMI.
- Input EMI filter and input/output connector should be placed far away from high dv/dt trace/nodes to avoid noise coupling. This is also critical for EMI.
- Sensitive signals (e.g., gate loop, control signals) should be placed far away from the high dV/dt trace/nodes as shown in Figure 23.
- Sensitive signals should be placed far away from the high magnetic field such as PFC choke, DC-DC power magnetics.

O *represents a high dv/dt switching node*



AC-DC Stage of OBC (Active Front End)

DC-DC Stage of OBC (CLLC Resonant Converter)

Figure 23: Critical switching nodes with high dv/dt of AC-DC and DC-DC stage of an OBC

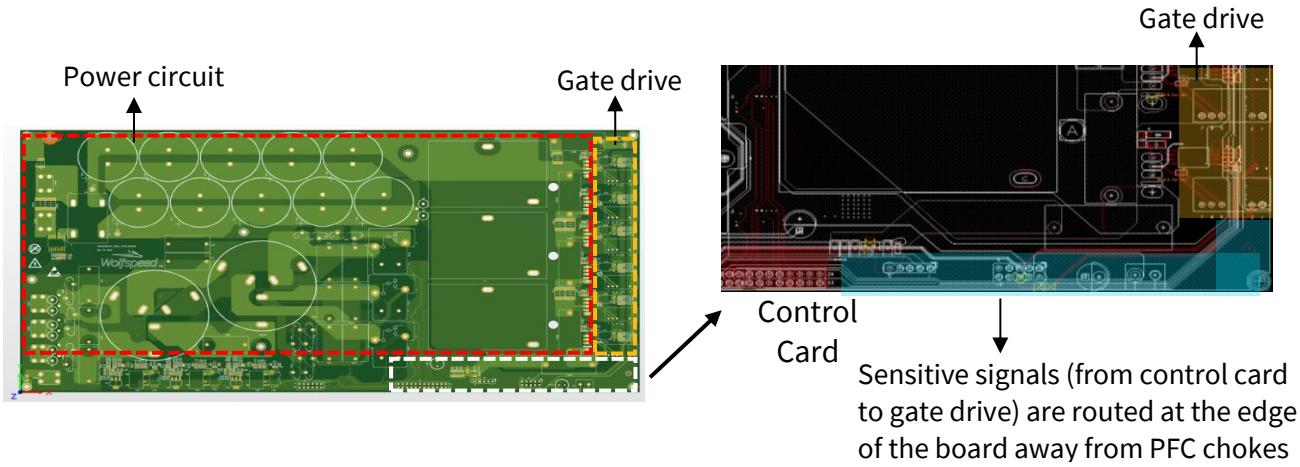


Figure 24: Component placement and control signals routing in AC-DC stage of an OBC

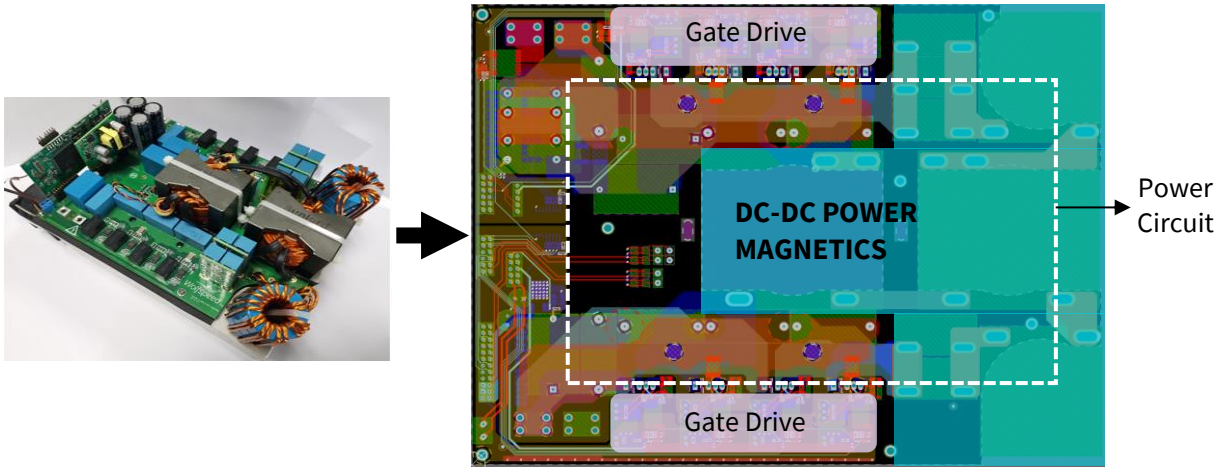


Figure 25: Component Placement in DC-DC stage of an OBC

Figure 24 and Figure 25 give some practical examples to illustrate the points discussed above. In Figure 24, it can be seen that the sensitive signals from the control card to gate drive are intentionally routed at the edge of the PCB to keep them from the PFC choke and the critical switching nodes as is required by the design goals. Further, in Figure 25, it can be seen that gate drive is away from high magnetic field area such as DC-DC transformers, chokes and resonant capacitors. There is also no overlap between gate loop and power loop. Further, sensitive signals (gate signals) are routed at the edge of PCB to keep them away from high magnetic field areas.

3.3 Impact of PCB Layout on Cooling of Discrete SiC MOSFETs

Placement of components is critical to cooling of MOSFETs. In addition to improving EMI performance and shielding sensitive signals from high magnetic fields, placement of a MOSFET can improve or deteriorate its cooling. This could result in non-uniform temperature sharing among MOSFETs mounted on same heatsink. Further, cooling of SMD MOSFETs depends on the size of the copper plane and number of layers used for heat dissipation, thermal via diameter, spacing, and copper thickness. Some of the good placement practices for improving thermal uniformity can be listed as below:

- MOSFETs should not be placed close to other heat sources (e.g., other power semiconductors). This can impair cooling of MOSFETs.
- Copper plane, preferably on multiple layers should be used to dissipate heat away from the MOSFET
- General recommendation for thermal via
    - Via spacing: 0.8 mm
    - Via diameter: 0.4 mm with 2.4 mil (60µm) coated copper thickness

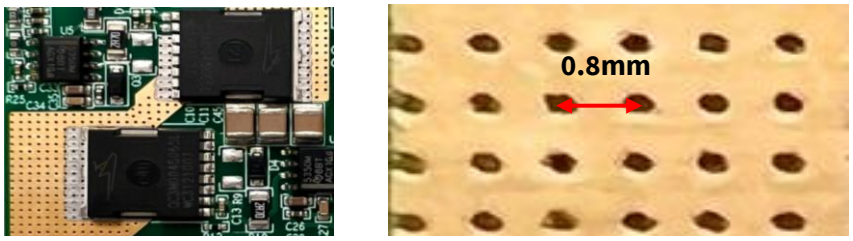


Figure 26: General recommendation for thermal vias

3.4 Common Thermal Solutions

To get the best performance out of a SiC device while ensuring minimum power losses, it becomes very important to have a good thermal management system that will keep the junction temperature as low as possible. Figure 27 gives an overview of common thermal management solutions for SMD MOSFETs and Table 1 provides a brief comparison of these technologies with their advantages and disadvantages [3]. To get more thorough information about thermal management solutions, it is highly recommended to read Wolfspeed article on *Thermal Solutions for Surface Mount Power Devices* [4].

(a) (b)

(c) (d)

Figure 27: Common thermal management solutions for SMD MOSFETs, (a) FR4 with thermal vias, (b) FR4 with Copper inlays, (c) Insulated Metal Substrate, (d) FR4 with AlN inlays

	FR4 with Thermal Vias	FR4 with Copper Inlay	Insulated Metal Substrate	FR4 with ALN inserts
Thermal Conductivity	Good	Better	Better	Best
Cost	Low	High	High	Highest
Electrical Isolation	No (Requires Isolating TIM)	No (Requires Isolating TIM)	Yes	Yes
Advantages	• Standard Manufacturing process • Layout Flexibility	• Layout Flexibility • Better thermal performance	• Better thermal performance • No additional TIM cost and thermal resistance	• Best thermal performance • No additional TIM cost and thermal resistance
Disadvantages	• High overall thermal resistance	• High manufacturing complexity • High TIM thermal resistance	• Higher manufacturing complexity • Layout only on 1 layer • High parasitic inductance and coupling capacitances • SMD connectors are needed for control signals, power inputs/outputs which poses assembly difficulty and reliability concern	• Higher manufacturing complexity • Longer lead times depending on availability of Ceramics

Table 1: Overview and comparison of thermal management solutions for SMD MOSFETs

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