

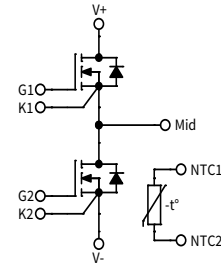
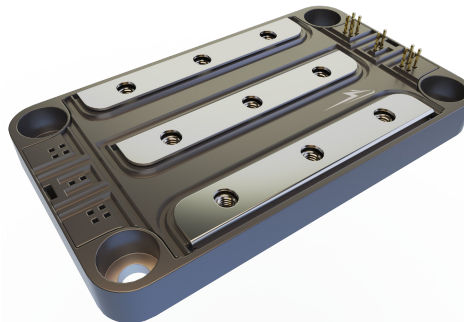
CAB760M12HM3R

1200 V, 760 A, Silicon Carbide, Half-Bridge Module

V_{DS}	1200 V
I_{DS}	760 A

Technical Features

- Low Inductance, Low Profile 62 mm Footprint
- High Junction Temperature (175 °C) Operation
- Implements Switching Optimized Third Generation SiC MOSFET Technology
- Light Weight AlSiC Baseplate
- High Reliability Silicon Nitride Insulator



Applications

- Railway & Traction
- Solar
- EV Chargers
- Industrial Automation & Testing

System Benefits

- Lightweight, Compact Form Factor with 62 mm Compatible Baseplate Enables System Retrofit
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- High Reliability Material Selection

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Voltage	V_{DS}			1200	V	$T_C = 25\text{ }^\circ\text{C}$	
Gate-Source Voltage, Maximum Value	$V_{GS(max)}$	-8		+19		Transient	Note 1
Gate-Source Voltage, Recommended	$V_{GS(op)}$		-4/+15			Static	Fig. 32
DC Continuous Drain Current	I_D		1015		A	$V_{GS} = 15\text{ V}, T_C = 25\text{ }^\circ\text{C}, T_{VJ} \leq 175\text{ }^\circ\text{C}$	Notes 2, 3 Fig. 20
			765			$V_{GS} = 15\text{ V}, T_C = 90\text{ }^\circ\text{C}, T_{VJ} \leq 175\text{ }^\circ\text{C}$	
DC Source-Drain Current (Body Diode)	$I_{SD(BD)}$		515			$V_{GS} = -4\text{ V}, T_C = 25\text{ }^\circ\text{C}, T_{VJ} \leq 175\text{ }^\circ\text{C}$	
Pulsed Drain-Source Current	I_{DM}		1530			t_{Pmax} limited by T_{VJmax} $V_{GS} = 15\text{ V}, T_C = 25\text{ }^\circ\text{C}$	
Power Dissipation	P_D		2206		W	$T_C = 25\text{ }^\circ\text{C}, T_{VJ} \leq 175\text{ }^\circ\text{C}$	Note 4 Fig. 20
Virtual Junction Temperature	$T_{VJ(op)}$	-40		175	$^\circ\text{C}$		

Note (1): Recommended turn-on gate voltage is 15 V with $\pm 5\%$ regulation tolerance

Note (2): Current limit at $T_C = 90\text{ }^\circ\text{C}$ calculated by $I_{D(max)} = \sqrt{(P_D/R_{DS(typ)})(T_{VJ(max)} - T_{VJ(max)})}$

Note (3): Verified by design

Note (4): $P_D = (T_{VJ} - T_C)/R_{TH(JC,typ)}$

MOSFET Characteristics (Per Position) ($T_{VJ} = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200				$V_{GS} = 0\text{ V}$, $T_{VJ} = -40\text{ }^{\circ}\text{C}$	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6	V	$V_{DS} = V_{GS}$, $I_D = 280\text{ mA}$	
			2.0			$V_{DS} = V_{GS}$, $I_D = 280\text{ mA}$, $T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}		15	400	μA	$V_{GS} = 0\text{ V}$, $V_{DS} = 1200\text{ V}$	
Gate-Source Leakage Current	I_{GSS}		0.12	3		$V_{GS} = 15\text{ V}$, $V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		1.33	1.73	$\text{m}\Omega$	$V_{GS} = 15\text{ V}$, $I_D = 760\text{ A}$	Fig. 2 Fig. 3
			2.13			$V_{GS} = 15\text{ V}$, $I_D = 760\text{ A}$, $T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Transconductance	g_{fs}		548		S	$V_{DS} = 20\text{ V}$, $I_{DS} = 760\text{ A}$	Fig. 4
			585			$V_{DS} = 20\text{ V}$, $I_{DS} = 760\text{ A}$, $T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Turn-On Switching Energy, $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 175\text{ }^{\circ}\text{C}$	E_{ON}		20.3 20.7 23.7		mJ	$V_{DS} = 600\text{ V}$, $I_D = 760\text{ A}$, $V_{GS} = -4\text{ V}/15\text{ V}$, $R_{G(ext)} = 1.0\text{ }\Omega$, $L = 13.7\text{ }\mu\text{H}$	Fig. 11 Fig. 13
Turn-Off Switching Energy, $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 175\text{ }^{\circ}\text{C}$	E_{OFF}		17.9 17.5 17.8				
Internal Gate Resistance	$R_{G(int)}$		0.47		Ω	$V_{AC} = 25\text{ mV}$, $f = 100\text{ kHz}$	
Input Capacitance	C_{iss}		79.4		nF	$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$, $V_{AC} = 25\text{ mV}$, $f = 100\text{ kHz}$	Fig. 9
Output Capacitance	C_{oss}		2.9				
Reverse Transfer Capacitance	C_{rss}		90				
Gate to Source Charge	Q_{GS}		768		nC	$V_{DS} = 800\text{ V}$, $V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 760\text{ A}$ Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		924				
Total Gate Charge	Q_G		2724				
FET Thermal Resistance, Junction to Case	R_{thJC}		0.068	0.073	$^{\circ}\text{C}/\text{W}$		Fig. 17

Diode Characteristics (Per Position) ($T_{VJ} = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Body Diode Forward Voltage	V_{SD}		5.4		V	$V_{GS} = -4\text{ V}$, $I_{SD} = 760\text{ A}$	Fig. 7
			4.7			$V_{GS} = -4\text{ V}$, $I_{SD} = 760\text{ A}$, $T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Reverse Recovery Time	t_{RR}		49		ns	$V_{GS} = -4\text{ V}$, $I_{SD} = 760\text{ A}$, $V_R = 600\text{ V}$ $di/dt = 20\text{ A/ns}$, $T_{VJ} = 175\text{ }^{\circ}\text{C}$	Fig. 32
Reverse Recovery Charge	Q_{RR}		17.0		μC		
Peak Reverse Recovery Current	I_{RRM}		540		A		
Reverse Recovery Energy $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 175\text{ }^{\circ}\text{C}$	E_{RR}		1.3 3.5 5.5		mJ	$V_{DS} = 600\text{ V}$, $I_D = 760\text{ A}$, $V_{GS} = -4\text{ V}/15\text{ V}$, $R_{G(ext)} = 1.0\text{ }\Omega$, $L = 13.7\text{ }\mu\text{H}$	Fig. 14

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Package Resistance, M1	R ₁₋₂		106.5		μΩ	T _C = 125 °C, Note 5
Package Resistance, M2	R ₂₋₃		126.3			T _C = 125 °C, Note 5
Stray Inductance	L _{Stray}		4.9		nH	Between Terminals 1 and 3
Case Temperature	T _C	-40		125	°C	
Weight	W		179		g	
Mounting Torque	M _S	3	4.5	5	N-m	Baseplate, M6 Bolts
		0.9	1.1	1.3		Power Terminals, M4 Bolts
Case Isolation Voltage	V _{isol}	4			kV	AC, 50 Hz, 1 min
Comparative Tracking Index	CTI	600				
Clearance Distance		13.07			mm	Terminal to Terminal
		6.00				Terminal to Baseplate
Creepage Distance		14.27				Terminal to Terminal
		12.34				Terminal to Baseplate

Note (5): Total Effective Resistance (Per Switch Position) = MOSFET R_{DS(on)} + Switch Position Package Resistance

Temperature Sensor (NTC) Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resistance at 25 °C	R ₂₅		4700		Ω	T _{NTC} = 25 °C
Tolerance of R ₂₅			±1		%	
Beta Value for 25 °C to 85 °C	B _{25/85}		3435		K	
Beta Value for 0 °C to 100 °C	B _{0/100}		3399		K	
Tolerance of B _{25/85}			±1		%	
Maximum Power Dissipation	P ₂₅		50		mW	

Steinhart & Hart Coefficients for NTC Resistance & NTC Temperature Computation (T in K)

$$\ln\left(\frac{R}{R_{25}}\right) = A + \frac{B}{T} + \frac{C}{T^2} + \frac{D}{T^3}$$

$$\frac{1}{T} = A_1 + B_1 \ln\left(\frac{R}{R_{25}}\right) + C_1 \ln^2\left(\frac{R}{R_{25}}\right) + D_1 \ln^3\left(\frac{R}{R_{25}}\right)$$

A	B	C	D
-1.289E+01	4.245E+03	-8.749E+04	-9.588E+06

A ₁	B ₁	C ₁	D ₁
3.354E-03	3.001E-04	5.085E-06	2.188E-07



Typical Performance

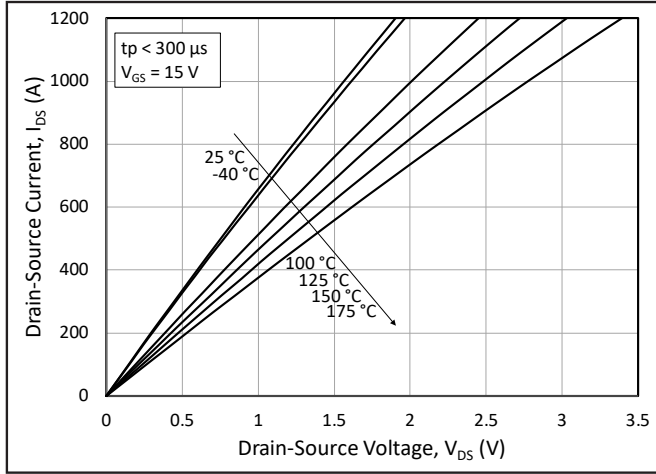


Figure 1. Output Characteristics for Various Junction Temperatures

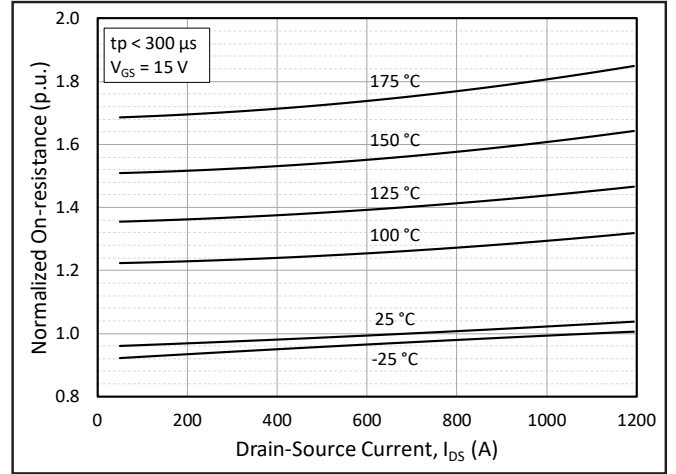


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

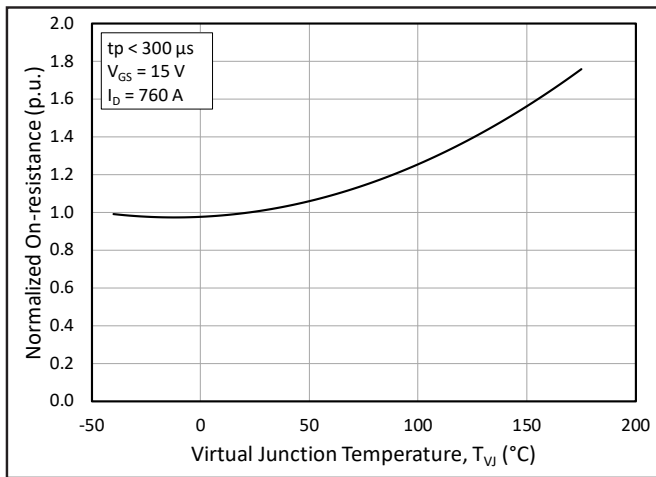


Figure 3. Normalized On-State Resistance vs. Junction Temperature

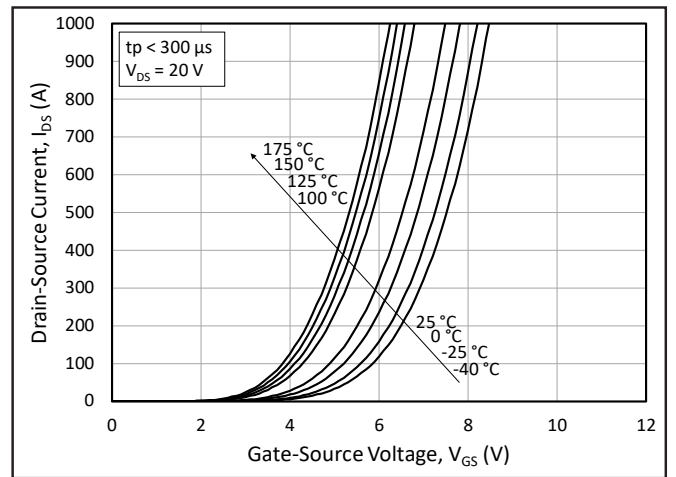


Figure 4. Transfer Characteristic for Various Junction Temperatures

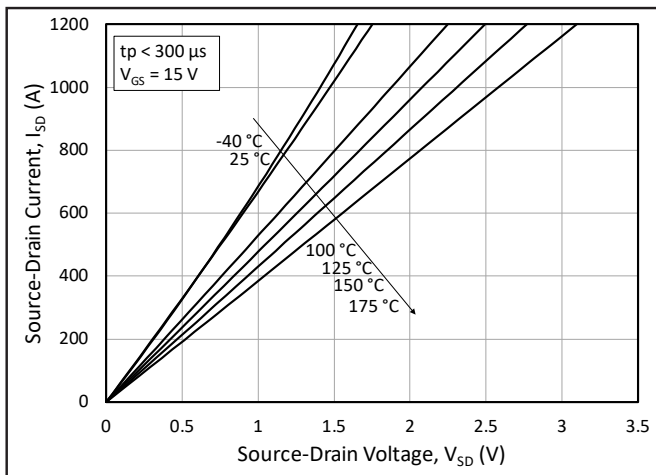


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 15\text{ V}$

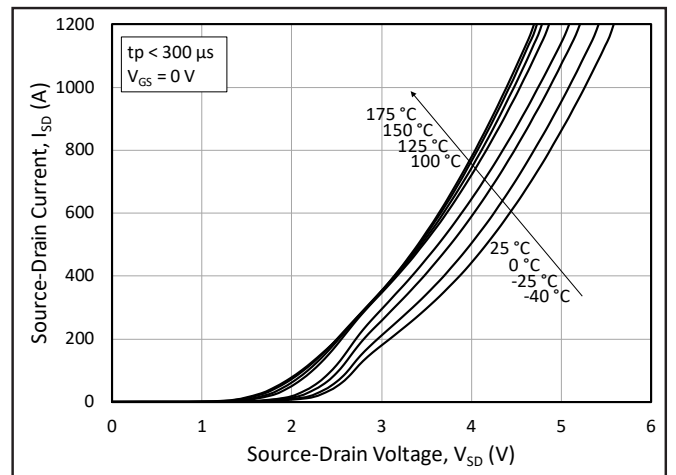


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 0\text{ V}$ (Body Diode)



Typical Performance

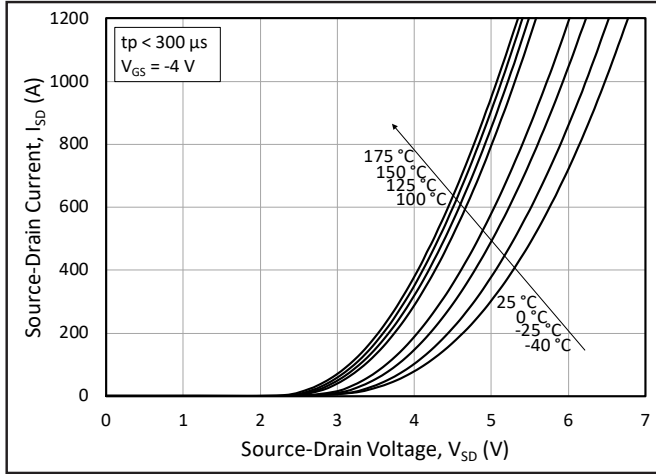


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = -4$ V (Body Diode)

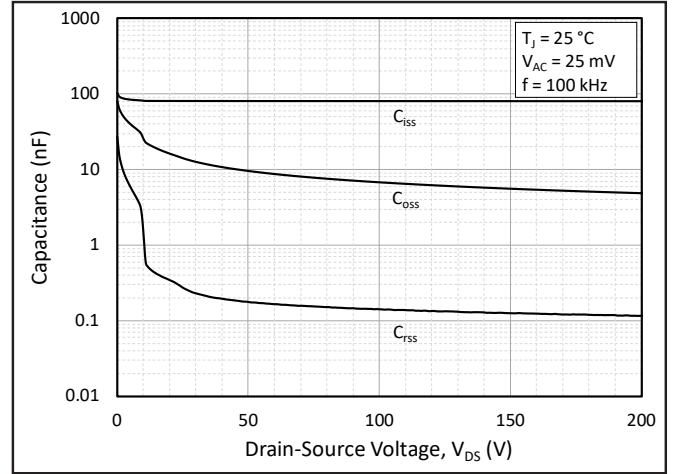


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200 V)

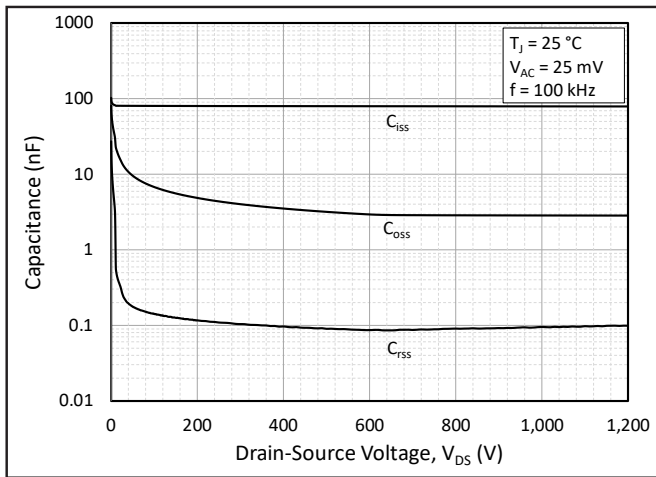


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200 V)

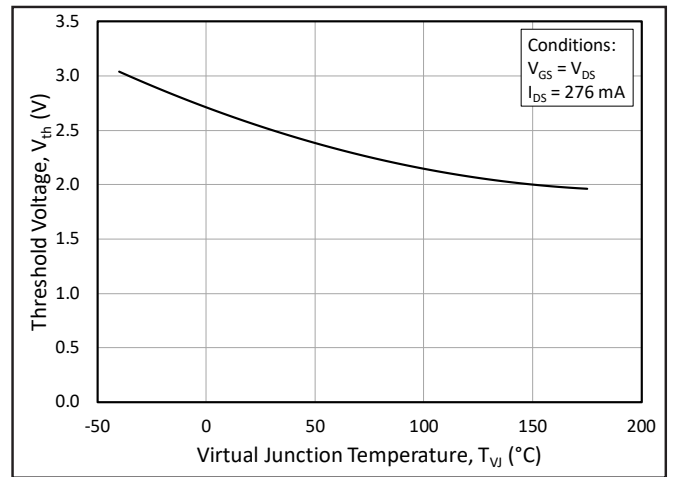


Figure 10. Threshold Voltage vs. Junction Temperature

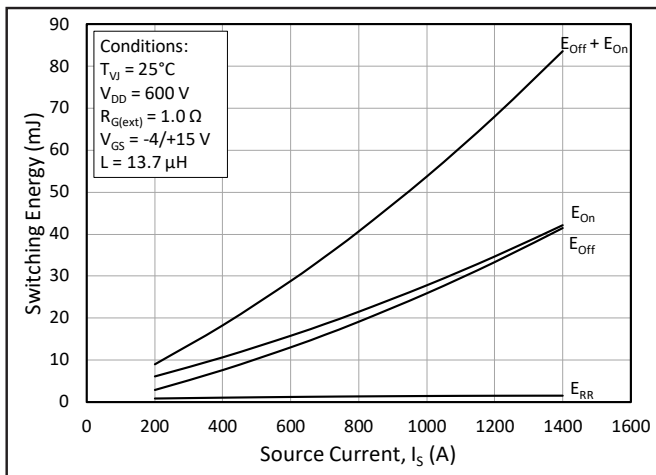


Figure 11. Switching Energy vs. Drain Current ($V_{DS} = 600$ V)

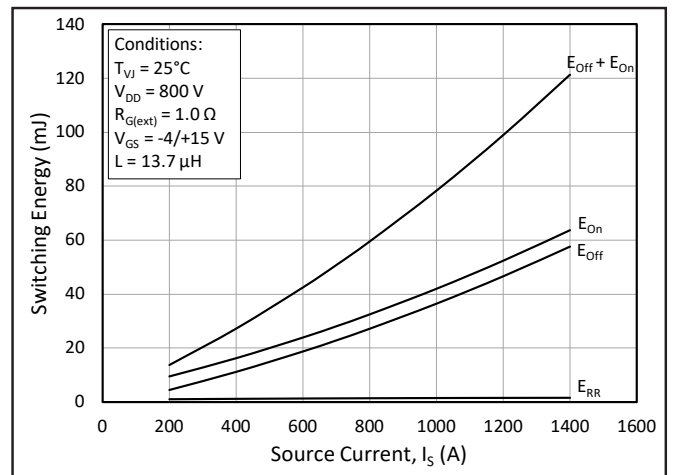


Figure 12. Switching Energy vs. Drain Current ($V_{DS} = 800$ V)



Typical Performance

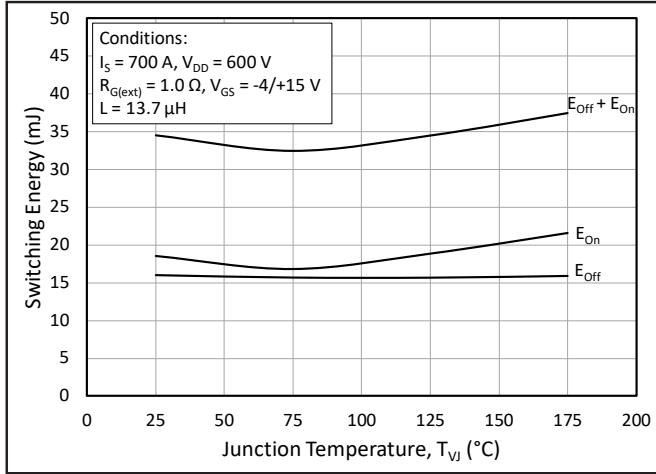


Figure 13. MOSFET Switching Energy vs. Junction Temperature

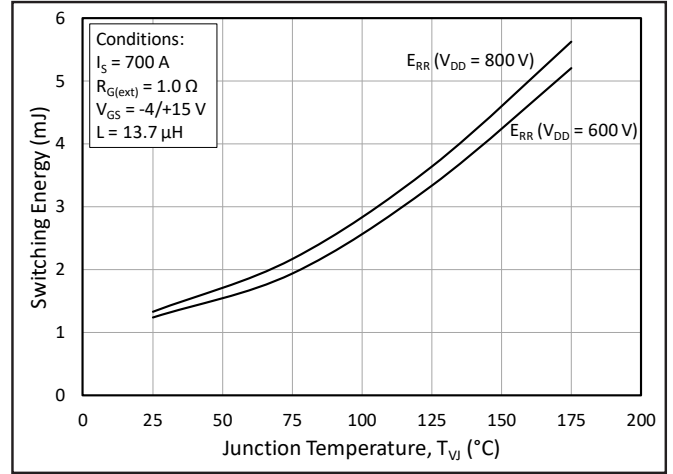


Figure 14. Reverse Recovery Energy vs. Junction Temperature

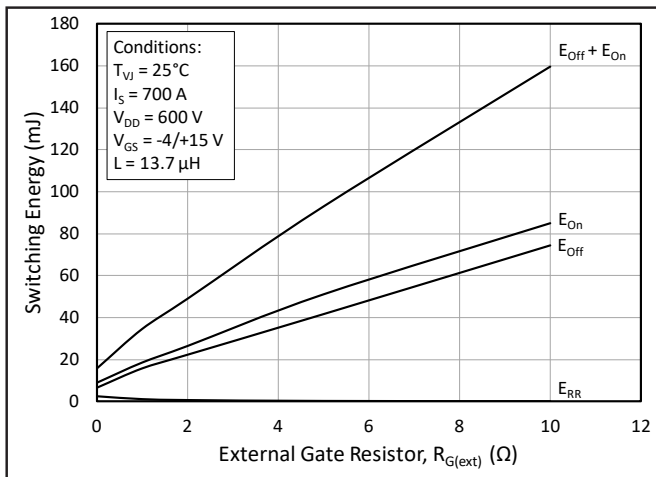


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

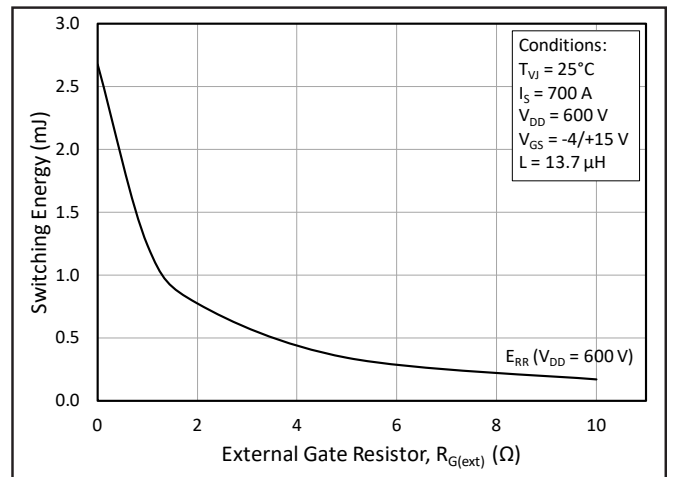


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

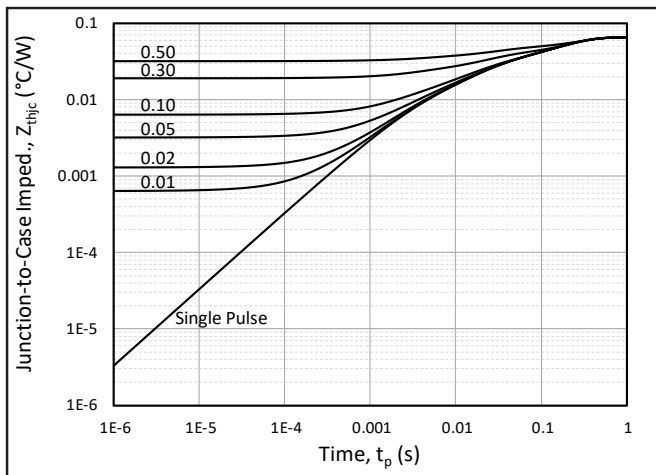


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, Z_{thJC} (°C/W)

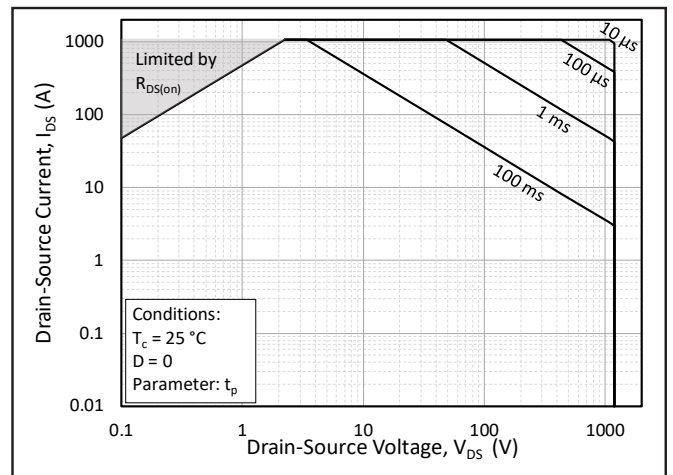


Figure 18. Forward Bias Safe Operating Area (FBSOA)



Typical Performance

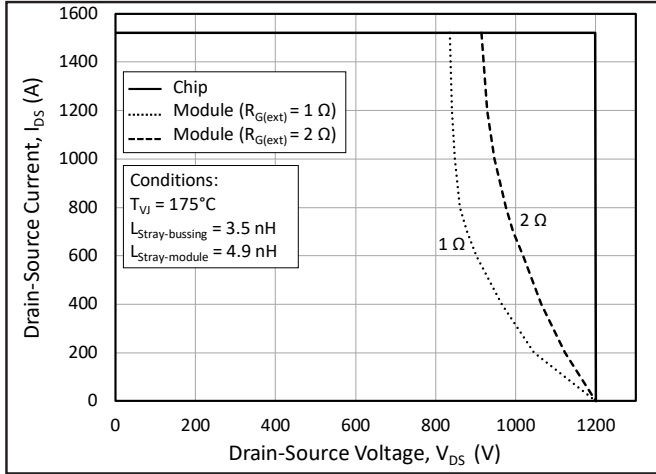


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

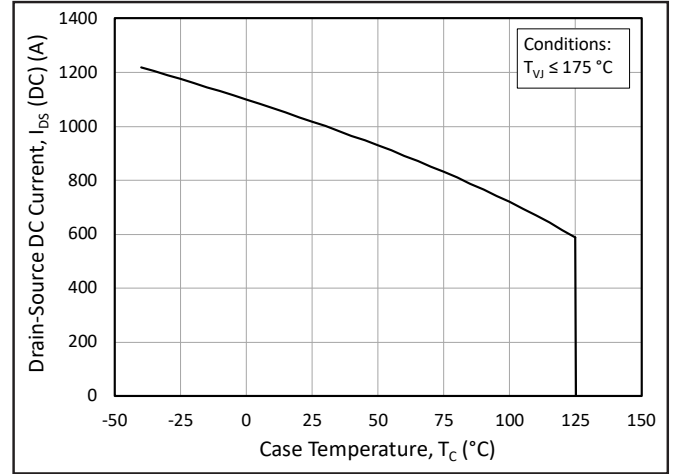


Figure 20. Continuous Drain Current Derating vs. Case Temperature

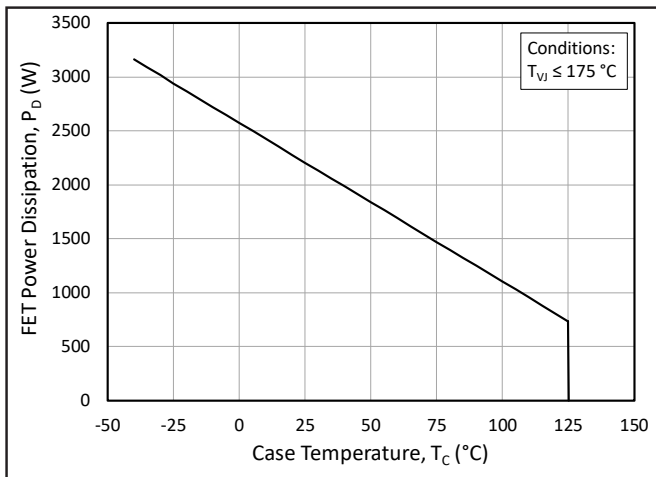


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

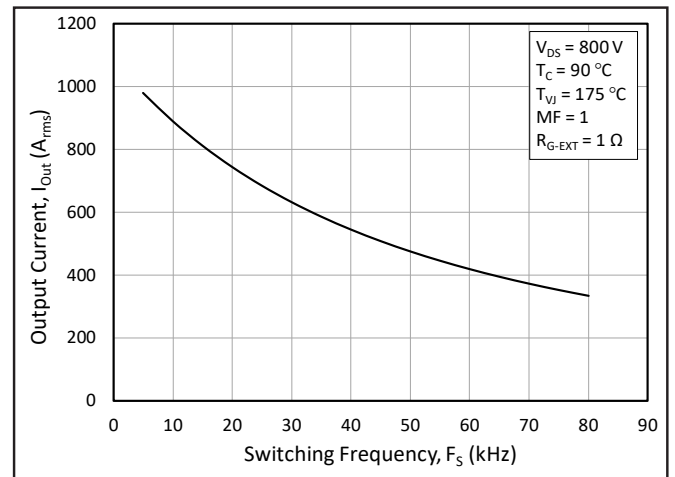


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

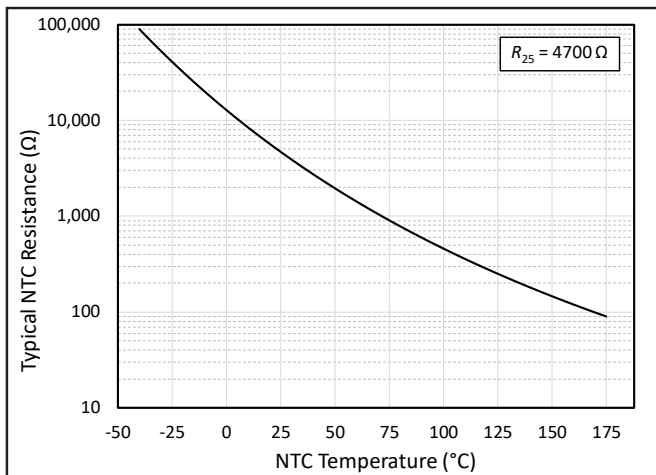


Figure 23. Typical NTC Resistance vs. Temperature



Timing Characteristics

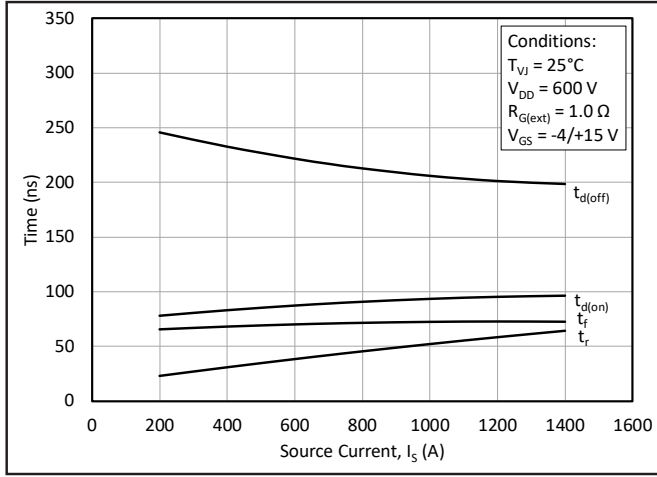


Figure 24. Timing vs. Source Current

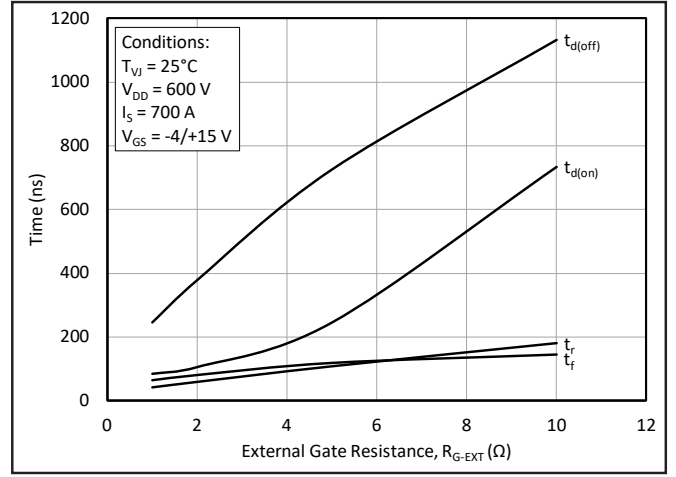


Figure 25. Timing vs. External Gate Resistance

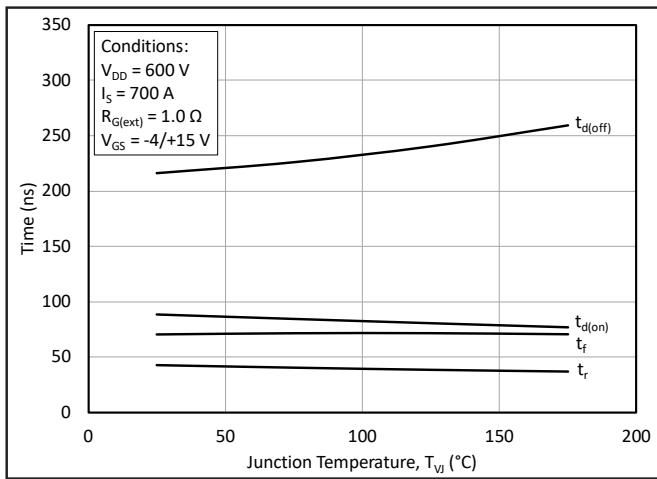


Figure 26. Timing vs. Junction Temperature

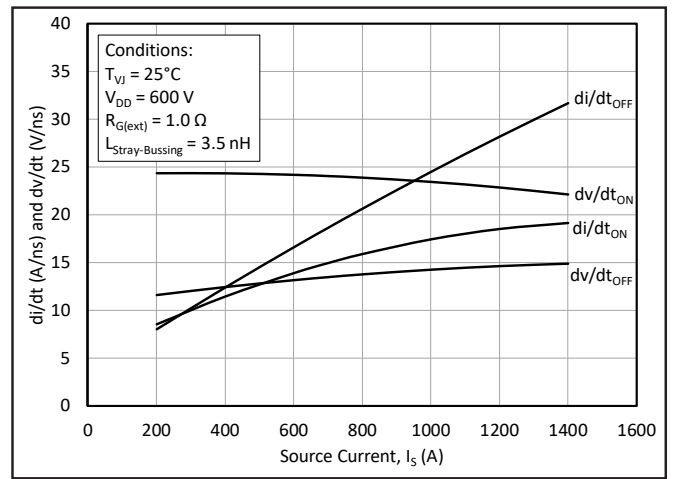


Figure 27. dv/dt and di/dt vs. Source Current

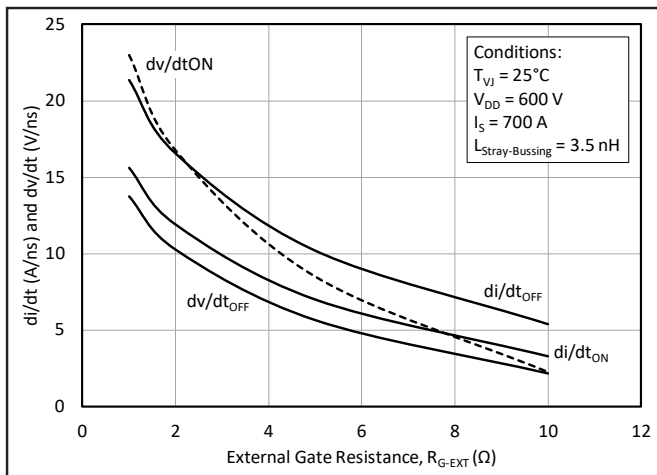


Figure 28. dv/dt and di/dt vs. External Gate Resistance

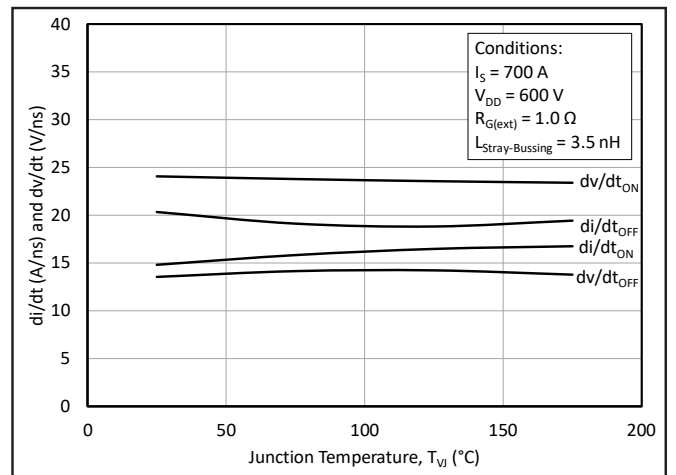


Figure 29. dv/dt and di/dt vs. Junction Temperature



Definitions

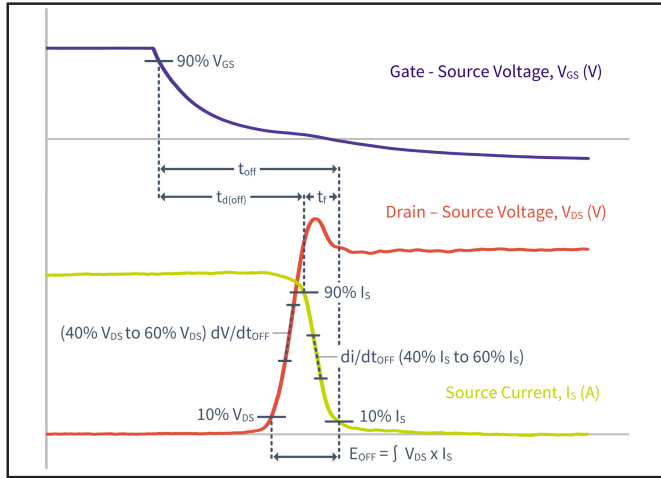


Figure 29. Turn-Off Transient Definitions

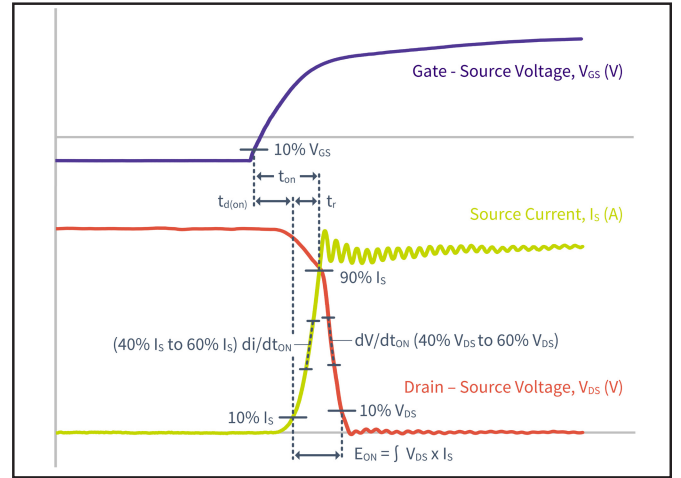


Figure 30. Turn-On Transient Definitions

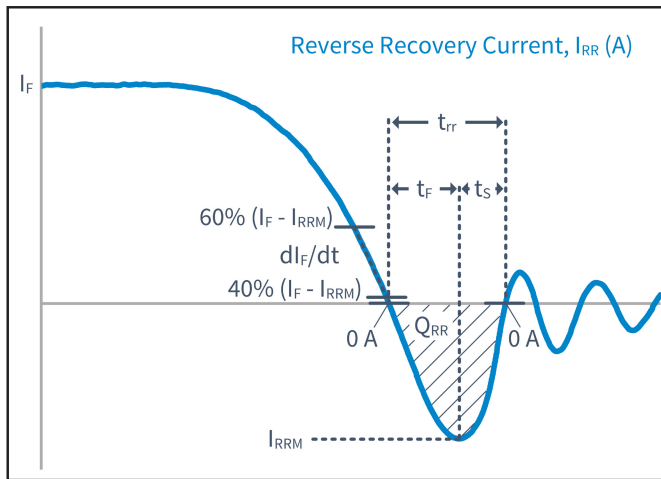


Figure 31. Reverse Recovery Definitions

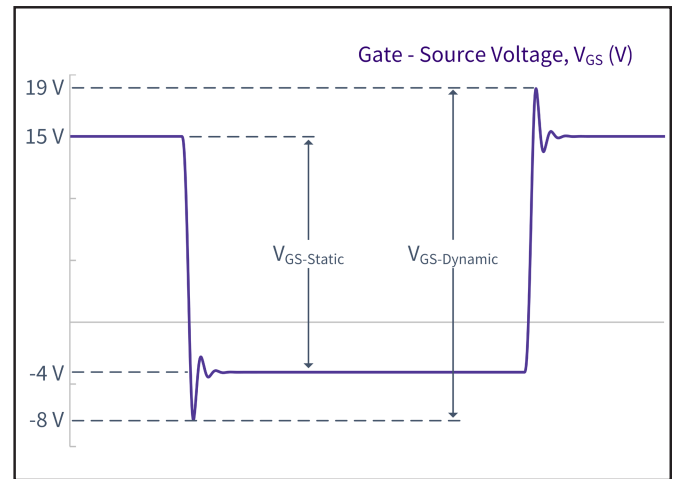
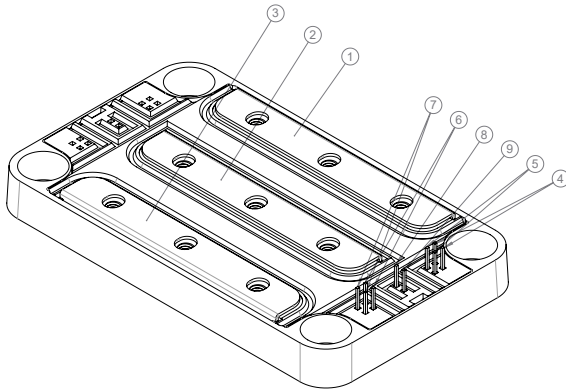


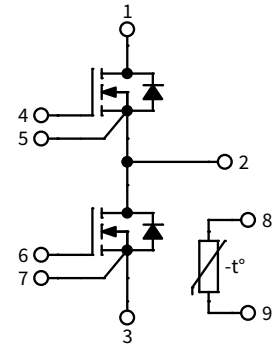
Figure 32. VGS Transient Definitions



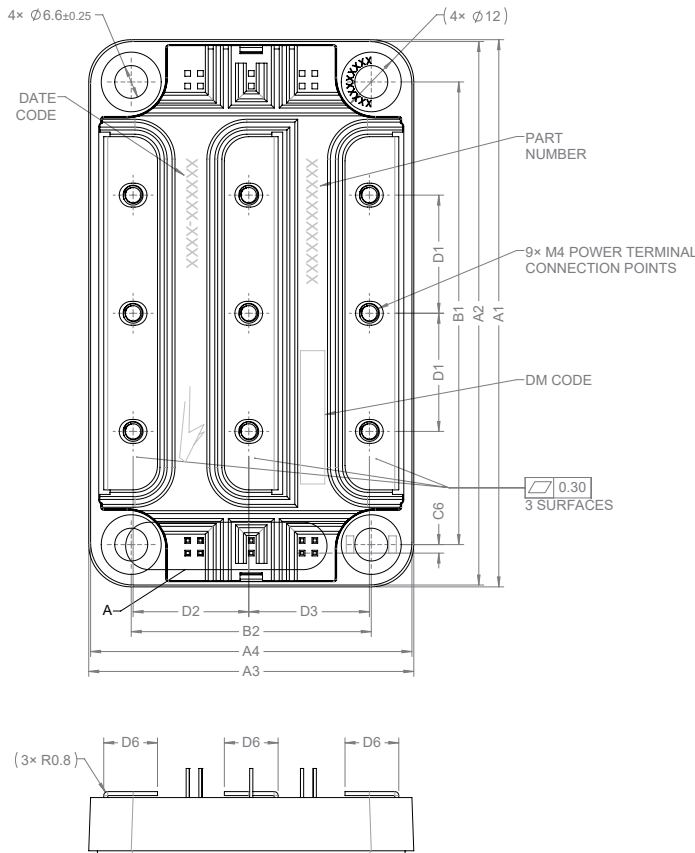
Schematic and Pin Out



PIN OUT SCHEME	
PIN	LABEL
①	V+
②	Mid
③	V-
④	G1, Top row pins (2)
⑤	K1, Bottom row pins (2)
⑥	G2, Top row pins (2)
⑦	K2, Bottom row pins (2)
⑧	NTC1
⑨	NTC2

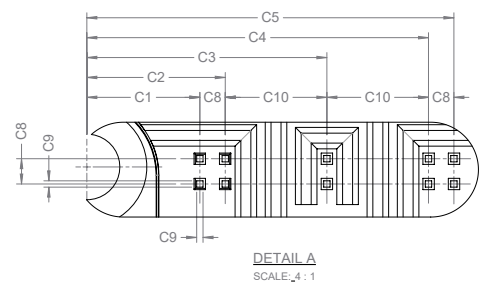


Package Dimensions (mm)



NOTE:
ALL MARKINGS SHALL
CONFORM TO PRC-00786.

DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	110.00	±0.60
A2	109.25	±0.60
A3	65.00	±0.60
A4	64.25	±0.60
A5	3.25	±0.30
A6	11.45	±0.60
B1	93.00	±0.30
B2	48.00	±0.30
C1	11.30	±0.40
C2	13.84	±0.40
C3	24.00	±0.40
C4	34.16	±0.40
C5	36.70	±0.40
C6	1.71	±0.40
C7	17.30	±0.50
C8	2.54	±0.30
C9	0.64	±0.30
C10	10.16	±0.40
D1	23.75	±0.50
D2	23.13	±0.50
D3	24.13	±0.50
D4	12.20	±0.50
D5	71.00	±0.30
D6	10.75	±0.30





Supporting Links & Tools

Evaluation Tools & Support

- [PLECS Models](#)
- [LTSpice Models](#)
- [SpeedFit 2.0 Design Simulator™](#)
- [Technical Support Forum](#)
- [Dynamic Characterization Evaluation Tool for the High Performance 62mm \(HM\) Module Platform](#)

Dual-Channel Gate Driver Board

- [CGD1700HB3P-HM3: Wolfspeed Gate Driver Board](#)
- [CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers](#)

Application Notes

- [CPWR-AN35: 62mm Thermal Interface Material Application Note](#)
- [CPWR-AN39: KIT-CRD-CIL12N-HM User Guide](#)
- [PRD-04814: Design Options for Wolfspeed® Silicon Carbide MOSFET Gate Bias Power Supplies](#)



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REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

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