Reliability of 150 nm, 28 V GaN HEMT Process up to Ka-band

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Wolfspeed has already reported [1, 2] the fabrication process, device characteristics, MMIC RF performance of a high-performance GaN-on-SiC HEMT featuring a 150 nm gate length (V5 process) for Ka-band applications. Excellent device performances have been demonstrated at Ka-band with output power density (P_{out}) exceeding 3 W/mm and peak power added efficiency (PAE) above 35 %. In this work we present the comprehensive reliability assessment and lifetime projection of 28 V rated 150 nm gate length process technology (G28V5). Moreover, in this work Ka-band device reliability (at 31.5 GHz) has also been assessed under RF accelerated life test (RF-ALT), as well as RF high temp operating life (RF-HTOL) stress. The GaN-on-SiC HEMT wafers were fabricated and processed on 100 mm high purity semi-insulating (HPSI) 4H-SiC substrates, and the devices were assembled, at Wolfspeed in Research Triangle Park, NC, USA.

Qualification test results HTRB, TC, DC-HTOL: The 1000 hours of high temperature reverse bias (HTRB) and 500 cycles of temperature cycle (TC) reliability tests were performed on 14.4 mm periphery devices to demonstrate the maturity of the technology. The 1000 hours of HTOL test was performed on 3.6 mm devices. No devices displayed a parametric change of 1 dB or more in critical RF parameters (namely *Gain*, P_{sat}) post stress. The changes in drain and gate leakages post stress were also well behaved and well below 5x shift as shown in Fig. 1(a-b). After HTRB the leakage actually reduced likely owing to the virtual gate effect. The HTRB in-situ gate leakage curve as shown in Fig. 1(c) correlates well with the post stress leakage measurement. Also, the changes in other critical DC parameters like *Ron*, *Vp*, *IDSS* were all well behaved and below the 10 % shift mark. Fig. 2(a-c) shows the shift in *Ron*, *IDSS* and P_{sat} post 1000 hours of HTOL stress as compared to the pre-stress data. Table-1 summarizes the test conditions, the sample sizes and the test results. The results demonstrate a lot tolerance percent defect (LTPD) of 3 or lower with 90 % statistical confidence level. To our knowledge, for deep submicron GaN HEMT this is the first successful demonstration of 1000 hours of HTRB test done at 300 % of its operating quiescent voltage with such large periphery devices.

The intrinsic reliability with RF-ALT at 3.5 GHz and DC-ALT: The RF-ALT study was performed on 3.6 mm discrete FETs at different junction temperatures (Tj) ranging from (360 – 400) °C, Pin=26 dBm (at peak PAE), Idq=200 mA, Vd=28 V. As shown in Fig. 3(a), based on the in-situ data a device failure time (TTF) was determined when the device had failed catastrophically or P_{out} was degraded more than 1 dB (whichever condition was met first). A fit to the data using an Arrhenius temperature-accelerated lifetime model and lognormal statistics yields a median time to failure (MTTF) prediction of over 1E6 hours at 225 °C junction temperature as shown in Fig. 3(b). Through FA the key failure mode for V5 was determined to be field plate (FP) voiding and ohmic contact degradation (likely relevant only at higher temperature) which is consistent with our finding with other Wolfspeed technologies [3]. Since FP stacks are similar across technologies and FP voiding is the main failure mode at the maximum operating temperature (225 °C) hence perhaps we expect similar MTTF under RF-ALT at 225 °C for V3 and V5 as shown in Fig. 3(b).

The DC-ALT test was performed on 3.6 mm gate periphery devices under DC drive conditions at the nominal drain operating voltage (28 V), high dissipated power of ~6 W/mm and junction temperatures (Tj) ranging from (350 – 380) °C. A device failure was defined as a condition in which a stressed device has 15% change in Idmax (for Vg=1 V and Vd=7.5 V). For any devices that did not reach the failure criterion by the conclusion of the test, their lifetimes were estimated by extrapolating the Idmax degradation to 15% decrease from its initial value by a sqrt(time) fit. A fit to the data using an Arrhenius temperature-accelerated lifetime model and lognormal statistics yields an activation energy of over 2 eV

and MTTF prediction of over 6E7 hours at 225 °C junction temperature as shown in Fig. 3(c). Although DC-ALT has a higher activation energy and gives longer lifetime predictions, but is not the most important reliability aspect at normal operating conditions, and would give an overly optimistic prediction, the RF-ALT capability and methodology that have been developed by Wolfspeed are considered to be more relevant to use conditions in typical applications.

Ka-band reliability evaluation: Pre-matched single stage MMICs with multi fingered FETs (6x50 μm) were used (shown in Fig. 4(a)) to evaluate reliability in the Ka-band (31.5 GHz) under RF-HTOL/ALT stress tests. A group of devices were stressed under Idq=40 mA, Vd=28 V, Pin=20 dBm and for two different Tj (225 °C and 360 °C). After 2000 hours of stressing for the RF-HTOL group (Tj=225 °C) and 1000 hours of stressing of the RF-ALT group (Tj=360 °C), neither of these devices showed a drop of 1 dB in P_{out} nor did they fail catastrophically (consistent with the lifetime projection data at 3.5 GHz). Post stress transistor transfer curves and power sweep results as presented in Fig. 4(b-c) demonstrate the perfectly functional devices after long hours of RF-ALT/HTOL stress at 31.5 GHz.

The on-state, off-state results coupled with the intrinsic reliability assessment up to 31.5 GHz demonstrate the maturity and reliability of V5 technology for Ka-band applications.

[1] *Optically-Defined 150 nm 28 V GaN HEMT Process for Ka-Band*, CS MANTECH,2019, K.M. Bothe et al.
[2] *A High Efficiency, Ka-Band, GaN-on-SiC MMIC with Low Compression,* BCICTS, 2019, B. Schmukler et al.
[3] *Reliability comparison of 28 V–50 V GaN-on-SiC S-band and X-band technologies*," Microelectronics Reliability, 2018, D. A. Gajewski et al.

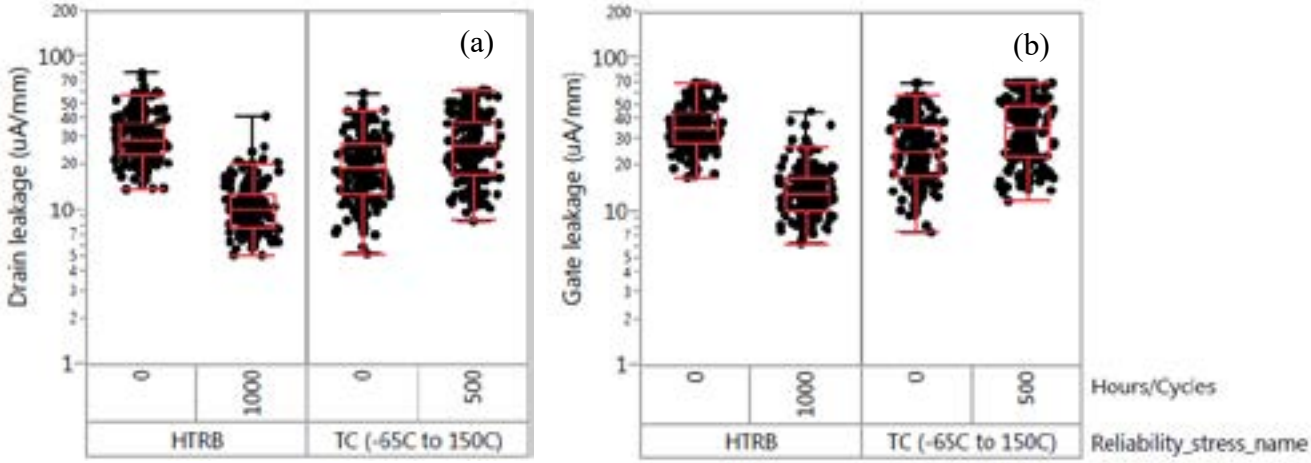

Fig.1 (a-b) Drain leakage and Gate leakage (Vd=10 V, Vg=-8 V) measured before and after reliability stress (HTRB and TC).

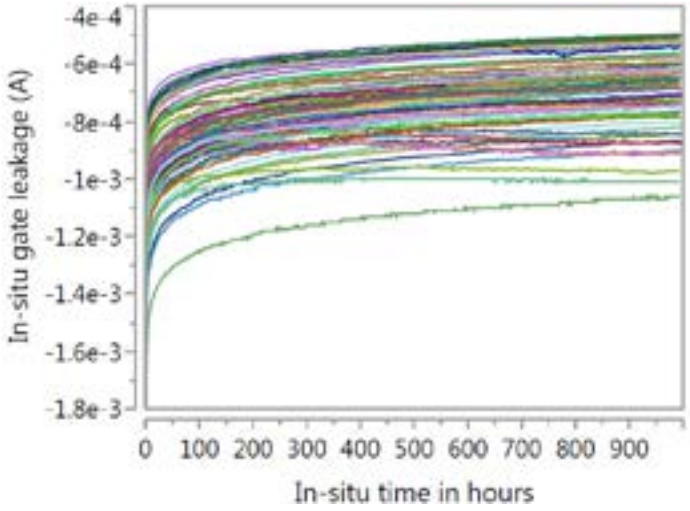

Fig.1 (c) In-situ gate leakage data of 77 devices (14.4 mm gate periphery device) under HTRB stress.

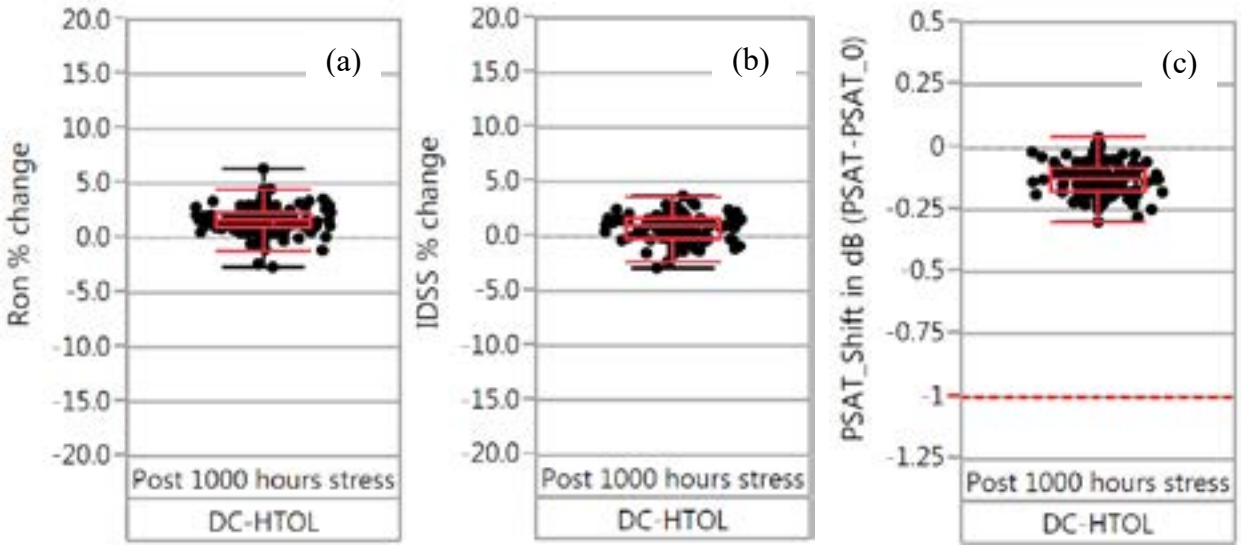

Fig.2 (a-c) Ron, IDSS and 3.5 GHz PSAT shift post 1000 hours of HTOL stress test as compared to pre-stress data.

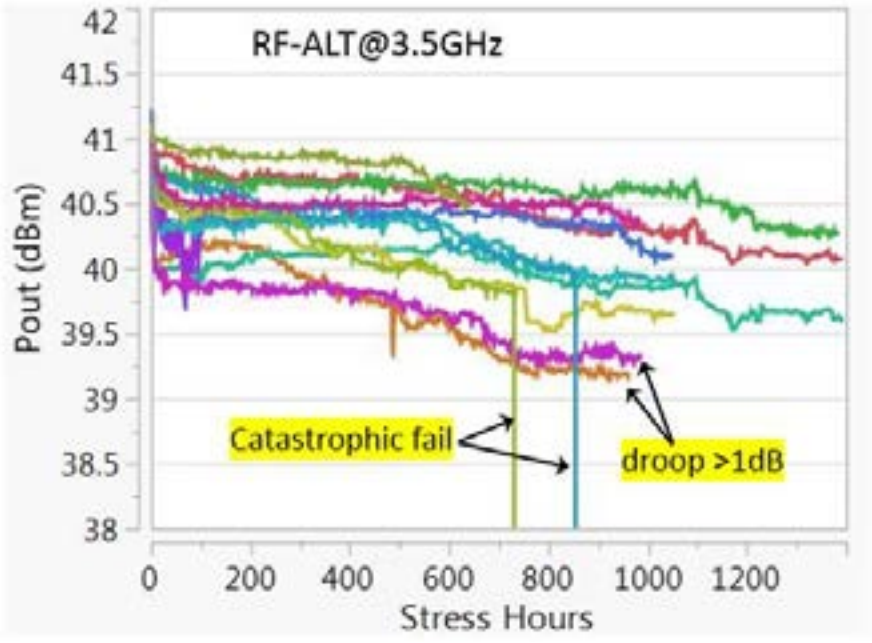

Fig.3 (a) Representative P_{out} degradation (dB) versus hours for a set of G28V5 devices under RF-ALT (3.5 GHz) at accelerated stress junction temperatures. The different curves represent sets of devices that can be considered equivalent for the purposes of this test.

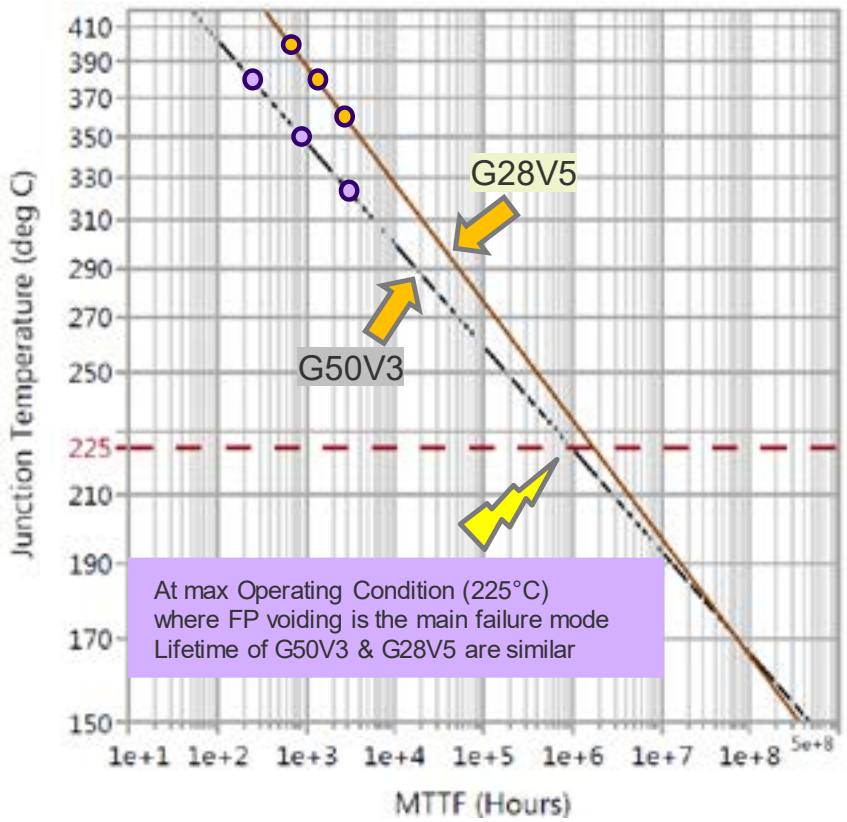

Fig.3 (b) MTTF versus junction temperature for G28V5 RF-ALT and G50V3 RF-ALT at 3.5 GHz.

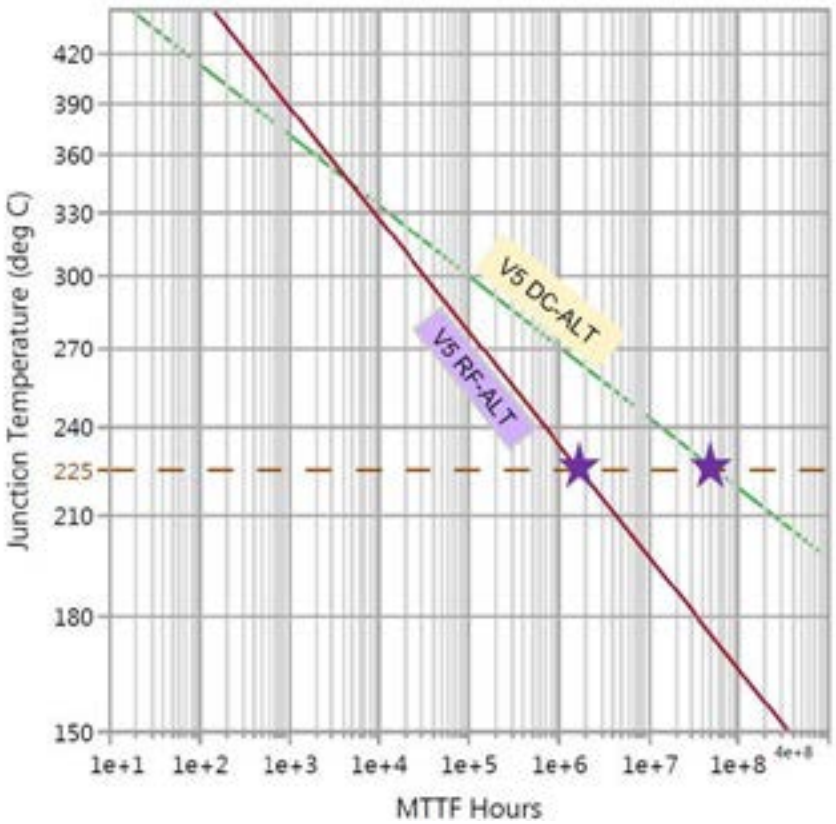

Fig.3 (c) MTTF versus junction temperature for G28V5 RF-ALT and DC-ALT. Stars represent fiducial points to illustrate the predicted lifetime at maximum rated junction temperature of 225 °C.

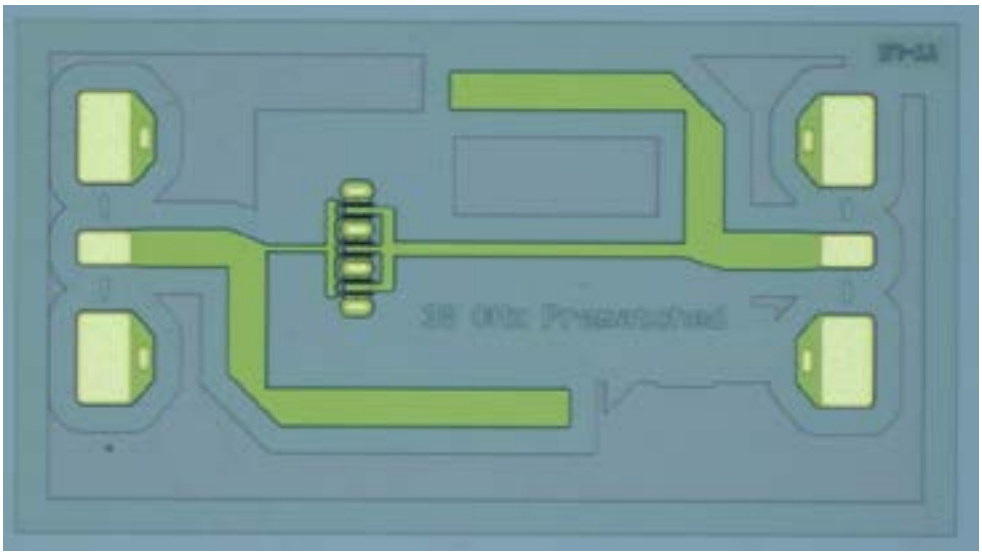

Fig.4 (a) The pre-matched single stage MMIC with multi fingered FET (6x50 µm).

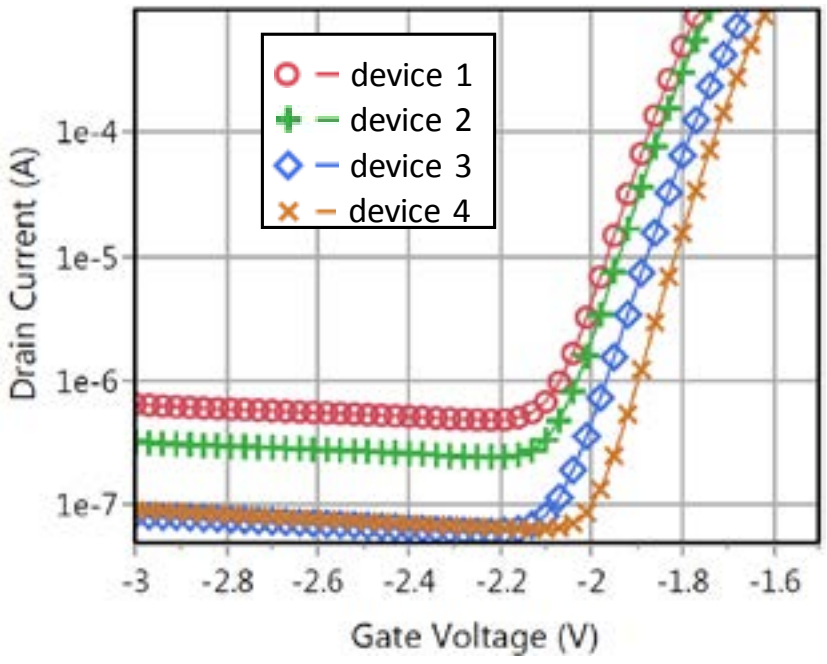

Fig.4 (b) The transfer curves of the stressed devices (6x50 µm) measured at Vd=10V post RF-HTOL/RF-ALT stress (at 31.5 GHz).

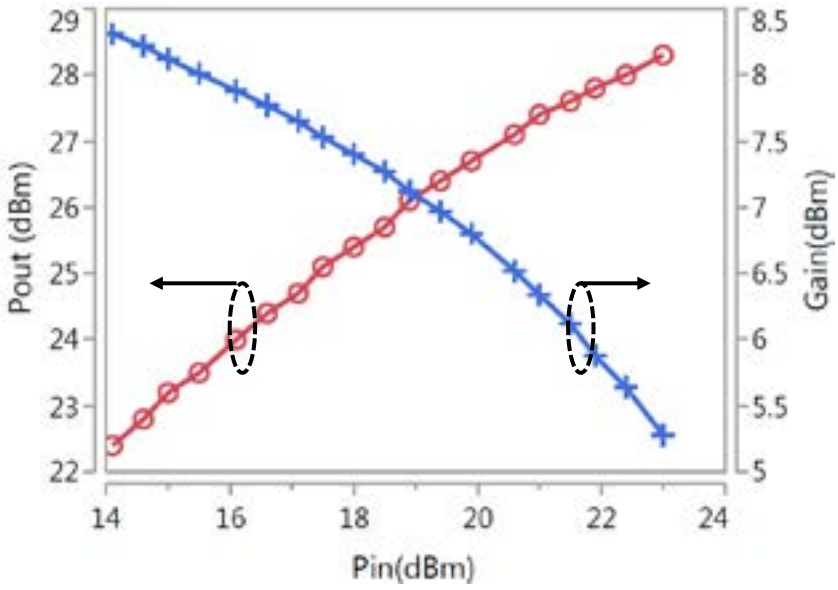

Fig.4 (c) Post RF-HTOL stress (at 31.5 GHz), power sweep on a 6x50 µm device.

Table 1: Qualification Test Results

Stress	**Stress Condition**	**Duration**	**# of Lots Sampled**	**# of Samples per Lot**	**Total Sample Size**	**# Failed**
DC-HTOL	VDS = 28 V, IDS = 514 mA, (Pdiss~4 W/mm), Tj = 225 °C	1000 Hours	3	≥ 25	77	0
HTRB	VDS = 84 V, VGS = -8 V, Ta = 150 °C	1000 Hours	3	≥ 25	77	0
TC	TA = -65 °C to 150 °C	500 Cycles	3	≥ 25	77	0