

C4MS015065L

Switching Optimized 650V 15mΩ Silicon Carbide Power MOSFET

Features

- Industry compatible drive voltage 15V...18V/-5V...0V
- Soft body diode with low Vds overshoot and ringing
- Low Rds(on) at high operating temperatures
- Improved device capacitance ratio (Ciss/Crss)
- High transient voltage robustness with improved lifetime
- Halogen free, RoHS compliant

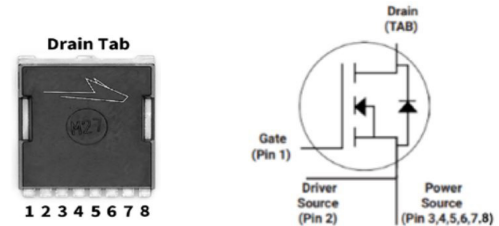
Benefits

- Higher efficiency with lower switching losses and EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system level cooling requirements

Typical Applications

- EV Chargers
- Solar/ESS
- Motor Control
- Industrial Power Supplies
- High Voltage DC/DC Converters

Package



Orderable Part number	Package type	Marking
C4MS015065L-TR	TOLL	C4MS015065L

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			650	V		
Maximum Gate - Source Voltage	$V_{GS(max)}$	-10		+23			
Absolute Maximum Gate-Source Voltage		-10		+25		Only if IPC-9592B derating guidelines are followed	Refer to AN-PRD-09634
DC Continuous Drain Current	I_D		141		A	$V_{GS} = 18V, T_C = 25^\circ C, T_J \leq 175^\circ C$	Note 1
			100			$V_{GS} = 18V, T_C = 100^\circ C, T_J \leq 175^\circ C$	
Pulsed Drain Current	I_{DM}			319		t_{Pmax} limited by T_{Jmax} $V_{GS} = 18V, T_C = 25^\circ C$	
Power Dissipation	P_D		468		W	$T_C = 25^\circ C, T_J = 175^\circ C$	Note 2
Operating Junction and Storage Temperature	T_J	-40		+175	$^\circ C$		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note(1): Current limit calculated by $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)}) / (T_{J(max)} - T_{J(max)})}$

Note(2): $P_D = (T_J - T_C) / R_{th(JC, typ)}$

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	3.9	V	$V_{DS} = V_{GS}, I_D = 12.6\text{ mA}$	Fig. 11 Refer to AN PRD-08999
			2.0		V	$V_{DS} = V_{GS}, I_D = 12.6\text{ mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 18\text{ V}, V_{DS} = 0\text{ V}$	
$V_{GS(op)}$	Operational Turn-On Gate - Source Voltage		+15...+18				See the following for guidelines: Appendix A1& AN PRD-09634
	Operational Turn-Off Gate - Source Voltage		-5...0				
$R_{DS(on)}$	Drain-Source On-State Resistance		15	19.5	m Ω	$V_{GS} = 18\text{ V}, I_D = 45.6\text{ A}$	Fig. 4, 5, 6
			22			$V_{GS} = 18\text{ V}, I_D = 45.6\text{ A}, T_J = 175^\circ\text{C}$	
			18			$V_{GS} = 15\text{ V}, I_D = 45.6\text{ A}$	
g_{fs}	Transconductance		33		S	$V_{DS} = 20\text{ V}, I_D = 45.6\text{ A}, T_J = 25^\circ\text{C}$	Fig. 7
			34			$V_{DS} = 20\text{ V}, I_D = 45.6\text{ A}, T_J = 175^\circ\text{C}$	
$R_{DS(on)Tempco}$	On resistance temperature coefficient		1.47			$V_{GS} = 18\text{ V}, I_D = 45.6\text{ A}$	Note 3
C_{iss}	Input Capacitance		3761		pF	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}$ $f = 100\text{ kHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
C_{oss}	Output Capacitance		237				
C_{rss}	Reverse Transfer Capacitance		8				
E_{oss}	C_{oss} Stored Energy		25		μJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		280		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0...400\text{ V}$	
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		445				
E_{on}	Turn-On Switching Energy (Body Diode FWD) $T_J = 25^\circ\text{C}$		124		μJ	$V_{DS} = 400\text{ V}, V_{GS} = -4\text{ V}/18\text{ V},$ $I_D = 45.6\text{ A},$ $R_{G(ext)} = 2\Omega, L(\sigma) = 25\text{ nH}$	Fig. 25, 27, 28
	$T_J = 175^\circ\text{C}$		131				
E_{off}	Turn-Off Switching Energy (Body Diode FWD) $T_J = 25^\circ\text{C}$		58		μJ	$R_{G(ext)} = 2\Omega, L(\sigma) = 25\text{ nH}$	Fig. 25, 27, 28
	$T_J = 175^\circ\text{C}$		60				
$R_{G(int)}$	Internal Gate Resistance		2.2		Ω	$f = 1\text{ MHz}$	
$t_{d(on)}$	Turn-On Delay Time		12.9		ns	$V_{DD} = 400\text{ V}, V_{GS} = -4\text{ V}/18\text{ V}$ $I_D = 45.6\text{ A}, R_{G(ext)} = 2\Omega,$ Timing relative to I_{DS} Inductive load	Fig. 26, 27, 28
t_r	Rise Time		5.2				
$t_{d(off)}$	Turn-Off Delay Time		40.2				
t_f	Fall Time		9.8				
Q_{gs}	Gate to Source Charge		43		nC	$V_{DS} = 400\text{ V}, V_{GS} = -4\text{ V}/18\text{ V}$ $I_D = 45.6\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		39				
Q_g	Total Gate Charge		146				

Note (3): $R_{DS(on)Tempco}$ refers to $R_{DS(on)}$ at 25°C / $R_{DS(on)}$ at 175°C

Note (4): Capacitance ratio is a FOM for Partial turn-on immunity PRD-06933

 $C_{o(er)}$, a lumped capacitance that gives the same stored energy as C_{oss} while V_{ds} is rising from 0 to 400V $C_{o(tr)}$, a lumped capacitance that gives the same charging time as C_{oss} while V_{ds} is rising from 0 to 400V

Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	$V_{GS} = -4\text{ V}, I_{SD} = 22.8\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.5		V	$V_{GS} = -4\text{ V}, I_{SD} = 22.8\text{ A}, T_J = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current	74		A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
I_{SM}	Diode Pulse Current		319	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{Jmax}	
t_{rr}	Reverse Recovery Time	10.4		ns	$V_{GS} = -4\text{ V}, I_S = 45.6\text{ A}, V_{SD} = 400\text{ V}$ $T_J = 175^\circ\text{C}, diF/dt = 10971\text{ A}/\mu\text{s}$	
Q_{rr}	Reverse Recovery Charge	448.5		nC		
I_{RRM}	Peak Reverse Recovery current	73		A		
E_{RR}	Reverse recovery Energy			mJ	$V_{DS} = 400\text{ V}, I_D = 45.6\text{ A},$ $V_{GS} = -4\text{ V}/18\text{ V}, R_{G(on)} = 2\ \Omega, L_\sigma = 25\text{ nH}$	
	$T_J = 25^\circ\text{C}$	0.14				
	$T_J = 175^\circ\text{C}$	0.15				

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.32	$^\circ\text{C}/\text{W}$		

Typical Performance

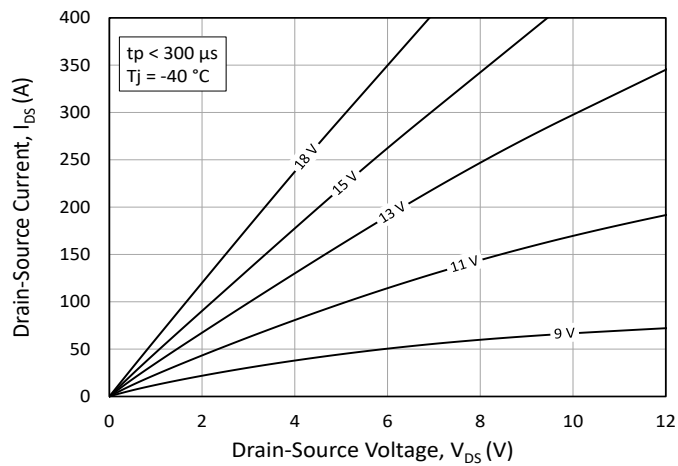
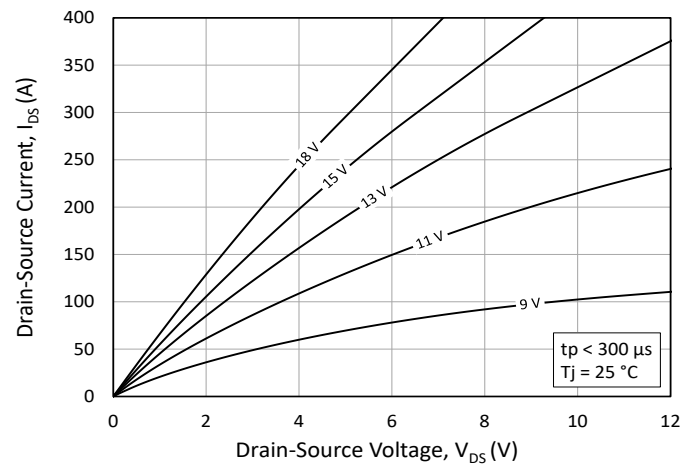
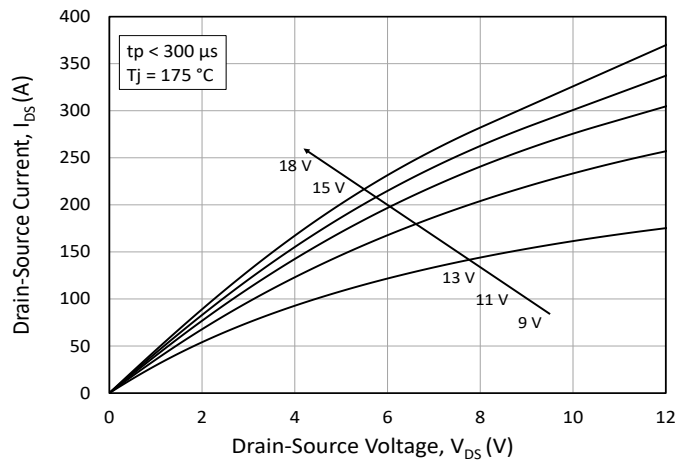
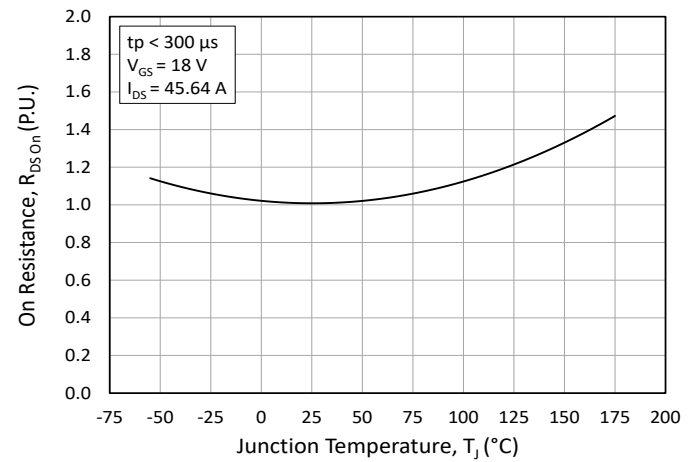
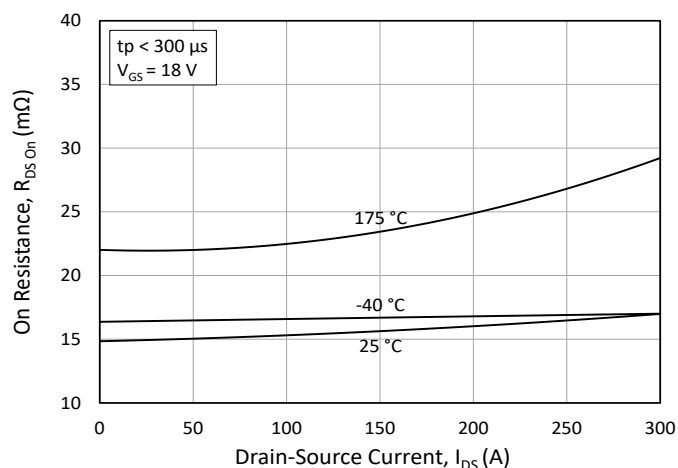
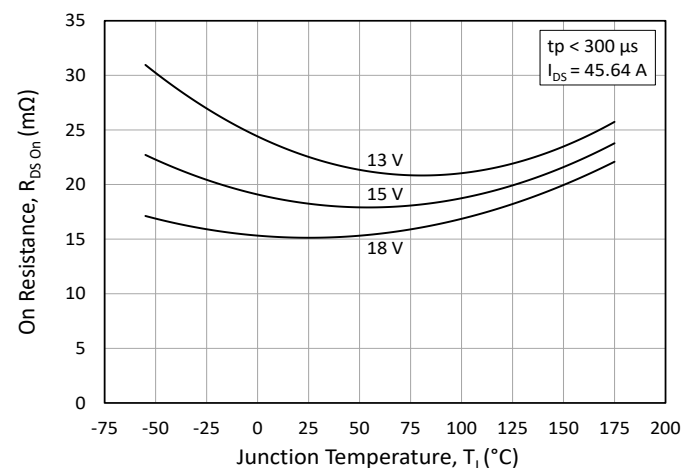
Figure 1. Output Characteristics $T_j = -40^{\circ}\text{C}$ Figure 2. Output Characteristics $T_j = 25^{\circ}\text{C}$ Figure 3. Output Characteristics $T_j = 175^{\circ}\text{C}$ 

Figure 4. Normalized On-Resistance vs. Temperature

Figure 5. On-Resistance vs. Drain Current
For Various TemperaturesFigure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

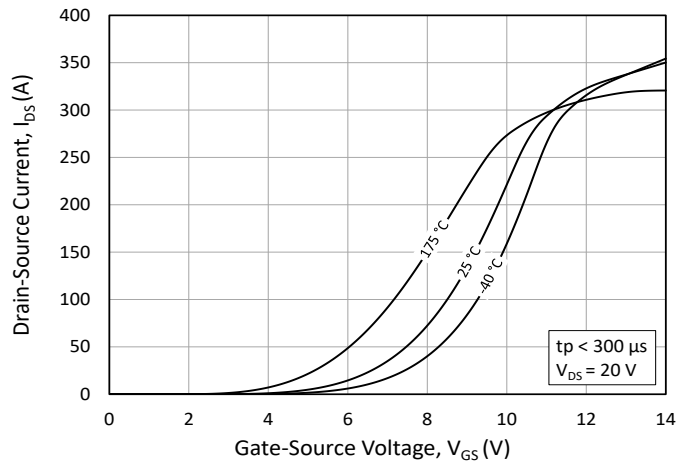


Figure 7. Transfer Characteristic for Various Junction Temperatures

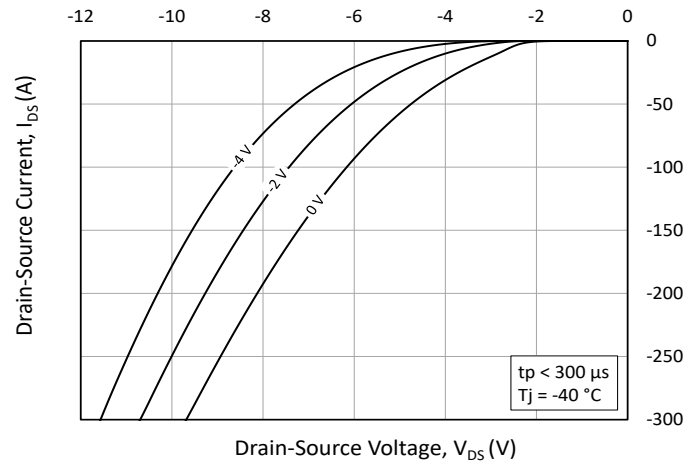


Figure 8. Body Diode Characteristic at -40 °C

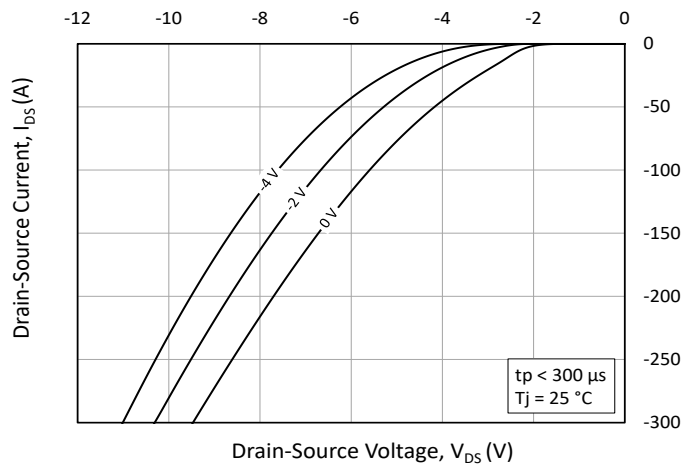


Figure 9. Body Diode Characteristic at 25 °C

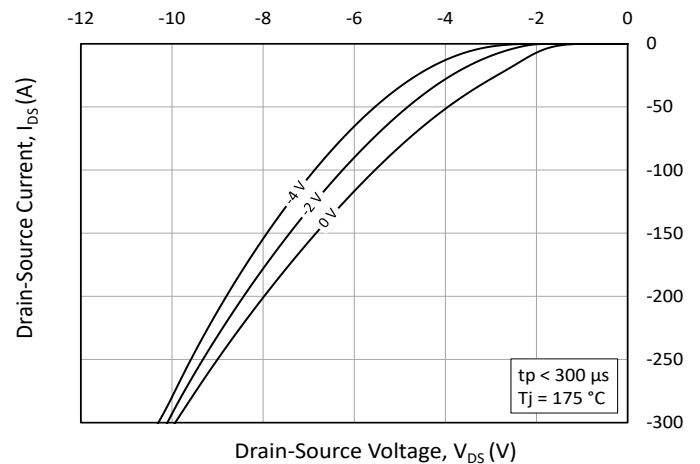


Figure 10. Body Diode Characteristic at 175 °C

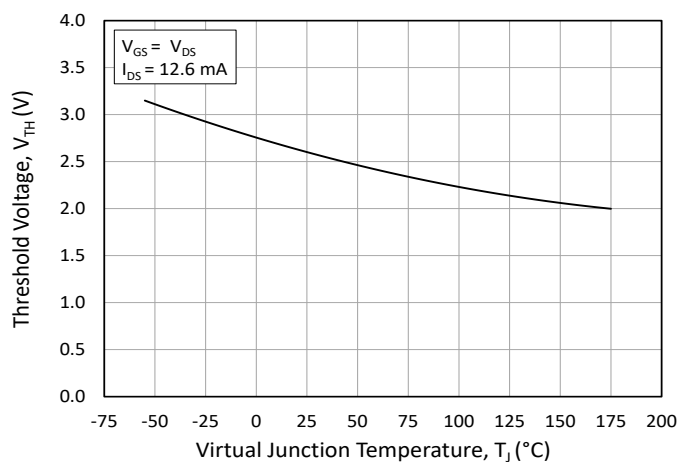


Figure 11. Threshold Voltage vs. Temperature

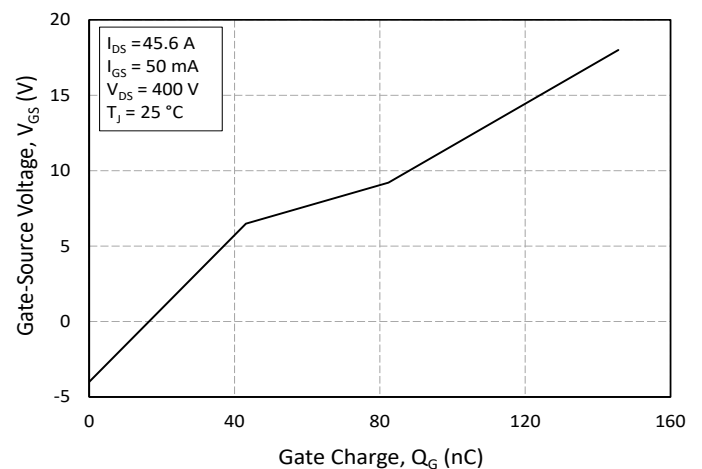


Figure 12. Gate Charge Characteristics

Typical Performance

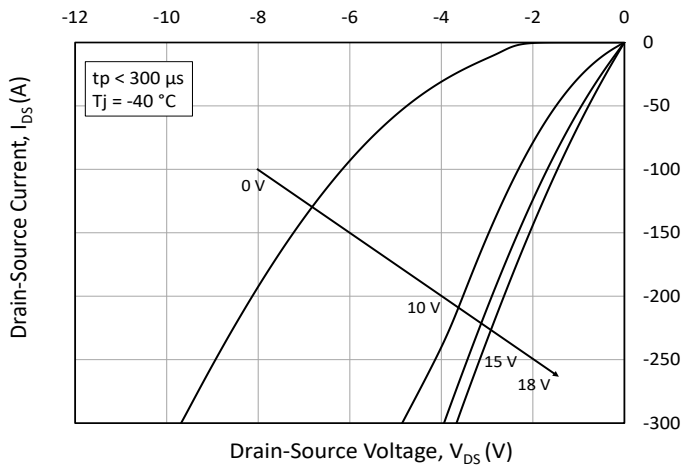


Figure 13. 3rd Quadrant Characteristic at -40°C

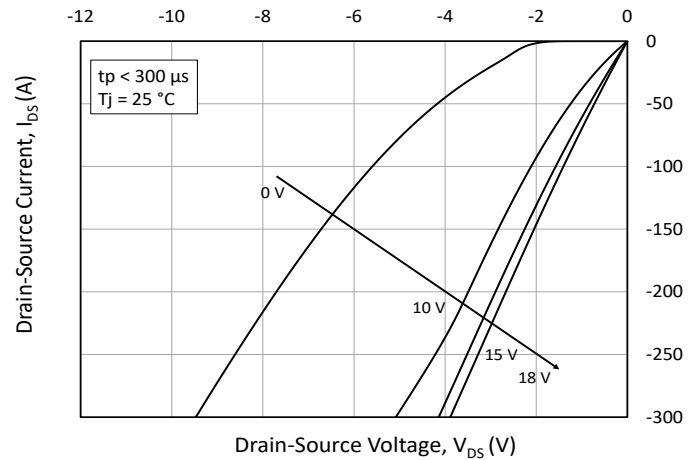


Figure 14. 3rd Quadrant Characteristic at 25°C

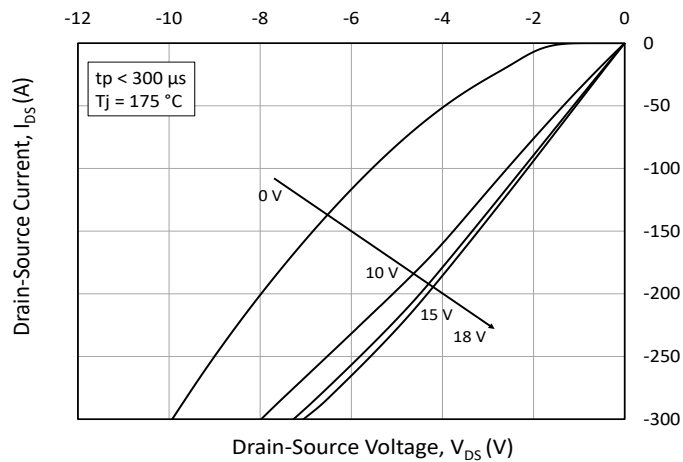


Figure 15. 3rd Quadrant Characteristic at 175°C

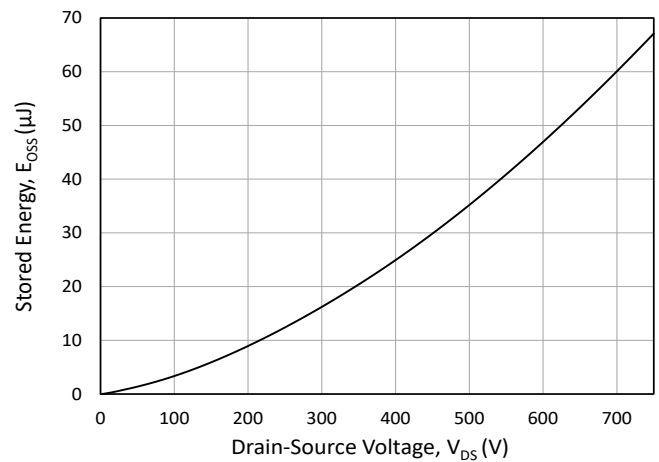


Figure 16. Output Capacitor Stored Energy

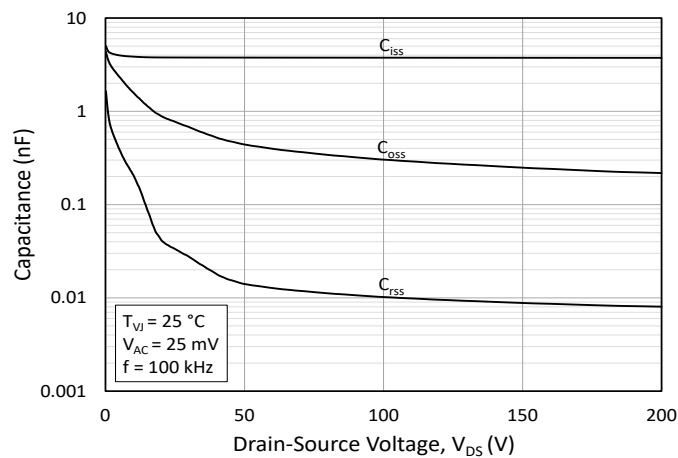


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

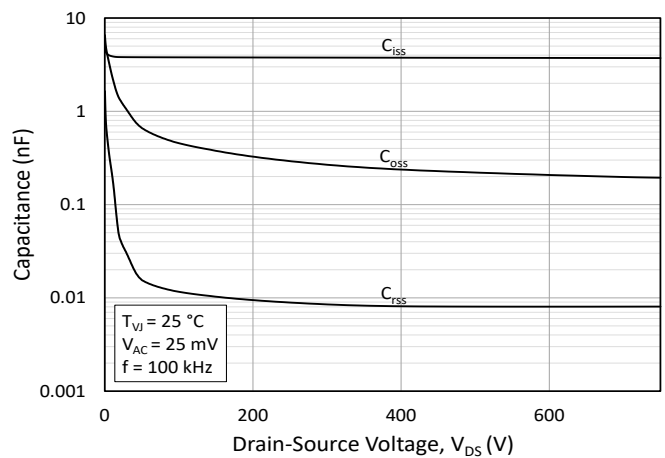


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650 V)

Typical Performance

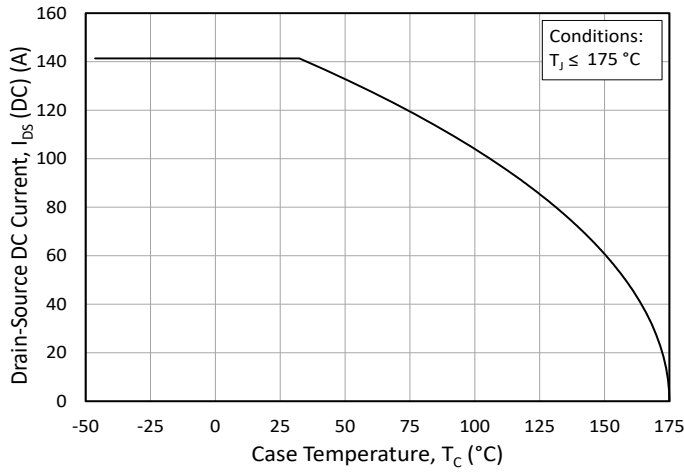


Figure 19. Continuous Drain Current Derating vs. Case Temperature

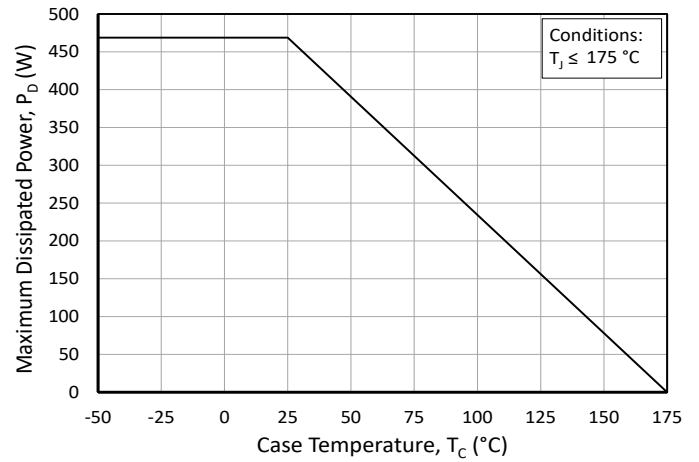


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

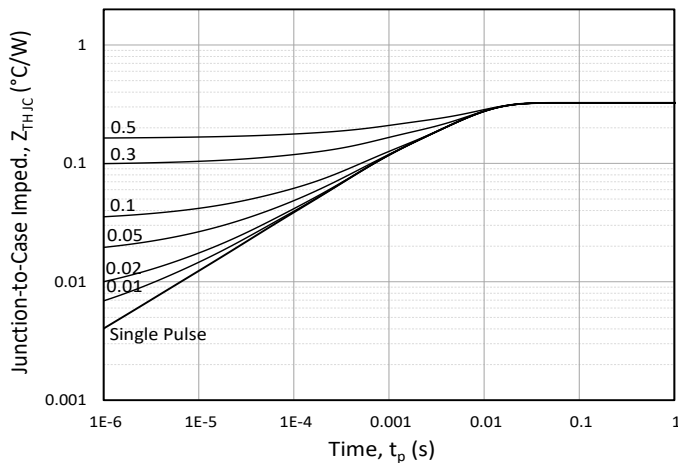


Figure 21. Transient Thermal Impedance (Junction - Case)

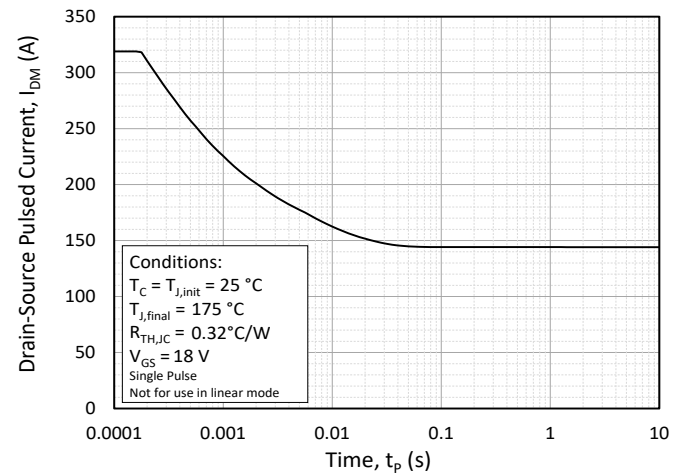
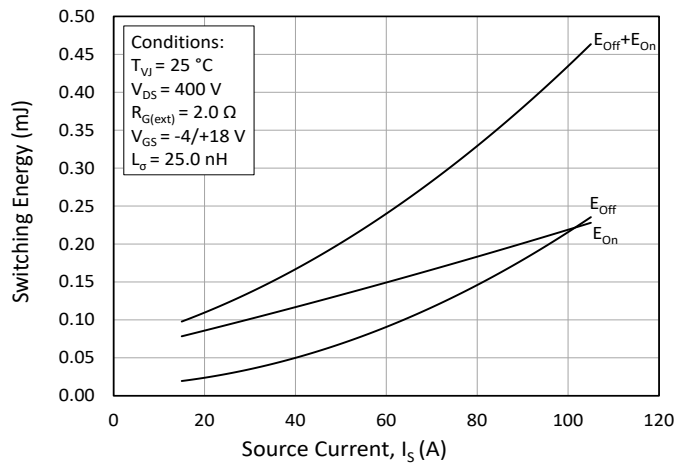
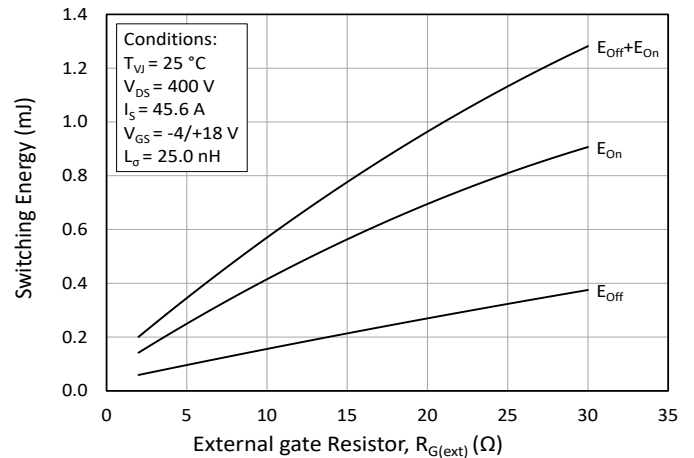


Figure 22. Safe Operating Area

Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 400 \text{ V}$)Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

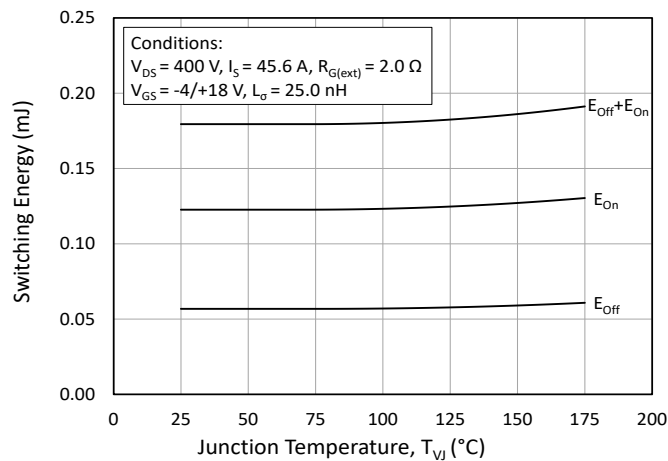


Figure 25. Clamped Inductive Switching Energy vs. Temperature

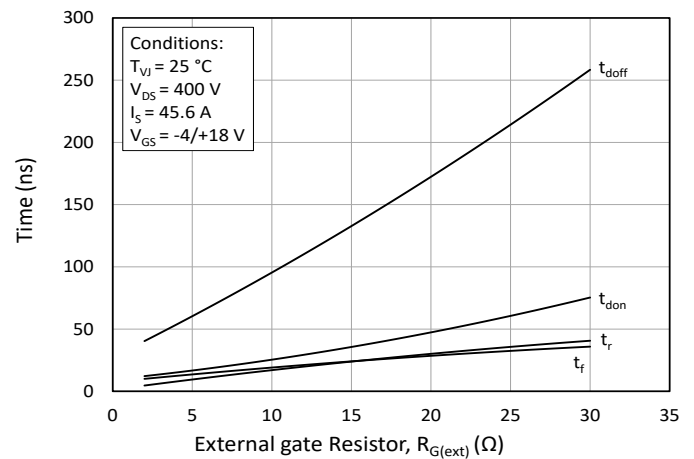


Figure 26. Switching Times vs. $R_{G(ext)}$

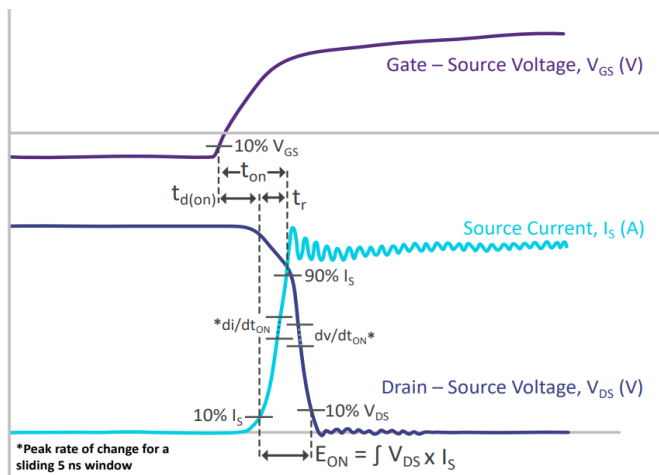


Figure 27. Turn On Switching Times Definition

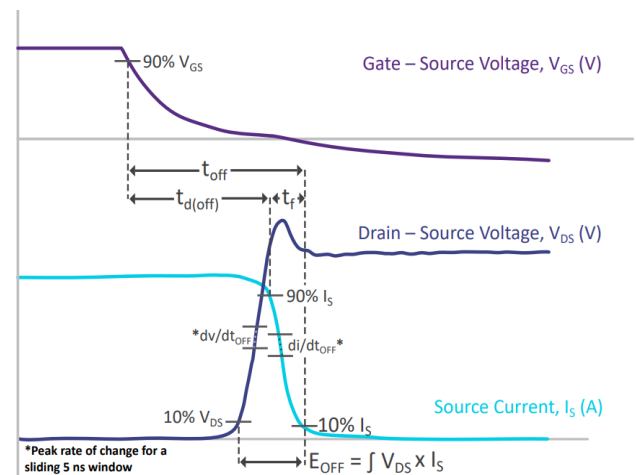


Figure 28. Turn Off Switching Times Definition

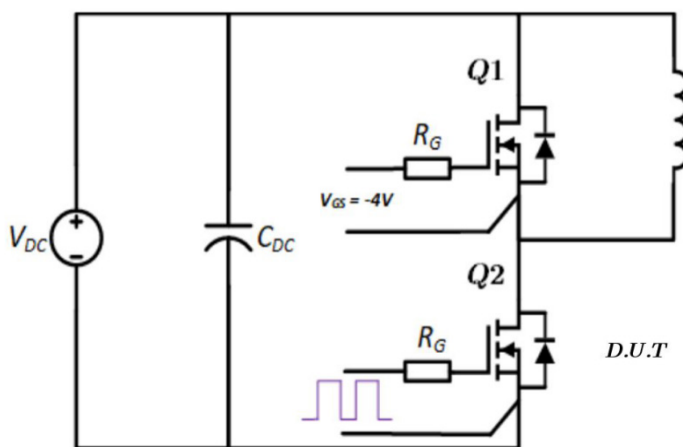


Figure 29. Clamped Inductive MOSFET Switching Waveform Test Circuit

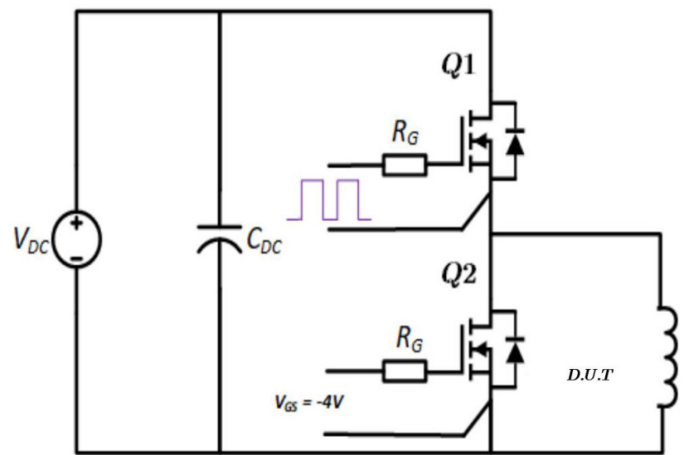
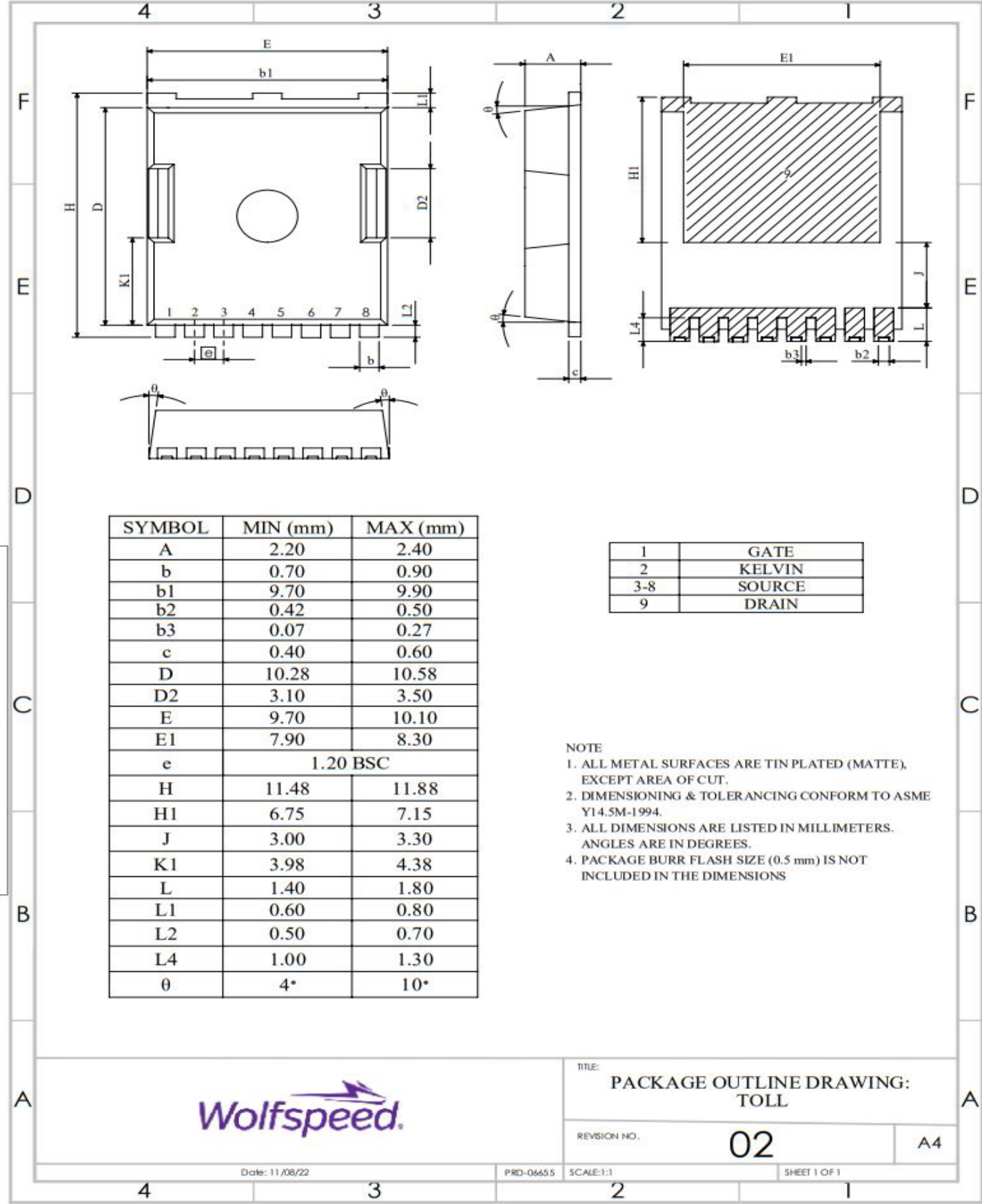


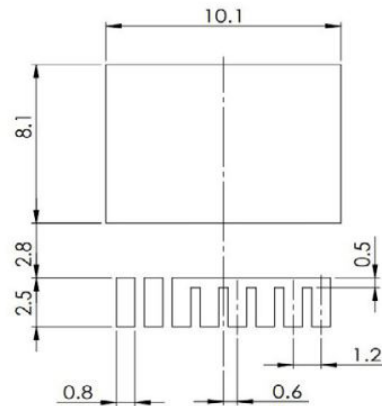
Figure 30. Clamped Inductive Body diode Switching Waveform Test Circuit

Package Dimensions



Recommended Solder Pad Layout

All dimensions in mm





Revision history

Document Version	Date of release	Description of changes
1	April 2026	Initial Release

Appendix

Appendix number	Description
A1	Following are some recommendations for 0V Gate Bias: - o Measure the VGS spike accurately using high-CMRR probes and low common mode noise measurements - o For the safe operation of the device the voltage spike shall remain <5V for a time duration of <40 ns



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