User Guide **PRD-10001**

CRD60DD12N-GMB 60 kW Isolated DC/DC User Guide

This document is prepared as a user guide to install and operate Wolfspeed® evaluation hardware.

All parts of this user guide are provided in English, and the Cautions are provided in English, Mandarin, and Japanese. If the end user of this board is not fluent in any of these languages, it is your responsibility to ensure that they understand the terms and conditions described in this document, including without limitation the hazards of and safe operating conditions for this board.

本文件中的所有内容均以英文书写，“注意”部分的内容以英文、中文和日语书写。作为本板子的终端用户，即使您不熟悉上述任何一种语言，您也应当确保正确理解本文件中的条款与条件，包括且不限于本板子的危险隐患以及安全操作条款。

当書類のすべての内容は英語で書きます。「注意点」の内容は英語、中国語、また日本語で書きます。当ボードの端末使用者は上記の言語が一つでもわからないなら、当端末使用者は当書類の条約と条件が理解できるのを確保すべきです。そして、当ボードの危険や安全に使用する条件を含み、また限りません。

Note: This Wolfspeed-designed evaluation hardware for Wolfspeed® components is a fragile, high-voltage, high-temperature power electronics system that is meant to be used as an evaluation tool in a lab setting and to be handled and operated by highly qualified technicians or engineers. When this hardware is not in use, it should be stored in an area that has a storage temperature ranging from -40° Celsius to 105° Celsius. If this hardware is transported, to avoid any damage to electronic components, special care should be taken during transportation to avoid damaging the board or its fragile components and the board should be transported carefully in an electrostatic discharge (ESD) bag, or with ESD or shorting protection that is the same as, or similar to, the protection that is or would be used by Wolfspeed when shipping this hardware. Please contact Wolfspeed at https://forum.wolfspeed.com/ if you have any questions about the protection of this hardware during transportation (and please rely only on forum responses from responders identified as Wolfspeed employees). The hardware does not contain any hazardous substances, is not designed to meet any industrial, technical, or safety standards or classifications, and is not a production-qualified assembly.

注意：本样机（易碎、高压、高温电力电子系统）由Wolfspeed为评估其功率半导体产品而设计，用以作为在实验室环境下由专业的技术人员或工程师处理和使用的评估工具。本样机不使用时，应存储在-40°C~105°C温度范围的区域内；如需运输样机，运输过程中应该特别小心，避免损坏电路板等易碎组件，且电路板应妥善放置于防静电 (ESD) 包装袋中，或采用其他与Wolfspeed发货时相同或类似的防静 电或短路保护措施。如果您对此硬件在运输之中的保护有任何疑问，请访问 https://forum.wolfspeed. com/，联系Wolfspeed。本样机不含任何有害物质，但其设计并非设计用于符合任何工业、技术或安全标准或分类，也不是可用于生产的组件。

注：Wolfspeed®コンポーネント向けにWolfspeedが設計したこの評価用ハードウェアは、脆弱な高電圧・高温パワーエレクトロニクスシステムであり、ラボ環境での評価ツールとして使用され、高度な資格を有する技術者またはエンジニアによって取り扱われ、操作されることを意図しています。このハードウェアを使用しない場合は、保管温度範囲が-40°Cから105°Cの場所で保管してください。このハードウェアを輸送する場合は、電子部品の損傷を避けるため、基板やその脆弱なコンポーネントに損傷を与えないよう特別な注意を払う必要があります。また基板は静電気放電（ESD）袋で慎重に輸送するか、Wolfspeedがこのハードウェアを輸送する際に使用している、または使用するであろう保護と同等または類似のESD保護または短絡保護を施してください。ハードウエアの輸送中の保護に関するご質問は、https://forum.wolfspeed.com/までお問い合わせください（フォーラムの回答をご覧になる場合は、Wolfspeed従業員が回答者であることが明記された投稿のみを参考にしてください）。このハードウェアは有害物質を含んでいませんが、いかなる産業・技術・安全基準または分類に適合するように設計されておらず、本番環境に適したアセンブリでもありません。

CAUTION

PLEASE CAREFULLY REVIEW THE FOLLOWING PAGES, AS THEY CONTAIN IMPORTANT INFORMATION REGARDING THE HAZARDS AND SAFE OPERATING REQUIREMENTS RELATED TO THE HANDLING AND USE OF THIS BOARD.

DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE BOARD. THERE CAN BE VERY HIGH VOLTAGES PRESENT ON THIS EVALUATION BOARD WHEN CONNECTED TO AN ELECTRICAL SOURCE, AND SOME COMPONENTS ON THIS BOARD CAN REACH TEMPERATURES ABOVE 50˚ CELSIUS. FURTHER, THESE CONDITIONS WILL CONTINUE FOR A SHORT TIME AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED.

Please ensure that appropriate safety procedures are followed when operating this board, as any of the following can occur if you handle or use this board without following proper safety precautions:

DEATH ▲ SERIOUS INJURY ▲ ELECTROCUTION ▲ ELECTRICAL SHOCK ▲ ELECTRICAL BURNS ▲ SEVERE HEAT BURNS

You must read this document in its entirety before operating this board. It is not necessary for you to touch the board while it is energized. All test and measurement probes or attachments must be attached before the board is energized. You must never leave this board unattended or handle it when energized, and you must always ensure that all bulk capacitors have completely

警告

请认真阅读以下内容，因为其中包含了处理和使用本板子有关的危险隐患和安全操作要求方面的重要信息。

请勿在通电情况下接触板子，在操作板子前应使大容量电容器的电荷完全释放。接通电源后，该评估板上通常会存在危险的高电压，板子上一些组件的温度可能超过50摄氏度。此外，移除电源后，上述情况可能会短时持续，直至大容量电容器电量完全释放。

操作板子时应确保遵守正确的安全规程，否则可能会出现下列危险：

死亡 ▲ 严重伤害 ▲ 触电 ▲ 电击 ▲ 电灼伤 ▲ 严重的热烧伤

请在操作本板子前完整阅读本文件。通电时禁止接触板子。所有测试与测量探针或附件必须在板子通电前连接。通电时，禁止使板子处于无人看护状态，且禁止操作板子。必须确保在操作板子前，大容量电容器已释放了所有电量。只有在切断板子电源，且大容量电容器完全放电后，才可更换待测试器件。

警告

ボードの使用、危険の対応、そして安全に操作する要求などの大切な情報を含むので、以下の内容をよく読んでください。

通電している時、ボードに接触するのは禁止です。ボードを処分する前に、大容量のコンデンサーで電力を完全に釈放すべきです。通電してから、ボードにひどく高い電圧が存在している可能性があります。ボードのモジュールの温度は50度以上になるかもしれません。また、電源を切った後、上記の状況がしばらく持続する可能性がありますので、大容量のコンデンサーで電力を完全に釈放するまで待ってください。

ボードを操作するとき、正確な安全ルールを守るのを確保すべきです。さもないと、以下の危険がある可能性があります:

死亡 ▲ 重症 ▲ 感電 ▲ 電撃 ▲ 電気の火傷 ▲ 厳しい火傷

当ボードを操作する前に、完全に当書類をよく読んでください。通電している時にボードに接触する必要がありません。通電する前に必ずすべての試験用のプローブあるいはアクセサリーをつないでください。通電している時に無人監視やボードを操作するのは禁止です。ボードを操作する前に、大容量のコンデンサーで電力を完全に釈放するのを必ず確保してください。ボードの電源を切った後、また大容量のコンデンサーで電力を完全に釈放した後、試験設備を取り換えることができます。

CRD60DD12N-GMB 60 kW Isolated DC/DC User Guide

Contents

1. Introduction

This user guide provides an overview of the Wolfspeed CRD60DD12N-GMB 60 kW isolated DC/DC converter reference design including key system specifications, sub-system functional descriptions, performance test data, and mechanical assembly. The CRD60DD12N-GMB design, shown in Figure 1, was developed to provide power electronics engineers with a hardware evaluation platform and reference design files to support early design-in activities of the Generation 4 Wolfspeed WolfPACK™ baseplate-less power module platform. The design is a dual active bridge (DAB) isolated DC/DC converter topology for use as the isolation and output regulation stages of applications such as electric vehicle (EV) fast chargers, energy storage, and renewable energy. In conjunction with this user guide, the complete suite of reference design files including schematics, printed circuit board (PCB) layout, Gerber files, bill of materials (BOM), and 3D mechanical files are available for download from the CRD60DD12N-GMB landing page on the Wolfspeed website.

Figure 1: CRD60DD12N-GMB 60 kW isolated DC/DC converter

The CRD60DD12N-GMB is an easy-to-use, flexible power stage designed around the CBB011M12GM4T (1200 V / 11 mΩ) Wolfspeed WolfPACK full-bridge power module shown in Figure 2. The module utilizes Wolfspeed's 4th generation MOSFET technology which features improved switching performance and a softer body diode compared to previous generations. The modules include pre-applied phase-changing thermal interface material (TIM) for strong thermal performance and easy system-level integration.

Figure 2: CBB011M12GM4T, 1200 V, 11 mΩ full-bridge power module

A high-level overview of the system architecture is provided in the block diagram shown in Figure 3. The design incorporates DC-link capacitance on both the primary and secondary sides of the converter, with low-inductance power planes connecting to the power modules to minimize parasitic effects. The power stage consists of two full-bridge modules – one on the primary side and one on the secondary side – which are electrically isolated from each other. Both modules are mounted on a shared liquid-cooled coldplate featuring integrated pin-fin structures beneath the power devices to enhance thermal performance.

The design also includes designated mounting points for a transformer, along with integrated current sensing to monitor transformer current as well as input and output DC currents. A general-purpose embedded controller is included, pre-loaded with baseline firmware to enable immediate operation. The firmware can be readily updated to support customization or further development. Additionally, the gate driver circuitry provides comprehensive protection and control features, including desaturation-based overcurrent protection, Miller clamping, independently configurable turn-on and turn-off gate resistors, and thermistor-based temperature feedback from the power modules for substrate temperature monitoring.

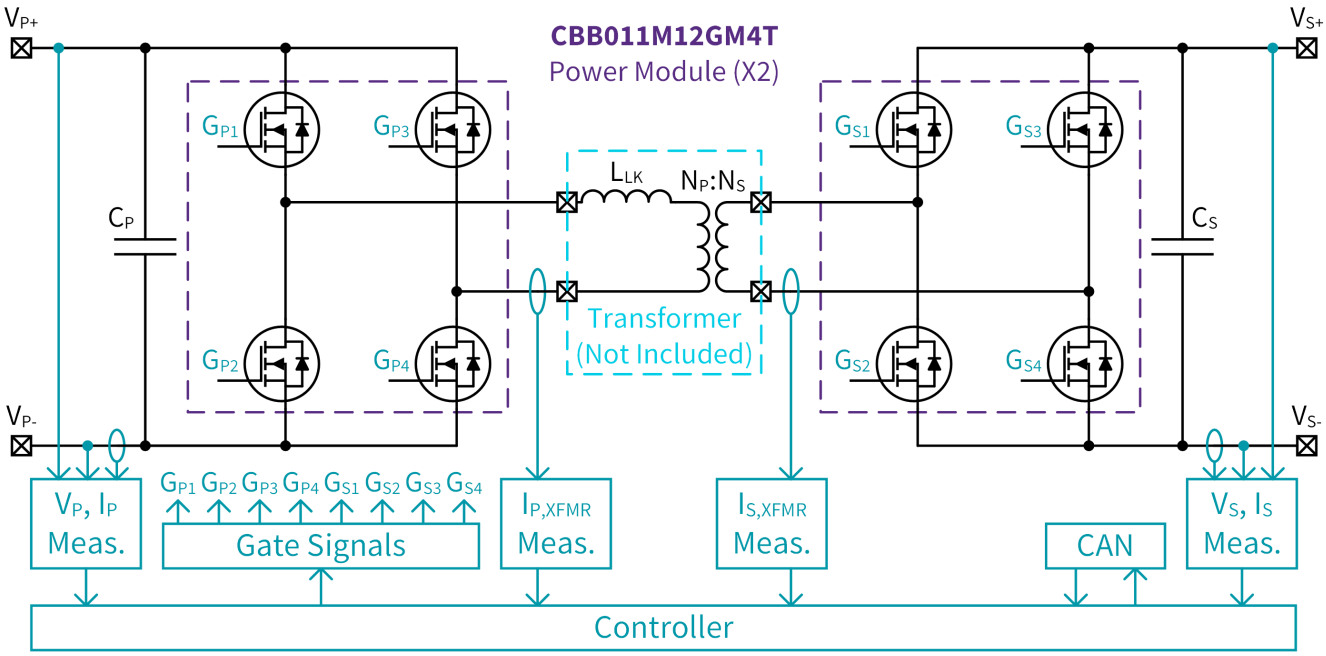

Figure 3: CRD60DD12N-GMB block diagram

By default, the CRD60DD12N-GMB is configured for evaluation as an isolated dual active bridge converter. However, because the design incorporates two electrically isolated full-bridge stages, the platform can be readily adapted to support other isolated converter topologies, such as series resonant converters, through the use of an appropriate transformer and external resonant components. This flexibility makes the system well suited for the evaluation, development, and scaling of high-power solutions in applications including EV fast charging, energy storage systems, and renewable energy conversion.

2. Design Features

This section highlights the design features of the CRD60DD12N-GMB design including key system specifications, a description of the various functional circuit groups, and a general input/output (I/O) pinout definitions.

2.1 Key System Specifications

- Two CBB011M12GM4T (1200 V / 11 mΩ) Wolfspeed WolfPACK full-bridge power modules
- General purpose controller (Texas Instruments® TMDSCNCD280039C) with customizable firmware
- Isolated temperature measurement included on the module substrates for temperature monitoring
- Isolated CAN communication for real-time monitoring and adjustments
- Separate turn-on and turn-off gate resistors for switching loss optimization
- Primary and secondary bulk capacitance with low-inductance routing in a compact form factor
- Isolated DC bus measurement circuitry for both the primary and secondary
- Isolated DC and transformer current measurements for both the primary and secondary
- Integrated desaturation overcurrent protection on all switch positions
- Cold plate design with integrated pin fins for improved cooling
- Gate measurement connectors for easy system troubleshooting and evaluation

Table 1: CRD60DD12N-GMB ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output Power	P_{OUT}	—	—	60	kW
Input DC Bus Voltage	V_{IN}	700	800	900	V
Output DC Bus Voltage[1]	V_{OUT}	400	800	900	V
Output Current	I_{OUT}	—	—	100	A
Switching Frequency (Fixed)	f_{sw}	—	100	—	kHz
Thermal Resistance, Coldplate-to-Fluid	$R_{th,ja}$	—	0.045	—	°C/W

[1] Power is derated for output voltages less than 600 V

2.2 Subsystem Functional Groups

The design is a combination of two printed circuit boards as shown in Figure 4. Renderings of the full assembly of circuit boards are shown in Figure 5 and Figure 6. The *Controller Stage*, shown in Figure 7 and abbreviated **CTRL** throughout this document, includes gate drivers, programmable general-purpose controller, and low-voltage peripherals to communicate with and operate the dual active bridge. The *Power Stage*, shown Figure 8 and abbreviated **PWR** throughout this document, includes the SiC power modules, bulk capacitors, and transformer connections. It connects all the high-power components through low-inductance routing. The various subsystem functional groups of this reference design are shown from the top and side profile views in Figure 9. A brief description of each of the labeled subsystems is provided in Table 2 with further details about each of the subsystems described in later parts of this document.

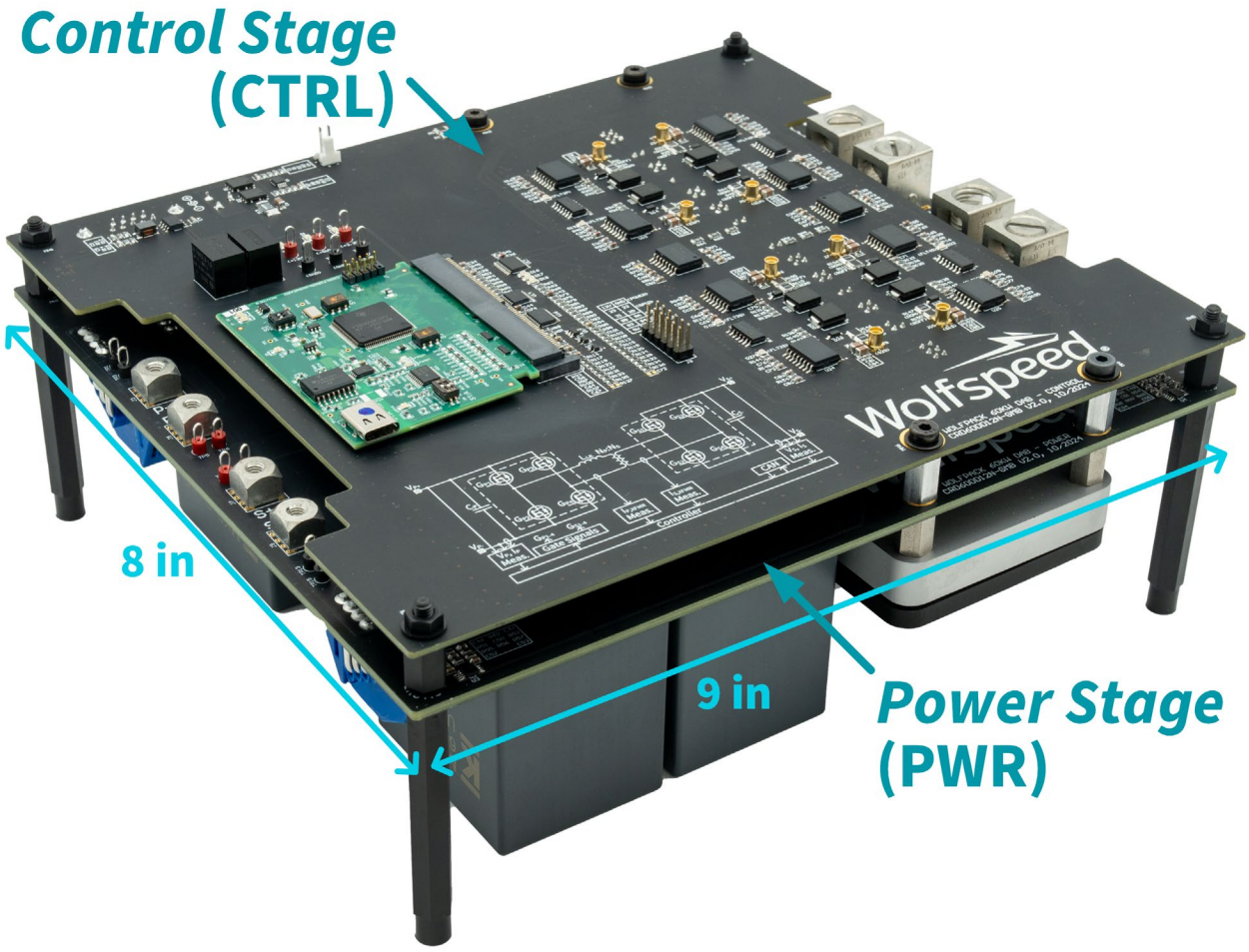

Figure 4: Circuit board labels on CRD60DD12N-GMB

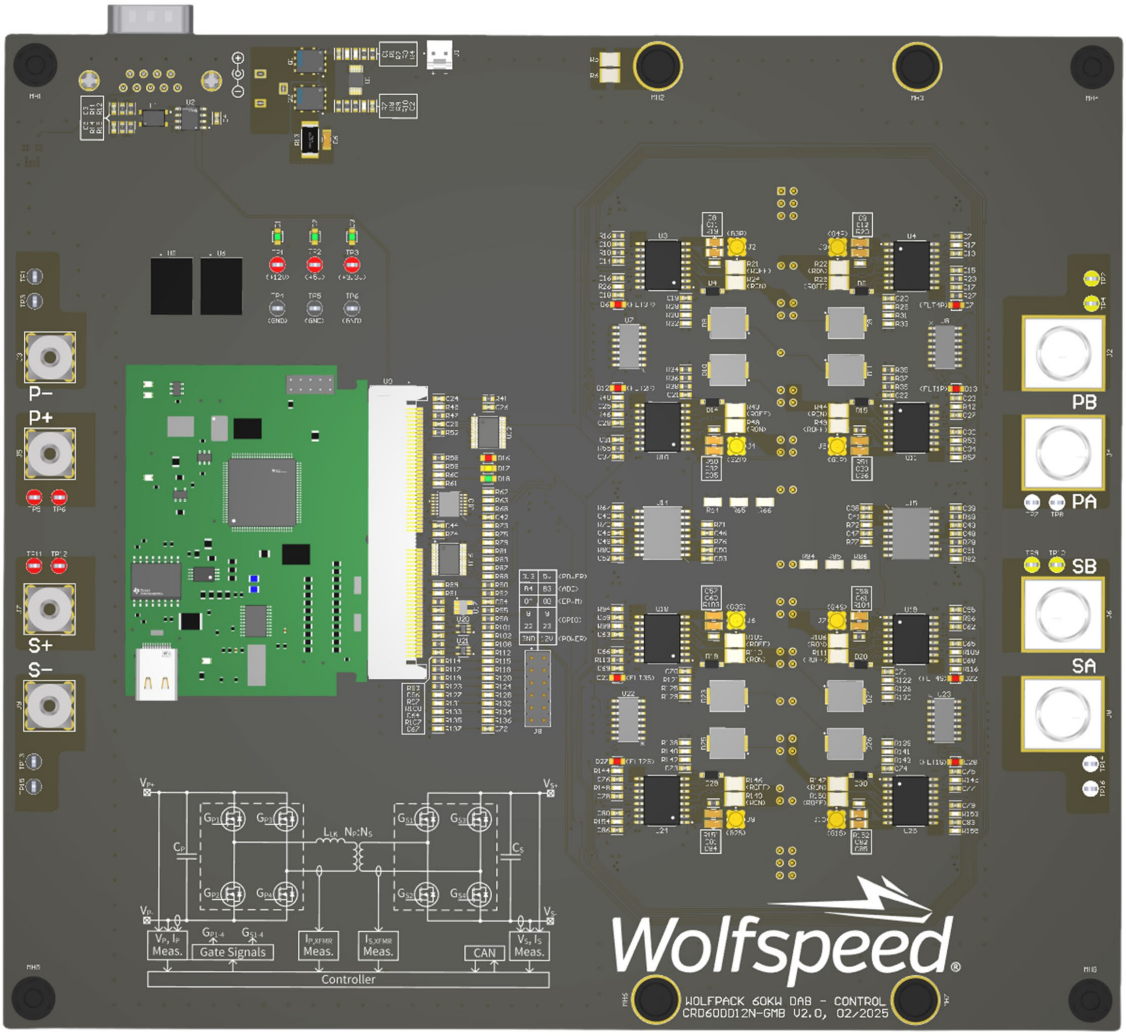

Figure 5: CRD60DD12N-GMB full assembly rendering - top view

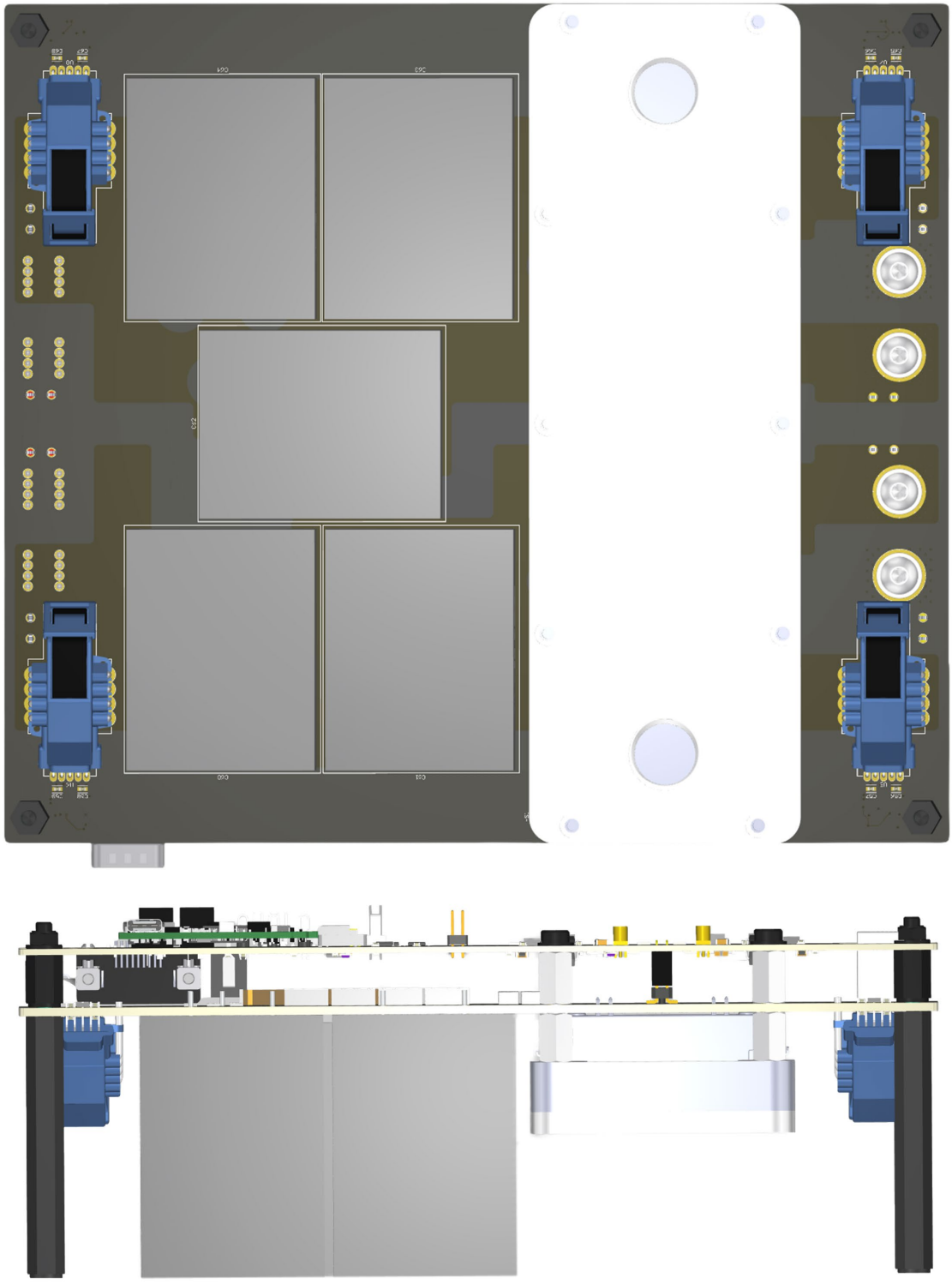

Figure 6: CRD60DD12N-GMB full assembly renderings - bottom and side views

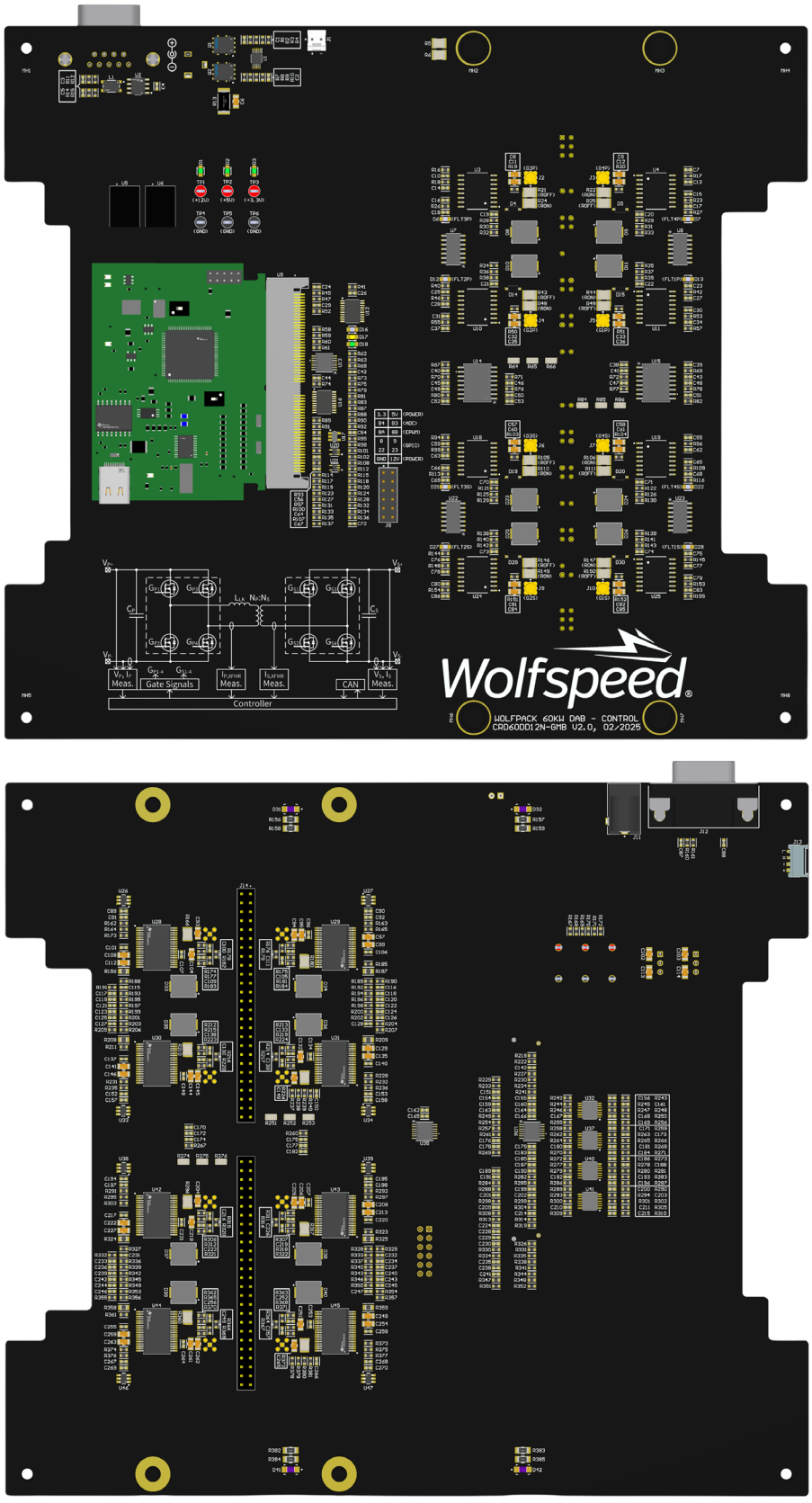

Figure 7: CRD60DD12N-GMB Control Stage renderings – top and bottom views

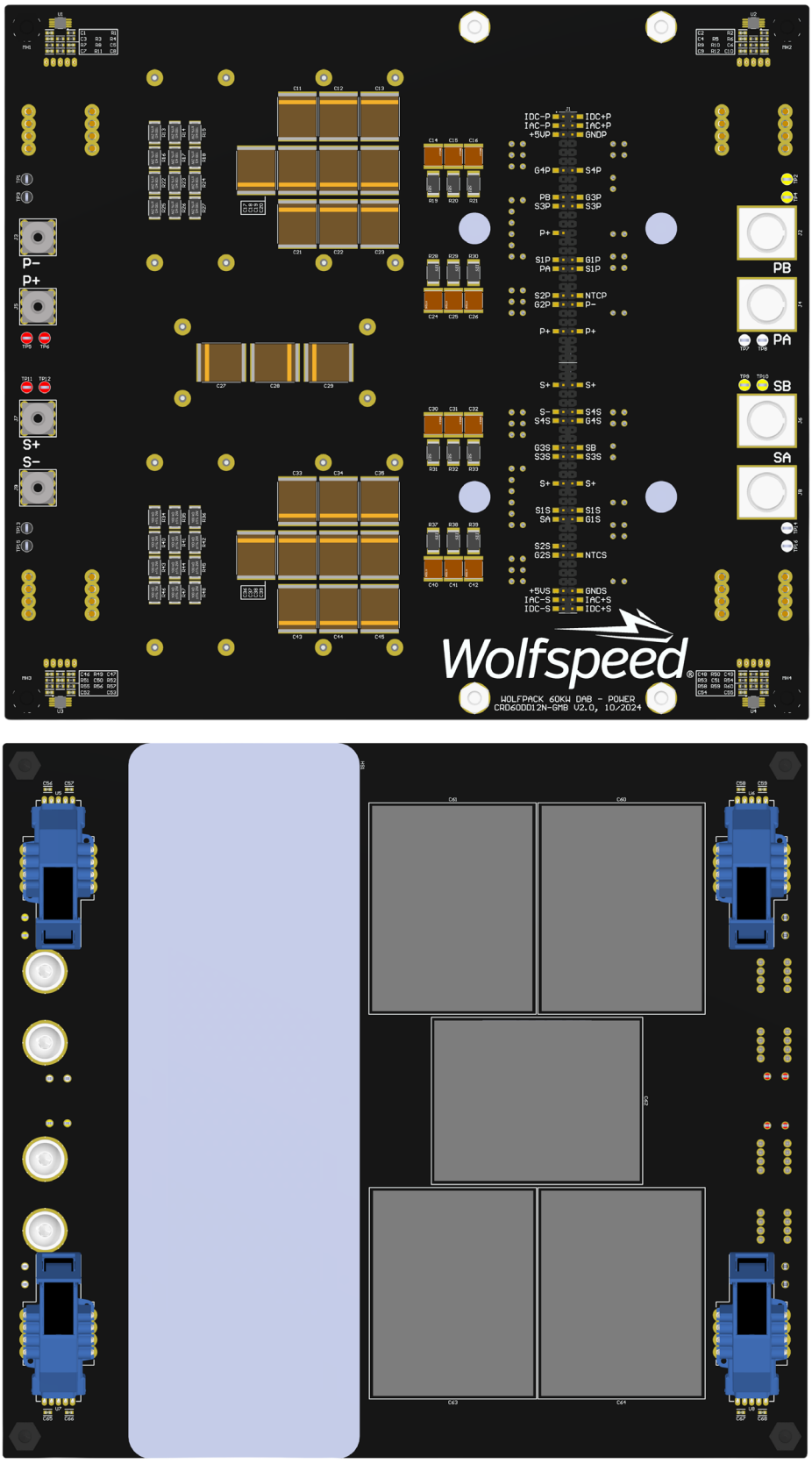

Figure 8: CRD60DD12N-GMB Power Stage board renderings – top and bottom views

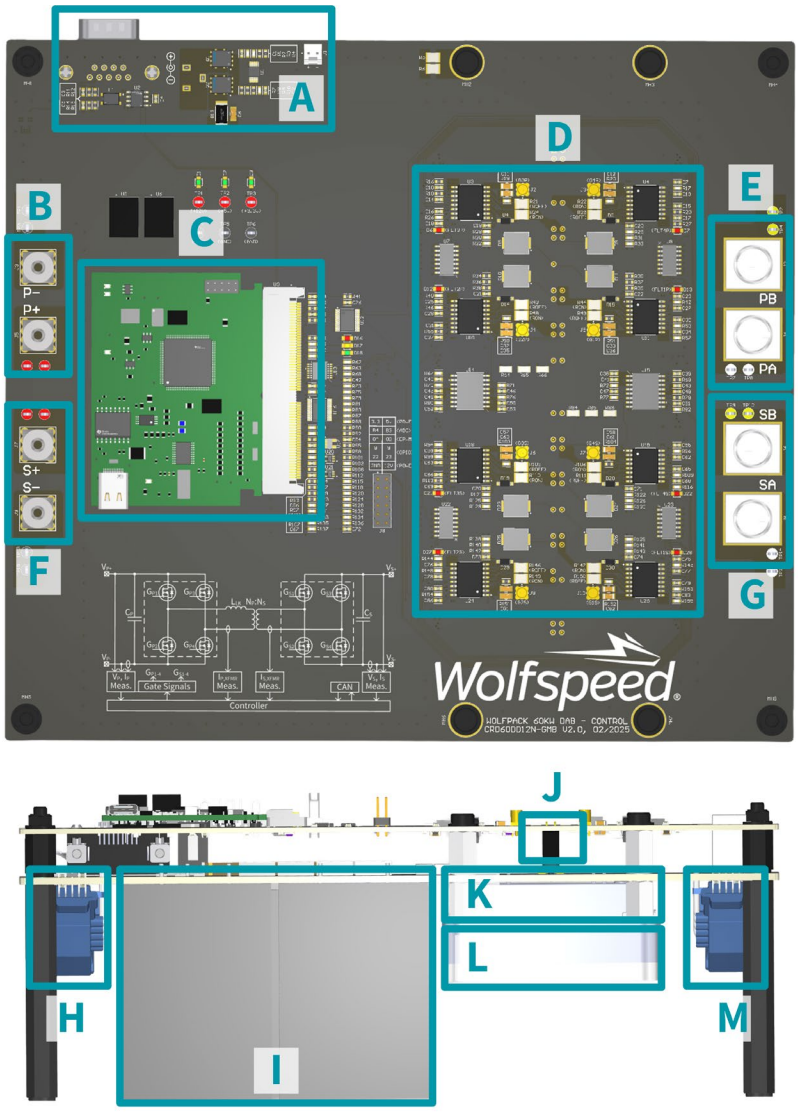

Figure 9: CRD60DD12N-GMB subsystems

Table 2: Subsystem functional group descriptions

Label	Description	Label	Description
A	Low-Voltage Peripherals	**H**	DC Current Measurements
B	Primary-Side DC Power Terminals	**I**	Bulk DC Capacitors
C	Controller	**J**	Circuit Board Interface Connector
D	Gate Drivers	**K**	CBB011M12GM4T Power Modules
E	Primary-Side AC Power Terminals	**L**	Liquid-Cooled Custom Coldplate
F	Secondary-Side DC Power Terminals	**M**	AC Current Measurements
G	Secondary-Side AC Power Terminals		

2.3 Input/Output Pinout

This design features a variety of ports for connecting power bussing, attaching peripherals, and communicating directly with the onboard controller. Each of these interfaces will be discussed in the later sections of this document. This section provides a quick reference to the pinouts of the various ports.

2.3.1 High Power Terminals

The high-power DC connections, shown in Figure 10, are made through Würth Elektronik® 7460307 terminals. These terminals are attached to the PCB through a press-fit process and require no solder for the PCB connection. The terminals include internal M4 threads to support mounting high-power wires or bus bars directly to the terminals using M4 screws. The high-power AC connections, also shown in Figure 10, are made through McMaster-Carr® 4164N12 lugs. These connectors are for both the primary and secondary sides of the high-frequency isolation transformer; these lugs can accept Litz wire with soldered terminations which are typical for high-frequency, high-power transformers.

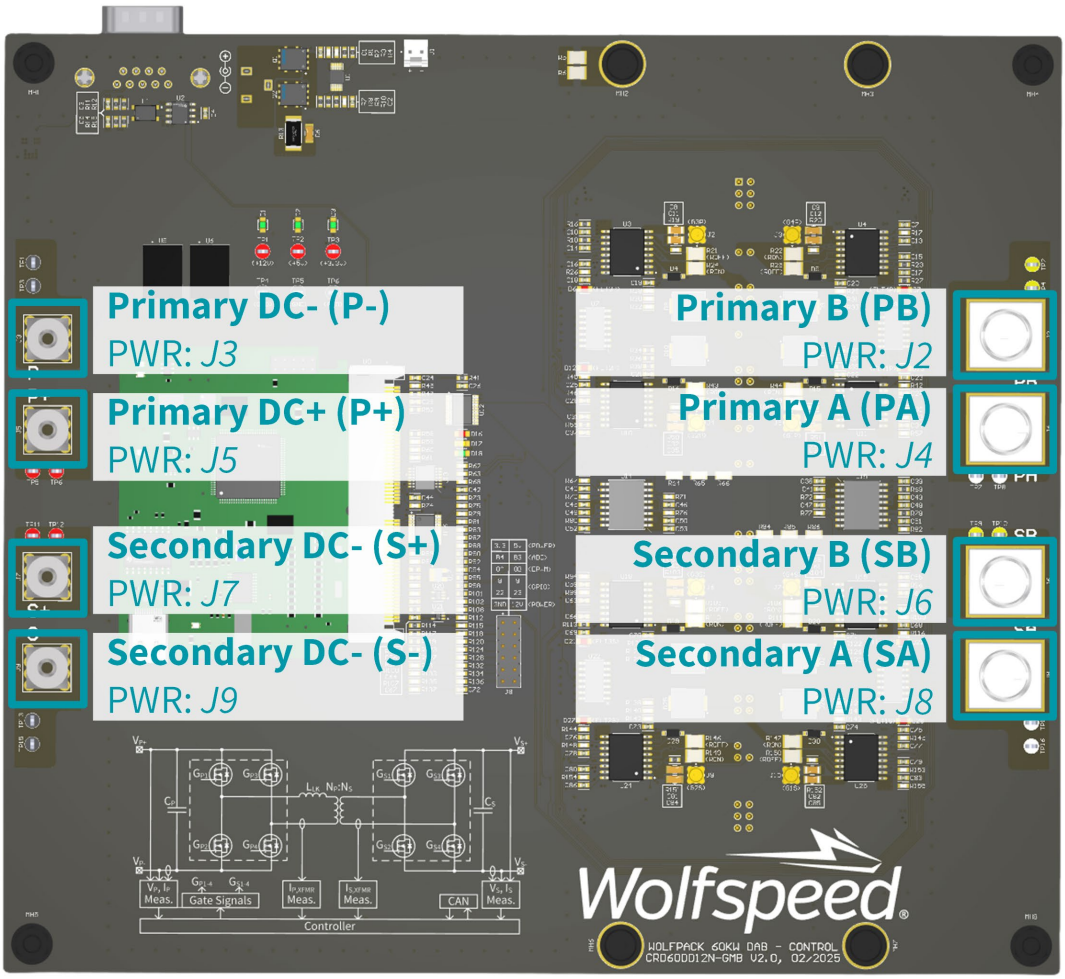

Figure 10: High-power terminal locations

2.3.2 Controller Power Connector Pinout

The controller board is powered from an external +12 V auxiliary power supply. The power is applied through a CUI Devices® PJ-102AH barrel connector (*J11* on the *Control Stage*) with the pinout shown in Figure 11. This connector is located in the Low-Voltage Peripherals subsystem (Label A) in Figure 9. **Auxiliary +12 V power must be supplied to the control board before applying power to the Power Stage.** The recommended mating connector is CUI Devices PP3-002A. The control board can be powered using a wall power adapter with a mating barrel jack connector such as the Phihong® PSAA30R-120-R wall adapter.

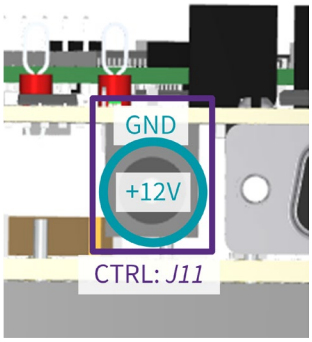

Figure 11: Controller power connector pinout (Control Stage J11)

2.3.3 CAN Port Pinout

The Controller Area Network (CAN) port is a standard male DB9 connector (Amphenol® L717SDE09PA4CH4RC309) with the pinout shown in Figure 12 and pin descriptions shown in Table 3. This CAN port can be mated with any standard DB9 female connector and is intended to be used with an isolated CAN adapter such as the PEAK System® PCAN-USB Pro FD or National Instruments® USB-8473. **Always use an isolated CAN adapter when communicating with this design from a host computer since the CAN port on this design is not isolated.**

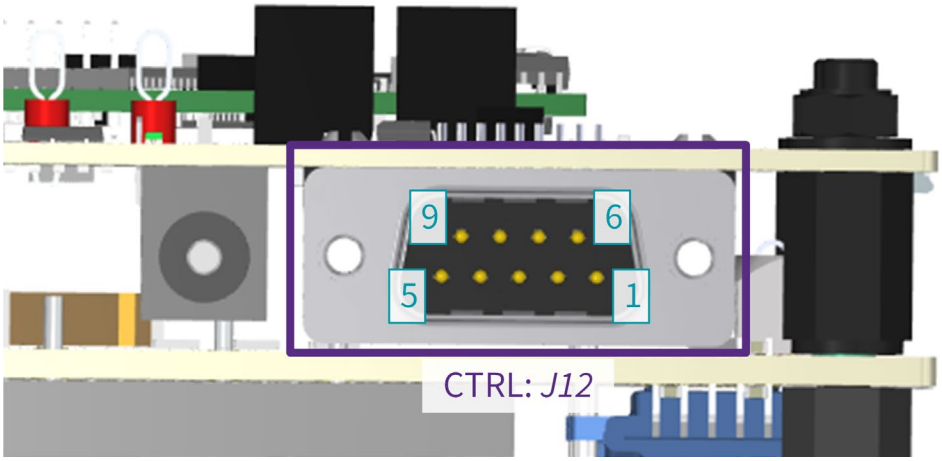

*Figure 12: CAN port connector pinout (Control Stage J9 attached to **CANA**)*

*Table 3: CAN port pinout (Control Stage J9 attached to **CANA**)*

Pin #	Name	Type	Description
1	NC0	—	No Connect
2	CANA_L	Digital (I/O)	Isolated CAN Port A Low
3	V-	Power	Isolated Ground
4	NC1	—	No Connect
5	SHLD	Power	Isolated Ground
6	O(V-)	—	No Connect
7	CANA_H	Digital (I/O)	Isolated CAN Port A High
8	NC2	—	No Connect
9	V+	Power	Isolated +5V Power

I = Input | O = Output

2.3.4 Board-to-Board Interface Connector Pinout

The *Power Stage* and *Control Stage* interface with each other through a single header connection in the center of the PCBs. This eliminates the need for cables to be routed between the circuit boards, avoiding issues such as the cables being routed over high *dV/dt* or *di/dt* areas. Since all the interface signals are routed through a single connection point, it eliminates needing to align multiple connectors on different sides of the PCBs when engaging the connectors. The interface connector from the viewpoint of the *Power Stage* is shown in Figure 13 with pin descriptions provided in Table 4. Several of the pins are removed from the connector to ensure that the system adheres to all creepage and clearance requirements. The connector on the *Power Stage* is TSM-128-01-L-DV-A and the connector on the *Control Stage* is SSW-126-01-G-D, both manufactured by Samtec®.

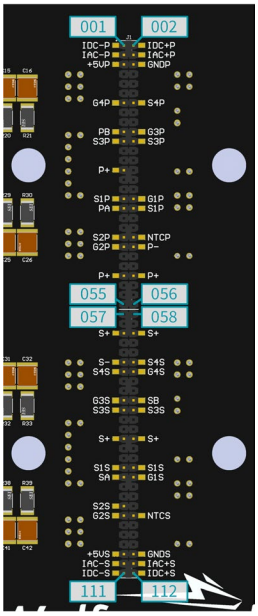

Figure 13: Board-to-board interface connector on power board (Power Stage J1, Control Stage J14)

Table 4: Board-to-board interface pinout (Power Stage J1, Control Stage J14)

#	Name	Description	#	Name	Description
1	IDC-P*	Negative line of primary DC current meas.	2	IDC+_P*	Positive line of primary DC current meas.
3	IAC-P*	Negative line of primary AC current meas.	4	IAC+_P*	Positive line of primary AC current meas.
5	+5VP	Power supply for primary current meas.	6	GND_P	Common for primary current meas.
7	NC	No connect. Pin removed from connector.	8	NC	No connect. Pin removed from connector.
9	NC	No connect. Pin removed from connector.	10	NC	No connect. Pin removed from connector.
11	NC	No connect. Pin removed from connector.	12	NC	No connect. Pin removed from connector.
13	G4_P	Gate output for primary MOSFET 4.	14	S4_P	Source reference for primary MOSFET 4.
15	NC	No connect. Pin removed from connector.	16	NC	No connect. Pin removed from connector.
17	NC	No connect. Pin removed from connector.	18	NC	No connect. Pin removed from connector.
19	PB	Primary Phs B (used for MOSFET 4 DESAT).	20	G3_P	Gate output for primary MOSFET 3.
21	S3_P	Source reference for primary MOSFET 3.	22	S3_P	Source reference for primary MOSFET 3.
23	NC	No connect. Pin removed from connector.	24	NC	No connect. Pin removed from connector.
25	NC	No connect. Pin removed from connector.	26	NC	No connect. Pin removed from connector.
27	P+	Primary DC+ (used for MOSFET 1 & 3 DESAT).	28	NC	No connect. Pin removed from connector.
29	NC	No connect. Pin removed from connector.	30	NC	No connect. Pin removed from connector.
31	NC	No connect. Pin removed from connector.	32	NC	No connect. Pin removed from connector.
33	S1_P	Source reference for primary MOSFET 1.	34	G1_P	Gate output for primary MOSFET 1.
35	PA	Secondary Phs A (used for MOSFET 2 DESAT).	36	S1_P	Source reference for primary MOSFET 1.
37	NC	No connect. Pin removed from connector.	38	NC	No connect. Pin removed from connector.
39	NC	No connect. Pin removed from connector.	40	NC	No connect. Pin removed from connector.
41	S2_P	Source reference for primary MOSFET 2.	42	NTC_P	Primary thermistor (referenced to S2_P).
43	G2_P	Gate output for primary MOSFET 2.	44	P-	Primary DC- (used for DC voltage meas).
45	NC	No connect. Pin removed from connector.	46	NC	No connect. Pin removed from connector.
47	NC	No connect. Pin removed from connector.	48	NC	No connect. Pin removed from connector.
49	P+	Primary DC+ (used for DC voltage meas).	50	P+	Primary DC+ (used for DC voltage meas).
51	NC	No connect. Pin removed from connector.	52	NC	No connect. Pin removed from connector.
53	NC	No connect. Pin removed from connector.	54	NC	No connect. Pin removed from connector.
55	NC	No connect. Pin removed from connector.	56	NC	No connect. Pin removed from connector.
57	NC	No connect. Pin removed from connector.	58	NC	No connect. Pin removed from connector.
59	NC	No connect. Pin removed from connector.	60	NC	No connect. Pin removed from connector.
61	S+	Secondary DC+ (used for DC voltage meas).	62	S+	Secondary DC+ (used for DC voltage meas).
63	NC	No connect. Pin removed from connector.	64	NC	No connect. Pin removed from connector.
65	NC	No connect. Pin removed from connector.	66	NC	No connect. Pin removed from connector.
67	S-	Secondary DC- (used for DC voltage meas).	68	S4_S	Source reference for secondary MOSFET 4.
69	S4_S	Source reference for secondary MOSFET 4.	70	G4_S	Gate output for secondary MOSFET 4.
71	NC	No connect. Pin removed from connector.	72	NC	No connect. Pin removed from connector.
73	NC	No connect. Pin removed from connector.	74	NC	No connect. Pin removed from connector.
75	G3_S	Gate output for secondary MOSFET 3.	76	SB	Secondary Phs B (used for MOSFET 4 DESAT).
77	S3_S	Source reference for secondary MOSFET 3.	78	S3_S	Source reference for secondary MOSFET 3.

#	Name	Description	#	Name	Description
79	NC	No connect. Pin removed from connector.	80	NC	No connect. Pin removed from connector.
81	NC	No connect. Pin removed from connector.	82	NC	No connect. Pin removed from connector.
83	S+	Secondary DC+ (used for MOSFET 3 DESAT).	84	S+	Secondary DC+ (used for MOSFET 1 DESAT).
85	NC	No connect. Pin removed from connector.	86	NC	No connect. Pin removed from connector.
87	NC	No connect. Pin removed from connector.	88	NC	No connect. Pin removed from connector.
89	S1_S	Source reference for secondary MOSFET 1.	90	S1_S	Source reference for secondary MOSFET 1.
91	SA	Secondary Phs A (used for MOSFET 2 DESAT).	92	G1_S	Gate output for secondary MOSFET 1.
93	NC	No connect. Pin removed from connector.	94	NC	No connect. Pin removed from connector.
95	NC	No connect. Pin removed from connector.	96	NC	No connect. Pin removed from connector.
97	S2_S	Source reference for secondary MOSFET 2.	98	NC	No connect. Pin removed from connector.
99	G2_S	Gate output for secondary MOSFET 2.	100	NTC_S	Secondary thermistor (referenced to S2_S).
101	NC	No connect. Pin removed from connector.	102	NC	No connect. Pin removed from connector.
103	NC	No connect. Pin removed from connector.	104	NC	No connect. Pin removed from connector.
105	NC	No connect. Pin removed from connector.	106	NC	No connect. Pin removed from connector.
107	+5V_S	Power supply for secondary current meas.	108	GND_S	Common for secondary current meas.
109	IAC-_S*	Negative line of secondary AC current meas.	110	IAC+_S*	Positive line of secondary AC current meas.
111	IDC-_S*	Negative line of secondary DC current meas.	112	IDC+_S*	Positive line of secondary DC current meas.

* Indicates differential pair

2.3.5 Spare +12 V Connector Pinout

The *Control Stage* includes a spare +12 V output connector, *J1*, for powering +12 V auxiliary equipment. This connector is 640456-2 manufactured by TE Connectivity, and the recommended mating connector is 1375820-2 also manufactured by TE Connectivity. The pinout for this connector is shown in Figure 14. This connector can be used to drive any always-on +12 V peripheral. For example, this output can be used to operate a fan to cool external equipment. Notably, this output is powered from the input controller power connector (see Section 2.3.2), so it is limited in output current drive strength. This connector should only be used to drive low-power peripherals. By default, this connector is not attached to anything.

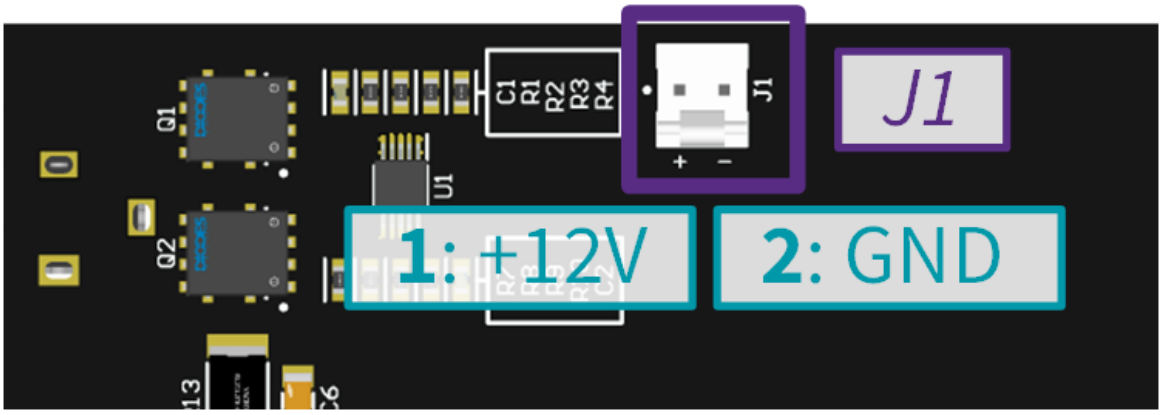

Figure 14: Spare +12 V power connector pinout (Control Stage J1)

2.3.6 Auxiliary Connector

The board includes a spare auxiliary header connector for troubleshooting and customization purposes. The pinout for the connector is shown Figure 15 and the pin descriptions are shown in Table 5. The connector uses standard 0.1” headers for easy interfacing; the part number for the header connector is 61301221121 manufactured by Würth Elektronik. The connector provides access to all the standard voltage rails on the Control board (+3.3 V, +5 V, and +12 V) and to input/outputs on the controller for analog-to-digital converter (ADC) pins, enhanced pulse width modulation (EPWM) pins, and general-purpose input/output (GPIO) pins. All the headers include several spots for adding passive elements for biasing or filtering the signals, as needed. The non-populated circuit components for filtering/biasing are shown in Figure 16.

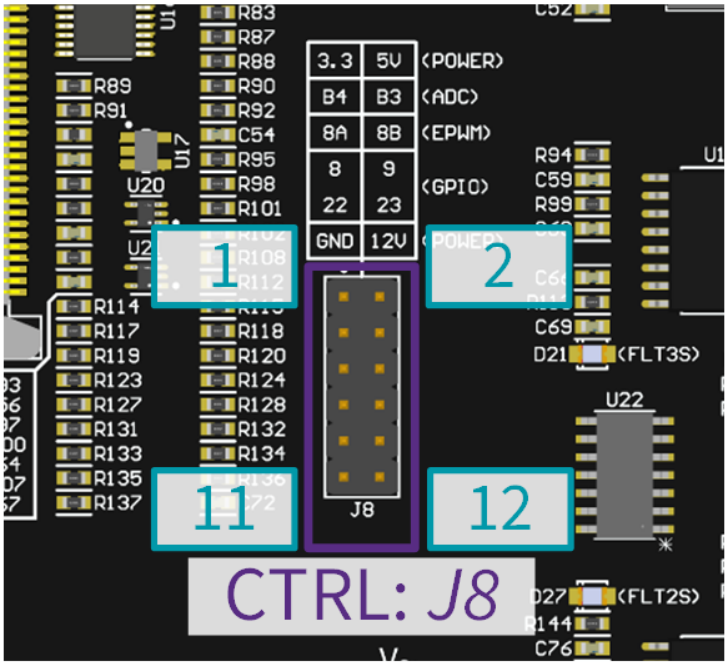

Figure 15: Auxiliary header connector (Control Stage J8)

Table 5: Auxiliary header connector pinout (control board J8)

#	Name	Description
1	+3.3 V	Power +3.3 V circuitry. Connected directly to +3.3 V rail.
2	+5 V	Power +5 V circuitry. Connected directly to +5 V rail.
3	ADCB4	Measure analog voltage. Connected to ADC B4
4	ADCB3	Measure analog voltage. Connected to ADC B3.
5	EPWM8A	Generate PWM outputs. Connected to EPWM 8A.
6	EPWM8B	Generate PWM outputs. Connected to EPWM 8B.
7	GPIO08	Read/control digital signal. Connected to GPIO 8.
8	GPIO09	Read/control digital signal. Connected to GPIO 9.
9	GPIO22	Read/control digital signal. Connected to GPIO 22.
10	GPIO23	Read/control digital signal. Connected to GPIO 23.
11	GND	Common reference.
12	+12 V	Power +12 V circuitry. Connected directly to +12 V rail.

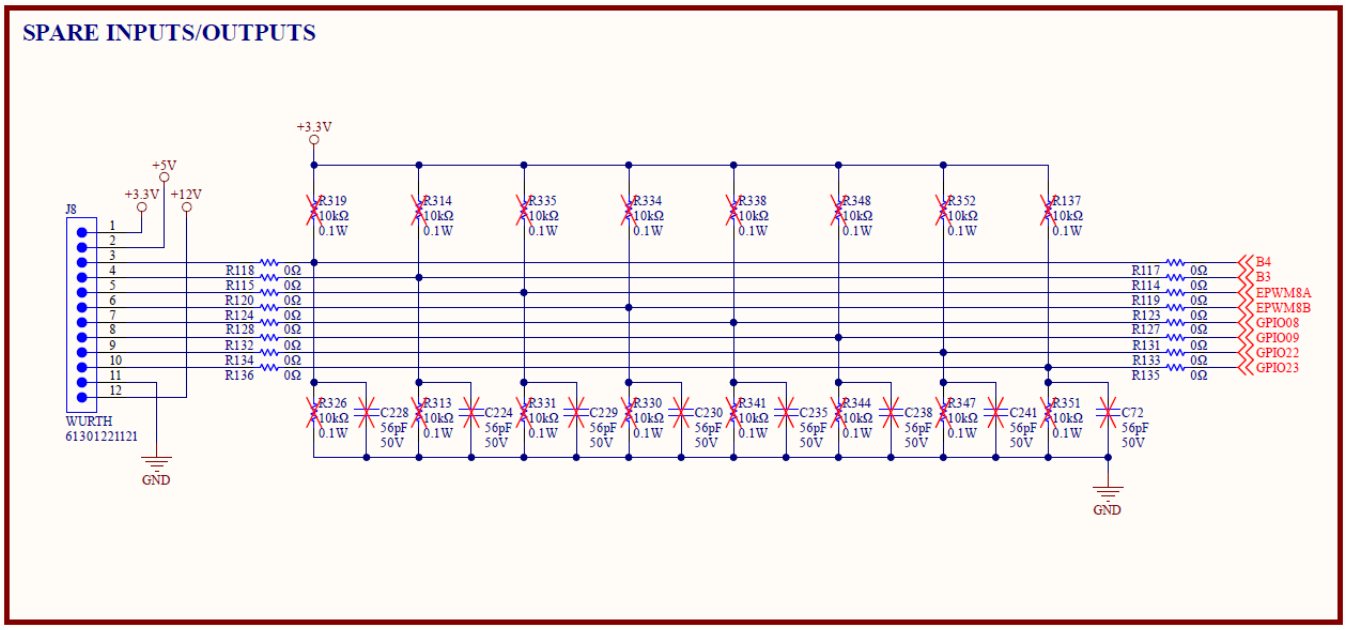

Figure 16: Auxiliary connector (Control Stage J8) filtering and biasing circuit options

3. System Description

CAUTION

IT IS NOT NECESSARY FOR YOU TO TOUCH THE BOARD WHILE IT IS ENERGIZED. WHEN DEVICES ARE BEING ATTACHED FOR TESTING, THE BOARD MUST BE DISCONNECTED FROM THE ELECTRICAL SOURCE AND ALL BULK CAPACITORS MUST BE FULLY DISCHARGED.

SOME COMPONENTS ON THE BOARD REACH TEMPERATURES ABOVE 50^0 CELSIUS. THESE CONDITIONS WILL CONTINUE AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED. DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE BOARD.

PLEASE ENSURE THAT APPROPRIATE SAFETY PROCEDURES ARE FOLLOWED WHEN OPERATING THIS BOARD AS SERIOUS INJURY, INCLUDING DEATH BY ELECTROCUTION OR SERIOUS INJURY BY ELECTRICAL SHOCK OR ELECTRICAL BURNS, CAN

警告

通电时不必接触板子。连接器件进行测试时，必须切断板子电源，且大容量电容器必须释放完所有电荷。

板子上一些组件的温度可能超过50摄氏度。移除电源后，上述情况可能会短暂持续，直至大容量电容器完全释放电荷。通电时禁止触摸板子，应在大容量电容器完全释放电荷后，再操作电路板。

请确保在操作电路板时已经遵守了正确的安全规程，否则可能会造成严重伤害，包括触电死亡、电击伤害、或电灼伤。，大容量电容器已释放了所有电量。只有在切断板子电源，且大容量电容器完全放电后，才可更换待测试器件。

警告

通電している時にボードに接触する必要がありません。設備をつないで試験する時、必ずボードの電源を切ってください。また、大容量のコンデンサーで電力を完全に釈放してください。

ボードのモジュールの温度は50度以上になるかもしれません。電源を切った後、上記の状況がしばらく持続する可能性がありますので、大容量のコンデンサーで電力を完全に釈放するまで待ってください。通電している時にボードに接触するのは禁止です。大容量のコンデンサーで電力をまだ完全に釈放していない時、ボードを操作しないでください。

ボードを操作している時、正確な安全ルールを守っているのを確保してください。さもなければ、感電、電撃、厳しい火傷などの死傷が出る可能性があります。

3.1 Power Stage Board

This section provides details regarding the various circuit elements on the *Power Stage* such as the power loop, methods employed to minimize parasitic inductance, and feedback measurements.

3.1.1 Power Loop

The power loop of this design connects bulk capacitors to the primary and secondary full bridges of the DAB. As discussed previously, this design utilizes two CBB011M12GM4T power modules: one for the primary and one for the secondary. These power modules, shown in Figure 2, are 1200 V rated, 11 mΩ full bridge devices with a baseplate-less mounting surface and pre-applied thermal interface material. For bulk capacitance, this design uses five total 65 µF low-inductance capacitors. The capacitors used are KEMET® C4AQNEW5650M3BJ film capacitors with a voltage rating of 1 kV. There are two parallel capacitors forming the primary-side DC bus (totaling 130 µF), and there are three parallel capacitors forming the secondary-side DC bus (totaling 195 µF). There is more secondary capacitance than primary capacitance since the primary side is typically attached to a grid-tied converter such as an Active Front End (AFE) with additional bulk capacitance on the output. The DC-link capacitor circuitry and the connections to the power module are shown in the schematic in Figure 17. The input and output DC terminals (see Section 2.3.1) connect directly to the DC bus capacitors and the power modules using low-inductance interleaved copper pours on the PCB. The PCB used in this design features interleaved DC+ and DC- copper layers to increase the flux cancellation between layers and reduce the inductance between the capacitors and the power module input pins. The interleaved DC+ and DC- layers are indicated in the notional PCB stack-ups shown in Figure 18, which shows the signals/planes on each circuit board layer in each section of the *Power Stage*.

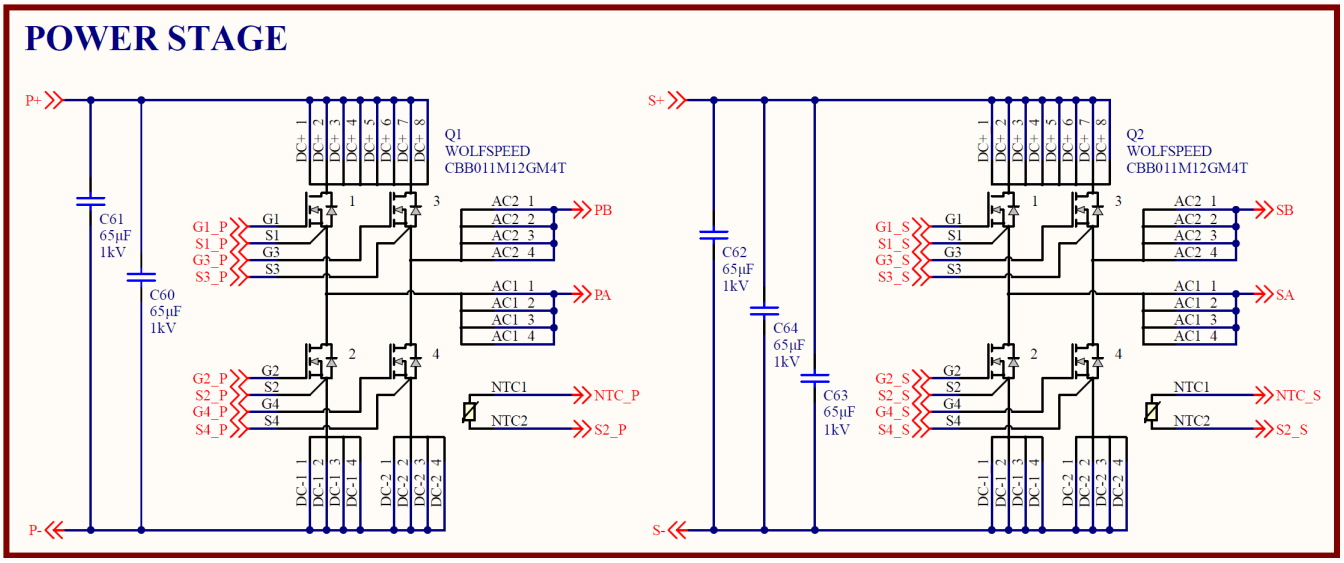

Figure 17: Power loop circuitry (bulk capacitors and power modules) on the Power Stage

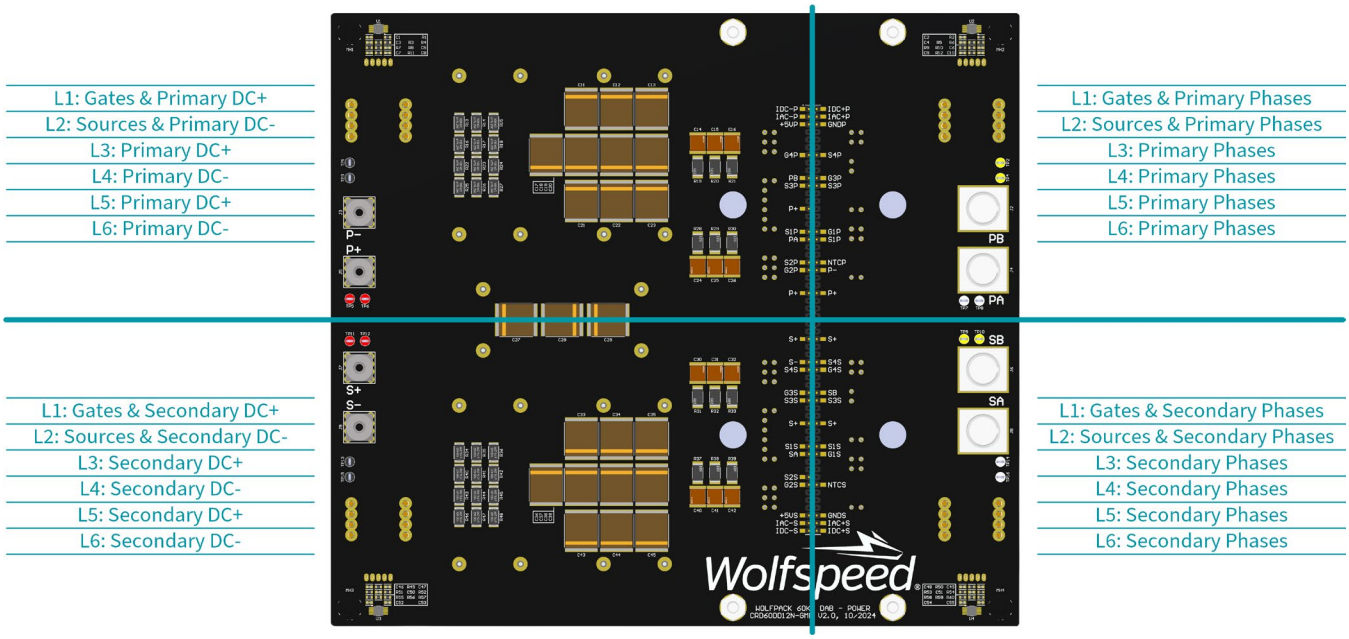

Figure 18: Layer stack-up of the various sections of the Power Stage PCB

3.1.2 High-Frequency Capacitors

The fast-switching characteristics of SiC MOSFETs enable significantly lower switching losses compared to conventional Si IGBTs. These reduced losses allow operation at higher switching frequencies, which in turn enables smaller passive components, more compact thermal management solutions, improved power density, and higher overall efficiency. As a result, SiC MOSFETs are well suited for high-performance, fast-switching DC/DC converter applications such as this DAB design. However, the rapid voltage and current transitions associated with SiC devices can excite parasitic inductances that are typically negligible in lower-frequency, IGBT-based systems. To mitigate these effects, the design employs interleaved DC+ and DC− power planes to promote flux cancellation and minimize parasitic inductance within the power loop. This approach results in an exceptionally low loop inductance. To further reduce the impact of parasitic elements, high-frequency decoupling capacitors are strategically placed close to the power module terminals, providing a low-inductance path for high-frequency current components. The schematic implementation of these capacitors is shown in Figure 19, and their physical placement on the *Power Stage* PCB is illustrated in Figure 20.

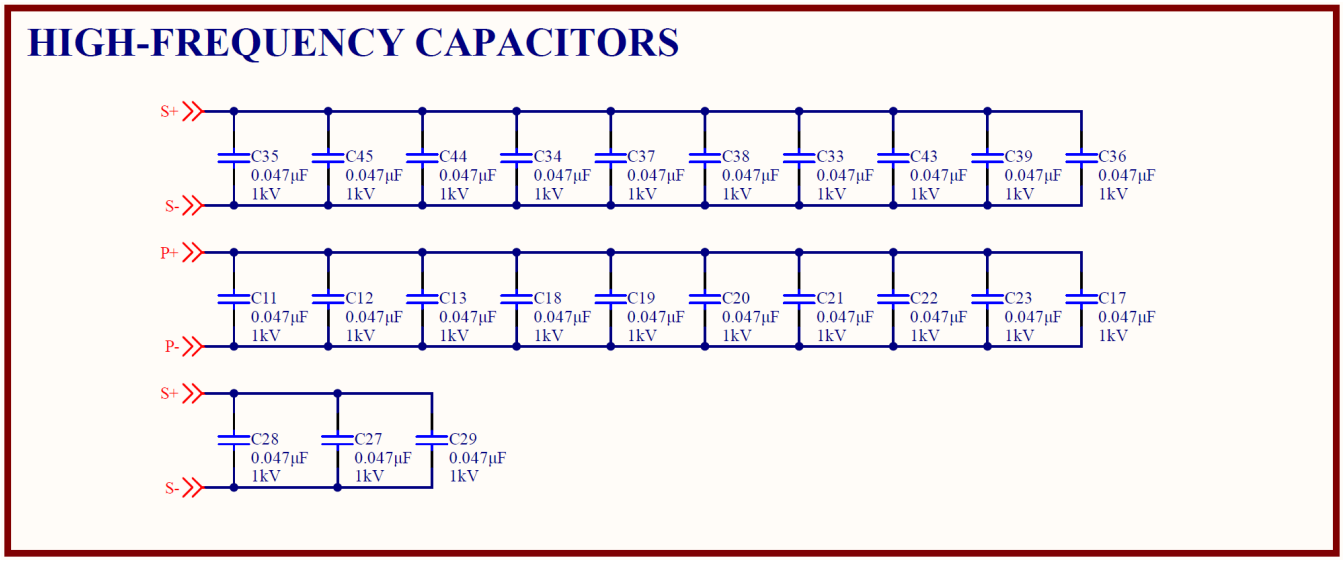

Figure 19: High-frequency capacitors on the Power Stage

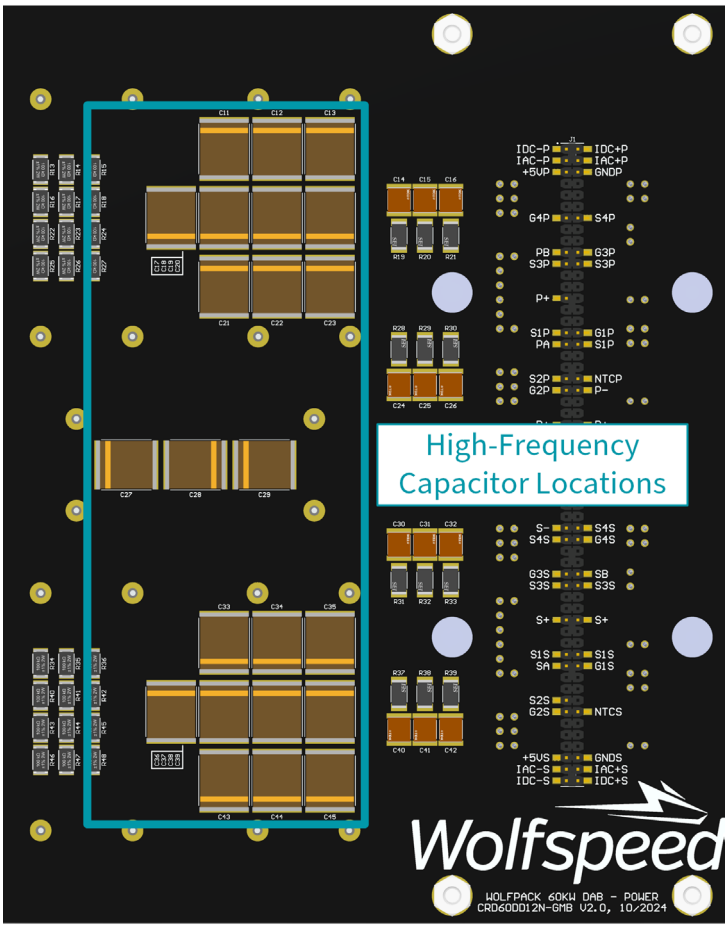

Figure 20: Locations of high-frequency capacitors on Power Stage

3.1.3 Snubber Circuits

The high *dV/dt* achievable with SiC MOSFETs is attractive in many applications since it leads to reduced switching losses and higher switching frequencies. However, it can introduce overshoot into the drain-to-source voltage (V_{DS}) of the semiconductor. In many designs with low-inductance PCB layout, the slight voltage overshoot is not an issue in the system assembly. However, in some designs – especially when operating a device close to its rated blocking voltage – the voltage overshoot can be problematic because it can lead to exceeding the safe-operating-area (SOA) of the device. By default, the *Power Stage* includes several provisions to limit V_{DS} overshoot on the device which are listed below.

- *Wolfspeed Generation 4 MOSFETs* include a softer body diode which significantly reduces V_{DS} overshoot due to the improved reverse recovery performance
- *Interleaved DC+ and DC- Layers* which achieve flux cancellation
- *Wide Copper Pours* which increase the cross-sectional areas
- *Compact Power Loop* with capacitors close to the modules which reduces the power loop area

These features together minimize the PCB inductance of the design and reduce the device V_{DS} overshoots. Even with these features, some users still prefer to use snubber elements to further reduce the risk of overshoot and ringing. The *Power Stage* includes a resistor-capacitor (RC) snubber circuit placed very close to the power module terminals to create a dissipative shunt path for high-frequency energy. When sized appropriately, an RC snubber can reduce the power module maximum overshoot voltage and damp oscillatory ringing. Figure 21 shows the influence on device V_{DS} of a CBB011M12GM4 full-bridge power module in an Analog Devices® LTspice® double-pulse test (DPT) simulation. The simulation was performed at a bus voltage of 800 V and a load current of 100 A. The introduction of the snubber elements reduces both the overshoot and the oscillations significantly. For more information about the DPT simulation for evaluating performance in different operating conditions, visit https://www.wolfspeed.com/tools-and-support/power/ltspice-and-plecs-models/.

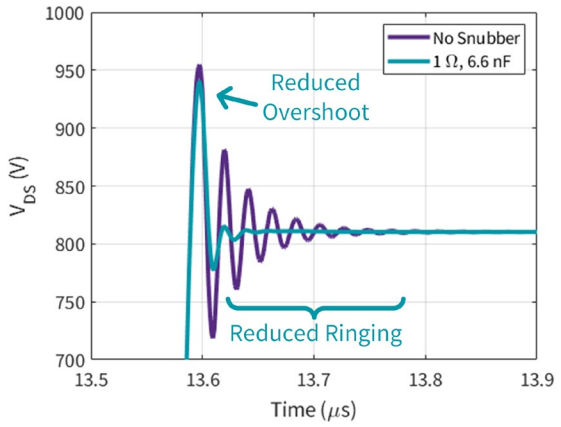

Figure 21: Simulation comparison with and without a snubber circuit

For the most effective RC snubber implementation, the snubber components need to be placed physically close to the terminals of the power module to limit the inductance between the MOSFETs and the snubber circuit elements. This design uses four individual RC snubber circuits so that each half-bridge can have snubber elements close to its power terminals. The RC snubber schematics are shown in Figure 22, and the PCB layout implementations are shown in Figure 23. If snubber customization is required, the snubber uses standard 2512 (6432 metric) footprint resistors and 2220 (5750 metric) footprint capacitors. These can be easily swapped for alternative components with the same package footprint. Notably, if adopting alternative snubber components, the capacitors should have a voltage rating greater than the peak V_{DS} overshoot of the device, and the resistors should have suitable power rating to dissipate the shunted high-frequency energy.

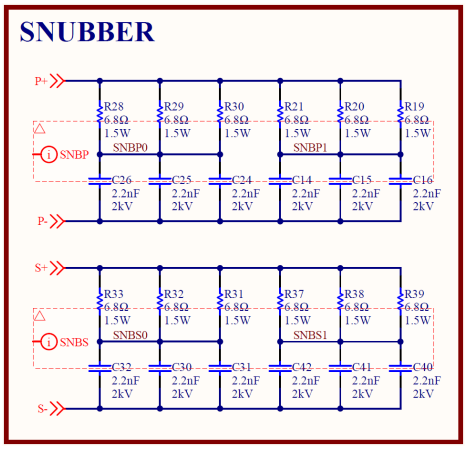

Figure 22: RC snubber circuit on Power Stage

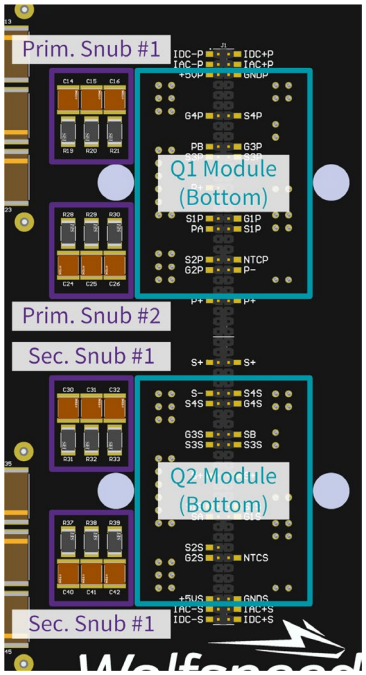

Figure 23: RC snubber circuit locations on Power Stage with respect to the power modules

3.1.4 Bleed Resistors

To ensure the DC-bus safely discharges after system shutdown, the design includes bleed resistors on both the primary and secondary sides of the circuits. These resistors discharge the bus to less than 50 V in under 3 minutes when the input voltage is removed from the system. These resistors are connected to the DC bus at all times to ensure the bus is always depleted after system shutdown. The bleed resistor circuits for both the primary and secondary are shown in Figure 24.

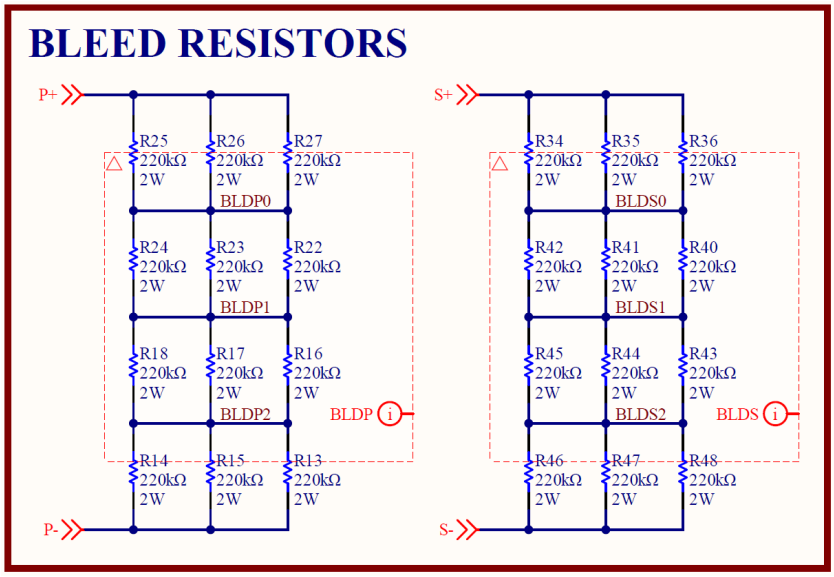

Figure 24: Bleed resistors on Power Stage

3.1.5 Current Measurements

Both the primary and the secondary side of the power stage include hall effect current sensors for measuring the DC input/output currents and the transformer currents. All four current measurements use LEM® HO 120-NP-0100 hall effect current sensors and are in the locations shown in Figure 25. These sensors each have a measuring range of ±300 A with a nominal 120 A_{rms} rating. For applications requiring different current measurement ranges, there are several pin compatible current sensors in the LEM HO XXX-NP family to enable larger dynamic measuring range or higher resolution measurements. The bidirectional measuring range of the sensors enables accurate measurements, even when power is being transferred from the secondary to the primary. Since these sensors are physically far from the controller, the output analog voltages of the sensors are transmitted differentially from the *Power Stage* to the *Control Stage*. The use of differential signals minimizes the effect of *dV/dt* noise affecting the feedback signals. All the sensors have the same biasing and single-ended-to-differential conversion circuits, as shown in Figure 26 and Figure 27.

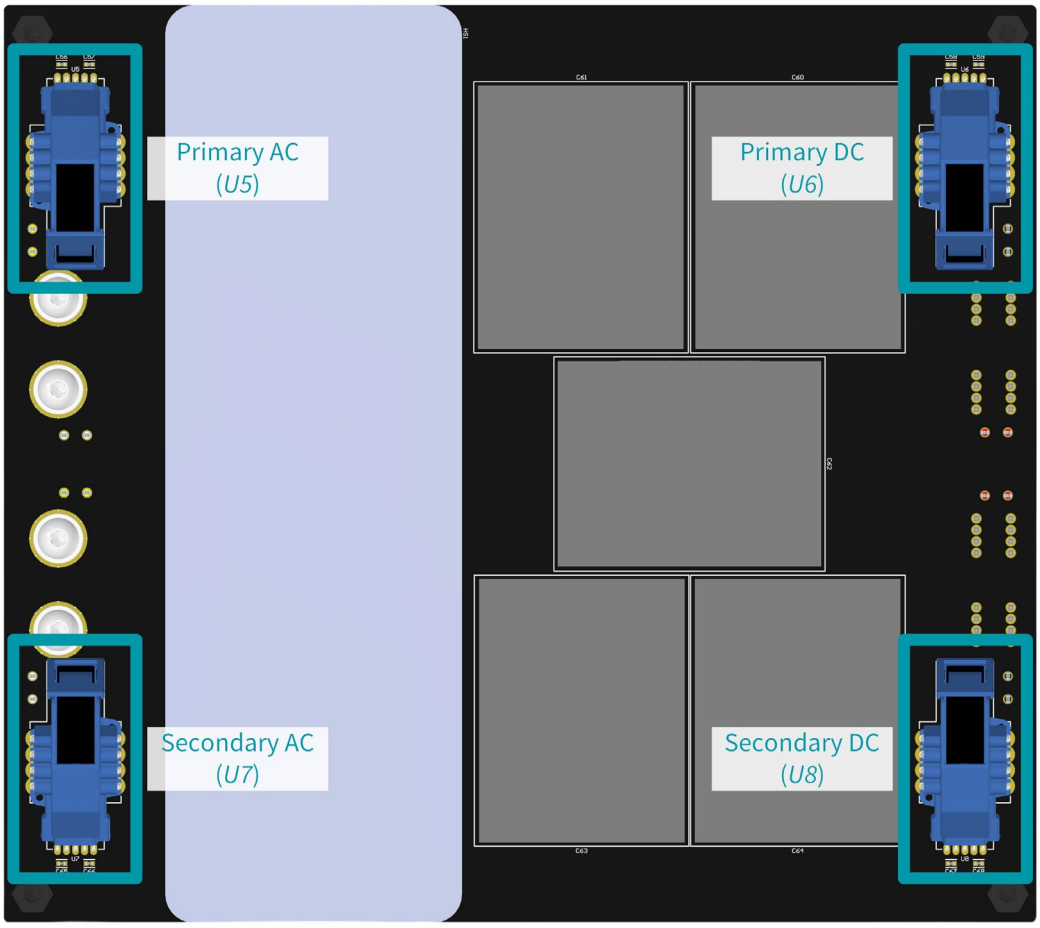

Figure 25: Current sensor locations on Power Stage

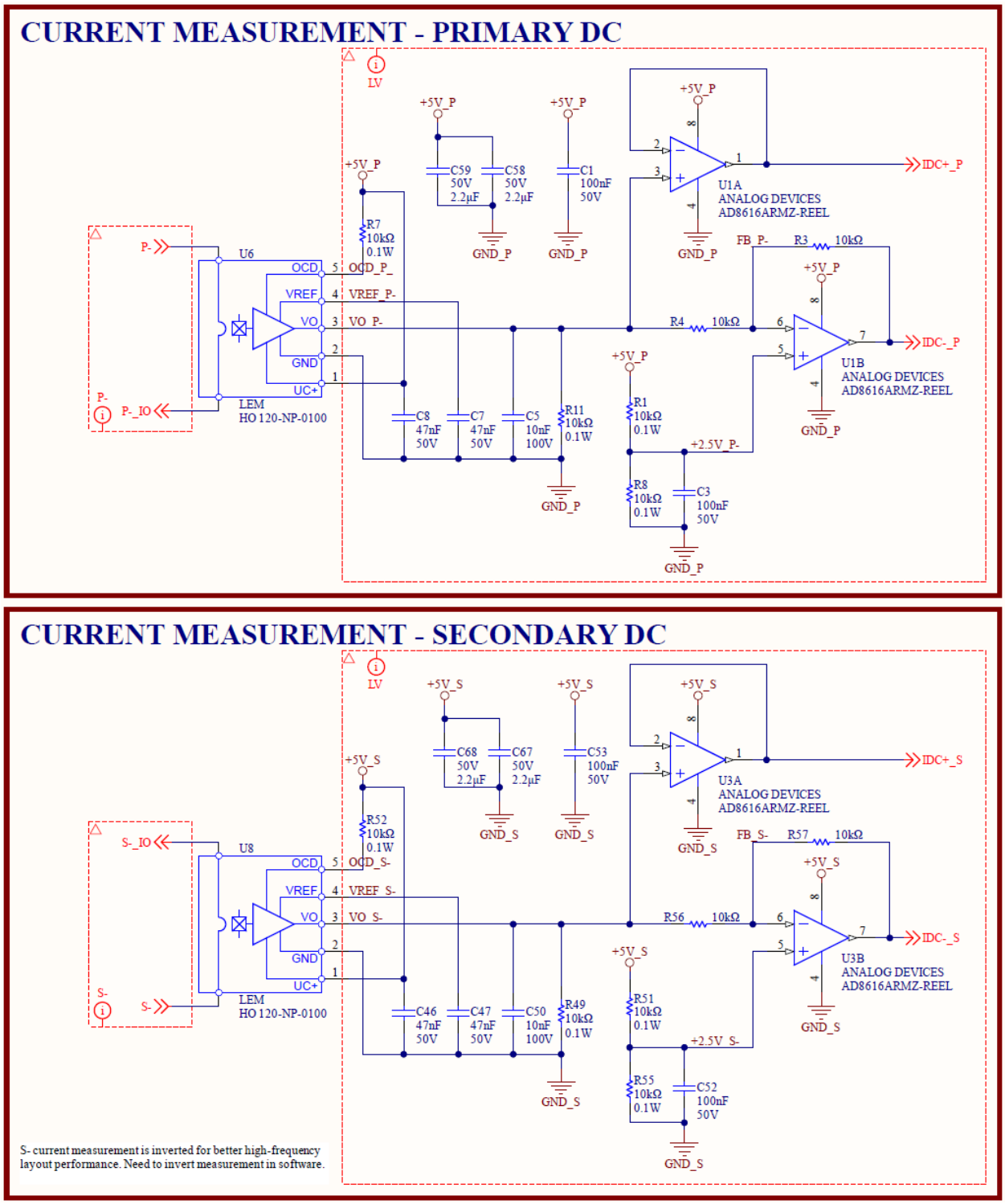

Figure 26: DC current sensor differential transmitter circuits on Power Stage

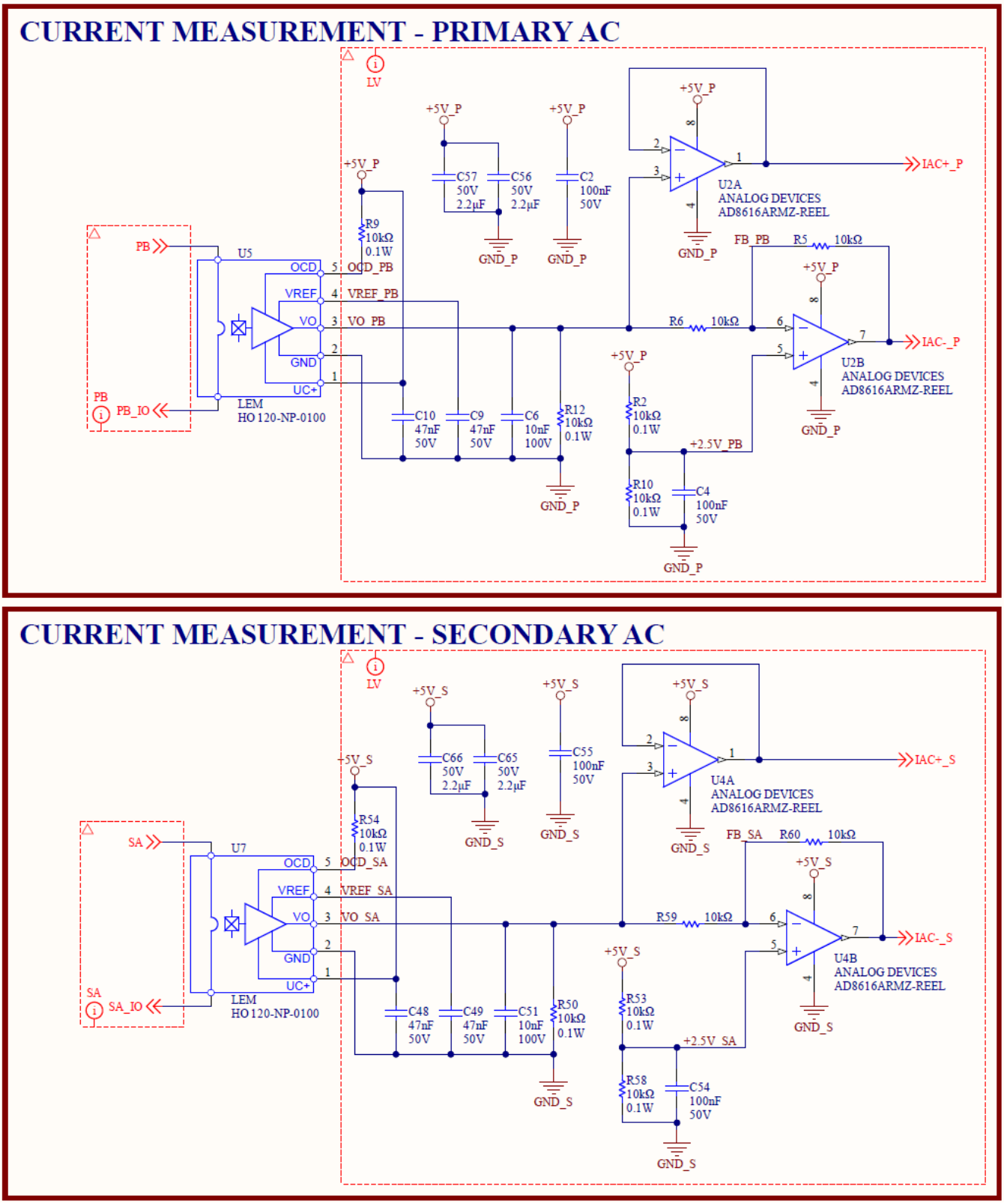

Figure 27: AC current sensor differential transmitter circuits on Power Stage

3.1.6 Test Points

The design includes a variety of test points to measure various signals on the board in order to evaluate the design and test various control schemes. The test points on the *Power Stage* are shown in Figure 28, and the corresponding signals are described in Table 6. The locations of all the test points on the CRD60DD12N-GMB are shown in Figure 35.

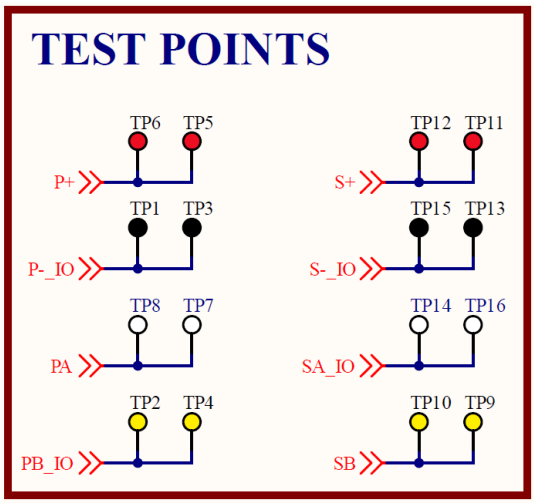

Figure 28: Test points on Power Stage

Table 6: Signal descriptions of test points on Power Stage

Designator	Signal	Color	Description
TP1	P-_IO*	Black	Negative primary DC-bus voltage
TP2	PB_IO*	Yellow	Primary phase B to transformer
TP3	P-_IO*	Black	Negative primary DC-bus voltage
TP4	PB_IO*	Yellow	Primary phase B to transformer
TP5	P+	Red	Positive primary DC-bus voltage
TP6			
TP7	PA	White	Primary phase A to transformer
TP8			
TP9	SB	Yellow	Secondary phase B to transformer
TP10			
TP11	S+	Red	Positive secondary DC-bus voltage
TP12			
TP13	S-_IO*	Black	Negative secondary DC-bus voltage
TP14	SA_IO*	White	Secondary phase A to transformer
TP15	S-_IO*	Black	Negative secondary DC-bus voltage
TP16	SA_IO*	Yellow	Secondary phase A to transformer

* "_IO" indicates the signal has passed through a hall-effect current sensor

3.1.7 Mounting

The *Power Stage* is supported on a surface by four long non-conductive standoffs in the corners of the PCB. The Control Stage is also supported in the four corners by shorter standoffs that stack on the longer standoffs supporting the *Power Stage*. Four short conductive standoffs in the corners of the cold plate are used to mount the coldplate to the *Power Stage*. Similar to the corner standoffs, these mounting holes are also used by the *Control Stage* by stacking short conductive standoffs between the *Power Stage* and the *Control Stage*. There are also two holes in the Power Stage which allow tool access to mount the power modules to the coldplate. All these mounting locations are shown in Figure 29.

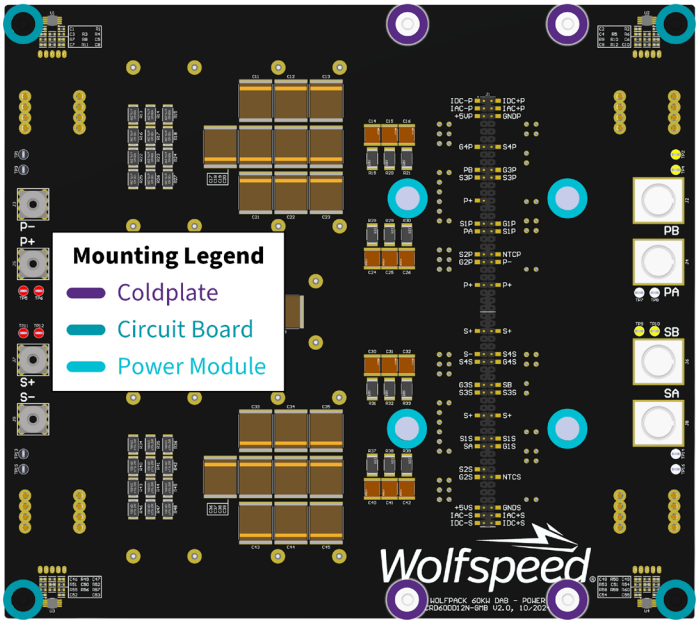

Figure 29: Mounting hole locations on Power Stage

3.2 Control Stage

This section provides details regarding the various circuit elements on the *Control Stage* such as the gate drivers, voltage measurement circuitry, current measurement circuitry, integrated instrumentation connections, overcurrent protection, temperature sensing, and CAN communication.

3.2.1 Gate Drivers

Each switch position on both the primary and secondary includes a dedicated, isolated gate driver for independent modulation of each switch position. These gate drivers each use the Texas Instruments® UCC21710 gate driver integrated circuit (IC) capable of 10 A maximum output current with independent turn-on and turn-off control, overcurrent protection, Miller clamp circuit, and analog feedback. Each switch position is powered by the Texas Instruments UCC14141-Q1 isolated power supply capable of supplying 1.5 W of power with bipolar output voltages. One example gate driver circuit is shown in Figure 30 for primary-side MOSFET switch position #1. Every gate driver is configured identically, with the exception of switch position 2 on both

the primary and secondary which also includes the thermistor feedback circuit (see Section 3.2.7). By default, the gate driver circuits are configured for output voltages of +15 V for turn on and -4 V for turn off. In order to adjust the gate driver voltages – for example to evaluate power module performance with difference bias voltages – change the resistor feedback circuit connected to the *FBVDD* (pin 34) and *FBVEE* (pin 35) pins of the IC in accordance with the UCC14141-Q1 datasheet.

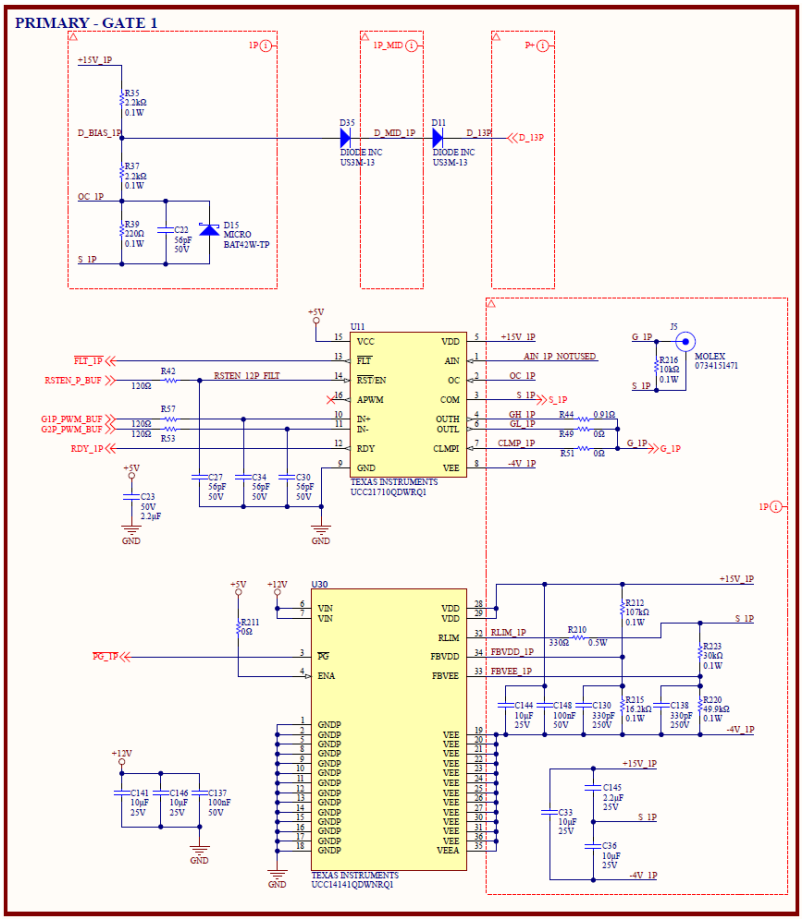

Figure 30: Example gate driver circuit on Control Stage (primary-side MOSFET position 1)

3.2.2 Voltage Sensing

The design includes voltage measurements for both the primary and secondary DC bus for enabling custom control schemes. The voltage measurements are performed using the Texas Instruments AMC3330-Q1 isolated amplifier with an integrated DC/DC converter. The bus voltages are reduced to a <1 V signal using a precision voltage divider and the isolated amplifier transmits a 0 to 2 V signal differentially to the controller. The circuit for the primary-side DC-bus voltage measurement is shown in Figure 31. The circuit is identical for the secondary-side voltage measurement. Critically, both these circuits remain isolated from each other to prevent bypassing the isolation barrier of the transformer. Transmitting the signal differentially increases the noise immunity of the signal. Near the controlCARD, the differential signals are converted back to a single-ended

using the circuit shown in Figure 32. Again, this circuit is identical for the secondary-side voltage measurement circuit. After the signal conditioning, the default firmware loaded on the CRD60DD12N-GMB design converts the measured signal to the corresponding voltage using

$$V = ADC \times 0.260978022$$

where

V: DC bus voltage (primary or secondary) [V]

ADC: sampled ADC register value [unitless, 0-4095].

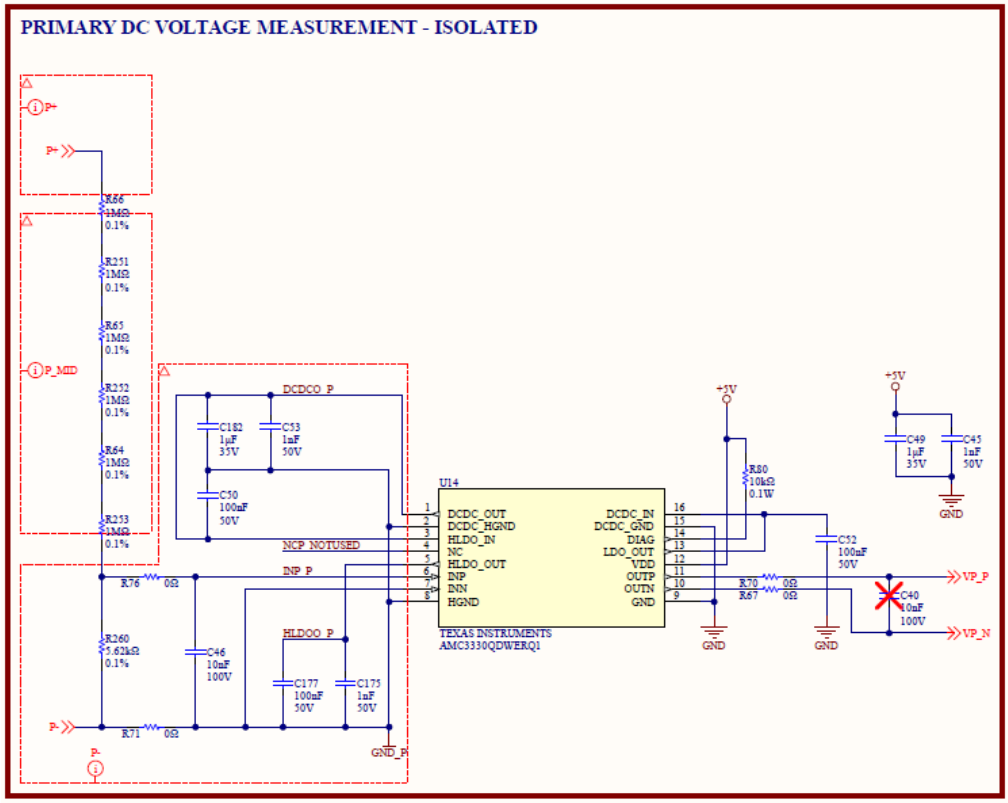

Figure 31: Primary-side isolated DC voltage measurement on Control Stage

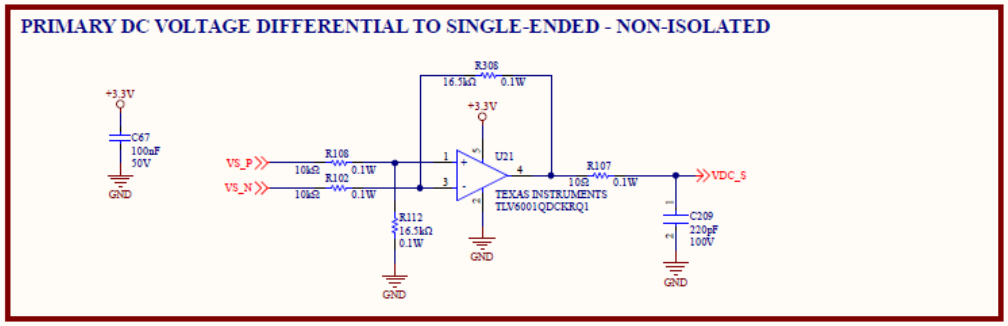

Figure 32: Primary-side differential to single-ended voltage measurement conversion on Control Stage

3.2.3 Current Sensing

The differential measurement signals from the hall-effect current sensors on the *Power Stage* (see Section 3.1.5) connect to the *Control Stage* through the interface connector. These differential signals are all converted to single-ended signals on the control board using the operational amplifier circuits shown in Figure 33. Note that the circuit is identical for the secondary-side current measurement circuits. After the signal conditioning, the default firmware loaded on the CRD60DD12N-GMB design converts the measured signal to the corresponding current using

$$I = ADC \times 0.163204610 - 333.88142337$$

where

I: DC or transformer current (primary or secondary) [A]

ADC: sampled ADC register value [unitless, 0-4095].

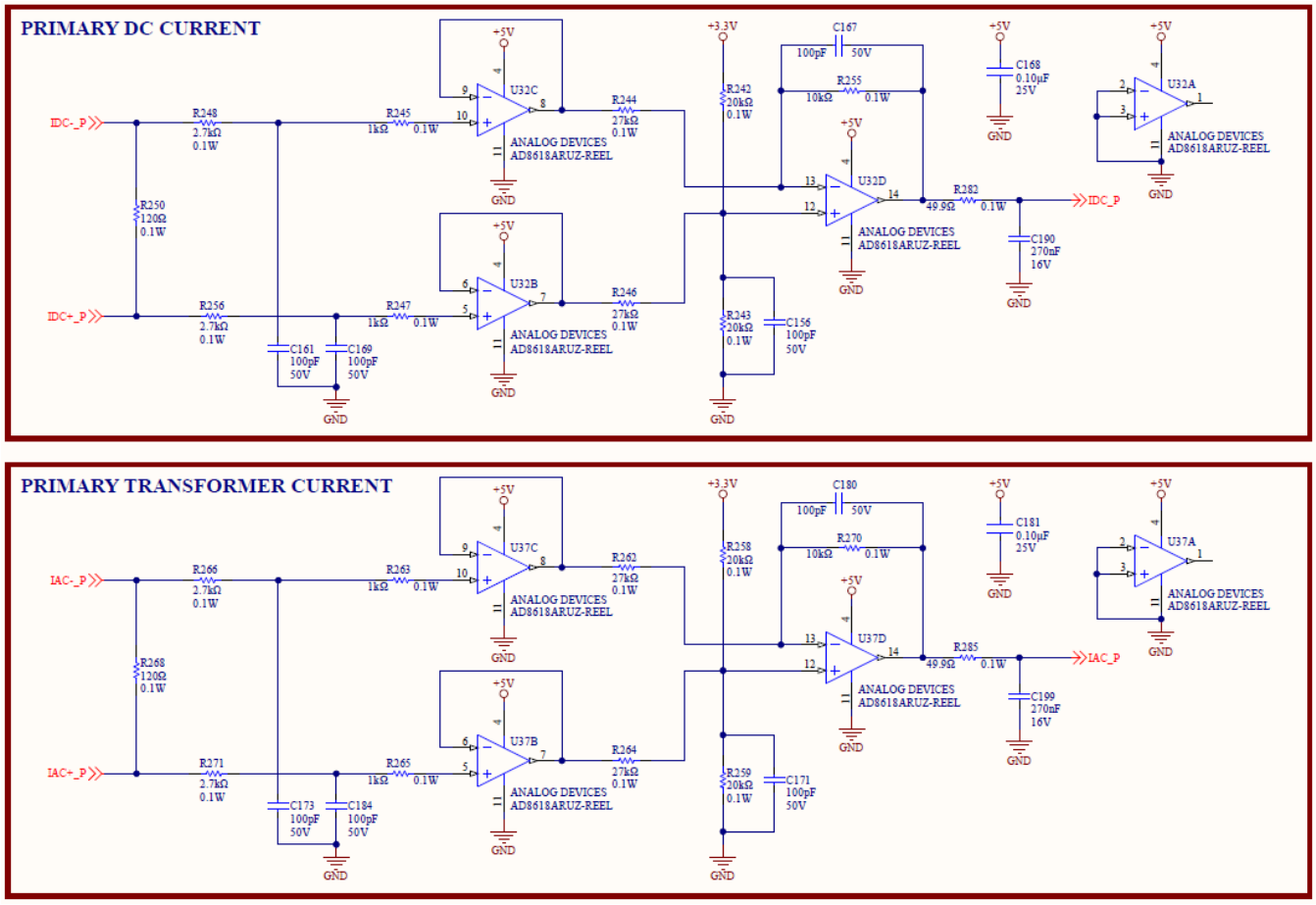

Figure 33: Primary-side differential-to-single ended current measurement conversion on Control Stage

3.2.4 Test Points

As discussed in Section 3.1.6, this design includes several test points for evaluating the system performance. In addition to the test points on the *Power Stage*, the *Control Stage* includes test points for monitoring the low-voltage power rails. The *Control Stage* test points are shown in Figure 34, and the corresponding pin descriptions are shown in Table 7. The location of all the CRD60DD12N-GMB test points (the test points on both the *Power Stage* and *Control Stage*) are shown in Figure 35.

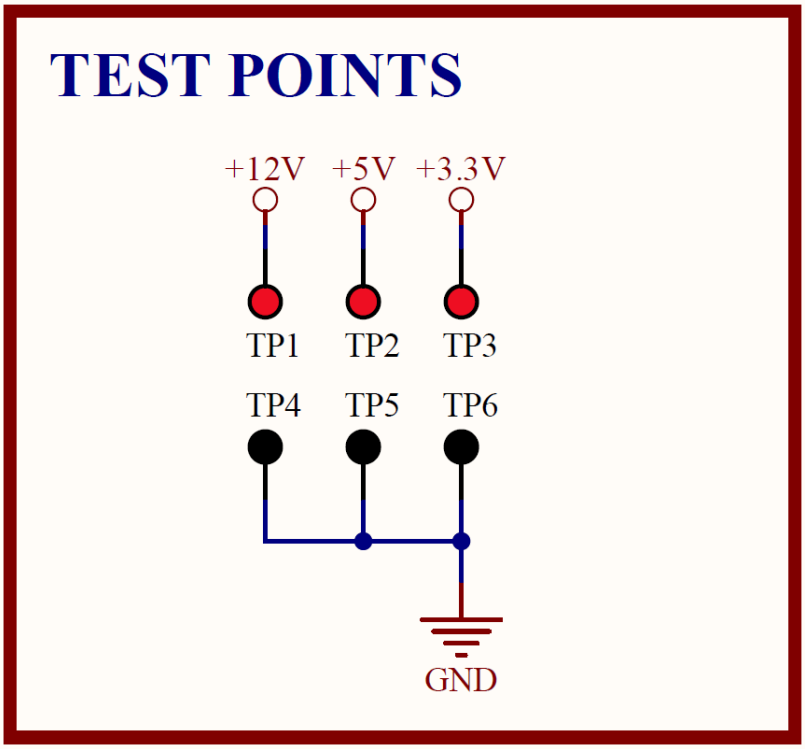

Figure 34: Test points on Control Stage

Table 7: Signal descriptions of the test points on Control Stage:

Designator	Signal	Color	Description
TP1	+12V	Red	Positive 12 V rail (referenced to GND)
TP2	+5V	Red	Positive +5 V rail (referenced to GND)
TP3	+3.3V	Red	Positive +3.3 V rail (referenced to GND)
TP4	GND	Black	Common reference for low-voltage signals
TP5			
TP6			

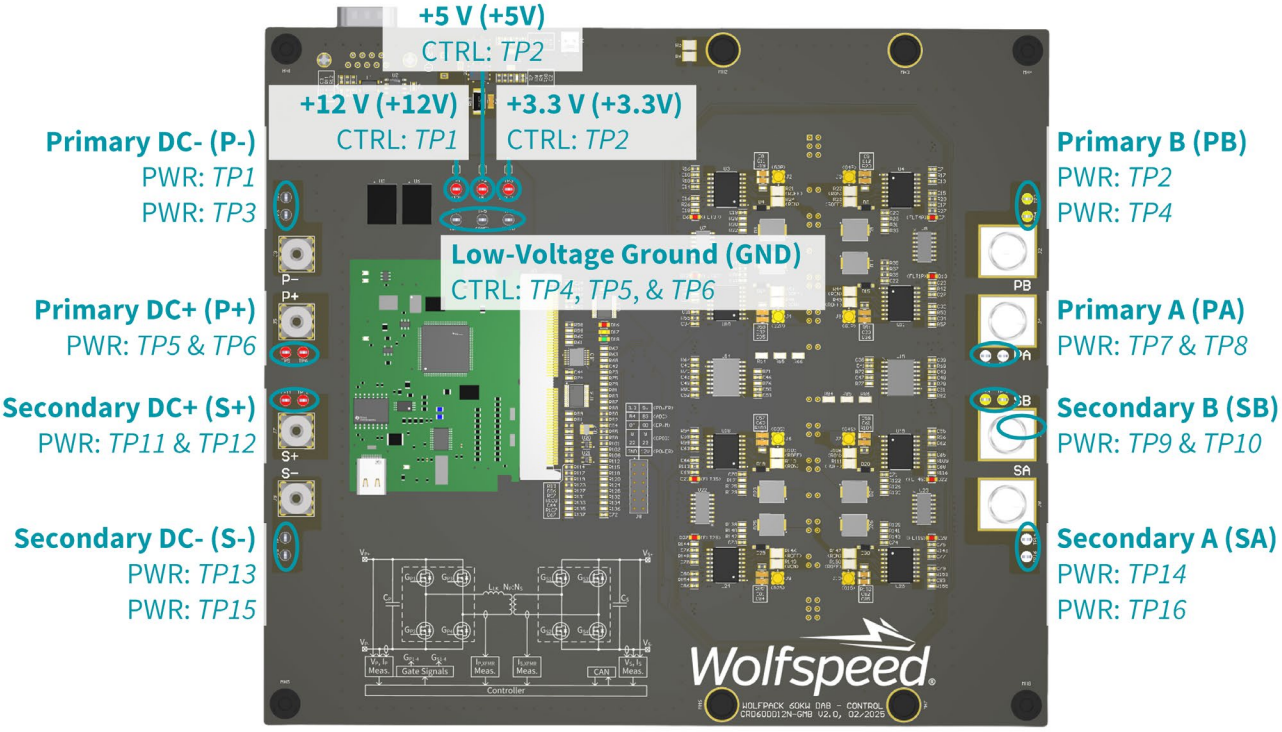

Figure 35: Test point locations on the CRD60DD12N-GMB

3.2.5 Metrology

To measure the MOSFET gate signals, each of the eight MOSFETs (four on the primary and four on the secondary) are connected to a dedicated micro-miniature coaxial (MMCX) connector, which are connected across the MOSFET gate and source terminals. These measurements use Molex® 0734151471 connectors and are in the locations shown in Figure 36. These are standard MMCX connectors intended to be monitored directly with an oscilloscope probe. Notably, during system operation, the gate measurements can float at the full bus voltage. Therefore, the gate measurements should not be monitored using single-ended oscilloscope probes due to the safety risks of high-voltage potentials being applied to the oscilloscope. It is recommended to perform these gate measurements with high-isolation probes such as the Tektronix® IsoVu™ series of oscilloscope probes.

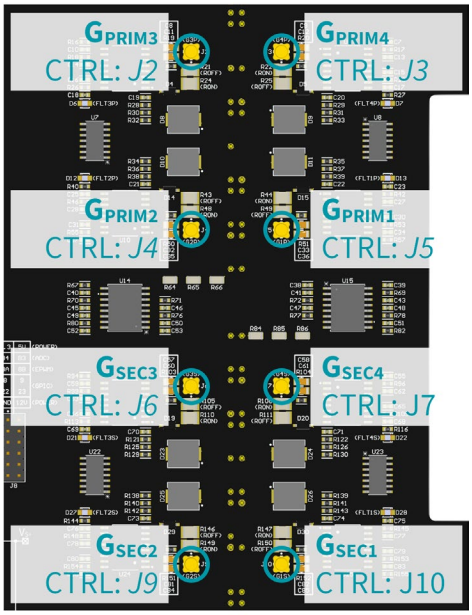

Figure 36: Gate measurement locations on Control Stage

3.2.6 Overcurrent Protection

The CRD60DD12N-GMB gate driver circuits include integrated overcurrent protection in the form of a desaturation circuit, often referred to as a DESAT circuit. The DESAT circuit monitors the drain-to-source voltage (V_{DS}) of the relevant switch position to check for increased on-state voltage due to high current flowing through the channel of the device. An elevated V_{DS} when the device is turned on indicates that the device is conducting excessive current, often in the form of a shoot-through or short circuit event. The DESAT circuit monitors this voltage and systematically shuts down the channel when a fault occurs. More information about the DESAT circuit functionality is found in **PRD-09301**.

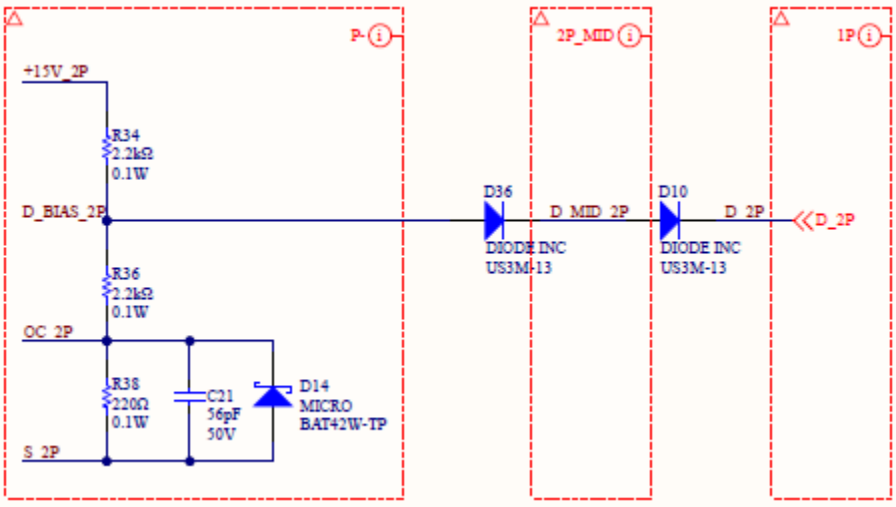

Figure 37: Example DESAT circuit on the Control Stage for primary-side MOSFET #2

When an overcurrent event occurs on one or more of the switch position(s), the tripped gate driver IC will engage a soft-turnoff feature to turn off the tripped device in a controlled manner. The faulted switch position(s) will visually indicate the fault by illuminating a red LED next to the gate driver IC and will transmit a fault signal to the controller. The default firmware will quickly disable all the other gate drivers using the C2000 trip zone hardware functionality. All the gate drivers will be held off until the faulted gate driver is reset. Note that without proper firmware implementation, only the tripped gate driver(s) will turn off after a fault condition. If an operator customizes the firmware, it is important to keep the functionality which quickly detects faults in one or more gate driver(s) and safely disables the remaining drivers.

3.2.7 Temperature Sensing

Every CBB011M12GM4T power module includes an integrated negative temperature coefficient (NTC) thermistor attached to the substrate of the power module. As discussed in Section 2.3.4, these connections to the power module are routed through the interface connector to be monitored by the controller. Monitoring the thermistor temperatures can be used to validate whether the cooling loop is working as intended. **Note that the power module thermistors are representative of the power module case temperature, not the die junction temperature** (see **PRD-08376** for more details). The CRD60DD12N-GMB uses the isolated analog sense functionality of the Texas Instruments UCC21710 gate driver IC to convert the thermistor resistance to a variable duty cycle ranging from 10% to 88% and operating with a 400 kHz carrier frequency. Since there is only one thermistor per module, only the gate driver IC connected to the MOSFET #2 switch position (on both the primary and secondary) includes the circuitry for the thermistor. The thermistor bias circuit is driven from the isolated power supply unit (PSU) of this gate driver switch position. The MOSFET#2 switch position was selected for the thermistor feedback circuit since, when possible, it is preferred to use a low-side switch position for improved noise immunity (see **PRD-09301**) and this switch position is physically close to the thermistor pins on the power module.

There are multiple circuit stages to the thermistor measuring circuits which are summarized in Figure 38. First, a bias circuit – shown in Figure 39 – is used to approximately linearize the thermistor measurements across the temperature ranges of interest. Second, the analog voltage is converted to a duty-cycle encoded square wave using the integrated isolated feedback pin of the Texas Instruments UCC21710 gate driver IC. Third, the output square wave is level shifted from a 5 V signal to a 3.3 V signal which can be monitored directly by the controller. Fourth, the square wave is converted to an analog signal using a RC low-pass filter with a very long time constant. The level-shifting and low-pass filter circuits are both shown in Figure 40. Finally, the analog voltage is read using an ADC and the corresponding temperature is calculated in software.

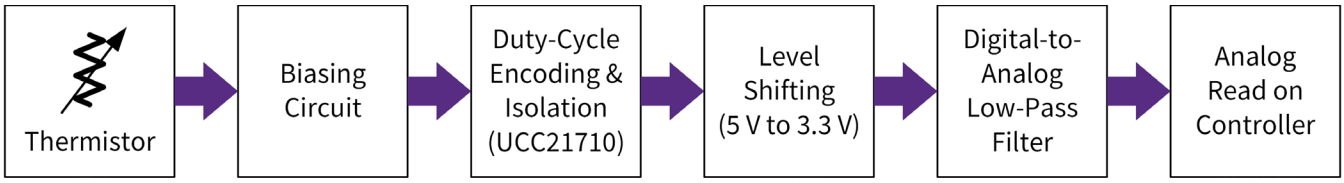

Figure 38: Thermistor feedback block diagram on the control board

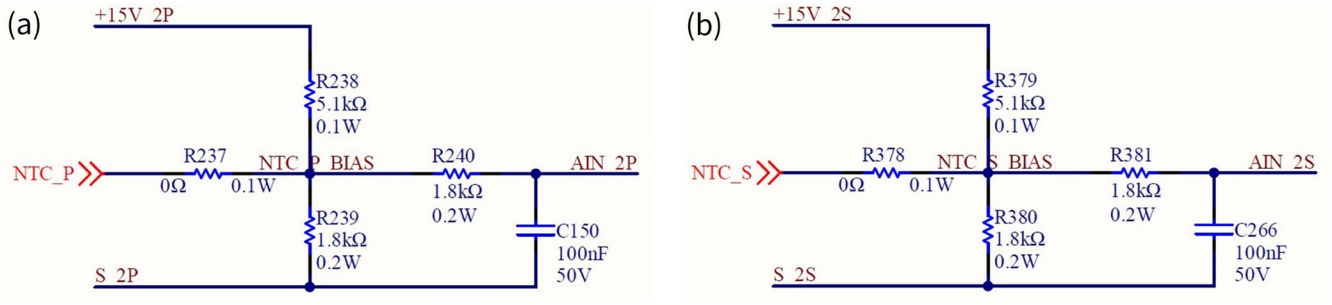

Figure 39: Isolated thermistor bias circuits on Control Stage: (a) primary and (b) secondary

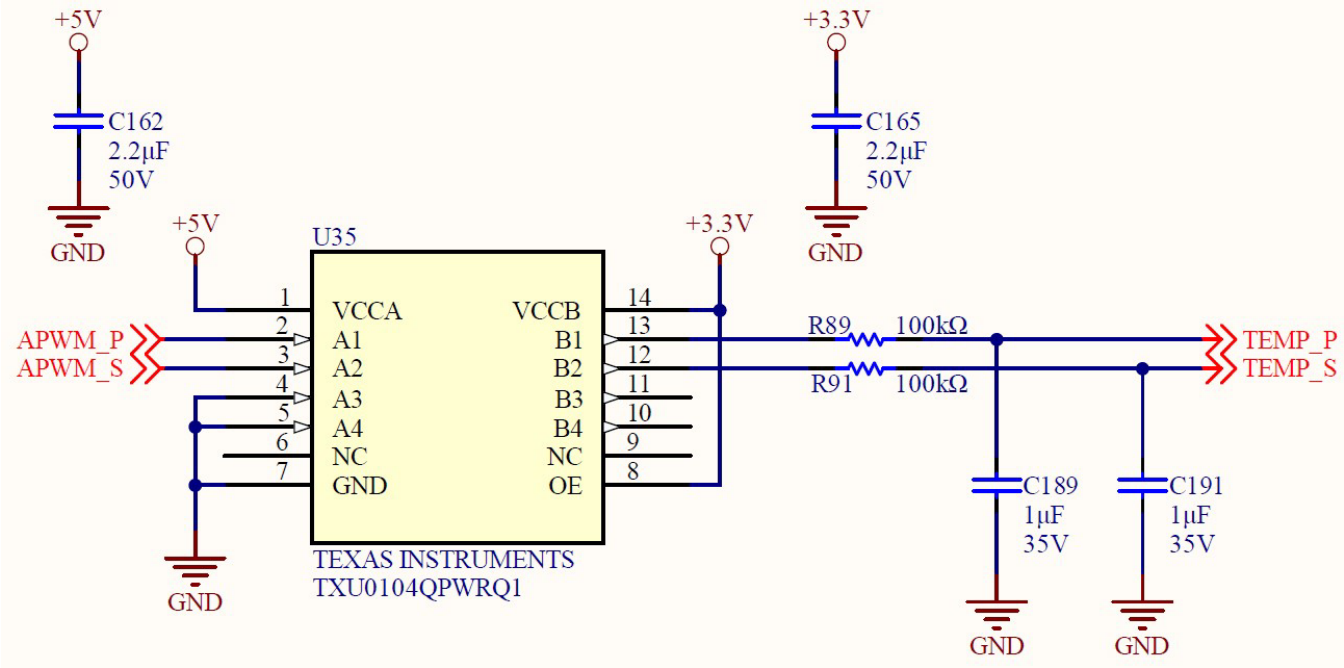

Figure 40: Non-isolated thermistor level-shifting and filtering on Control Stage

Notably, the measurement is performed with an ADC rather than directly measuring the duty-cycle encoded signal using an integrated feature such as the enhanced capture (ECAP) functionality. Since the duty-cycle is encoded at a 400 kHz carrier frequency, this is computationally intensive to perform ECAP interrupts at this frequency. Considering substrate temperature changes typically occur with time constants in the range of seconds, using the heavy compute resources of ECAP were determined to be unnecessary, and the

measurement is instead performed with a simple ADC measurement. With the default firmware, the sampled ADC is converted to its equivalent temperature using

$$T_{MODULE} = (5.65705 \times 10^{-15})x^2 - (5.68188 \times 10^{-11})x^4 + (2.24057 \times 10^{-7})x^3 - (4.31519 \times 10^{-4})x^2 + (4.42508 \times 10^{-1})x - (1.63170 \times 10^{2})$$

where

T_{MODULE}: power module thermistor temperature [°C]

x: sampled ADC register value [unitless, 0-4095].

This equation and conversion process are identical for both the primary and secondary module thermistors. The design also includes an integrated thermistor on the PCB for measuring the ambient board temperature. The conditioning circuit for this measurement is shown in Figure 41. The ambient temperature is measured with a simple ADC and converted to its equivalent temperature using

$$V_{meas} = ADC \times \frac{3.3}{4095}$$

$$T_{PCB} = -7.57401237395V_{meas}^3 + 42.23609778616V_{meas}^2 - 112.01168695609V_{meas} + 145.50862022202$$

where

V_{meas}: voltage at the controller ADC input pin [V]

ADC: measured ADC register value [unitless, 0-4095]

T_{PCB}: measured ambient temperature on the PCB [°C].

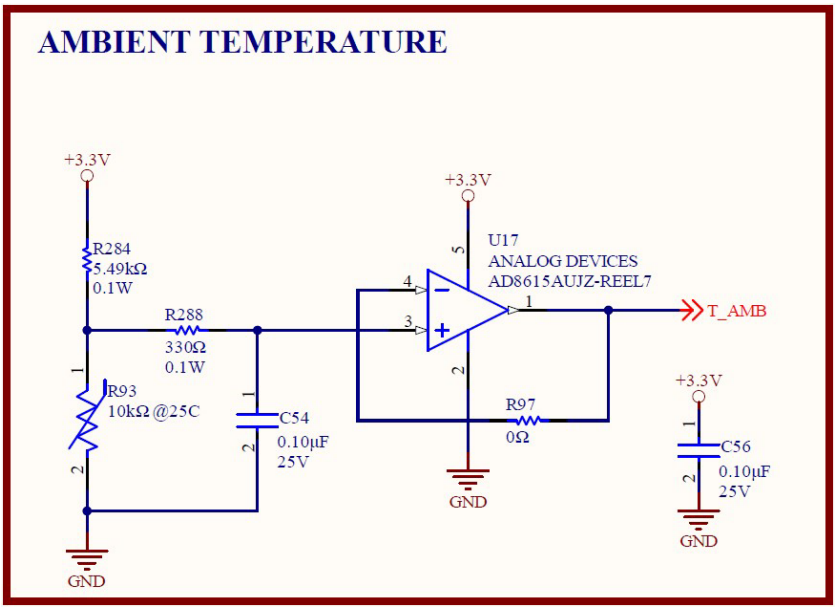

Figure 41: Ambient temperature measurement circuit on Control Stage

3.2.8 CAN Communication

The circuit includes CAN interface hardware allowing users to communicate with the design for real-time monitoring and updating operating conditions. The CAN circuitry is shown in Figure 42. The signals are filtered with a common-mode (CM) choke and Y-capacitors to aid with signal integrity. The Texas Instruments TCAN1044VDRQ1 IC used for the CAN communication supports extended CAN, though the functionality is not employed in the default CRD60DD12N-GMB firmware. The CAN onboard the CRD60DD12N-GMB is not isolated, so an **isolated** CAN adapter must be employed when connecting this design to a host computer.

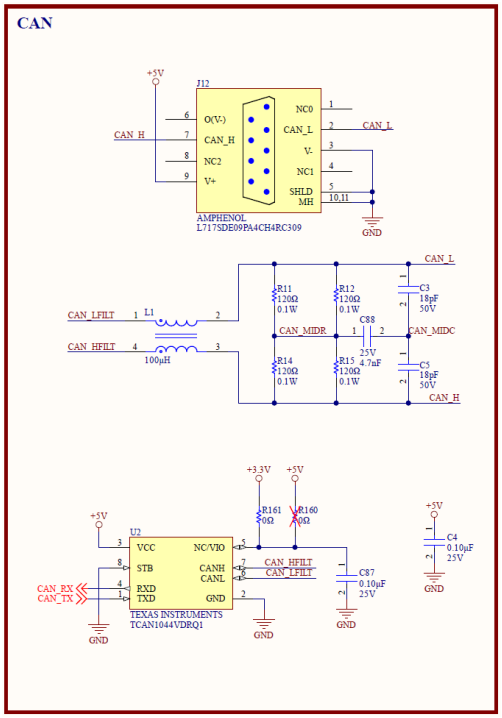

Figure 42: CAN communication hardware on Control Stage

4. Controller and Firmware

The *Control Stage* of the CRD60DD12N-GMB converter was designs around the F280039C controlCARD™ (TMDSCNCD280039C) from the Texas Instruments (TI) C2000™ family of real-time microcontrollers. The controlCARD, shown in Figure 43, plugs directly into the controller PCB. The on-board isolated XDS110 USB-to-JTAG debug probe is a convenient interface to run and debug firmware without additional hardware by connecting a USB-C cable between *J1:A* and a host computer. More information about running firmware is provided in the next section. While the CRD60DD12N-GMB inverter was exclusively tested with the F280039C controlCARD™, theoretically, any microcontroller daughter card with an equivalent pinout could be used. To this end, and to aid with user code development, the complete pinout of the controlCARD, *U5*, along with signal descriptions of utilized pins are shown in Figure 44.

Figure 43: Texas Instruments F280039C controlCARD

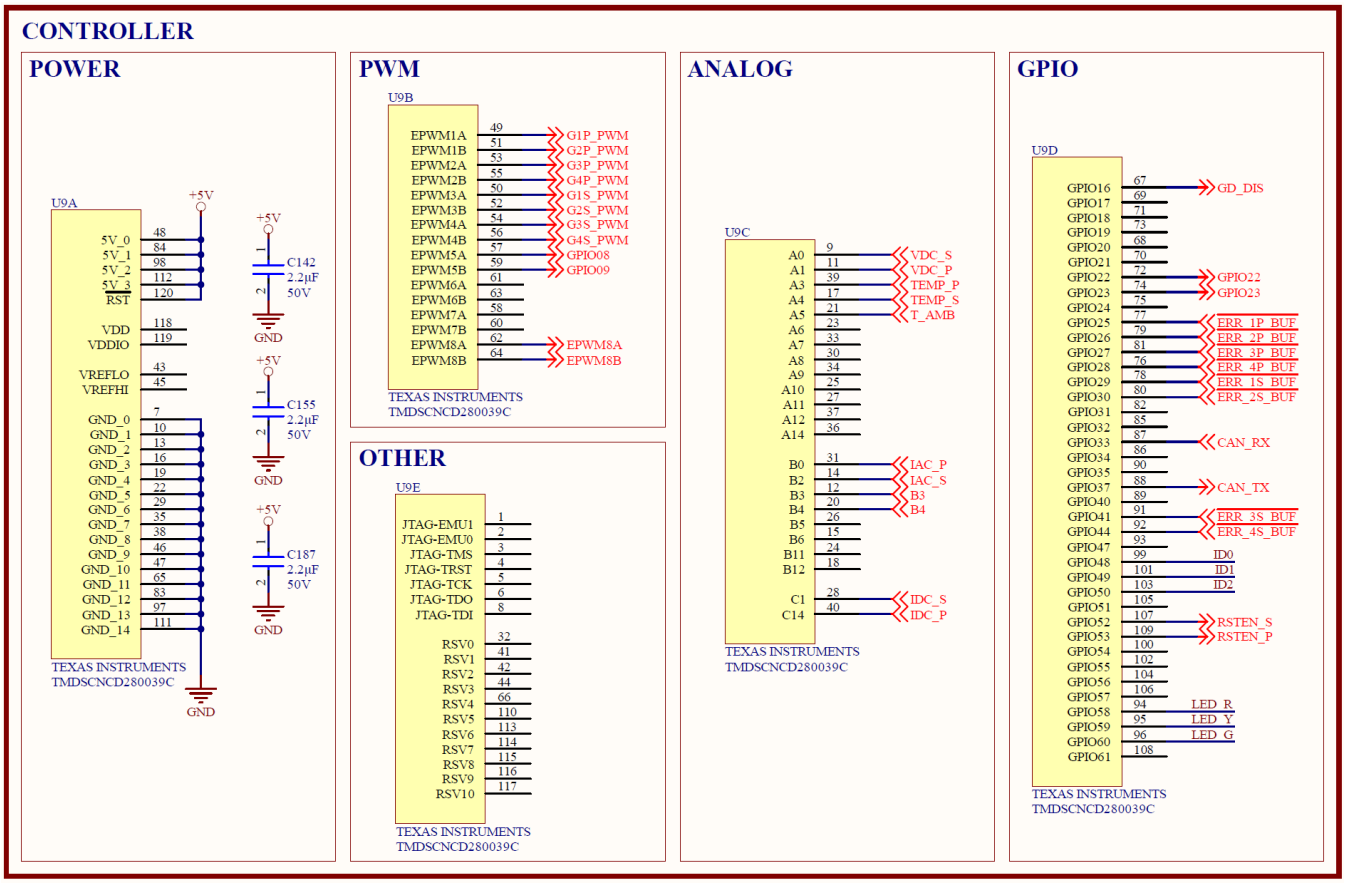

Figure 44: Pinout of controlCARD, U9, on Control Stage

4.1 Firmware

Wolfspeed provides firmware that consists of basic open-loop single-phase-shift (SPS) control of the dual active bridge along with a graphical user interface (GUI) that manipulates the parameters of the open-loop control from a host computer via the CAN protocol. This control suite allows users to test the reference design at the desired test conditions without the need to modify the controller firmware. Alternatively, the provided

firmware source code can be modified at the user's discretion or used as a starting point for users to develop and implement their own application-specific control law. The firmware and GUI for the CRD60DD12N-GMB reference design can be downloaded from Wolfspeed's website on the CRD60DD12N-GMB landing page.

The CRD60DD12N-GMB firmware is provided as a Code Composer Studio™ (CCS) project. The project was developed and tested with CCS version 12.8.1, so this version or newer is recommended to build and run this project. If not installed, download and install CCS from the TI website. The CCS User's Guide provides more details about CCS installation and use.

The software project was also developed and built with TI's C2000Ware to provide device-specific drivers and libraries. C2000Ware version 5.03.00.00 was used for development and testing, so this version or newer is recommended. C2000Ware is a separate installation from CCS, so if not installed, download and install C2000Ware from the TI website. Once the required software is installed, the following instructions can be used to import and run the provided CRD60DD12N-GMB firmware CCS project. To import the project into CCS, click **Project** → **Import CCS Projects** and browse to the local directory where the downloaded project was saved <*Local Directory*>\CRD60DD12N-GMB and click **Select Folder**. Verify the CRD60DD12N-GMB Firmware project was discovered and click **Finish**. Once properly imported, the project should look like Figure 45.

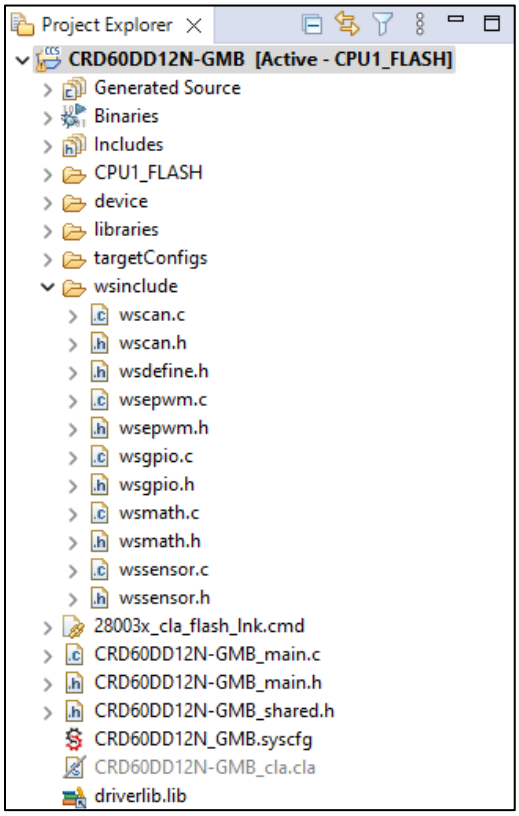

Figure 45: CRD60DD12N-GMB firmware CCS project explorer view

The default build configuration is *CPU1_FLASH* with the linker command file *28003x_generic_flash_lnk.cmd* specified to run the program from Flash memory and the *TMS320F280039C.ccxml* target configuration file to use the on-board XDS100 USB Debug Probe on the F280039C controlCARD. The *wsincude* folder contains all the hardware-specific source files to run the design including the drivers for current, voltage, and temperature sensing, along with the CAN communication protocol.

To build the project, click **Project** → **Build Project** or click on the **Build** icon button on the toolbar. Monitor the **Console** pane to confirm the project was successfully built without any errors. Address any errors listed in the **Problems** pane, if any occur. If there are no errors, go to **Run** → **Debug** or click on the **Debug** icon to launch a debug session. Once the debug session is launched, the program will be halted at the start of main(). Go to **Run** → **Resume** or click the **Resume** icon to start running the code. Add desired variables to the **Expressions** pane and click the **Continuous Refresh** icon to continuously monitor them during the debug session.

4.2 CAN Communication GUI

In addition to the open-loop single phase shift control law being executed by the code, a CAN communication protocol is also operating in the background to provide the ability to manipulate the parameters of the open-loop control from a host computer using the Wolfspeed provided GUI. Once downloaded and extracted, run the *GMB DAB CAN Interface.exe* file where the Wolfspeed Dual Active Bridge CAN Interface control window will appear as shown in Figure 46.

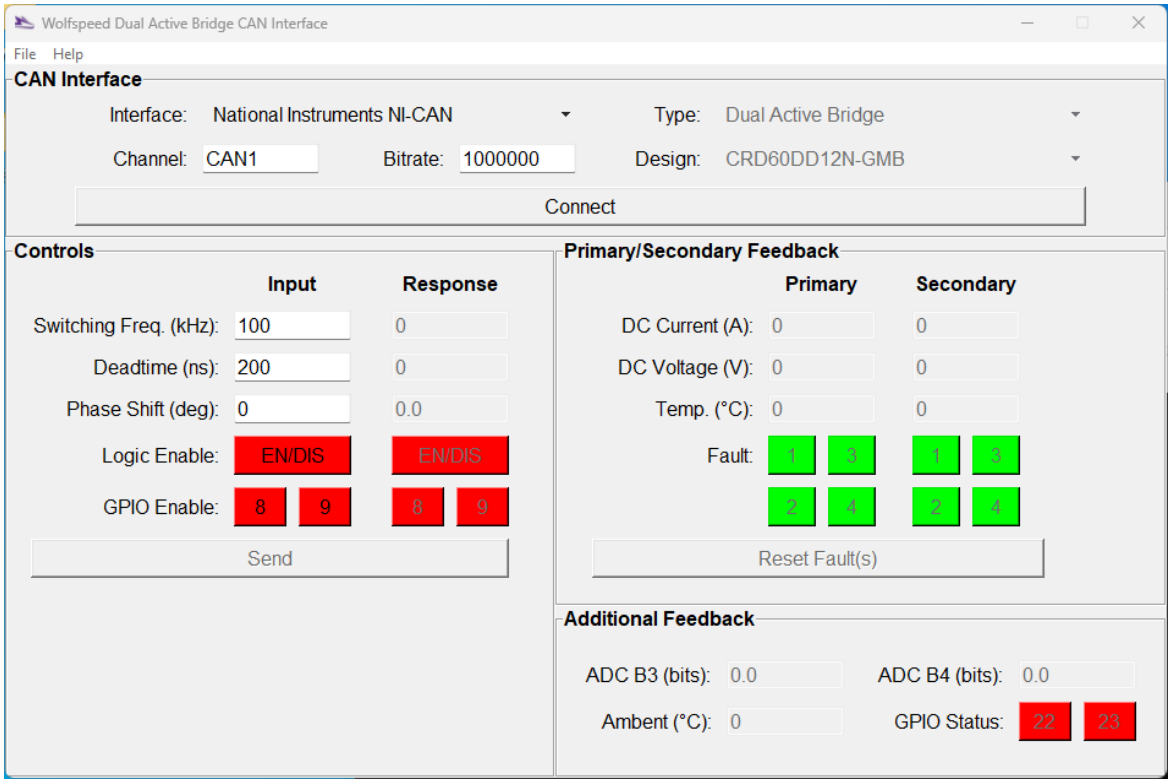

Figure 46: GMB dual active bridge CAN interface GUI

To connect to the design via CAN, first connect the host computer to the CRD60DD12N-GMB design through an **isolated** USB-to-CAN adapter connected to *J9* on the Control Stage. In contrast to many Wolfspeed reference designs which use integrated isolated CAN, the CAN onboard the CRD60DD12N-GMB is not isolated, so an isolated CAN-to-USB adapter must be employed. Ensure that the CRD60DD12N-GMB is powered on and configure the protocol in the *CAN Interface* section at the top of the dialog window. Click on the drop-down menu to select the proper **Interface** and input the correct settings for **Channel** and **Bit Rate** as determined by the CAN hardware adapter being used. Once the proper settings are configured, click **Connect**. The GUI was built using the python-can library which provides support for various hardware adapters. A full list of CAN Interface Modules supported by this library along with the configuration settings can be found at https://python-can.readthedocs.io/en/stable/. Wolfspeed validated system operation at power with two CAN adapters which are summarized in Table 8 along with the associated configuration settings. For best performance, Wolfspeed recommends using one of these adapters when evaluating the CRD60DD12N-GMB hardware.

Table 8: Recommended isolated CAN adapters

Recommended CAN Adapters	Interface	Bit Rate
PEAK System PCAN-USB Pro FD	PCAN_USBBUS**x**[1]	1000000
National Instruments USB-8473	CAN**x**[1]	1000000

[1] : **x** is 0 or 1 depending on the configuration; recommended to try both numbers during initial setup

Once communication is established by clicking **Connect**, a command window will also show a log of the raw CAN packets that are sent and received on the CAN bus. If there is an invalid packet, a warning will be printed, and the errors will be displayed in this window. By default, the CAN packets are transmitted and encoded/decoded in code approximately once every second. The *Controls* section at the bottom left of the window can be used to change various operating parameters on the CRD60DD12N-GMB design while the system is operating.

The GUI control panel provides **Inputs** fields that consist of three numerical inputs and three toggle buttons. Pressing the **Send** button sends a new CAN packet with the populated values of each input field. A description of each **Inputs** field is given below.

Switching Frequency field is the frequency of the output PWM in kHz. The default value is 100 = 100 kHz. The input range is 80 – 100.

Deadtime field is the dead time between the complementary high-side and low-side switch position PWM for each bridge-leg in nanoseconds (ns). The default value is 200 = 200 ns dead time. The input range is 100 – 2000.

Phase Shift field is the phase shift between the primary and secondary full bridges of the dual active bridge in degrees. The default value is 0 = 0 degrees (i.e. no phase shift). The input range is -90 – +90 and the input accepts resolution to ±0.1 degree.

Logic Enable toggle-button enables and disables the PWM logic of all eight switch positions. By default, the logic is disabled, so the toggle-button is highlighted red. When enabled, the toggle-button will turn green.

GPIO Enable toggle-buttons enable and disable the output GPIO pins of the *J8 Control Stage* auxiliary connector (see Section 2.3.6). These GPIO outputs can be utilized for controlling external sensors or hardware for user customizations. By default, the logic is disabled, so the toggle-buttons are highlighted red. When enabled, the toggle-buttons will turn green.

Response field displays the values contained in the most recent packet sent from the controller, indicating the status of each control parameter or confirming values were properly updated after a new input packet was sent.

Also included in the information sent by the controller in each packet are the feedback values. The values critical for most users are shown in the *Primary/Secondary Feedback* section of the GUI. This section displays the DC bus voltages (V), DC currents, and power module thermistor temperatures (°C) for both the primary and secondary. When a fault occurs, all the PWM signals are disabled by the controller and the corresponding phase(s) will appear as red in the **Fault** response field. In addition, when a fault occurs, the **Send** button will be disabled, the **Reset Fault(s)** button will be enabled, and the **Logic Enable** will be disabled. After the fault is identified, a user should first safely resolve the issue causing the fault. When the inverter is in a safe state to re-start, press the **Reset Fault(s)** button to clear the faults and enable the converter to be operated again. Upon receiving the reset command, the controller will apply the proper signal sequence to reset the fault(s) on the gate drivers. After the fault is cleared, the **Fault** response fields will return to green status the **Send** button will be enabled again, allowing for reestablished converter operation.

The *Additional Feedback* section of the GUI can be used for user customization. The onboard thermistor temperature (°C) is shown in the **Ambient (°C)** field. The status of the GPIO inputs connected to the *J8 Control Stage* auxiliary connector (see Section 2.3.6) are displayed in the **GPIO Status** field. These GPIO inputs use 3.3 V logic by default and will appear as red when the signal is low and green when the signal is high. By default, the ADC fields show the current sampled ADC register value (0-4095) of the ADC inputs connected to the *J8 Control Stage* auxiliary connector. These fields can be customized by navigating to **File** → **Configure ADCs** to open the window shown in Figure 47. This window allows operators to apply custom sensor scaling to the measured ADC values without having to modify the CRD60DD12N-GMB firmware.

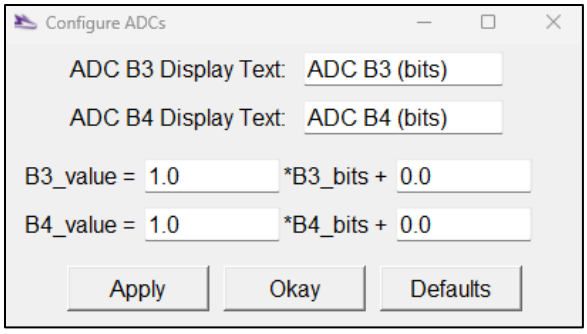

Figure 47: Configure ADCs window

To utilize the window, first change the **ADC Display Text** to provide information about the sensor input such as the sensor name and units. Second, change the scaling values to convert the ADC register value to the appropriate sensor units. The application accepts linear equations for scaling the sensor values. For example, assume that a voltage sensor is attached to ADC B3 and requires the below scaling

$$V_{sensor} = 0.0008 \cdot ADC + 1.65$$

where

V_{sensor}: measured sensor voltage [V]

ADC: sampled ADC register value [unitless, 0-4095].

In this example, the *Configure ADCs* window could be configured as shown in Figure 48. Select **Okay** once the settings are properly configured. The updated **ADC Display Text** will be shown in the **Additional Feedback** section of the GUI as shown in Figure 49, and the sensor feedback from the CRD60DD12N-GMB will be automatically scaled by the inputted equation when displayed in the GUI. This customization provides more useful feedback from any auxiliary sensors connected to the board. A full **Help** window for operating the GUI is not supported at this time. Navigating to Help → About provides GUI version information through the window shown in Figure 50.

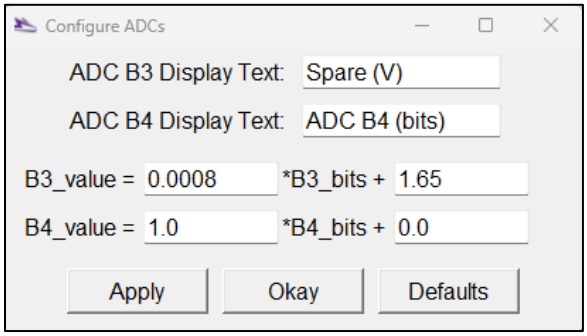

Figure 48: Example Configure ADCs window

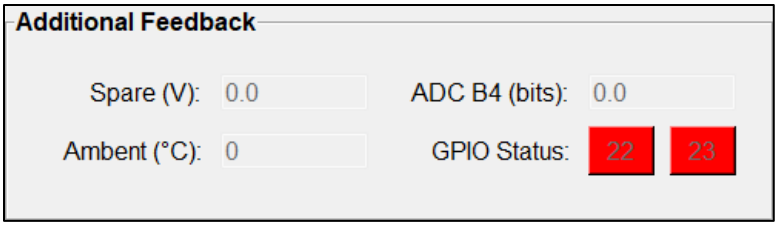

Figure 49: Example updated Additional Feedback section

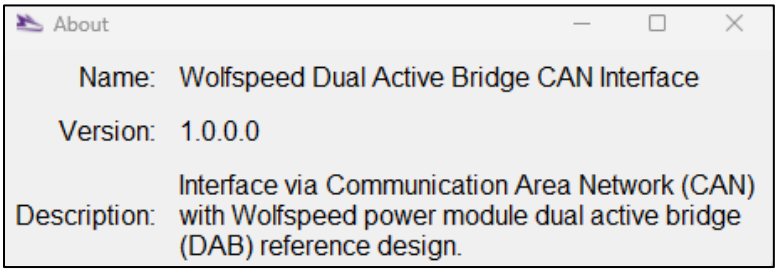

Figure 50: GUI About window

5. Performance

During development, Wolfspeed performed several measurements to characterize the thermal behavior of this reference design and to evaluate its performance at various operating conditions. This section details the measured characterization of the CRD60DD12N-GMB.

5.1 Coldplate

The thermal performance of the module and system is influenced by its ability to reject heat from the device junction to its ambient environment. The baseplate-less design of the Wolfspeed CBB011M12GM4T already reduces the device thermal impedance compared to a similarly sized power module since less material (i.e. baseplate) is present in the thermal path. To further maintain thermal integrity, this design uses a custom form-fit cold plate for cooling the power modules. Renderings of the cold plate are shown in Figure 51. The design uses an array of pin fins under the power modules to improve thermal performance. The coldplate includes two 1/2" female NPT threads for attaching the inlet and outlet water connections to the coldplate. The coldplate and pin fins are symmetrical, so the coolant can be routed in either direction, though it is recommended for the coolant to flow through the output stage of the DAB first since the output stage is stressed more in typical operation. This coolant flow orientation is shown in Figure 52.

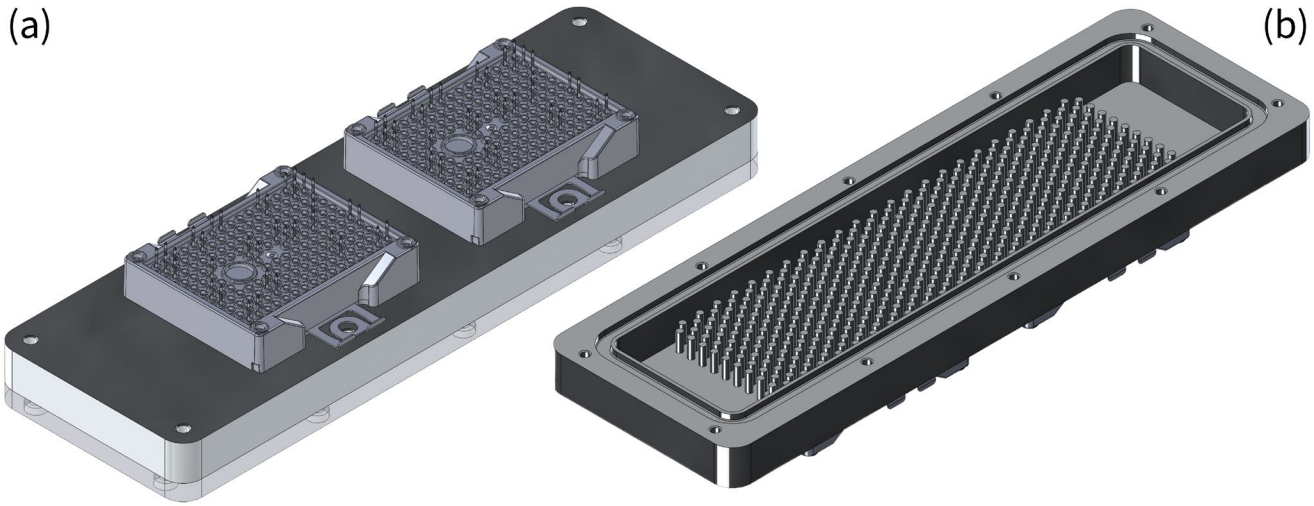

Figure 51: Custom CRD60DD12N-GMB coldplate renderings: (a) top and (b) pin fins

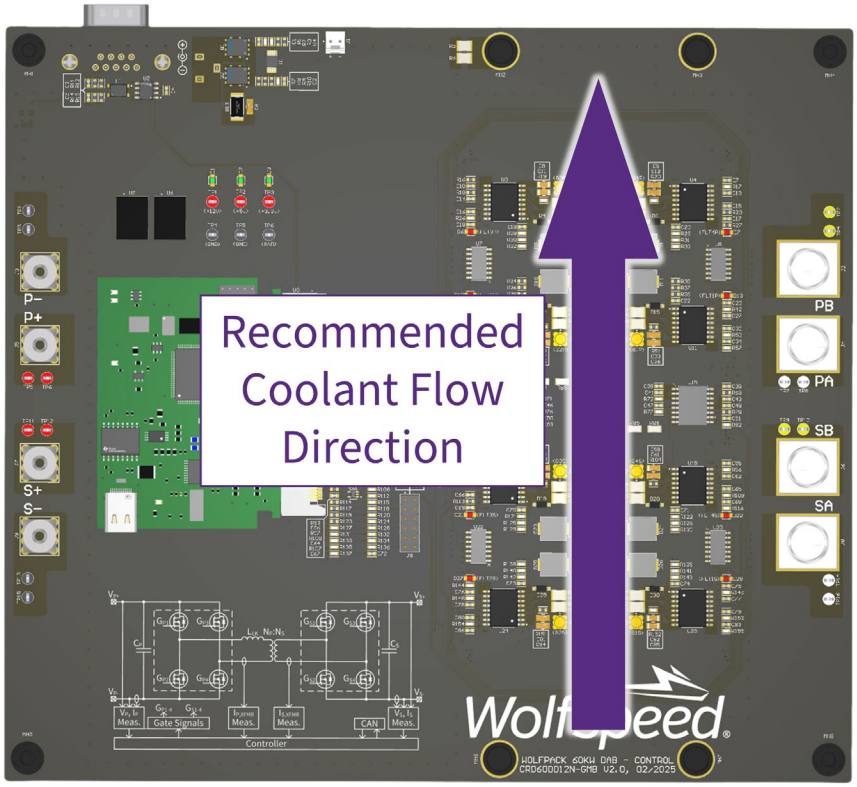

Figure 52: Recommended coolant direction from secondary to primary

The coldplate is attached to the Power Stage through four conductive standoffs which are all floating with respect to any voltage potentials on the *Power Stage*, as shown in Figure 29 and Figure 53(a). Each of these standoffs are also connected to the *Control Stage* through conductive standoffs. One of standoffs (*MH2*), grounds the coldplate to the low-voltage ground on the *Control Stage*, as shown in Figure 53(b). The coldplate

can be floated with respect to any voltage potential by removing the 0 Ω resistors (*R5* and *R6*) on the *Control Stage* to disconnect the coldplate from the low-voltage ground power rail.

The coldplate pieces are machined from 6061 aluminum and mechanical drawings for the coldplate pieces are provided in Section 6. The coldplate pieces clamp together using ten M3 bolts and a VE70.125-012 o-ring manufactured The O-Ring Store® with a 142 mm inside diameter. The design includes two 1/2" NPT female to male 90° elbow adapters (McMaster-Carr® 50785K451) and two 1/2" NPT male to 3/4" hose adapters (McMaster-Carr 5346K68) to enable users to easily attach 3/4" hose to the design for input and output coolant connections.

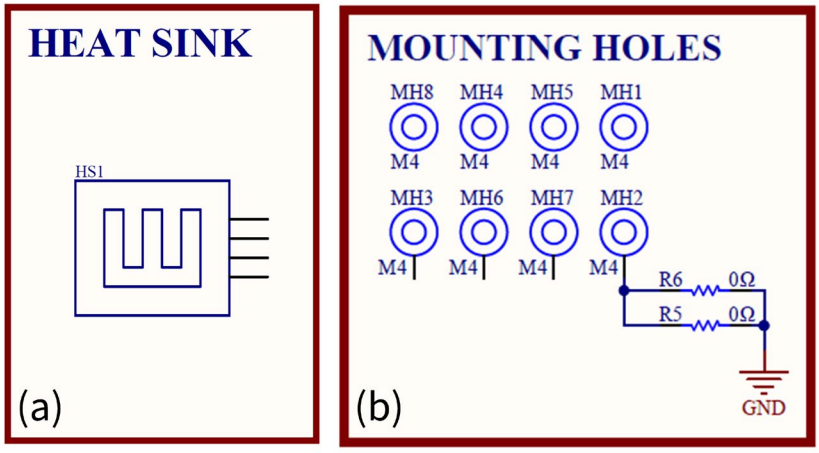

Figure 53: Schematic of the coldplate connections on the (a) Power Stage and (b) Control Stage

The junction-to-heatsink thermal impedance, Z_{th}, for the power module is provided in the device datasheet. However, to evaluate the thermal performance of the entire thermal stack-up of this reference design, the thermal impedance of coldplate was also characterized. Characterizing the coldplate within the system was performed using a Siemens® Simcenter POWERT3ster™, which is an all-in-one thermal evaluation instrument to determine the thermal impedance of devices and applications. The single pulse transient thermal impedance measurements of the module, heatsink, and the combination of the two were used to determine the coldplate-to-thermal impedance of 0.045 K/W. Note that these measurements are for a single switch position of the power module. This impedance can be used for hand calculations of design power losses or to populate simulations.

5.2 Transformer

The CRD60DD12N-GMB design is intended to demonstrate best practices with SiC MOSFETs such as routing and gate driver design. Though the design does not include a transformer by default, Wolfspeed recommends a custom 81989-01 transformer developed by Egston Pulse a YAGEO Company shown in Figure 54. The transformer is 202 mm (L) by 81 mm (W) by 73 mm (H) and the measured transformer characteristics at 100 kHz are shown in Table 9. The transformer is designed to be mounted to a coldplate with liquid cooling and can be added in series with the output of the *Power Stage* coldplate.

Figure 54: CRD60DD12N-GMB connected to YAGEO transformer

Table 9: Custom transformer characteristics (measured at 100 kHz)

Description	Parameter	Value
Leakage Inductance	L_σ	7.5 µH
Magnetizing Inductance	L_m	329 µH
Winding Resistance	R_w	78 mΩ
Core-Loss Resistance	R_c	1.24 Ω

5.3 Experimental Validation

5.3.1 Setup

The system was configured with an Elektro-Automatik® 11500-60 electronic load allowing the CRD60DD12N-GMB to be operated up to the rated power of the electronic load. The design was powered with a Magna Power® TSD1000-30/208+LXI power supply unit with a rated output of up to 1000 V and 30 kW. The custom YAGEO 81989-01 transformer discussed in Section 5.2 was used as the isolation transformer for this testing. The transformer coldplate was added in series with the output of the CRD60DD12N-GMB coolant loop. The system was cooled with 20°C pre-mixed antifreeze coolant at 9 L/min. The gate voltages, transformer currents, transformer voltages, and output voltage were measured using a Tektronix MSO50B oscilloscope with a rated bandwidth of 1 GHz. These measurements were performed with the isolated high-bandwidth probes summarized in Table 10. The efficiency measurements were performed with a Hioki® PW6001 power analyzer and Hioki CR6872 50 A, 10 MHz AC/DC current sensors.

Table 10: Oscilloscope probes use for experimental measurements

Measurement	Description	Probe	Description
$V_{XFMR,PRIM}$, $V_{XFMR,SEC}$	Primary & Secondary Transformer Voltages	Tektronix THDP0200	1.5 kV, 200 MHz, Differential Voltage Probe
$V_{GS,PRIM4}$, $V_{GS,SEC4}$	Primary & Secondary MOSFET #4 Gate Voltages	Tektronix IsoVu™ TIVH05	50x Tip, 1 GHz, Optically Isolated Probe
$I_{XFMR,PRIM}$, $I_{XFMR,SEC}$	Primary & Secondary Transformer Currents	Tektronix TCP0150	150 A, 20 MHz, AC/DC Current Probe
V_{OUT}	Secondary DC Output Voltage	Tektronix THDP0200	1.5 kV, 200 MHz, Differential Voltage Probe

5.3.2 Results

The system was evaluated at several load operating conditions to validate the system performance. The operating conditions used for the experimental sweep are shown in Table 11. An example oscilloscope waveform is shown in Figure 55, demonstrating the system operation over the duration of several switching periods at an output load of 22.7 kW. Additional measurements were performed for shorter time durations to validate other system performance parameters, such as voltage overshoot. An efficiency sweep across a range of output powers is presented in Figure 57. To validate the long-term performance of the evaluation board, the inverter was operated for over 30 minutes under these same load conditions. The thermal image in Figure 56 was taken at the end of the allotted time, demonstrating adequate thermal performance of the power modules. The temperature scale is in degree Celsius, and at that time, the thermistor temperature was reading 24 °C. Before shipment, each inverter kit is burned in at ~22 kW to confirm system operation.

Table 11: Experimental operating conditions

Description	Parameter	Value
Input Bus Voltage	V_{IN}	800 V
Output Bus Voltage	V_{OUT}	800 V
Switching Frequency	f_{SW}	100 kHz
Deadtime	t_{DEAD}	200 ns
Turn-On Gate Resistance	$R_{G,ON}$	1 Ω
Turn-Off Gate Resistance	$R_{G,OFF}$	0 Ω
Output Power	P_{OUT}	10-23 kW
Phase Shift	ϕ	2.5-5.0°

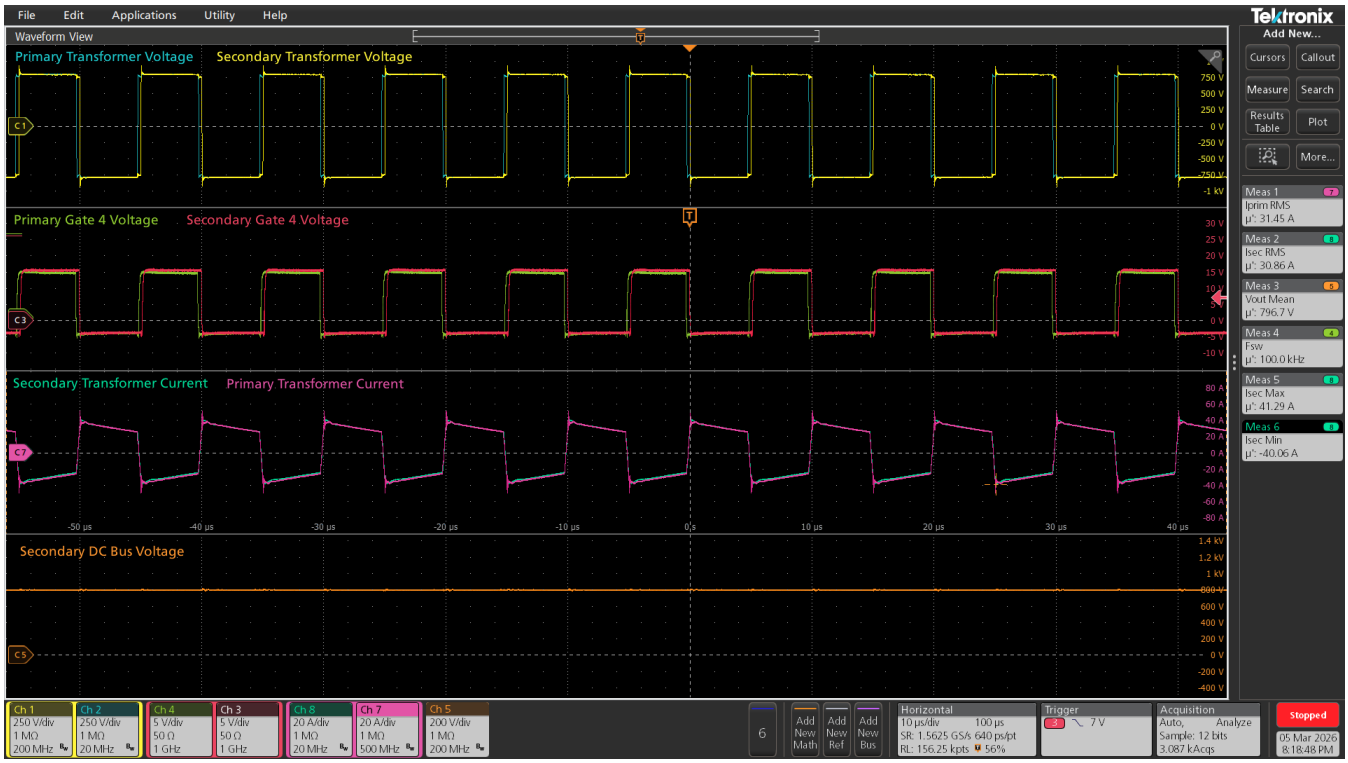

Figure 55: Example oscilloscope measurements at P_{OUT} = 22.7 kW

Figure 56: Output full-bridge module temperature at 22.7 kW

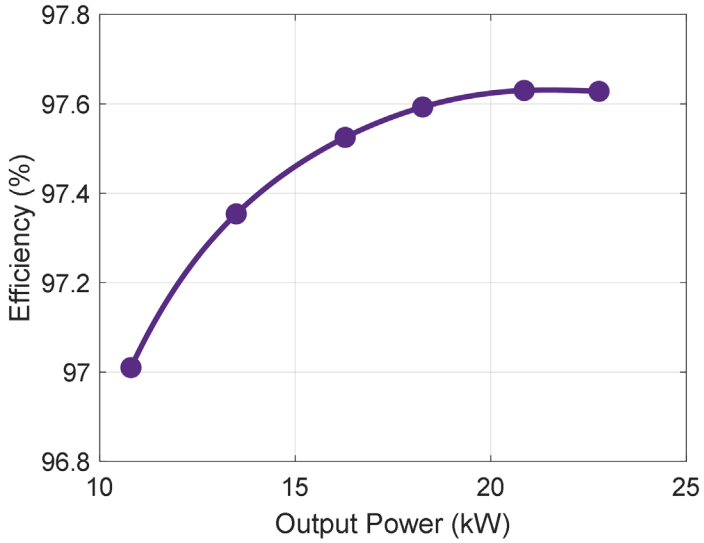

Figure 57: Efficiency vs output power experimental results

5.4 Simulation

A Plexim® PLECS® simulation of the hardware is included as a download with the design files. The top-level of the simulation is shown in Figure 58, and the various subsystems are explained in the following sections. The simulation values are populated using the initialization script found by navigating to **Simulation → Simulation parameters… → Initialization**. The simulation can be employed by interested users as a replacement for purchasing the hardware, as a tool to evaluate whether to purchase the hardware, and/or as a tool for making custom modifications to the controller. This simulation requires an active license of PLECS in order to run the simulation (PLECS Standalone 4.9.7 or newer is recommended). Licenses for PLECS can be purchased at https://www.plexim.com/products/plecs. More information about how to use PLECS can be found in the help guides on the PLECS website and in the program documentation. For users not familiar with PLECS, tutorials covering basic usage of the software are available at https://www.plexim.com/support/tutorials.

As with the actual hardware, the power stage of the inverter uses the Wolfspeed CBB011M12GM4T full-bridge baseplate-less modules. The power module model is included in the simulation zip folder, so the simulation can be run by simply unzipping the download folder and navigating to **Simulation → Start**.

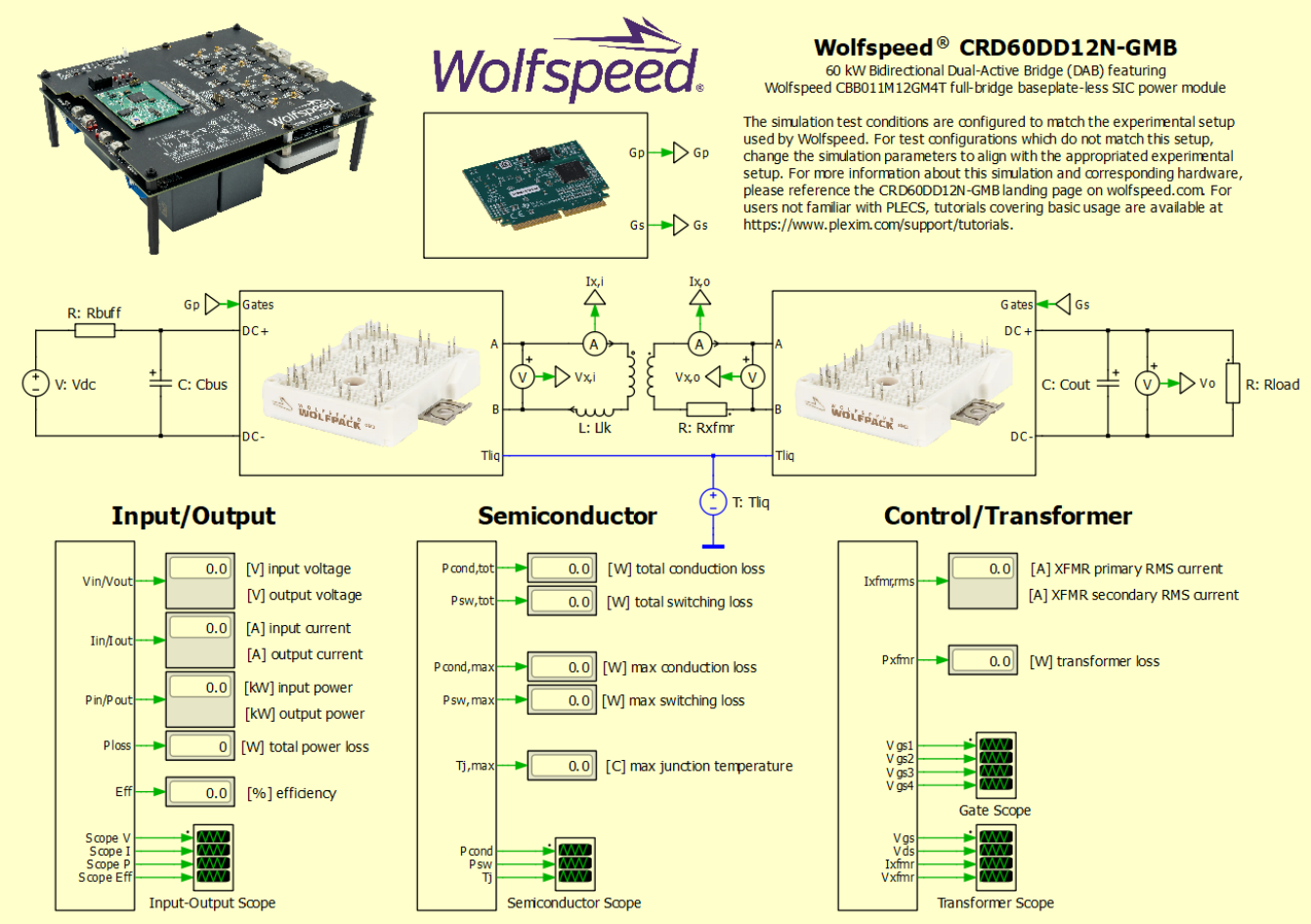

Figure 58: CRD60DD12N-GMB simulation

5.4.1 Power Stage

The power stage subsystems includes the power module MOSFET models and the corresponding thermal networks to the ambient coolant temperature. As described in Section **Error! Reference source not found.** of this document, the thermal impedance of the heatsink in this system was directly measured and an equivalent thermal resistance was fit to the data. When paired with the PLECS model of the Wolfspeed CBB011M12GM4T, this produces an accurate thermal model of the entire system. The Wolfspeed CBB011M12GM4T model is based on extensive experimental characterization of the modules. The primary-side power stage simulation model is shown in Figure 59, and the secondary-side power stage simulation model is shown in Figure 60.

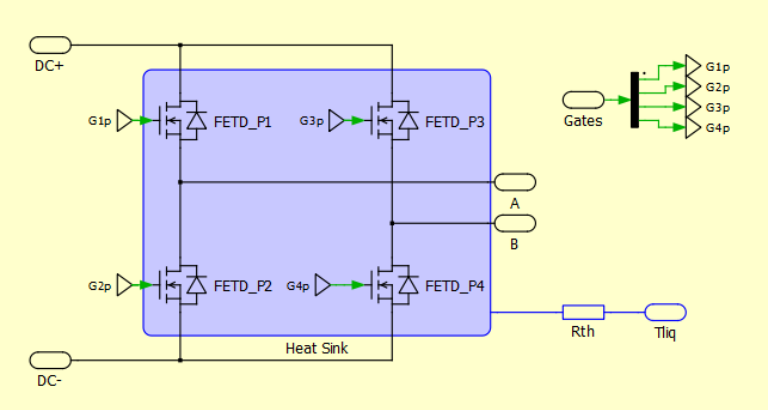

Figure 59: Simulation primary-side power stage

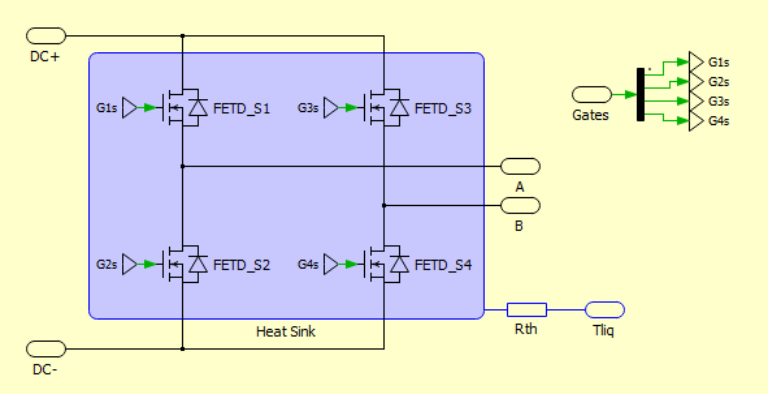

Figure 60: Simulation secondary-side power stage

5.4.2 Controller

The simulation parameters are configured to match the setup used to validate the hardware discussed in Section 53. To match that configuration, the simulation uses single phase shift control for generating the gate signals and is operated in an open-loop configuration. The SPS controller used to generate gate signals is shown in Figure 61.

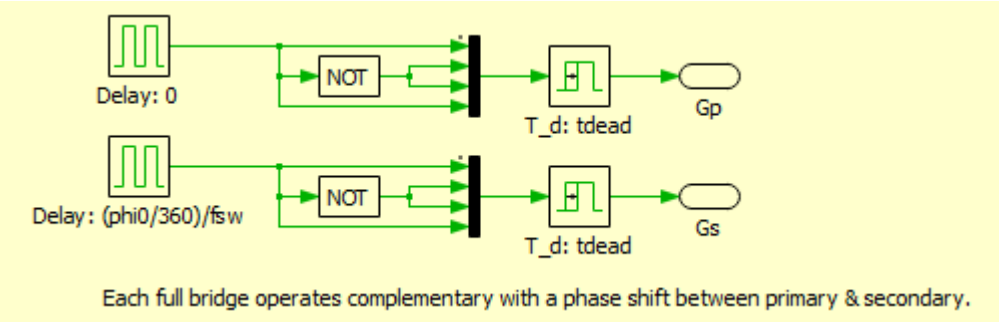

Figure 61: Simulation single-phase-shift controller

5.4.3 Performance Monitors

The simulation includes subsystem to monitor the primary performance characteristics of the model. Figure 62 shows the performance monitor for the semiconductors. This subsystem monitors conduction losses, switching losses, and junction temperature of all the switch positions. Figure 63 shows the performance monitor for the transformer and control signals. This subsystem monitors the transformer losses, voltages, and currents along the gate control signals. Figure 64 shows the performance monitor for the input and output operating characteristics of the simulation. This subsystem monitors input/output voltage, current, power, and losses to provide an overview of the simulation.

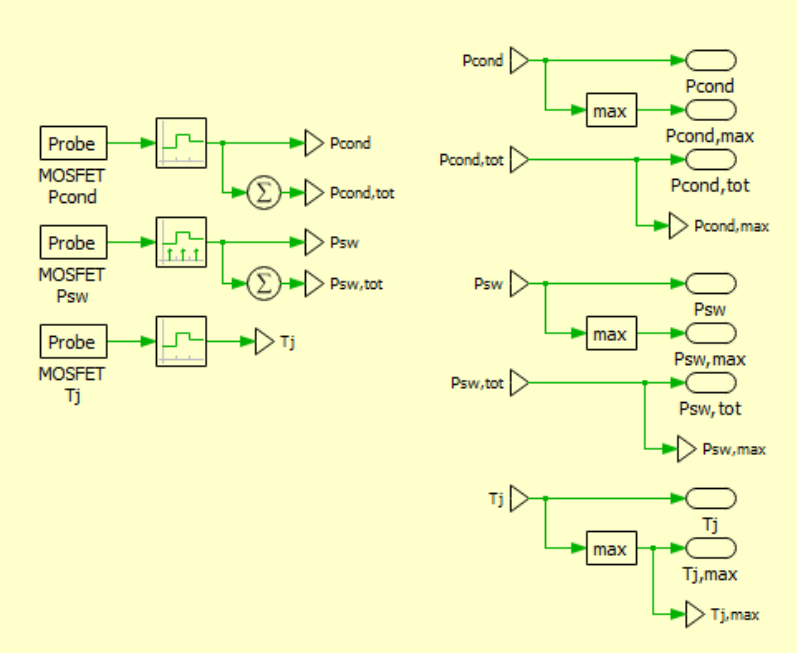

Figure 62: Semiconductor simulation performance monitor

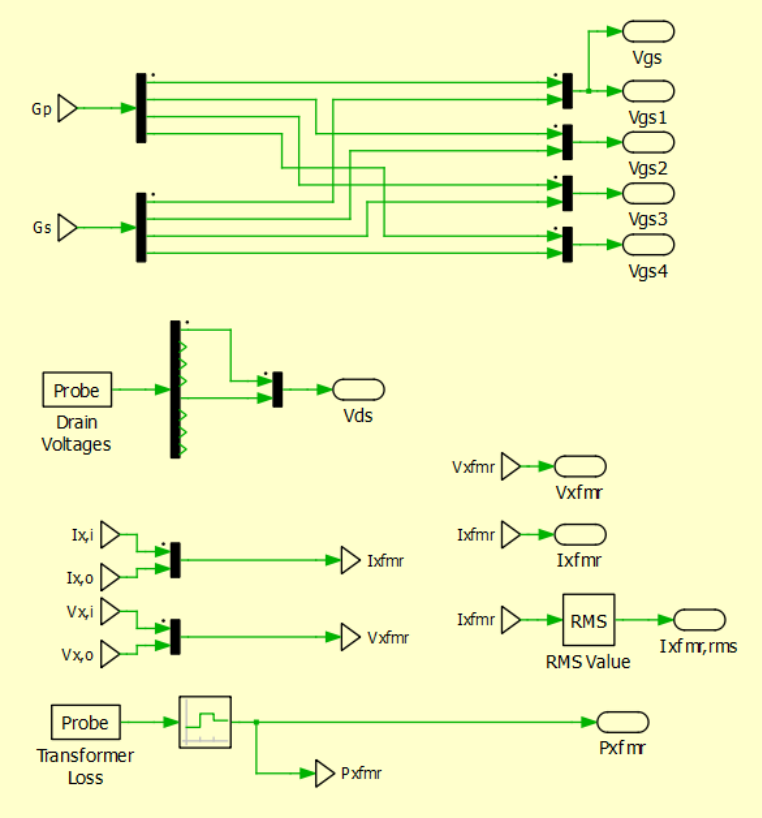

Figure 63: Transformer and gate simulation performance monitor

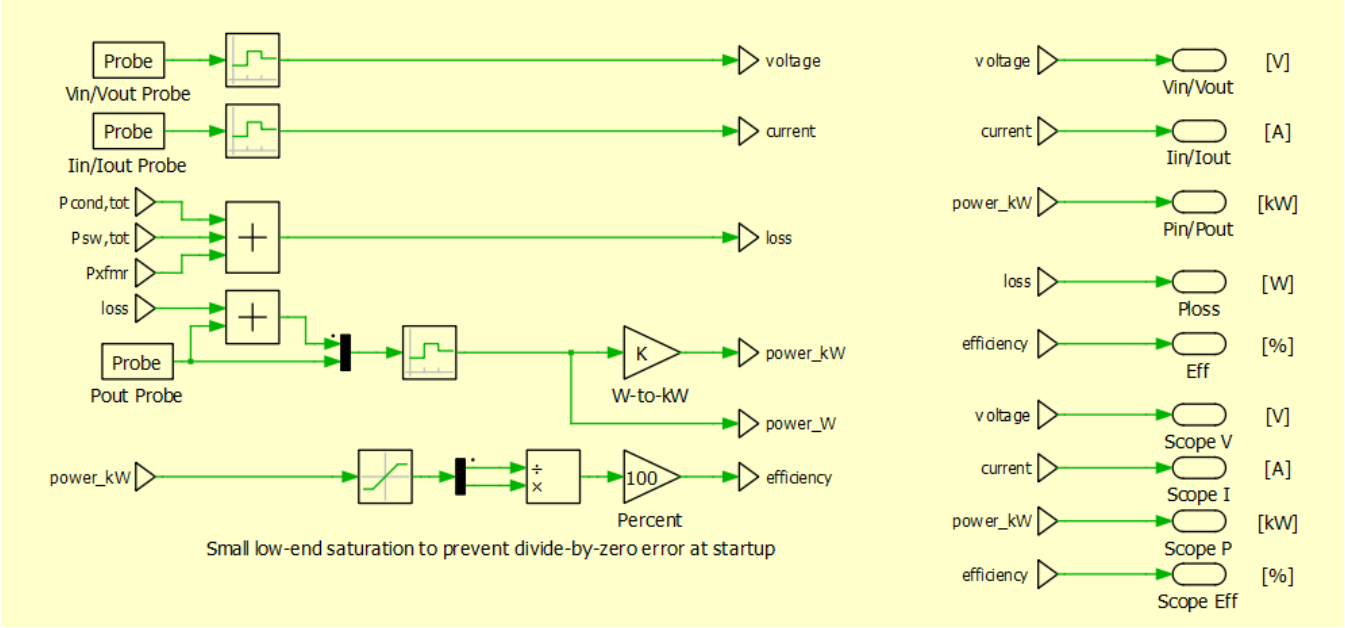

Figure 64: Input/output simulation performance monitor

6. Dimensions

in [mm]

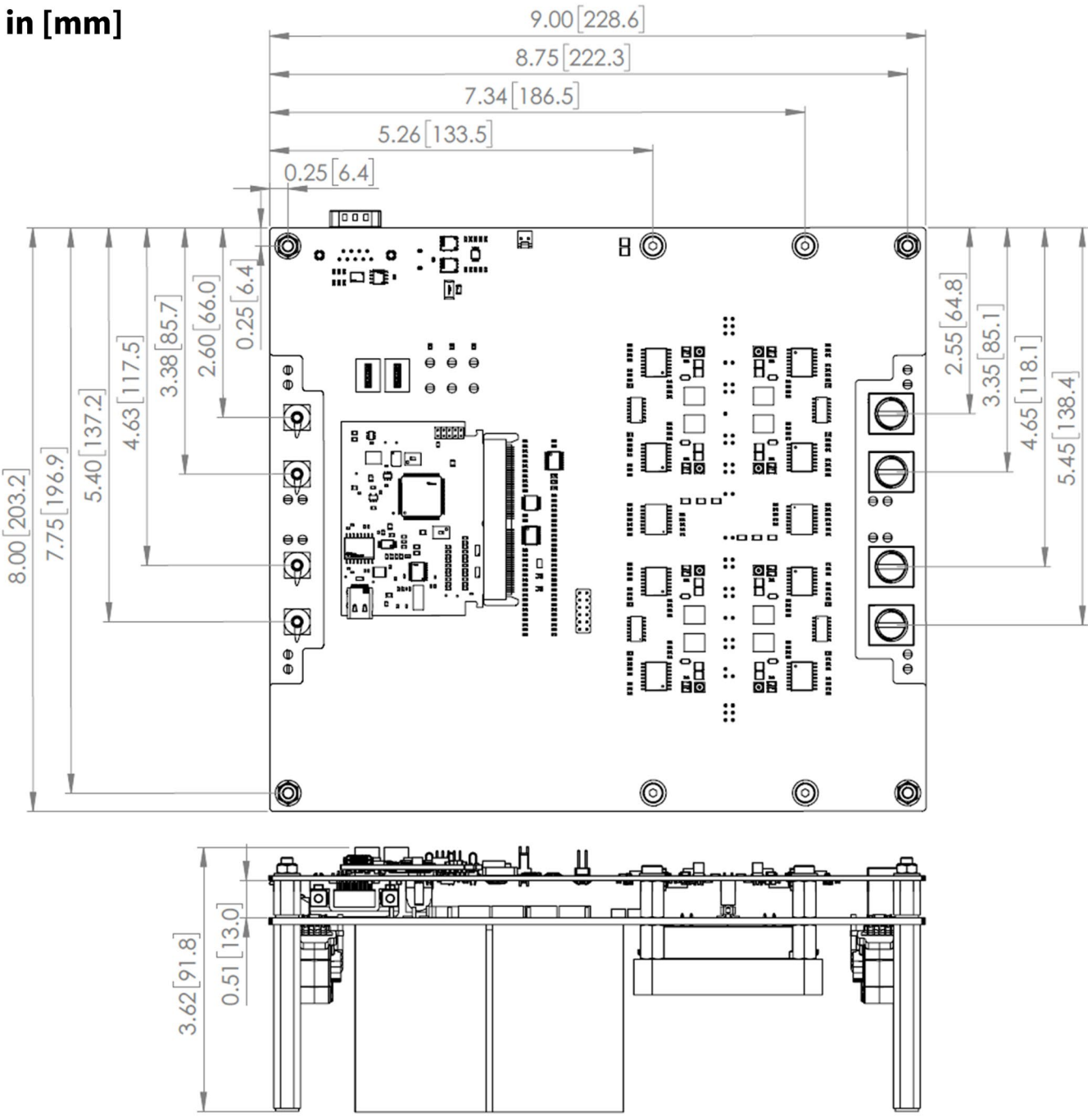

Figure 65: Dimensions of the CRD60DD12N-GMB dual active bridge

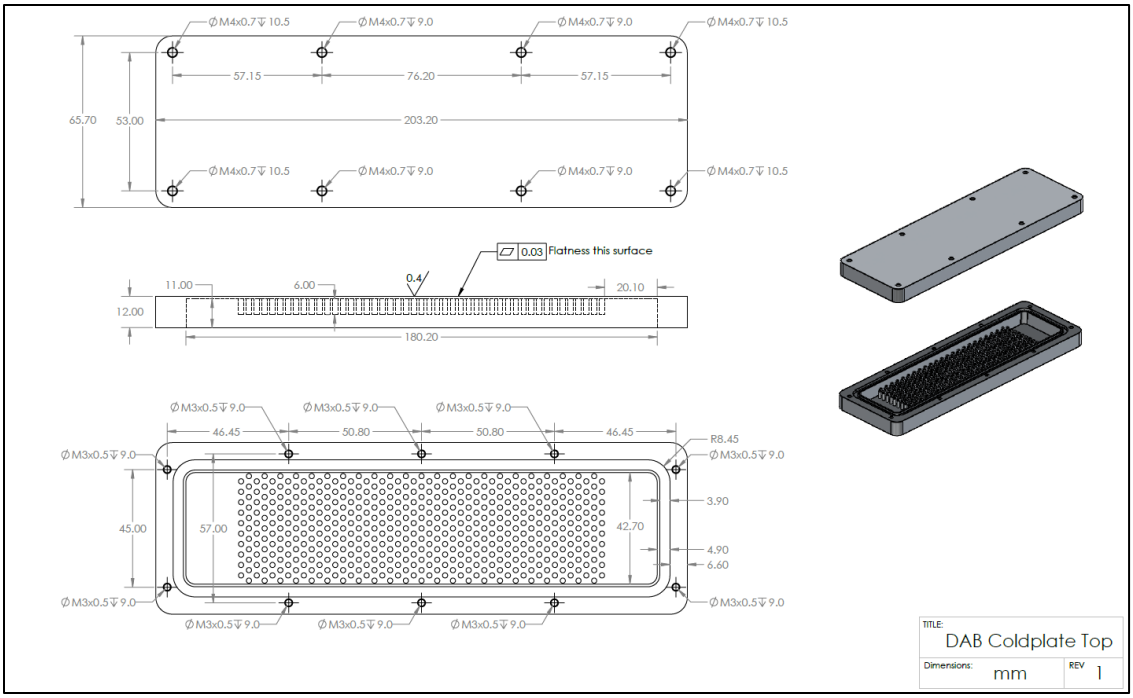

Figure 66: Mechanical drawing of custom coldplate top piece

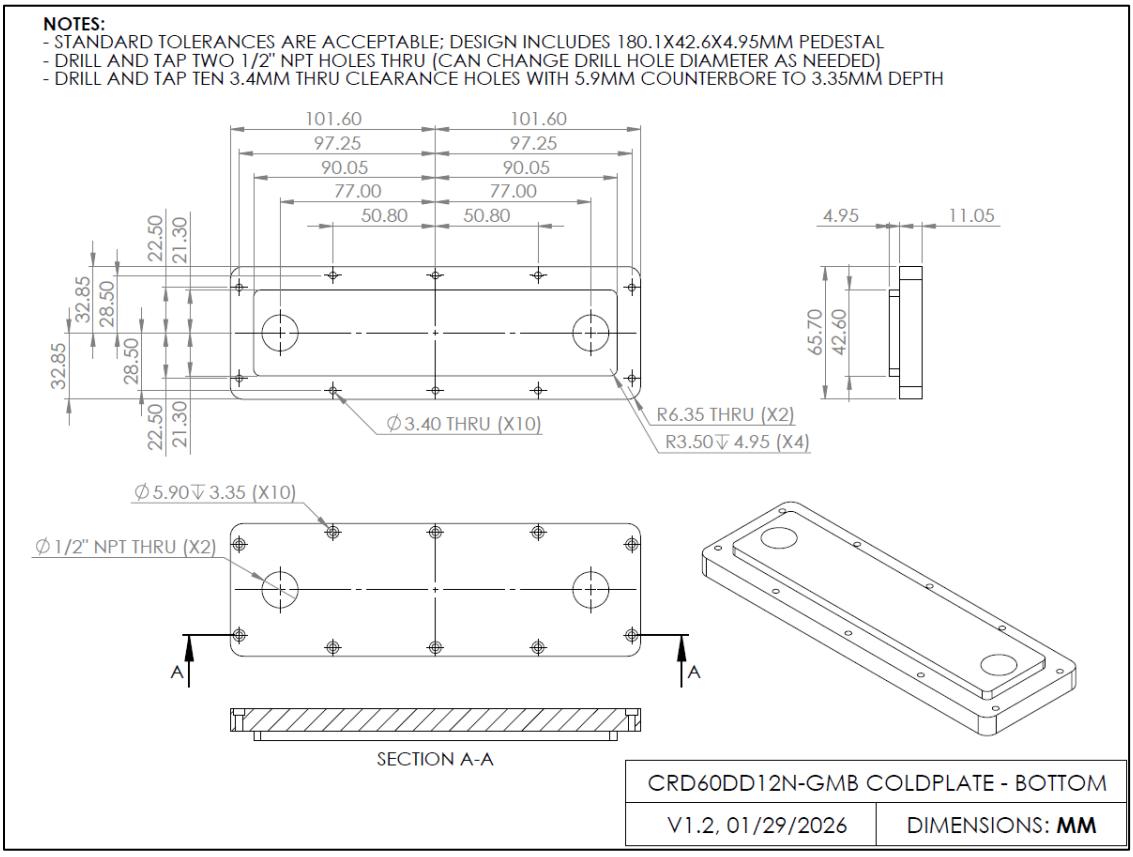

Figure 67: Mechanical drawing of custom coldplate bottom piece

7. Supporting Links and Tools

The following links provide additional information about the 1.2 kV GM WolfPACK power module portfolio and design tools for using the devices. Please navigate to the landing page for this design for additional links and support.

- 1.2 kV GM Module Product Family
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum
- All LTspice Models
- All PLECS Models

Revision History

Date	Revision	Changes
May 2026	1	Initial Release

IMPORTANT NOTES

PURPOSES AND USE

Wolfspeed, Inc. (on behalf of itself and its affiliates, "Wolfspeed") reserves the right in its sole discretion to make corrections, enhancements, improvements, or other changes to the board or to discontinue the board.

THE BOARD DESCRIBED IS AN ENGINEERING TOOL INTENDED SOLELY FOR LABORATORY USE BY HIGHLY QUALIFIED AND EXPERIENCED ELECTRICAL ENGINEERS TO EVALUATE THE PERFORMANCE OF WOLFSPEED POWER SWITCHING DEVICES. THE BOARD SHOULD NOT BE USED AS ALL OR PART OF A FINISHED PRODUCT. THIS BOARD IS NOT SUITABLE FOR SALE TO OR USE BY CONSUMERS AND CAN BE HIGHLY DANGEROUS IF NOT USED PROPERLY. THIS BOARD IS NOT DESIGNED OR INTENDED TO BE INCORPORATED INTO ANY OTHER PRODUCT FOR RESALE. THE USER SHOULD CAREFULLY REVIEW THE DOCUMENT TO WHICH THESE NOTIFICATIONS ARE ATTACHED AND OTHER WRITTEN USER DOCUMENTATION THAT MAY BE PROVIDED BY WOLFSPEED (TOGETHER, THE "DOCUMENTATION") PRIOR TO USE. USE OF THIS BOARD IS AT THE USER'S SOLE RISK.

OPERATION OF BOARD

It is important to operate the board within Wolfspeed's recommendations and environmental considerations as described in the Documentation. Exceeding specified ratings (such as input and output voltage, current, power, or environmental ranges) may cause property damage. If you have questions about these ratings, please contact Wolfspeed prior to connecting interface electronics (including input power and intended loads). Any

loads applied outside of a specified output range may result in adverse consequences, including unintended or inaccurate evaluations or possible permanent damage to the board or its interfaced electronics. Please consult the Documentation prior to connecting any load to the board. If you have any questions about load specifications for the board, please contact Wolfspeed at forum.wolfspeed.com for assistance (and please rely only on forum responses from responders identified as Wolfspeed employees).

Users should ensure that appropriate safety procedures are followed when working with the board as serious injury, including death by electrocution or serious injury by electrical shock or electrical burns can occur if you do not follow proper safety precautions. It is not necessary in proper operation for the user to touch the board while it is energized. When devices are being attached to the board for testing, the board must be disconnected from the electrical source and any bulk capacitors must be fully discharged. When the board is connected to an electrical source and for a short time thereafter until board components are fully discharged, some board components will be electrically charged and/or have temperatures greater than 50 ˚ Celsius. These components may include bulk capacitors, connectors, linear regulators, switching transistors, heatsinks, resistors and SiC diodes that can be identified using a board schematic. Users should contact Wolfspeed for assistance if a board schematic is not included in the Documentation or if users have questions about a board's components. When operating the board, users should be aware that these components will be hot and could electrocute or electrically shock the user. As with all electronic evaluation tools, only qualified personnel knowledgeable in handling electronic performance evaluation, measurement, and diagnostic tools should use the board.

USER RESPONSIBILITY FOR SAFE HANDLING AND COMPLIANCE WITH LAWS

Users should read the Documentation and, specifically, the various hazard descriptions and warnings contained in the Documentation, prior to handling the board. The Documentation contains important safety information about voltages and temperatures.

Users assume all responsibility and liability for the proper and safe handling of the board. Users are responsible for complying with all safety laws, rules, and regulations related to the use of the board. Users are responsible for (1) establishing protections and safeguards to ensure that a user's use of the board will not result in any property damage, injury, or death, even if the board should fail to perform as described, intended, or expected, and (2) ensuring the safety of any activities to be conducted by the user or the user's employees, affiliates, contractors, representatives, agents, or designees in the use of the board. User questions regarding the safe usage of the board should be directed to Wolfspeed at forum.wolfspeed.com (but please rely only on forum responses from responders identified as Wolfspeed employees).

In addition, users are responsible for:

- compliance with all international, national, state, and local laws, rules, and regulations that apply to the handling or use of the board by a user or the user's employees, affiliates, contractors, representatives, agents, or designees.
- taking necessary measures, at the user's expense, to correct radio interference if operation of the board causes interference with radio communications. The board may generate, use, and/or radiate radio frequency energy, but it has not been tested for compliance within the limits of computing devices pursuant to Federal Communications Commission or Industry Canada rules, which are designed to provide protection against radio frequency interference.

● compliance with applicable regulatory or safety compliance or certification standards that may normally be associated with other products, such as those established by EU Directive 2011/65/EU of the European Parliament and of the Council on 8 June 2011 about the Restriction of Use of Hazardous Substances (or the RoHS 2 Directive) and EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (or WEEE). The board is not a finished end product and therefore may not meet such standards. Users are also responsible for properly disposing of a board's components and materials.

NO WARRANTY

THE BOARD IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, INCLUDING BUT NOT LIMITED TO ANY WARRANTY OF NON-INFRINGEMENT, MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE, WHETHER EXPRESS OR IMPLIED. THERE IS NO REPRESENTATION THAT OPERATION OF THIS BOARD WILL BE UNINTERRUPTED OR ERROR FREE.

LIMITATION OF LIABILITY

IN NO EVENT SHALL WOLFSPEED BE LIABLE FOR ANY DAMAGES OF ANY KIND ARISING FROM USE OF THE BOARD. WOLFSPEED'S AGGREGATE LIABILITY IN DAMAGES OR OTHERWISE SHALL IN NO EVENT EXCEED THE AMOUNT, IF ANY, RECEIVED BY WOLFSPEED IN EXCHANGE FOR THE BOARD. IN NO EVENT SHALL WOLFSPEED BE LIABLE FOR INCIDENTAL, CONSEQUENTIAL, OR SPECIAL LOSS OR DAMAGES OF ANY KIND, HOWEVER CAUSED, OR ANY PUNITIVE, EXEMPLARY, OR OTHER DAMAGES. NO ACTION, REGARDLESS OF FORM, ARISING OUT OF OR IN ANY WAY CONNECTED WITH ANY BOARD FURNISHED BY WOLFSPEED MAY BE BROUGHT AGAINST WOLFSPEED MORE THAN ONE (1) YEAR AFTER THE CAUSE OF ACTION ACCRUED.

INDEMNIFICATION

The board is not a standard consumer or commercial product. As a result, any indemnification obligations imposed upon Wolfspeed by contract with respect to product safety, product liability, or intellectual property infringement do not apply to the board.