E4MS045075U2

Automotive Silicon Carbide Power MOSFET

Features

- Industry compatible drive voltage 15 V ...18 V/-4 V ...0 V
- Low $R_{DS(on)}$ at high operating temperatures
- Improved device capacitance ratio (C_{iss}/C_{rss})
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

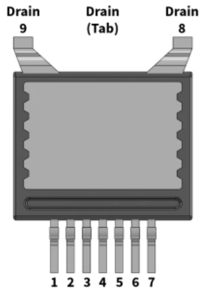
Benefits

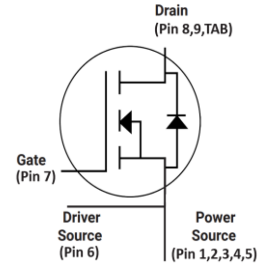
- Higher efficiency with lower switching losses and EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system level cooling requirements

Typical Applications

- Onboard charger
- High voltage DC/DC converters
- HVAC compressors
- Battery management systems

Package





Orderable Part Number	Package Type	Marking
E4MS045075U2-TR	U2 (TSC)	E4MS045075U2

Absolute Maximum Ratings

Stress beyond those listed under absolute maximum ratings may damage the device.

Symbol	Parameter	Min.	Max.	Unit	Conditions	Note
$V_{DS(max)}$	Drain-Source Voltage		750	V		
$V_{GS(max)}$	Maximum Gate – Source Voltage (Transient)	-10	+23	V		Note 1
I_D	DC Continuous Drain Current		47	A	V_{GS} = 18 V, T_c = 25 °C, $T_J \le$ 175 °C	Note 2
			33	A	V_{GS} = 18 V, T_c = 100 °C, $T_J \le$ 175 °C	Note 2
I_{DM}	Pulsed Drain Current		102	A	V_{GS} = 18 V, T_c = 25 °C, t_{Pmax} limited by T_{jmax}	
P_D	Power Dissipation		156	W	T_c = 25 °C, T_J = 175 °C	Note 3
T_J, T_{stg}	Operating Junction and Storage Temperature	-55	+175	°C		
T_L	Solder Temperature		260	°C	According to JEDEC J-STD-020	

Note (1): Refer to AN PRD-09634
Note (2): Current limit calculated by $I_{D(max)} = \sqrt{(P_D/R_{DS(typ)}/(T_{J(max)}, I_{D(max)}))}$
Note (3): $P_D = (T_J - T_C) / R_{th(JC,Max)}$

Electrical Characteristics (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain – Source Breakdown Voltage	750			V	V_{GS} = 0 V, I_D =100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	3.9	V	V_{DS} = V_{GS}, I_D = 4 mA	Fig. 11, Note 1
			2.0		V	V_{DS} = V_{GS}, I_D = 4 mA, T_J = 175 °C	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	µA	V_{DS} = 750 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 18 V, V_{DS} = 0 V	
$V_{GS(op)}$	Recommended Turn on Gate-Source Voltage		+15…+18		V		Note 4
	Recommended Turn off Gate-Source Voltage		-4…0				
$R_{DS(on)}$	Drain-Source On-State Resistance		45	58.5	mΩ	V_{GS} = 18 V, I_D = 14.5 A	Fig. 4, 5, 6
			66.2			V_{GS} = 18 V, I_D = 14.5 A, T_J = 175 °C	
			54.9			V_{GS} = 15 V, I_D = 14.5 A	
g_{fs}	Transconductance		10.2		S	V_{DS} = 20 V, I_D = 14.5 A	Fig. 7
			10			V_{DS} = 20 V, I_D = 14.5 A, T_J = 175 °C	
$R_{DS(on)Tempco}$	On Resistance Temperature Coefficient		1.47			V_{GS} = 18 V, I_D = 14.5 A	Note 5
C_{iss}	Input Capacitance		1201		pF	V_{GS} = 0 V, V_{DS} = 500 V f = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		77				
C_{rss}	Reverse Transfer Capacitance		2.8				
C_{iss}/C_{rss}	Capacitance Ratio		430				Note 6
E_{oss}	C_{OSS} Stored Energy		12.2		µJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		97		pF	V_{GS} = 0 V, V_{DS} = 0 V … 500 V	Note 7
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		151				
E_{on}	Turn-On Switching Energy (Body Diode FWD) T_j = 25 °C T_j = 175 °C		51 51		µJ	V_{DS} = 500 V, V_{GS} = -4 V / 18 V, I_D = 14.5 A, $R_{G(ext)}$ = 2 Ω, $L_σ$ = 25 nH	Fig. 25, 27, 29
E_{off}	Turn-Off Switching Energy (Body Diode FWD) T_j = 25 °C T_j = 175 °C		10 10				Fig. 25, 28, 29
$t_{d(on)}$	Turn-On Delay Time		9.1		ns	V_{DS} = 500 V, V_{GS} =-4 V / 18 V, I_D = 14.5 A, $R_{G(ext)}$ = 2 Ω, $L_σ$ = 25 nH Timing relative to I_{DS} Inductive load	Fig. 26, 27, 29
t_r	Rise Time		2.5				
$t_{d(off)}$	Turn-Off Delay Time		18.5				Fig. 26, 28, 29
t_f	Fall Time		8.5				
$R_{G(int)}$	Internal Gate Resistance		2.3		Ω	f = 1 MHz	
Q_{gs}	Gate to Source Charge		14		nC	V_{DS} = 500 V, V_{GS} = -4 V/ 18 V I_D = 14.5 A	Fig. 12
Q_{gd}	Gate to Drain Charge		13.5				
Q_g	Total Gate Charge		48.6				

Note (4): Refer to AN PRD-08999.
Note (5): $R_{DS(on)Tempco}$ refers to $R_{DS(on)}$ at 175 °C / $R_{DS(on)}$ at 25 °C. This is a E4MS 750 V product family value.
Note (6): Capacitance ratio is a FOM for partial turn-on immunity AN PRD-06933. This is a E4MS 750 V product family value.
Note (7): $C_{o(er)}$, a lumped capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to 500 V.
$C_{o(tr)}$, a lumped capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to 500 V.

Reverse Diode Characteristics (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	V_{GS} = -4 V, I_{SD} = 7.25 A, T_J = 25 °C	Fig. 8, 9, 10
		4.5			V_{GS} = -4 V, I_{SD} = 7.25 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		24	A	V_{GS} = -4 V, T_C = 25 °C	
I_{SM}	Diode Pulse Current		102		V_{GS} = -4 V, pulse width t_p limited by T_{jmax}	
t_{rr}	Reverse Recovery Time	7.3		ns	V_{GS} = -4 V, I_{SD} = 14.5 A, V_R = 500 V, di_f/dt = 9147 A/µs, $R_{G(ext)}$ = 2 Ω, L_σ = 25 nH	Fig. 30
Q_{rr}	Reverse Recovery Charge	171		nC		
I_{RRM}	Peak Reverse Recovery Current	38		A		
E_{RR}	Reverse Recovery Energy T_j = 25 °C T_j = 175 °C	 71.3 62		µJ		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.74	0.96	°C/W		

Typical Performance

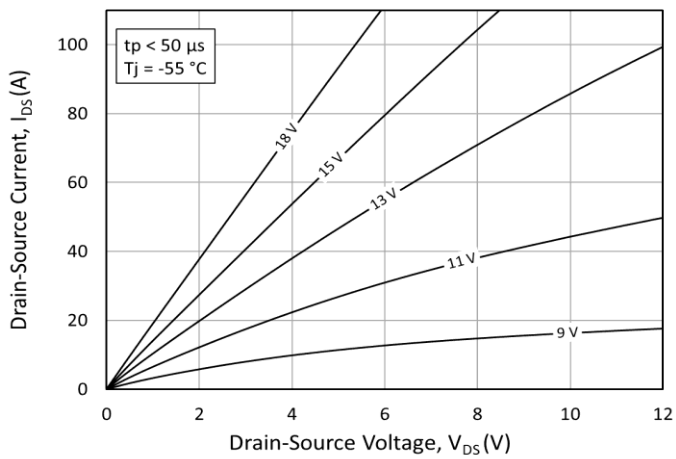


Figure 1. Output Characteristics T_{VJ} = -55 °C

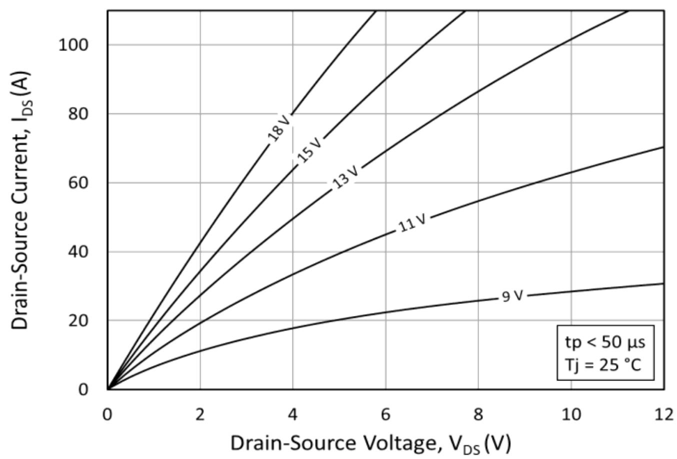


Figure 2. Output Characteristics T_{VJ} = 25 °C

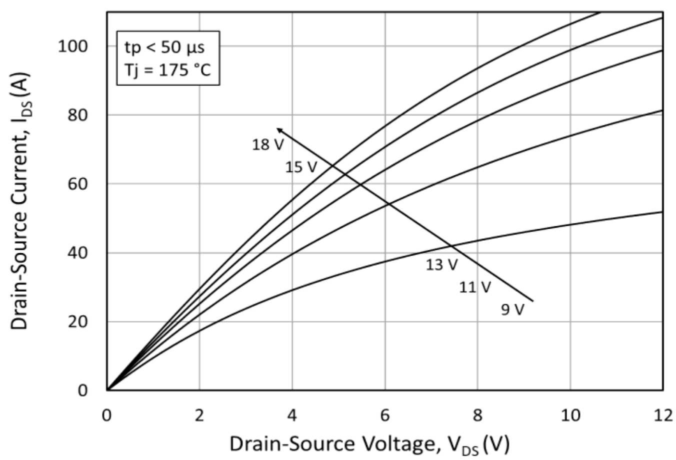


Figure 3. Output Characteristics T_{VJ} = 175 °C

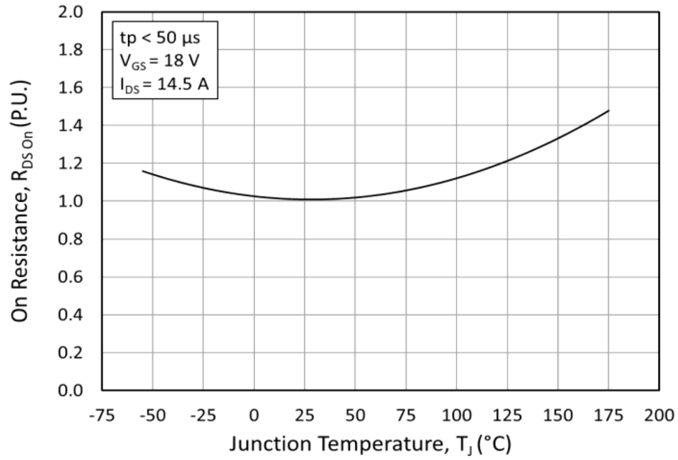


Figure 4. Normalized On-Resistance vs. Temperature

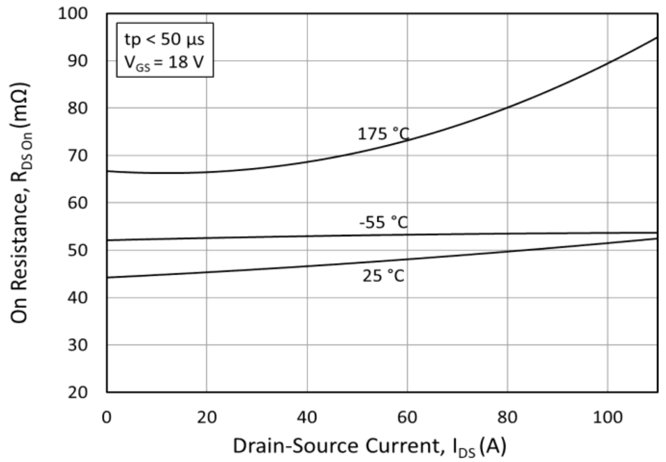


Figure 5. On-Resistance vs. Drain Current for Various Temperatures

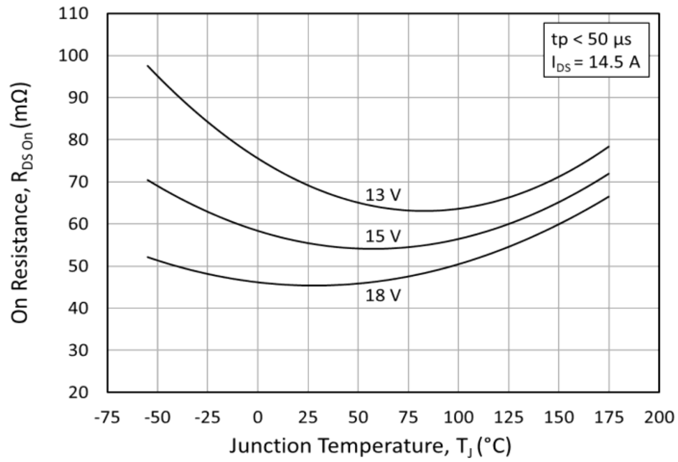


Figure 6. On-Resistance vs. Temperature for Various Gate Voltages

Typical Performance

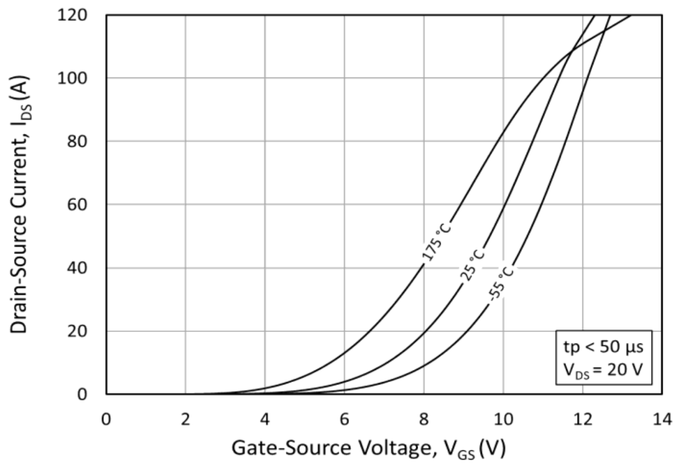


Figure 7. Transfer Characteristic for Various Junction Temperatures

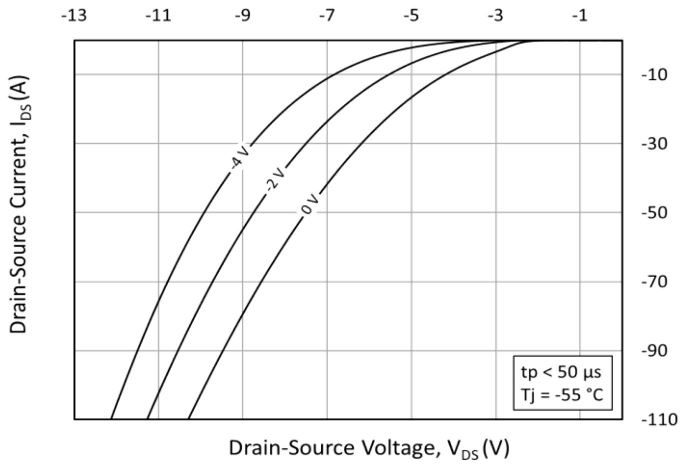


Figure 8. Body Diode Characteristic at T_{VJ} = -55 °C

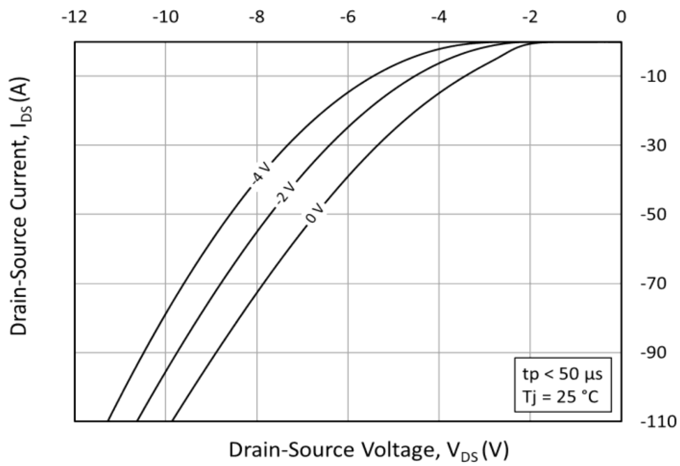


Figure 9. Body Diode Characteristic at T_{VJ} = 25 °C

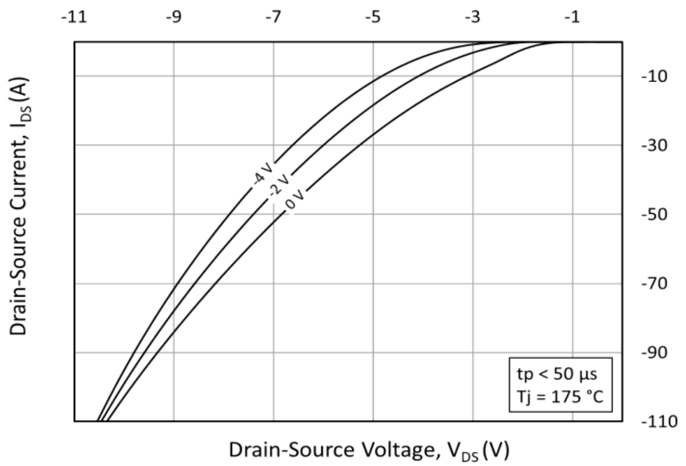


Figure 10. Body Diode Characteristic at T_{VJ} = 175 °C

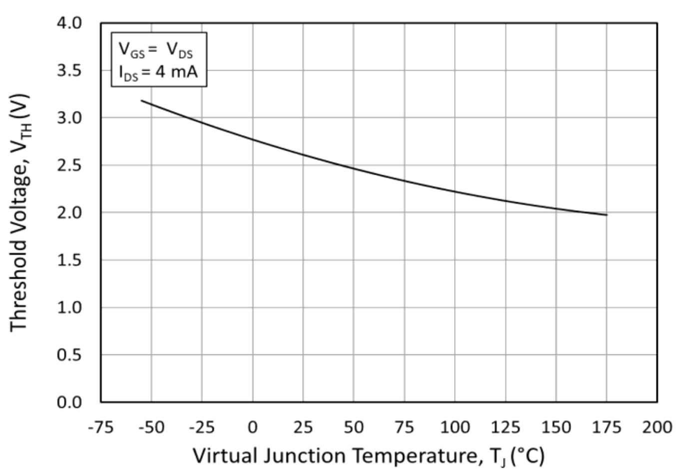


Figure 11. Threshold Voltage vs. Temperature

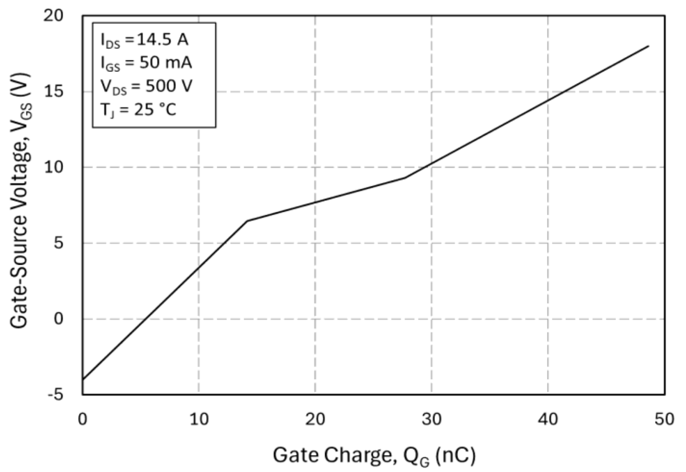


Figure 12. Gate Charge Characteristics

Typical Performance

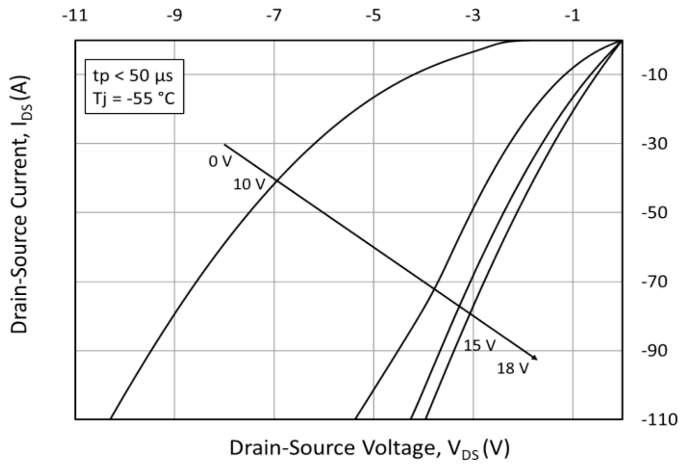


Figure 13. 3rd Quadrant Characteristic at T_{VJ} = -55 °C

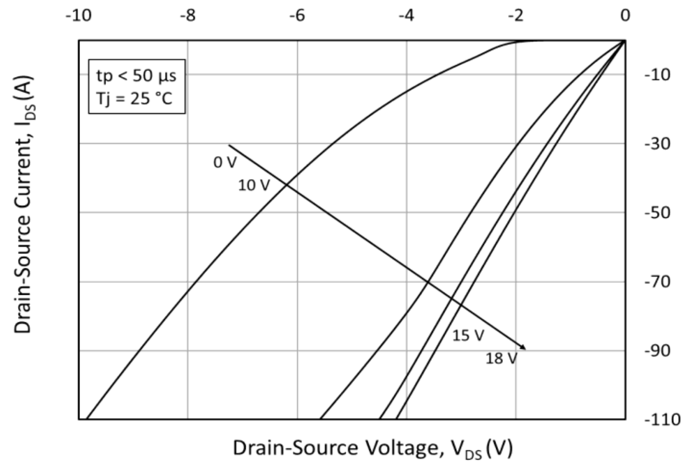


Figure 14. 3rd Quadrant Characteristic at T_{VJ} = 25 °C

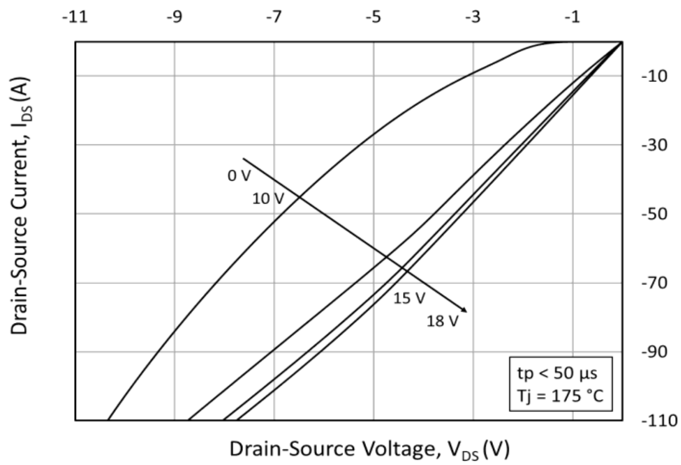


Figure 15. 3rd Quadrant Characteristic at T_{VJ} = 175 °C

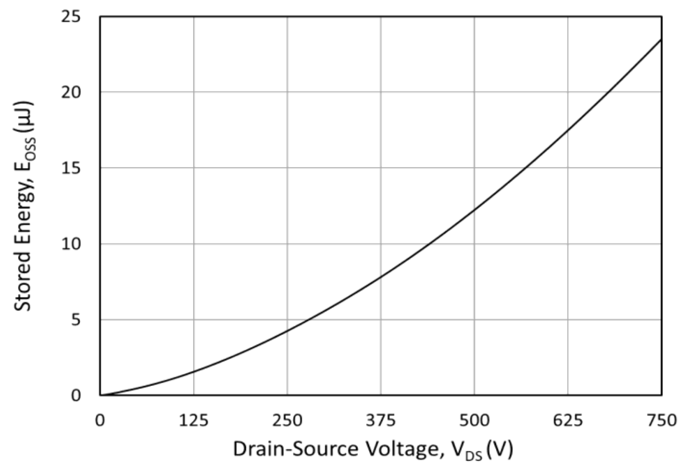


Figure 16. Output Capacitor Stored Energy

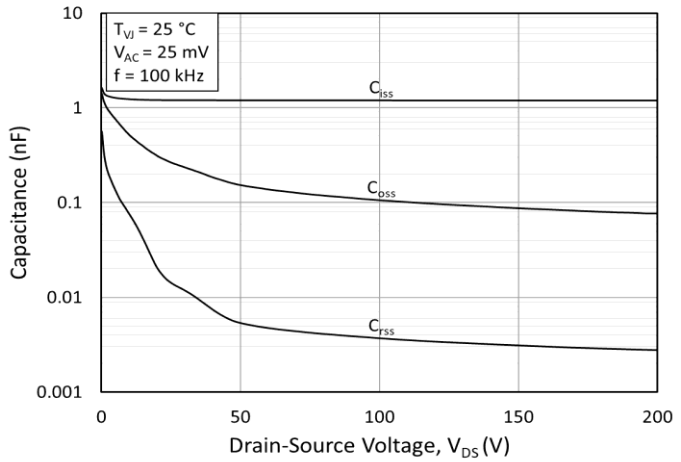


Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

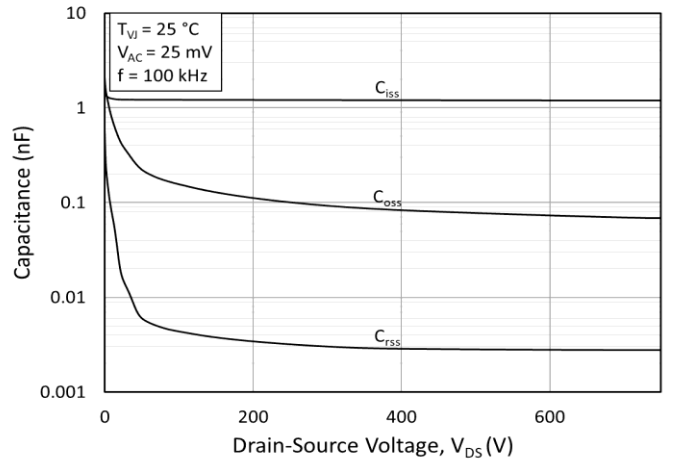


Figure 18. Capacitances vs. Drain-Source Voltage (0-750 V)

Typical Performance

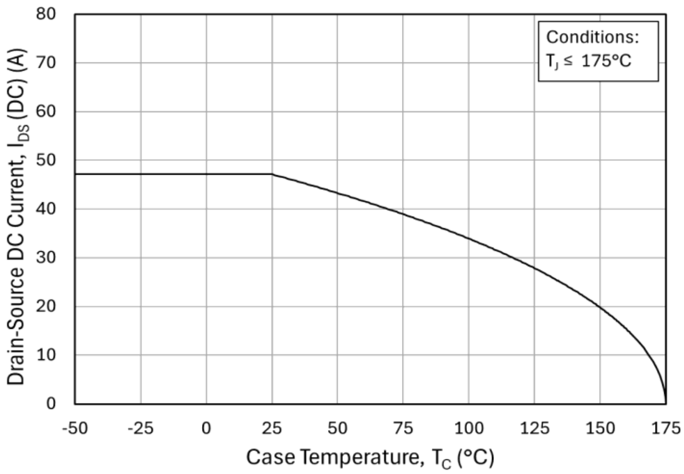


Figure 19. Continuous Drain Current Derating vs. Case Temperature

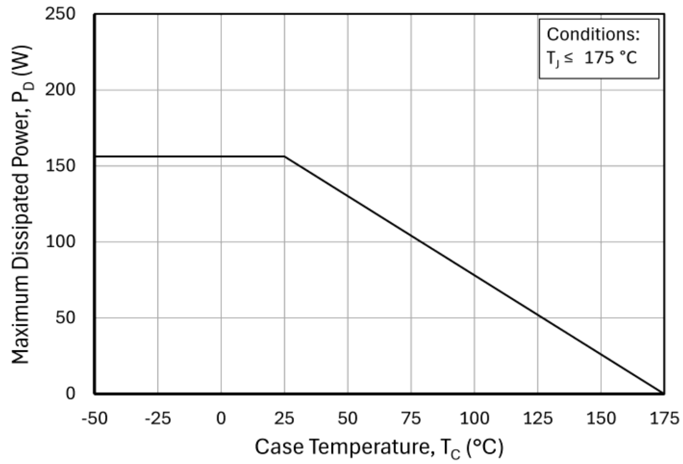


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

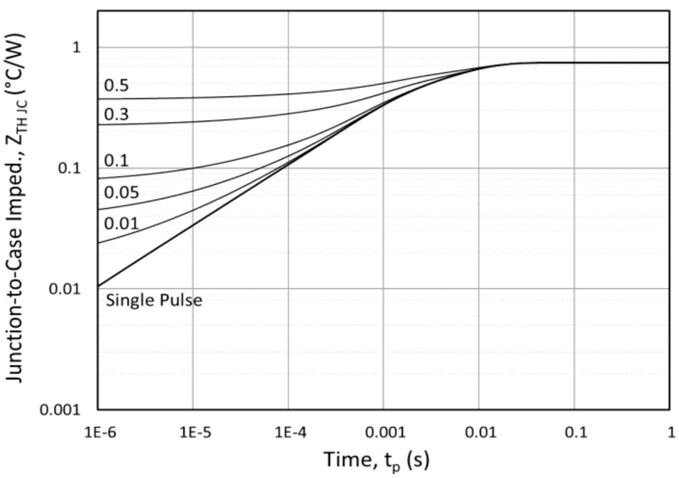


Figure 21. Transient Thermal Impedance (Junction - Case) °C

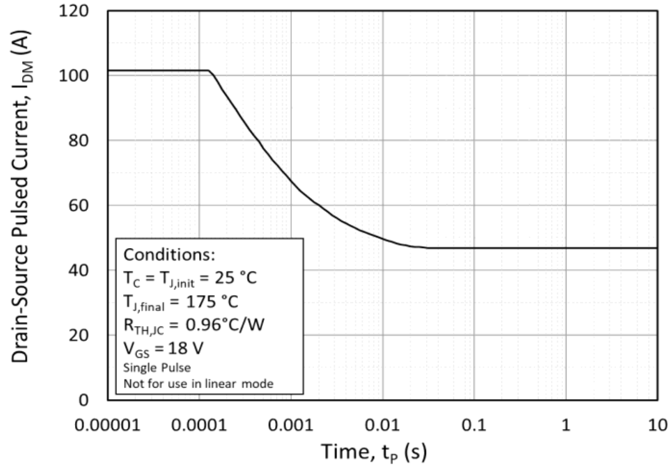


Figure 22. Safe Operating Area

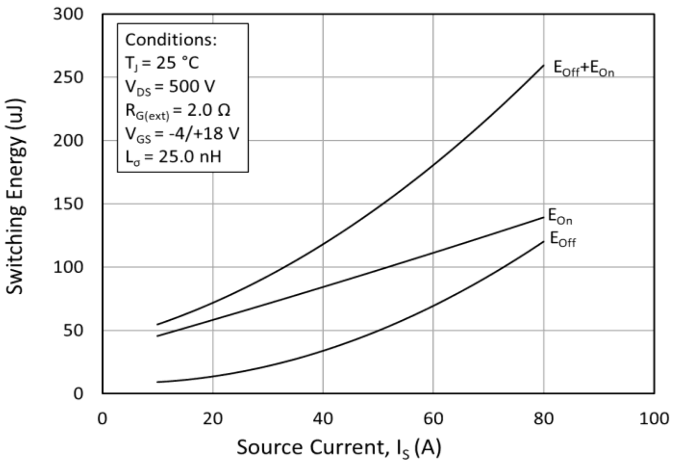


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 500 V)

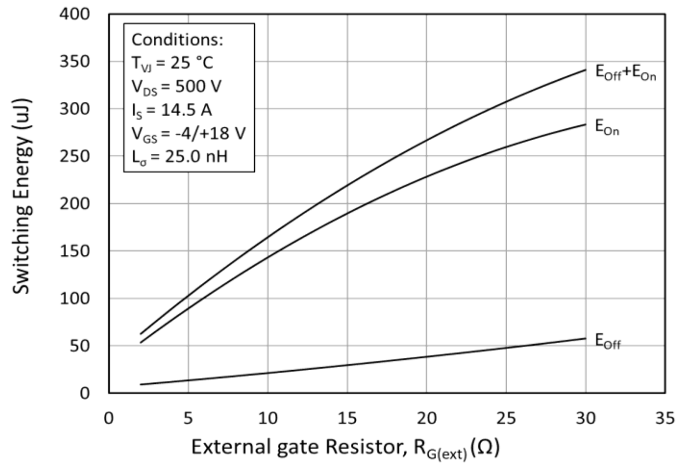


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

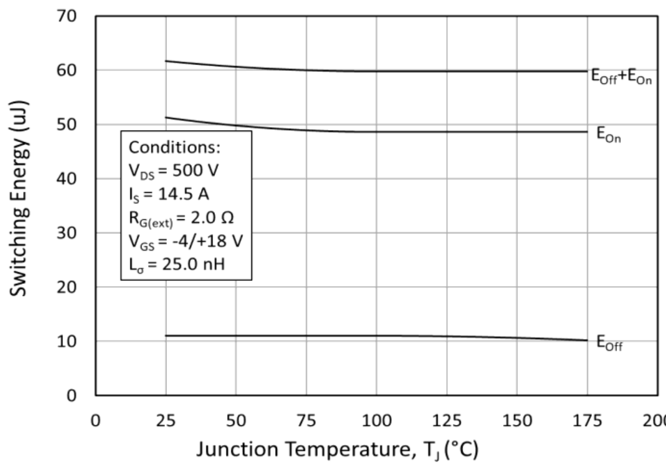


Figure 25. Clamped Inductive Switching Energy vs. Temperature

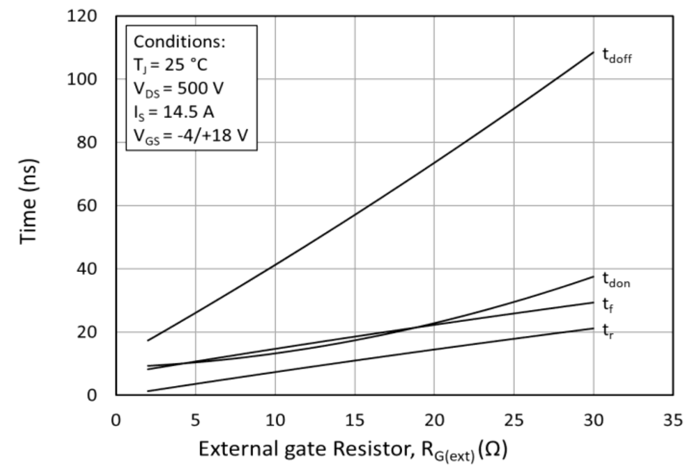


Figure 26. Switching Times vs. $R_{G(ext)}$

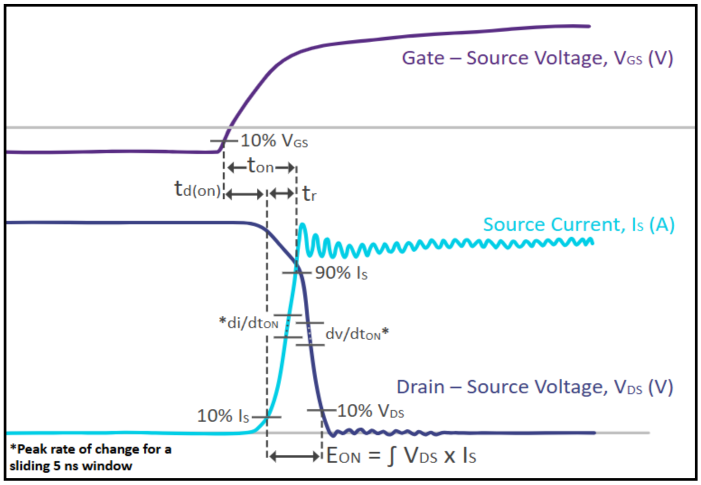


Figure 27. Turn On Switching Time Definition

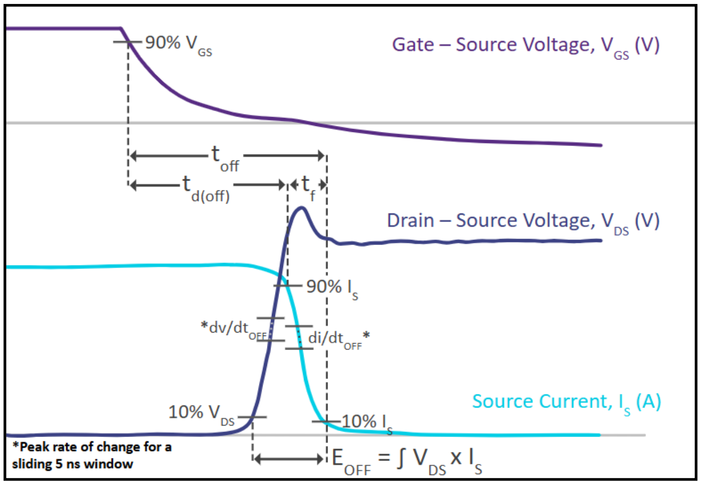


Figure 28. Turn Off Switching Time Definition

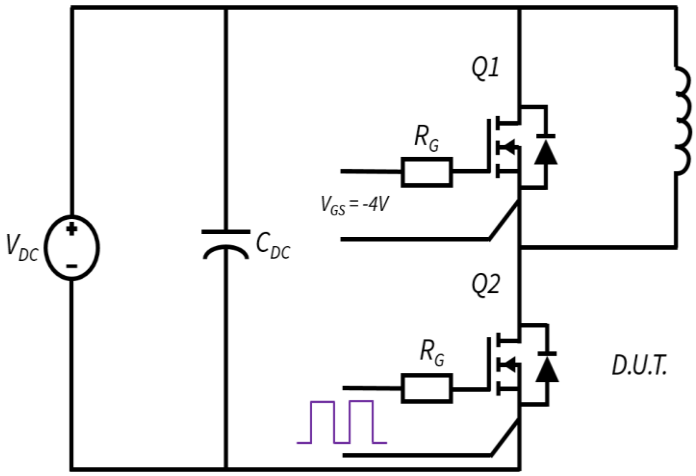


Figure 29. Clamped Inductive MOSFET Switching Waveform Test Circuit

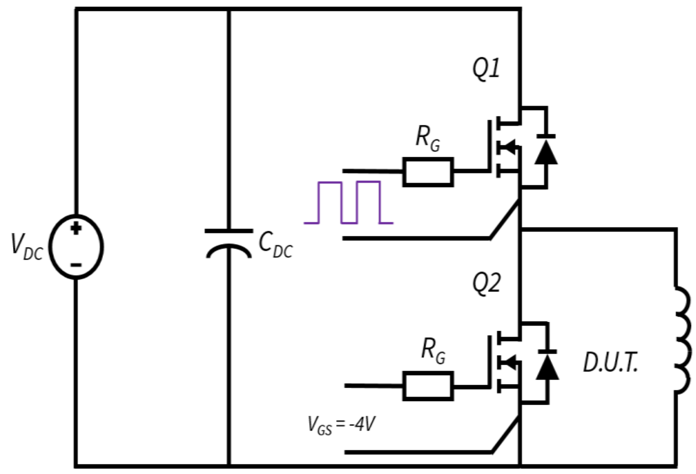
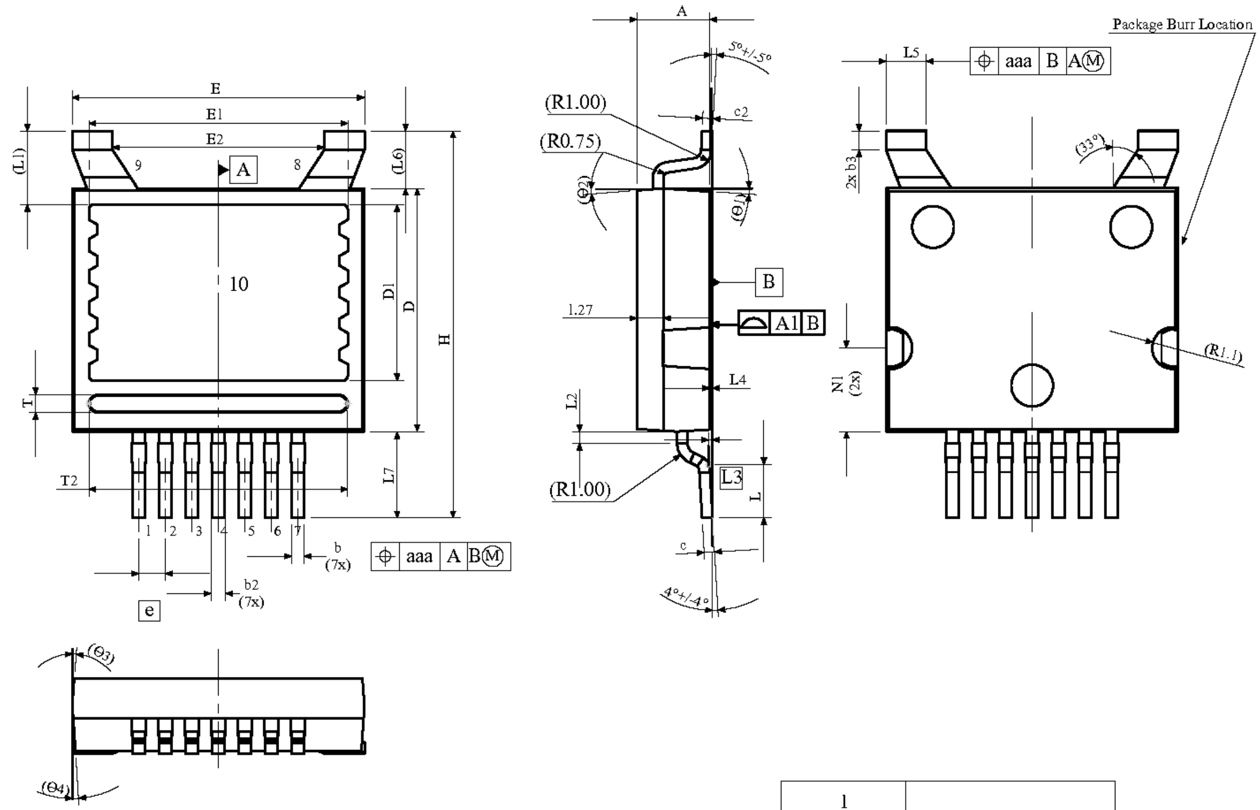


Figure 30. Clamped Inductive Body Diode Switching Waveform Test Circuit

Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	3.40	3.60
A1	---	0.05
b	0.50	0.70
b2	0.50	1.00
b3	0.85	1.05
c	0.40	0.60
c2	0.40	0.60
D	11.55	11.75
D1	8.30	8.50
E	13.92	14.12
E1	12.22	12.42
E2	9.92	10.22
e	BSC 1.27	
H	18.00	19.00
L	2.47	2.67
L1	BSC 3.51	
L2	0.3	0.73
L3	BSC 0.26	
L4	0.09	0.2
L5	1.83	2.13
L6	BSC 2.75	
L7	4.03	4.23
T	0.75	0.95
T2	12.30	12.50
N1	3.90	4.10
Θ1	0°	8°
Θ2	0°	8°
Θ3	0°	8°
Θ4	0°	8°
aaa	---	0.10

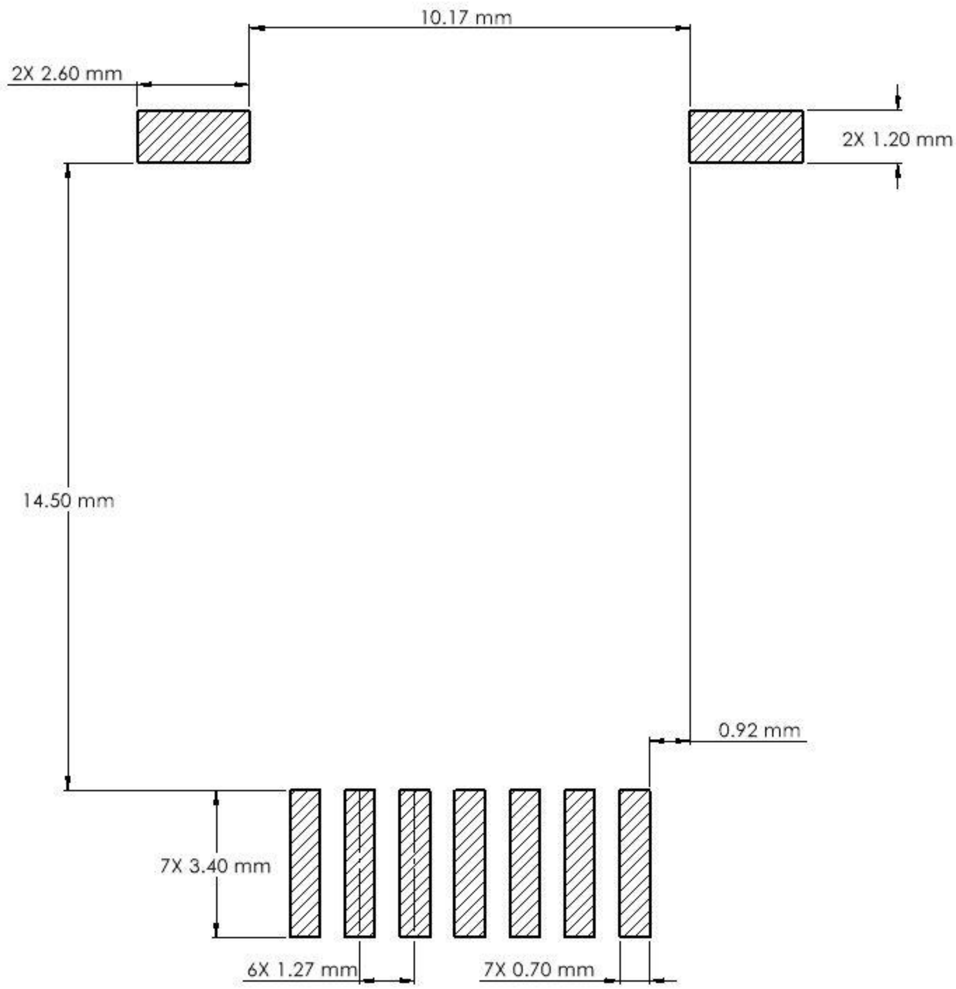
1	SOURCE
2	
3	
4	
5	
6	DRIVER SOURCE
7	GATE
8	DRAIN
9	DRAIN
10	DRAIN

NOTE

1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Recommended Solder Pad Layout

All dimensions in mm



Revision History

Documents Version	Date of Change	Description of Changes
1	June 2026	Initial Release

Appendix

Appendix Number	Description
A1	The following are recommendations for turning off the MOSFET with 0 V: • Measure the V_{GS} spike accurately using high-CMRR probes and low common mode noise measurements. • For the safe operation of the device, the voltage spike shall remain < 5 V for a time duration of < 40 ns.

Notes & Disclaimers

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REACh Compliance

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

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