E4MS025120QT

Automotive Silicon Carbide Power MOSFET

Features

- Industry compatible drive voltage 15 V …18 V/-4 V …0 V
- Low $R_{DS(on)}$ at high operating temperatures
- Improved device capacitance ratio (C_{iss}/C_{rss})
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

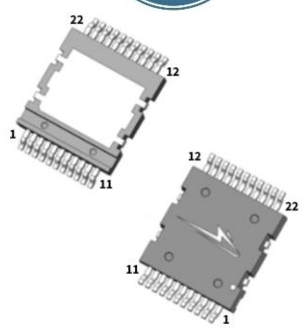
Benefits

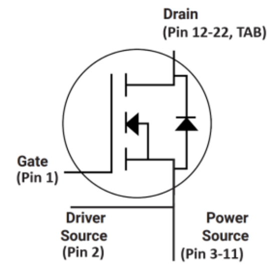
- Higher efficiency with lower switching losses and EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system level cooling requirements

Typical Applications

- Onboard charger
- High voltage DC/DC converters
- HVAC compressors
- Battery management systems

Package





Orderable Part Number	Package Type	Marking
E4MS025120QT-TR	Q-TSC	E4MS025120QT

Absolute Maximum Ratings

Stress beyond those listed under absolute maximum ratings may damage the device.

Symbol	Parameter	Min.	Max.	Unit	Conditions	Note
$V_{DS(max)}$	Drain-Source Voltage		1200	V		
$V_{GS(max)}$	Maximum Gate – Source Voltage (Transient)	-10	+23	V		Note 1
I_D	DC Continuous Drain Current		88	A	V_{GS} = 18 V, T_c = 25 °C, $T_J \leq$ 175 °C	Note 2
			63	A	V_{GS} = 18 V, T_c = 100 °C, $T_J \leq$ 175 °C	
I_{DM}	Pulsed Drain Current		274	A	V_{GS} = 18 V, T_c = 25 °C, t_{Pmax} limited by T_{jmax}	
P_D	Power Dissipation		375	W	T_c = 25 °C, T_J = 175 °C	Note 3
T_J, T_{stg}	Operating Junction and Storage Temperature	-55	+175	°C		
T_L	Solder Temperature		260	°C	According to JEDEC J-STD-020	

Note (1): Refer to AN PRD-09634
Note (2): Current limit calculated by $I_{D(max)} = \sqrt{(P_D/R_{DS(typ)}/(T_{J(max)}, I_{D(max)}))}$
Note (3): $P_D = (T_J - T_C) / R_{th(JC,Max)}$

Electrical Characteristics (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain – Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D =100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	3.9	V	V_{DS} = V_{GS}, I_D = 10.8 mA	Fig. 11, Note 1
			2.0		V	V_{DS} = V_{GS}, I_D = 10.8 mA, T_J = 175 °C	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	µA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 18 V, V_{DS} = 0 V	
$V_{GS(op)}$	Recommended Turn on Gate-Source Voltage		+15…+18		V		Note 4
	Recommended Turn off Gate-Source Voltage		-4…0				
$R_{DS(on)}$	Drain-Source On-State Resistance		25	33	mΩ	V_{GS} = 18 V, I_D = 39.2 A	Fig. 4, 5, 6
			47			V_{GS} = 18 V, I_D = 39.2 A, T_J = 175 °C	
			28			V_{GS} = 15 V, I_D = 39.2 A	
g_{fs}	Transconductance		28		S	V_{DS} = 20 V, I_D = 39.2 A	Fig. 7
			27			V_{DS} = 20 V, I_D = 39.2 A, T_J = 175 °C	
$R_{DS(on)Tempco}$	On Resistance Temperature Coefficient		1.88			V_{GS} = 18 V, I_D = 39.2 A	Note 5
C_{iss}	Input Capacitance		3087		pF	V_{GS} = 0 V, V_{DS} = 1000 V f = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		103				
C_{rss}	Reverse Transfer Capacitance		4.7				
C_{iss}/C_{rss}	Capacitance Ratio		630				Note 6
E_{oss}	C_{OSS} Stored Energy		63		µJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		145		pF	V_{GS} = 0 V, V_{DS} = 0 V … 800 V	Note 7
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		238				
E_{on}	Turn-On Switching Energy (Body Diode FWD) T_j = 25 °C T_j = 175 °C		 394 470		µJ	V_{DS} = 800 V, V_{GS} = -4 V / 18 V, I_D = 39.2 A, $R_{G(ext)}$ = 1 Ω, L_σ = 25 nH	Fig. 25, 27, 29
E_{off}	Turn-Off Switching Energy (Body Diode FWD) T_j = 25 °C T_j = 175 °C		 57 64				Fig. 25, 28, 29
$t_{d(on)}$	Turn-On Delay Time		12		ns	V_{DS} = 800 V, V_{GS} =-4 V / 18 V, I_D = 39.2 A, $R_{G(ext)}$ = 1 Ω, L_σ = 25 nH Timing relative to I_{DS} Inductive load	Fig. 26, 27, 29
t_r	Rise Time		4				
$t_{d(off)}$	Turn-Off Delay Time		36				Fig. 26, 28, 29
t_f	Fall Time		11				
$R_{G(int)}$	Internal Gate Resistance		2.6		Ω	f = 1 MHz	
Q_{gs}	Gate to Source Charge		35		nC	V_{DS} = 800 V, V_{GS} = -4 V/ 18 V I_D = 39.2 A	Fig. 12
Q_{gd}	Gate to Drain Charge		30				
Q_g	Total Gate Charge		125				

Note (4): Refer to AN PRD-08999.
Note (5): $R_{DS(on)Tempco}$ refers to $R_{DS(on)}$ at 175 °C / $R_{DS(on)}$ at 25 °C. This is a E4MS 1200 V product family value.
Note (6): Capacitance ratio is a FOM for partial turn-on immunity AN PRD-06933. This is a E4MS 1200 V product family value.
Note (7): $C_{o(er)}$, a lumped capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to 800 V.
$C_{o(tr)}$, a lumped capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to 800 V.

Reverse Diode Characteristics (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	V_{GS} = -4 V, I_{SD} = 19.6 A, T_J = 25 °C	Fig. 8, 9, 10
		4.6			V_{GS} = -4 V, I_{SD} = 19.6 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		60	A	V_{GS} = -4 V, T_C = 25 °C	
I_{SM}	Diode Pulse Current		274		V_{GS} = -4 V, pulse width t_p limited by T_{jmax}	
t_{rr}	Reverse Recovery Time	14		ns	V_{GS} = -4 V, I_{SD} = 39.2 A, V_R = 800 V, di_f/dt = 15810 A/µs, $R_{G(ext)}$ = 1 Ω, L_σ = 25 nH	Fig. 30
Q_{rr}	Reverse Recovery Charge	742		nC		
I_{RRM}	Peak Reverse Recovery Current	94		A		
E_{RR}	Reverse Recovery Energy T_j = 25 °C T_j = 175 °C	 102 256		µJ		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.31	0.40	°C/W		

Typical Performance

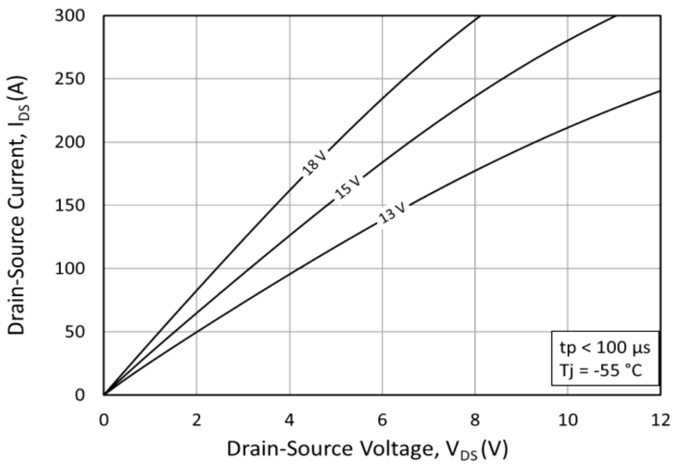


Figure 1. Output Characteristics T_{VJ} = -55 °C

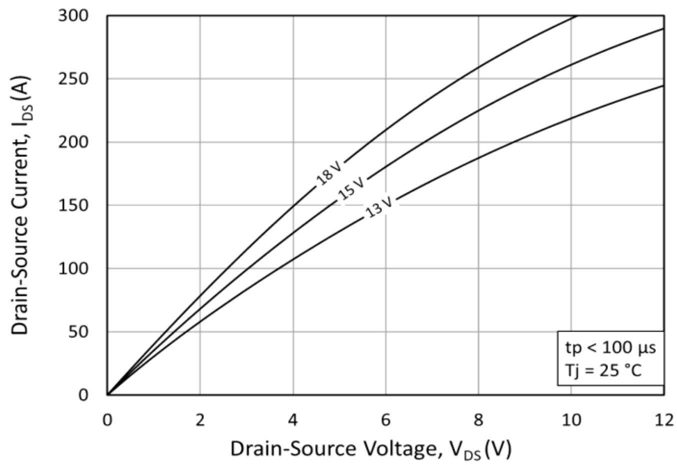


Figure 2. Output Characteristics T_{VJ} = 25 °C

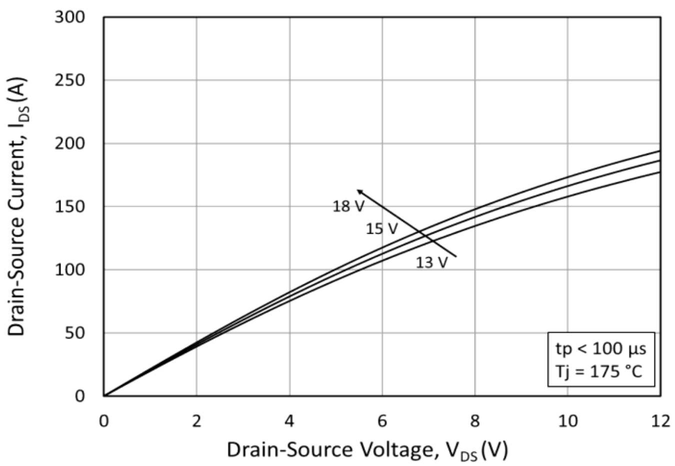


Figure 3. Output Characteristics T_{VJ} = 175 °C

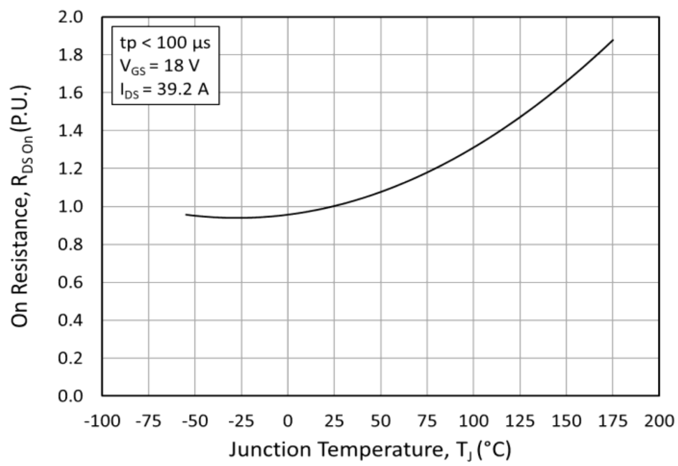


Figure 4. Normalized On-Resistance vs. Temperature

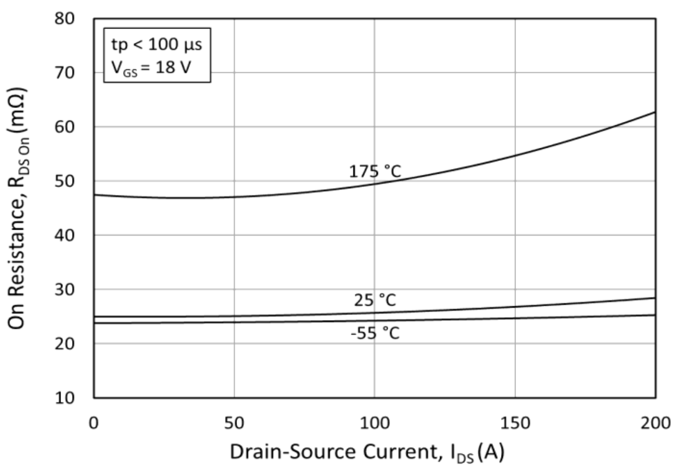


Figure 5. On-Resistance vs. Drain Current for Various Temperatures

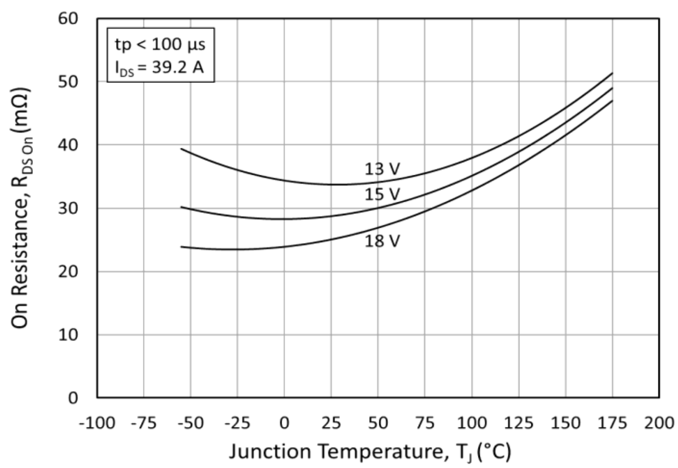


Figure 6. On-Resistance vs. Temperature for Various Gate Voltages

Typical Performance

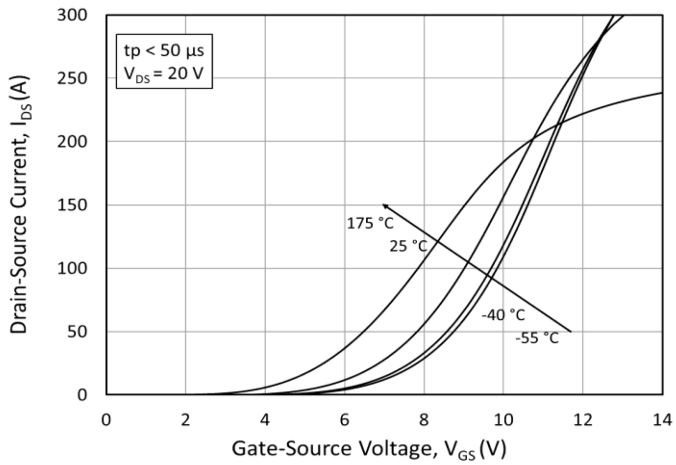


Figure 7. Transfer Characteristic for Various Junction Temperatures

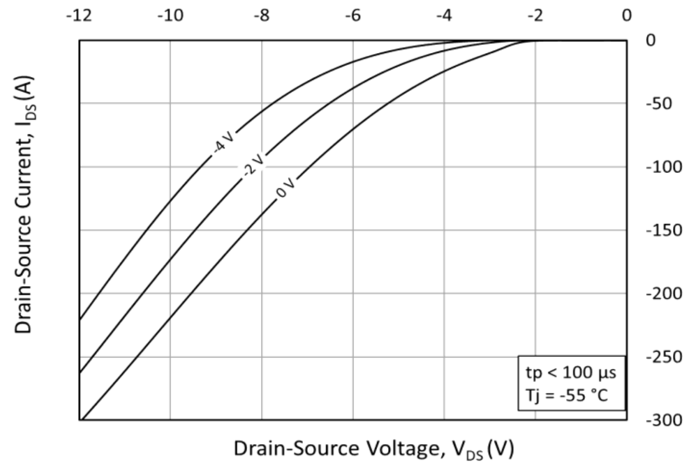


Figure 8. Body Diode Characteristic at T_{VJ} = -55 °C

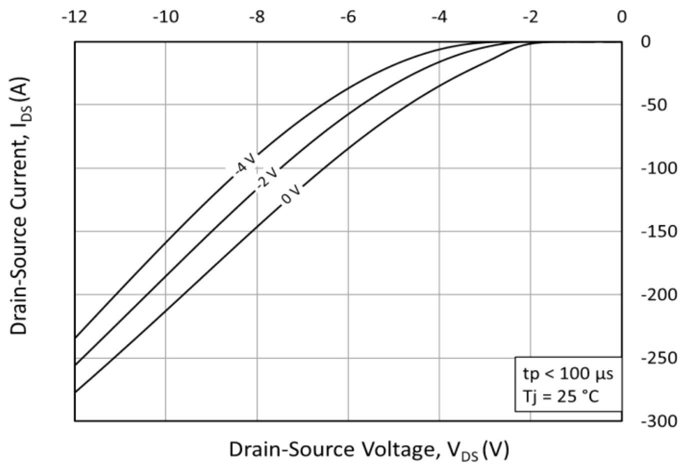


Figure 9. Body Diode Characteristic at T_{VJ} = 25 °C

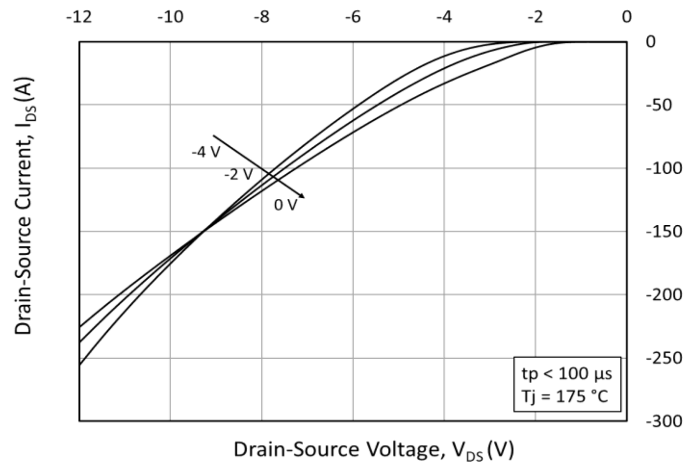


Figure 10. Body Diode Characteristic at T_{VJ} = 175 °C

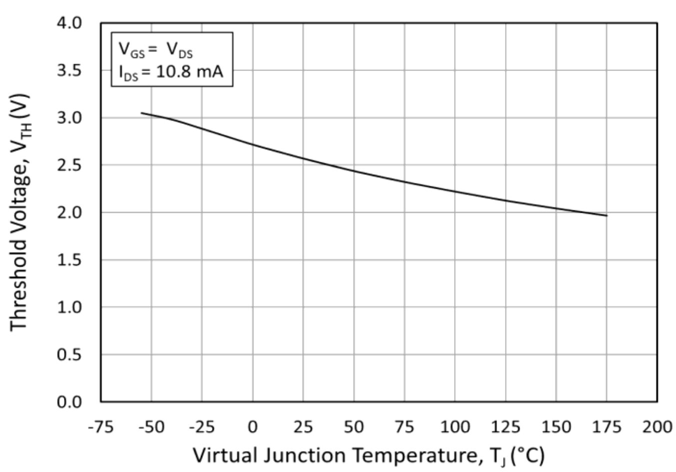


Figure 11. Threshold Voltage vs. Temperature

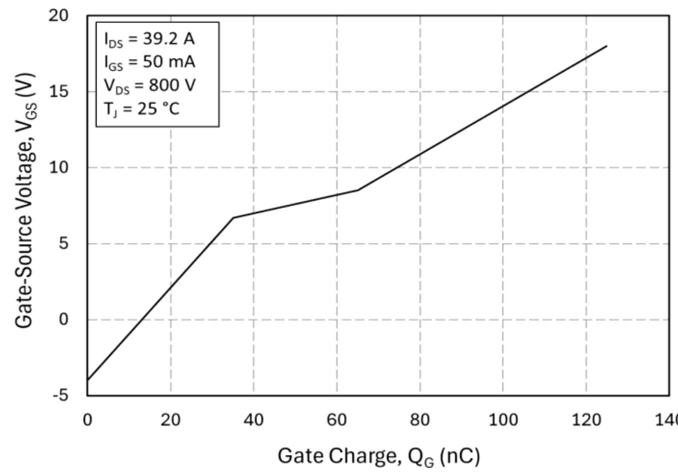


Figure 12. Gate Charge Characteristics

Typical Performance

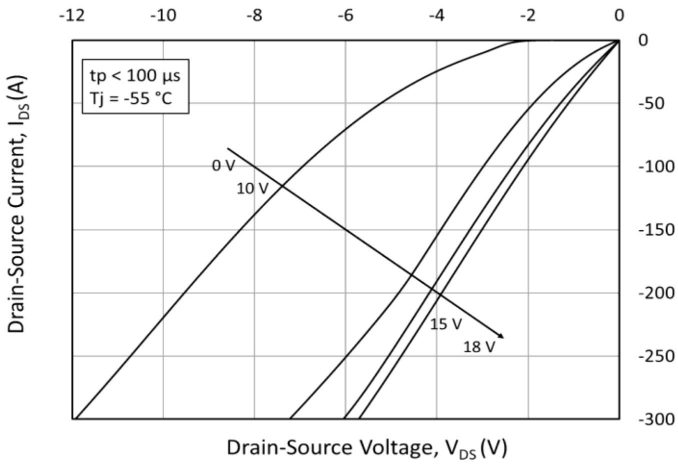


Figure 13. 3rd Quadrant Characteristic at T_{VJ} = -55 °C

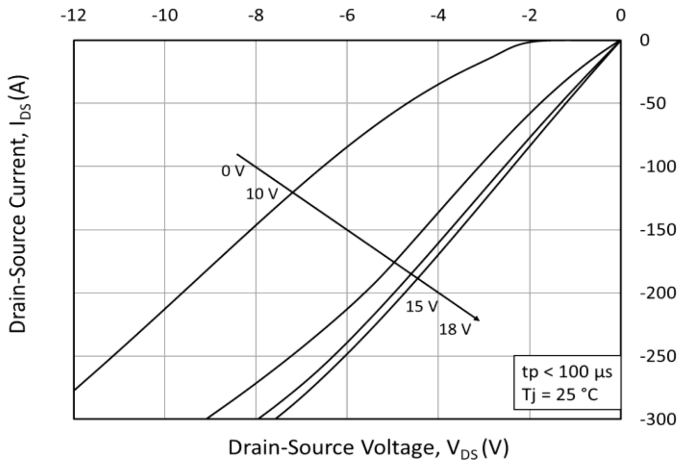


Figure 14. 3rd Quadrant Characteristic at T_{VJ} = 25 °C

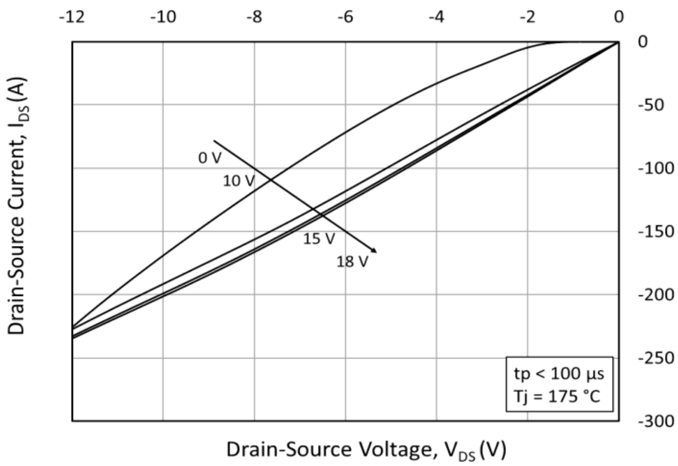


Figure 15. 3rd Quadrant Characteristic at T_{VJ} = 175 °C

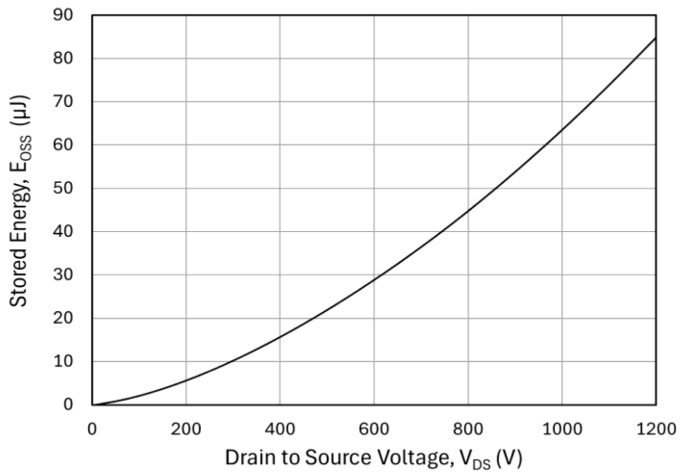


Figure 16. Output Capacitor Stored Energy

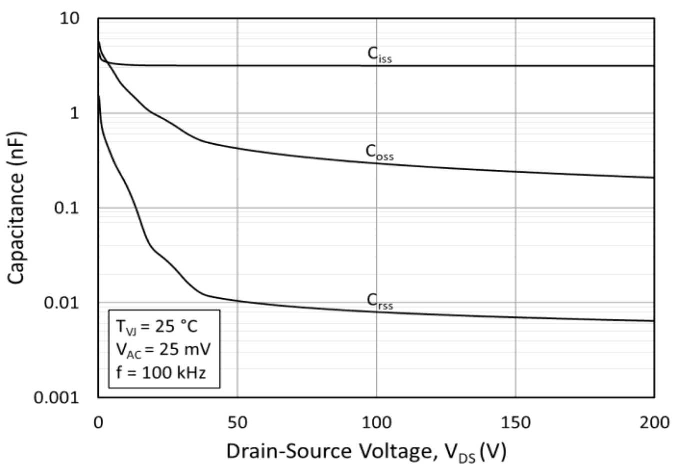


Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

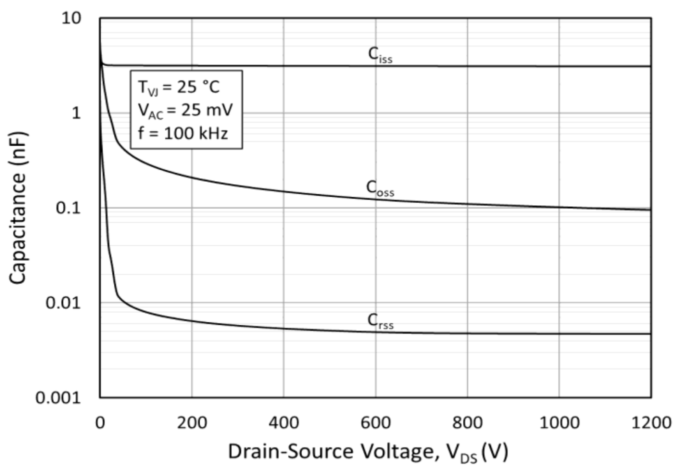


Figure 18. Capacitances vs. Drain-Source Voltage (0-1200 V)

Typical Performance

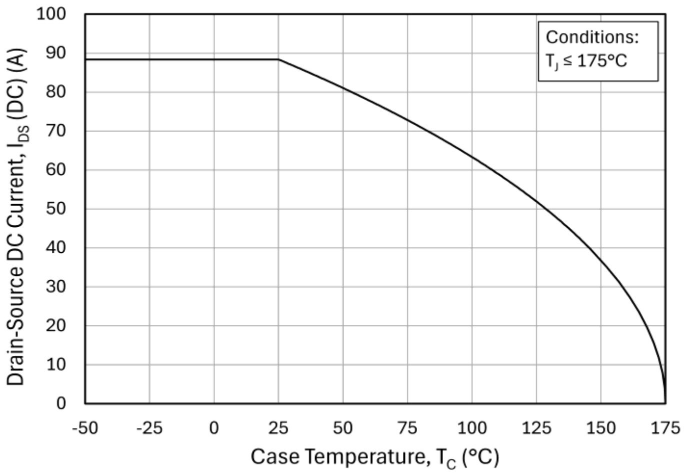


Figure 19. Continuous Drain Current Derating vs. Case Temperature

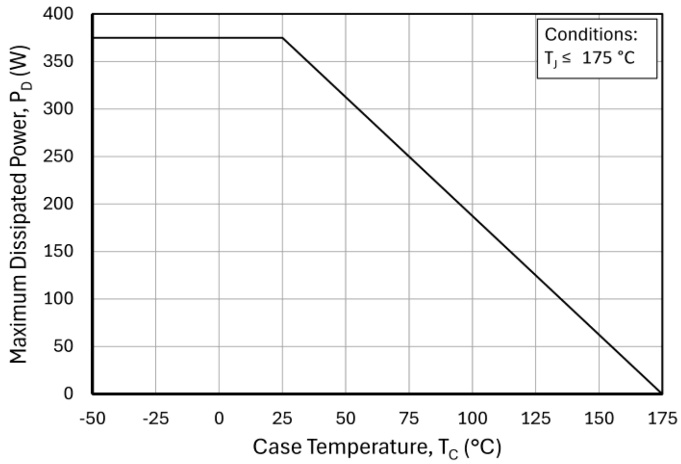


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

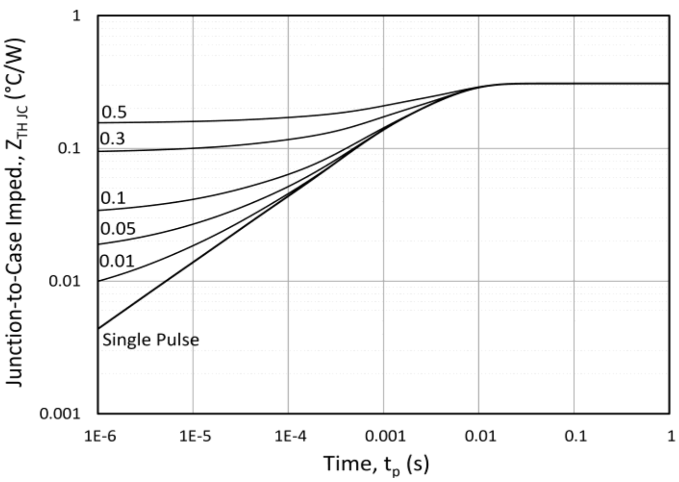


Figure 21. Transient Thermal Impedance (Junction - Case) °C

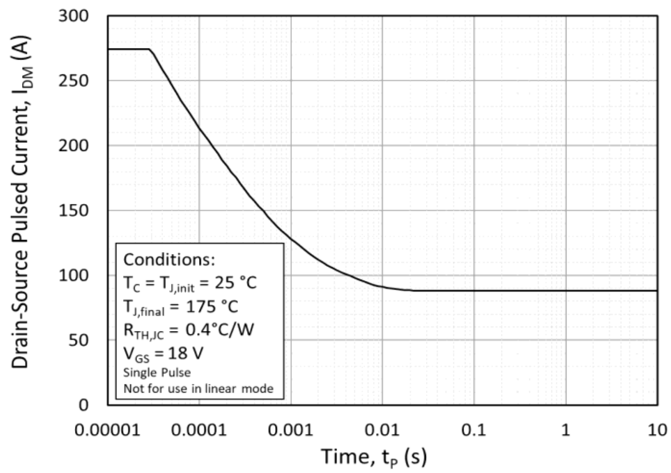


Figure 22. Safe Operating Area

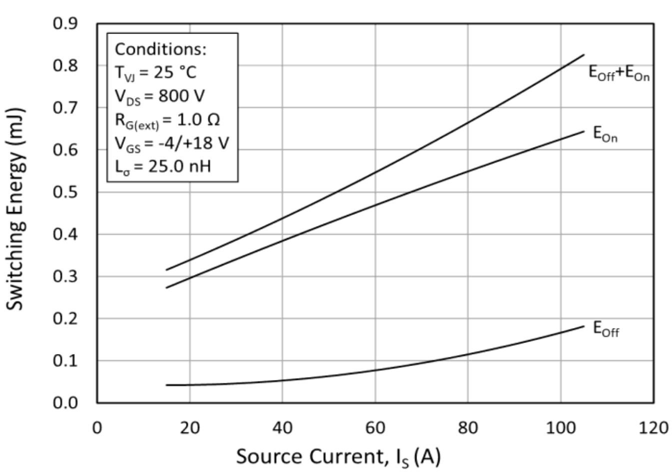


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 800 V)

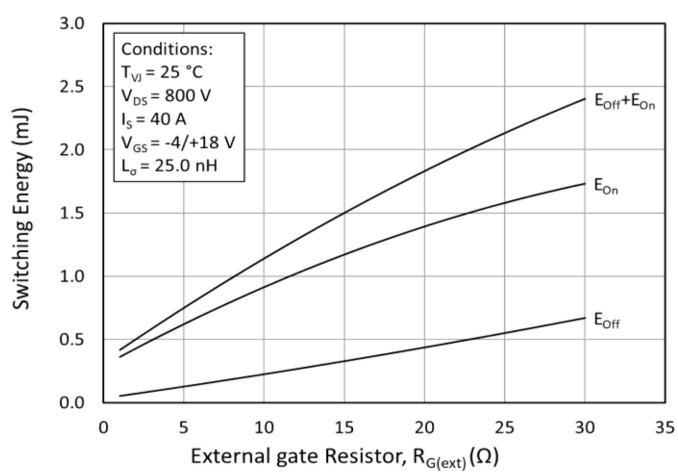


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

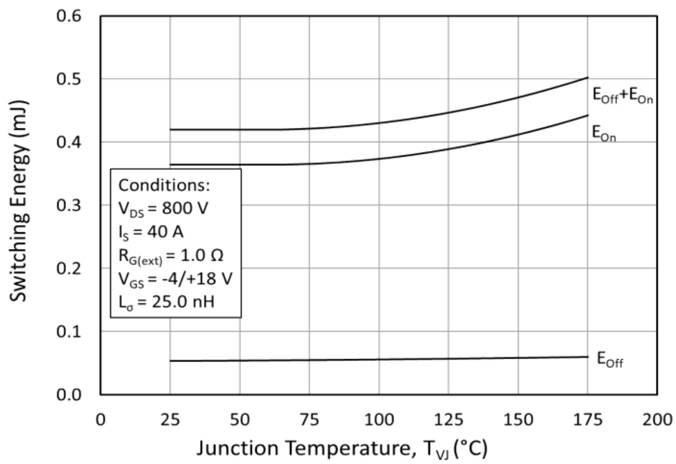


Figure 25. Clamped Inductive Switching Energy vs. Temperature

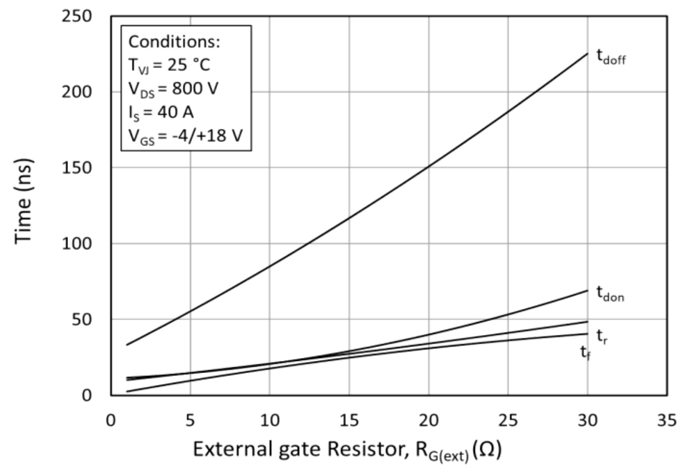


Figure 26. Switching Times vs. $R_{G(ext)}$

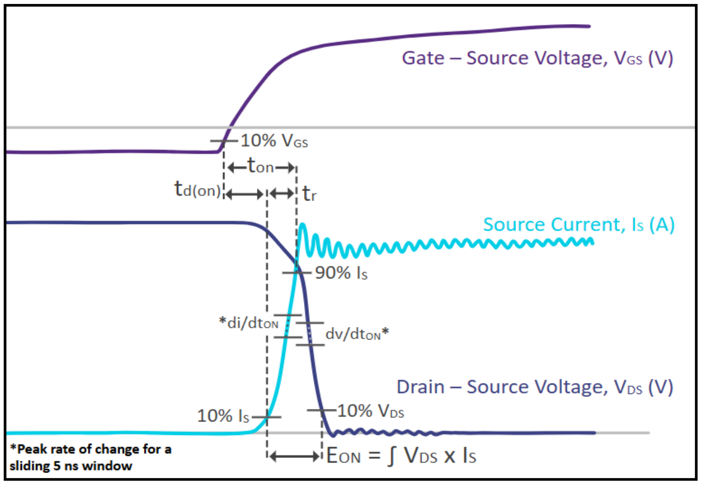


Figure 27. Turn On Switching Time Definition

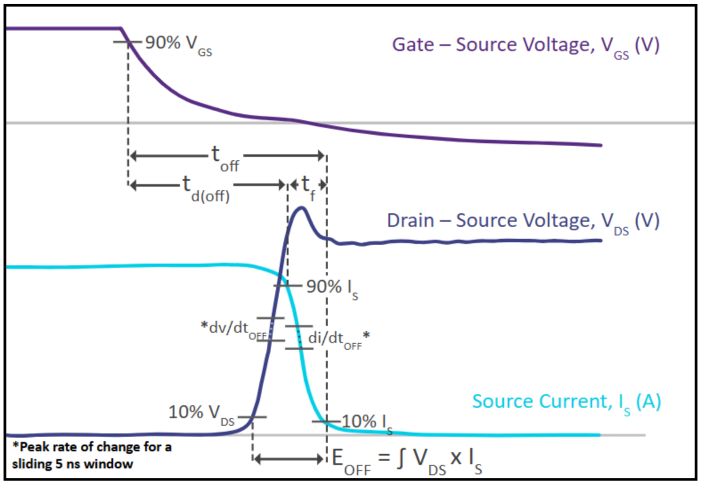


Figure 28. Turn Off Switching Time Definition

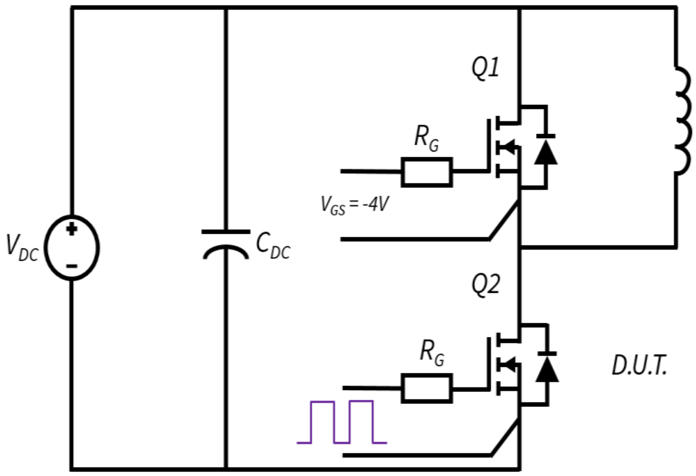


Figure 29. Clamped Inductive MOSFET Switching Waveform Test Circuit

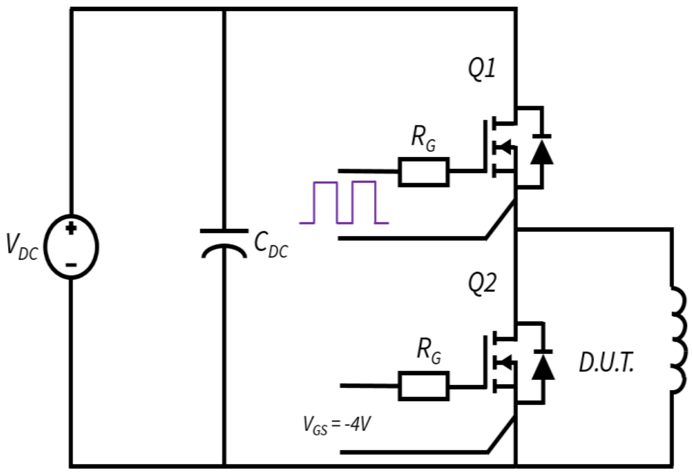
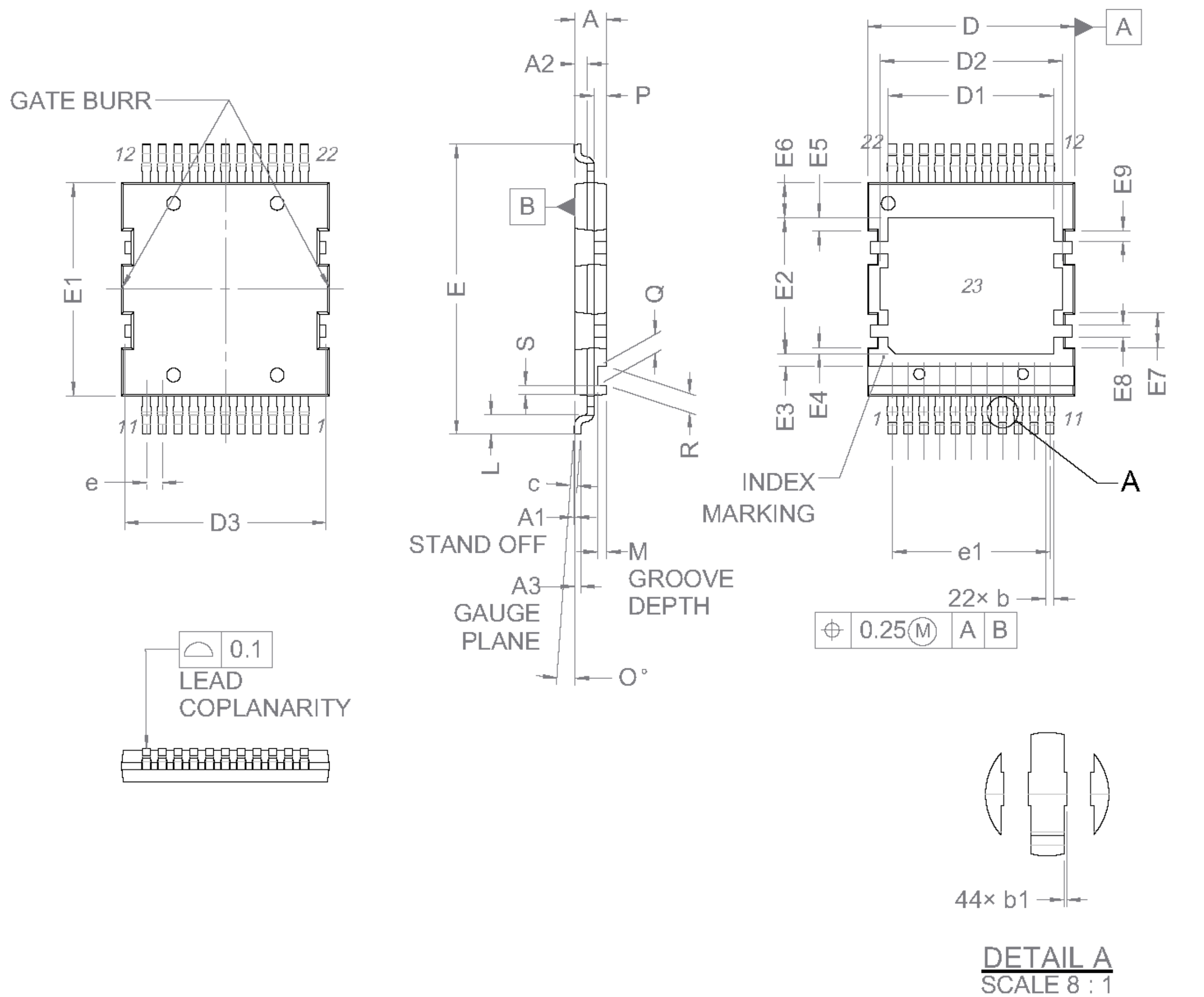


Figure 30. Clamped Inductive Body Diode Switching Waveform Test Circuit

Package Dimensions



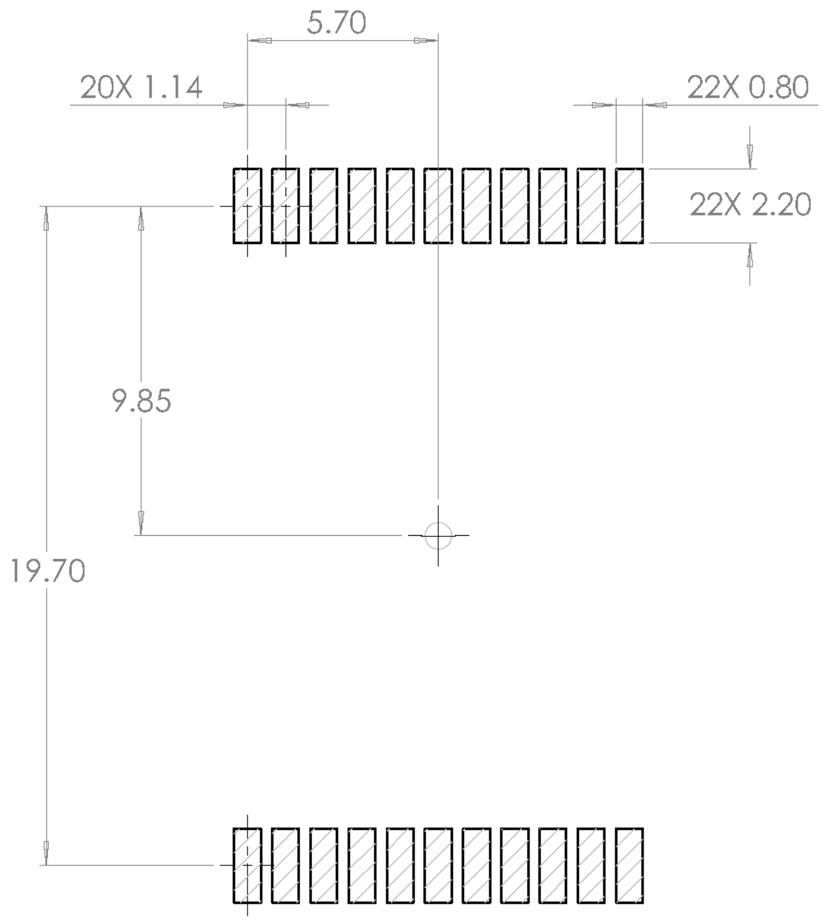
SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A	2.2	2.35	E6	2.53	
A1	0	0.15	E7	2.4	
A2	0.9		E8	0.9	
A3	0.5		E9	0.75	
b	0.5	0.7	e	1.14	
b1	-	0.15	e1	11.4	
c	0.46	0.58	L	1.3	
D	14.9	15.1	M	0.6	
D1	12		N	22	
D2	13.2		O	0°	8°
D3	14.5	14.7	P	0.9	
E	20.81	21.11	P1	0.7	0.9
E1	15.3	15.5	P2	0.9	1.1
E2	9.83		Q	1.6	
E3	0.625		R	1.7	
E4	0.45		S	0.631	
E5	0.95				

PIN	DESCRIPTION
1	GATE
2	KELVIN
3-11	SOURCE
12-23	DRAIN

NOTE:
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT
2. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES IN DEGREES
3. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
4. DIMENSIONS DO NOT INCLUDE MOLD FLASH (0.15mm MAX PER SIDE) OR GATE BURR (0.3mm MAX)
5. THE LEAD SIDE IS COMPREHENSIVE OF THE THICKNESS OF THE LEAD FINISH MATERIAL

Recommended Solder Pad Layout

All dimensions in mm



Revision History

Documents Version	Date of Change	Description of Changes
1	May 2026	Initial Release
2	June 2026	• Updated Package Type • Corrected L_σ to 25 nH • Corrected Voltage in Note 7 • Adjusted Figures 19 to 22

Appendix

Appendix Number	Description
A1	The following are recommendations for turning off the MOSFET with 0 V: • Measure the V_{GS} spike accurately using high-CMRR probes and low common mode noise measurements. • For the safe operation of the device, the voltage spike shall remain < 5 V for a time duration of < 40 ns.

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REACh Compliance

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