E4MS015075J2

Automotive Silicon Carbide Power MOSFET

Features

- Industry compatible drive voltage 15 V ...18 V/-4 V ...0 V
- Soft body diode with low V_{DS} overshoot and ringing
- Low $R_{DS(on)}$ at high operating temperatures
- Improved device capacitances ratio (C_{iss}/C_{rss})
- High transient voltage robustness with improved lifetime
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

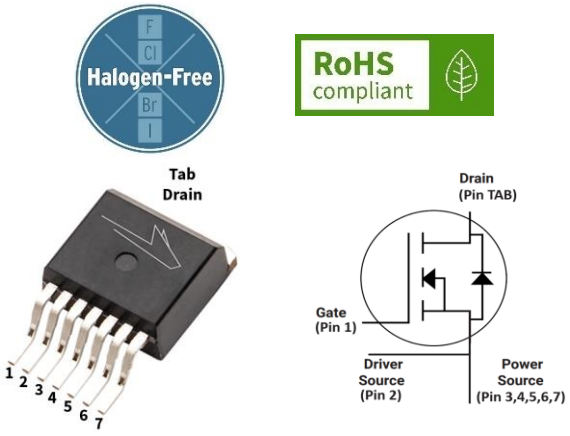
Benefits

- Higher efficiency with lower switching losses and EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system level cooling requirements

Typical Applications

- Onboard charger
- High voltage DC/DC converters
- HVAC compressors
- Battery management systems

Package



Orderable Part Number	Package Type	Marking
E4MS015075J2-TR	TO-263-7XL	E4MS015075J2

Absolute Maximum Ratings

Stress beyond those listed under absolute maximum ratings may damage the device.

Symbol	Parameter	Min.	Max.	Unit	Conditions	Note
$V_{DS(max)}$	Drain-Source Voltage		750	V		
$V_{GS(max)}$	Maximum Gate – Source Voltage (Transient)	-8	+23			Note 1
I_D	DC Continuous Drain Current		136	A	V_{GS} = 18 V, T_c = 25 °C, $T_J \leq$ 175 °C	Note 2
			95		V_{GS} = 18 V, T_c = 100 °C, $T_J \leq$ 175 °C	
I_{DM}	Pulsed Drain Current		319		V_{GS} = 18 V, T_c = 25 °C, t_{Pmax} limited by T_{jmax}	
P_D	Power Dissipation		433	W	T_c = 25 °C, T_J = 175 °C	Note 3
T_J, T_{stg}	Operating Junction and Storage Temperature	-55	+175	°C		
T_L	Solder Temperature		260		According to JEDEC J-STD-020	

Note (1): Refer to AN PRD-09634
Note (2): Current limit calculated by $I_{D(max)} = \sqrt{(P_D/R_{DS(typ)}/(T_{J(max)}, I_{D(max)}))}$
Note (3): $P_D = (T_J - T_C) / R_{th(JC,Max)}$

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Electrical Characteristics (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain – Source Breakdown Voltage	750			V	V_{GS} = 0 V, I_D =100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2	2.6	3.9	V	V_{DS} = V_{GS}, I_D = 12.55 mA	Fig. 11, Note 1
			2		V	V_{DS} = V_{GS}, I_D = 12.55 mA, T_J = 175°C	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	µA	V_{DS} = 750 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 18 V, V_{DS} = 0 V	
$V_{GS(op)}$	Recommended Turn on Gate-Source Voltage		+15…+18		V		Note 4
	Recommended Turn off Gate-Source Voltage		-4…0				
$R_{DS(on)}$	Drain-Source On-State Resistance		15	19.5	mΩ	V_{GS} = 18 V, I_D = 45.6 A	Fig. 4, 5, 6
			22			V_{GS} = 18 V, I_D = 45.6 A, T_J = 175°C	
			18			V_{GS} = 15 V, I_D = 45.6 A	
g_{fs}	Transconductance		33		S	V_{DS} = 20 V, I_D = 45.6 A	Fig. 7
			34			V_{DS} = 20 V, I_D = 45.6 A, T_J = 175 °C	
$R_{DS(on)Tempco}$	On resistance temperature coefficient		1.47			V_{GS} = 18 V, I_D = 45.6 A	Note 5
C_{iss}	Input Capacitance		3748		pF	V_{GS} = 0 V, V_{DS} = 500 V f = 100kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		218				
C_{rss}	Reverse Transfer Capacitance		8				
E_{oss}	C_{OSS} Stored Energy		35.7		µJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		280		pF	V_{GS} = 0 V, V_{DS} = 0 V … 500 V	Note 6
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		445				
E_{on}	Turn-On Switching Energy (Body Diode FWD) T_j = 25 °C T_j = 175 °C		201 203		µJ	V_{DS} = 500 V, V_{GS} = -4 V / 18 V, I_D = 45.6 A, $R_{G(ext)}$ = 2 Ω, $L_σ$ = 25 nH	Fig. 25, 27, 29
E_{off}	Turn-Off Switching Energy (Body Diode FWD) T_j = 25 °C T_j = 175 °C		70 71				Fig. 25, 28, 29
$t_{d(on)}$	Turn-On Delay Time		12.9		ns	V_{DS} = 500 V, V_{GS} =-4 V / 18 V, I_D = 45.6 A, $R_{G(ext)}$ = 2 Ω, $L_σ$ = 25 nH	Fig. 26, 27, 29
t_r	Rise Time		5.2				
$t_{d(off)}$	Turn-Off Delay Time		40.2				Fig. 26, 28, 29
t_f	Fall Time		9.8				
$R_{G(int)}$	Internal Gate Resistance		2.2		Ω	f = 1MHz	
Q_{gs}	Gate to Source Charge		41		nC	V_{DS} = 500 V, V_{GS} = -4 V/ 18 V I_D = 45.6 A	Fig. 12
Q_{gd}	Gate to Drain Charge		43				
Q_g	Total Gate Charge		147				

Note (4): Refer to AN PRD-08999.
Note (5): $R_{DS(on)Tempco}$ refers to $R_{DS(on)}$ at 25°C / $R_{DS(on)}$ at 175°C. This is a E4MS 750 V product family value.
Note (6): $C_{o(er)}$, a lumped capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to 500 V.
$C_{o(tr)}$, a lumped capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to 500 V.

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Reverse Diode Characteristics (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	V_{GS} = -4 V, I_{SD} = 22.8 A, T_J = 25°C	Fig. 8, 9, 10
		4.5			V_{GS} = -4 V, I_{SD} = 22.8 A, T_J = 175°C	
I_S	Continuous Diode Forward Voltage		70	A	V_{GS} = -4 V, T_C = 25°C	
I_{SM}	Diode Pulse Current		319		V_{GS} = -4 V, pulse width t_p limited by T_{jmax}	
t_{rr}	Reverse Recovery Time	10.6		ns	V_{GS} = -4 V, I_{SD} = 45.6 A, V_R = 500 V, di_f/dt = 11288 A/µs, T_J = 175 °C, $R_{G(ext)}$ = 2 Ω, L_σ = 25 nH	Fig. 30
Q_{rr}	Reverse Recovery Charge	467.5		nC		
I_{RRM}	Peak Reverse Recovery Current	75		A		
E_{RR}	Reverse Recovery Energy T_j = 25 °C T_j = 175 °C	160 170		µJ		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.3	0.39	K/W		

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Typical Performance

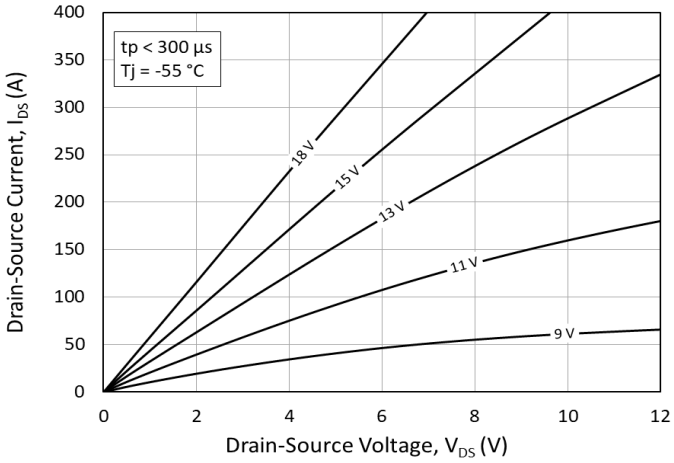

Figure 1. Output Characteristics T_{VJ} = -55 °C

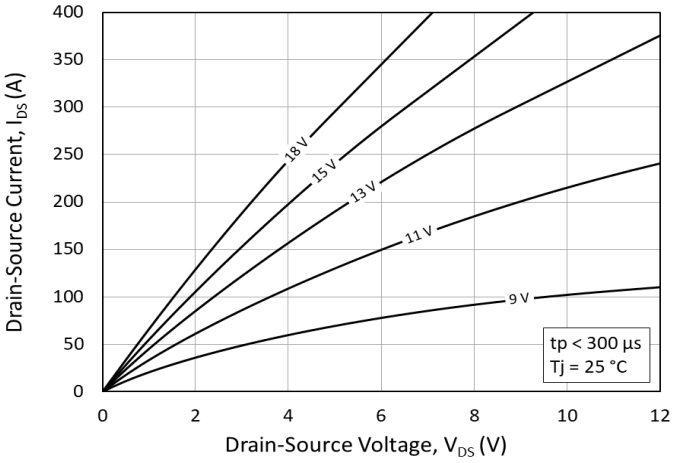

Figure 2. Output Characteristics T_{VJ} = 25 °C

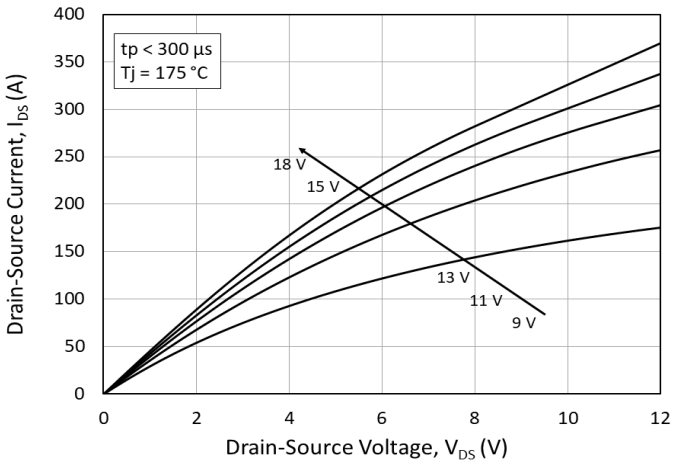

Figure 3. Output Characteristics T_{VJ} = 175 °C

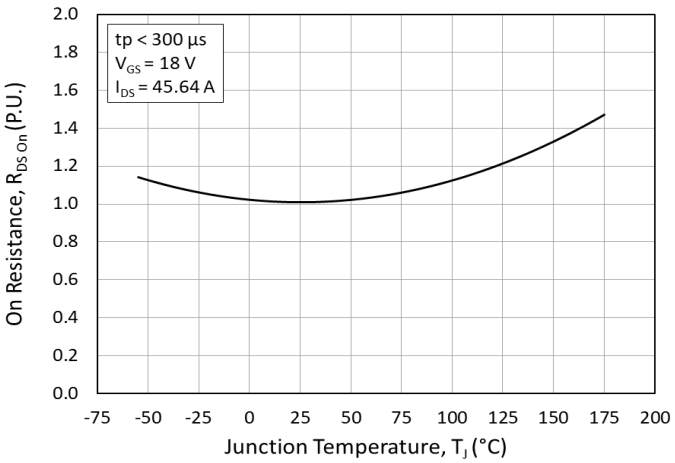

Figure 4. Normalized On-Resistance vs. Temperature

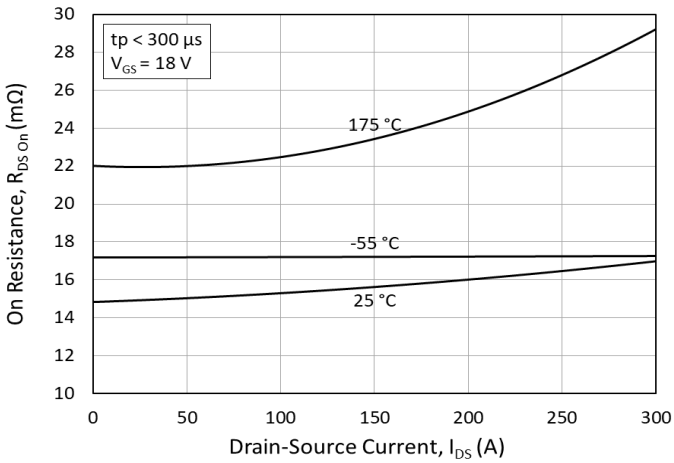

Figure 5. On-Resistance vs. Drain Current for Various Temperatures

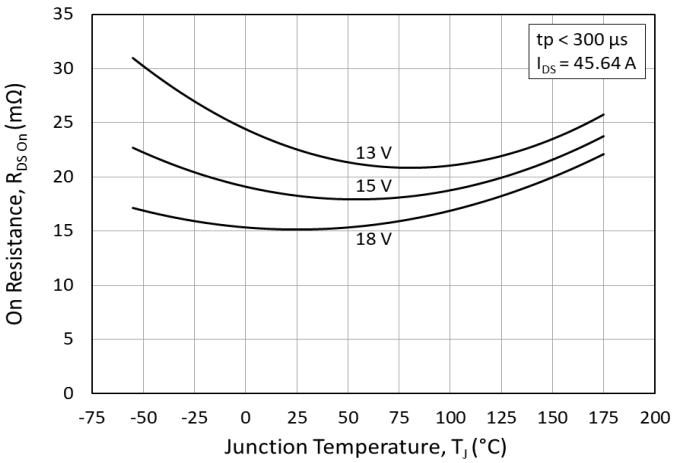

Figure 6. On-Resistance vs. Temperature for Various Gate Voltages

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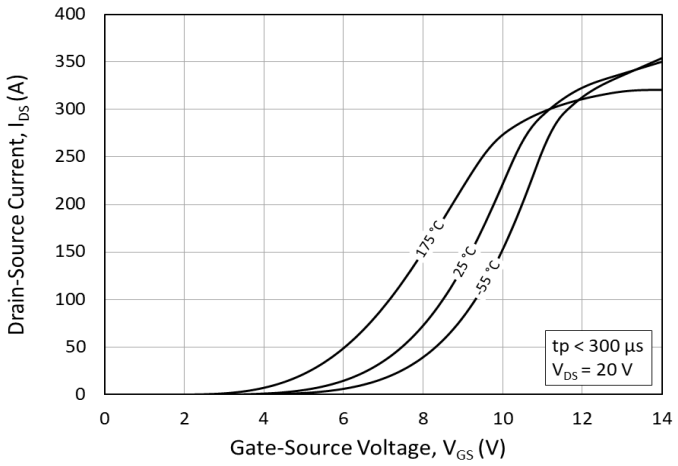

Figure 7. Transfer Characteristic for Various Junction Temperatures

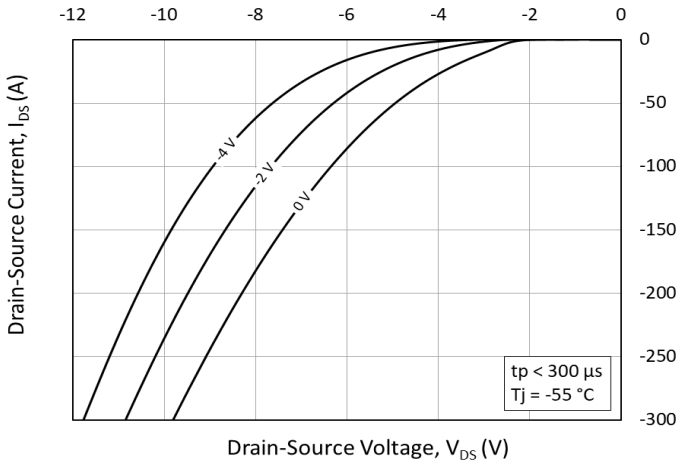

Figure 8. Body Diode Characteristic at T_{VJ} = -55 °C

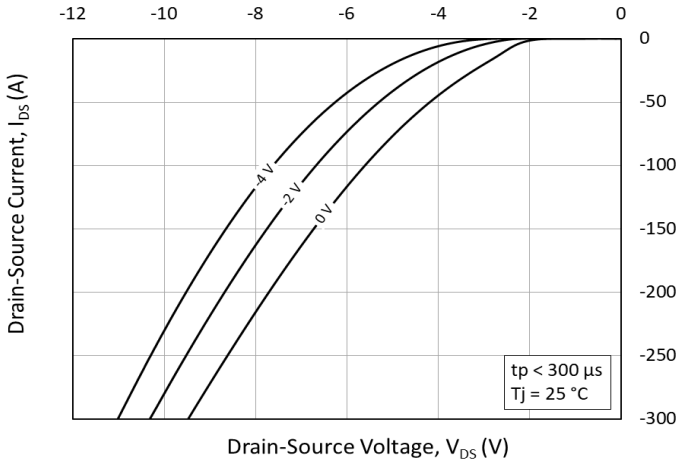

Figure 9. Body Diode Characteristic at T_{VJ} = 25 °C

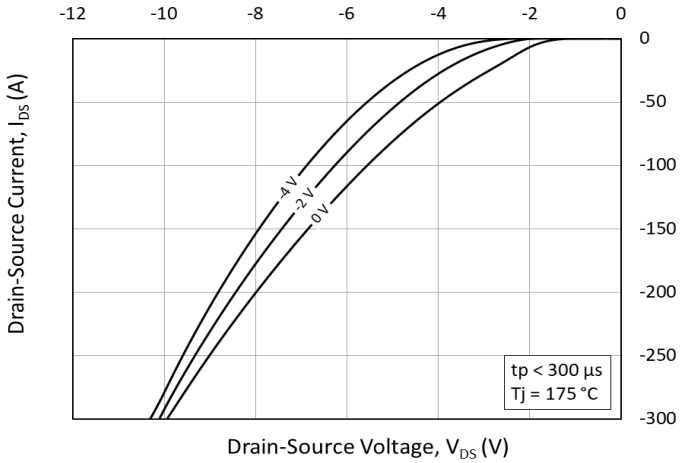

Figure 10. Body Diode Characteristic at T_{VJ} = 175 °C

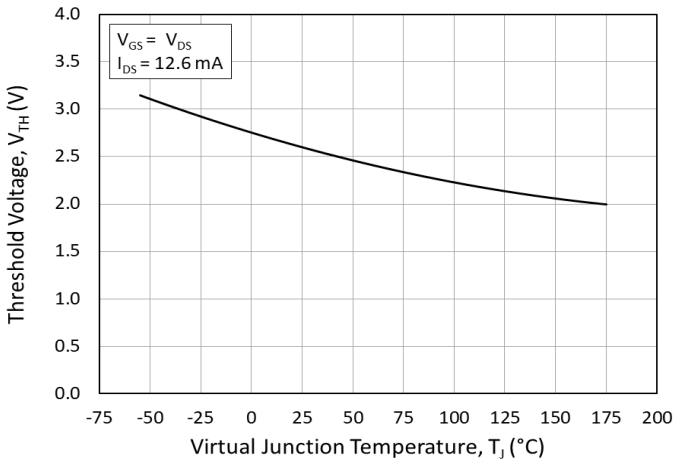

Figure 11. Threshold Voltage vs. Temperature

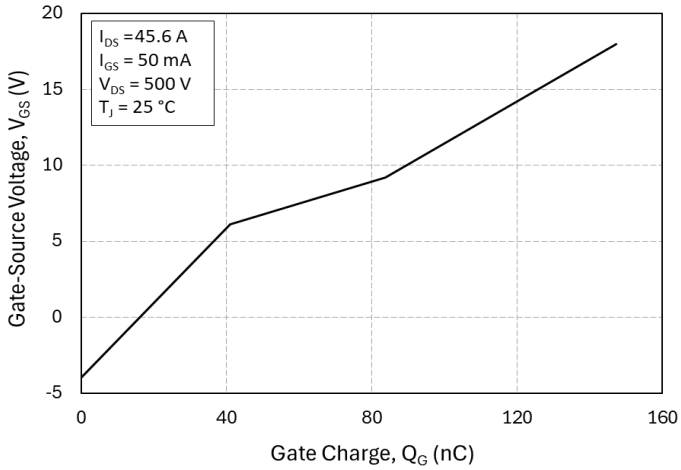

Figure 12. Gate Charge Characteristics

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Typical Performance

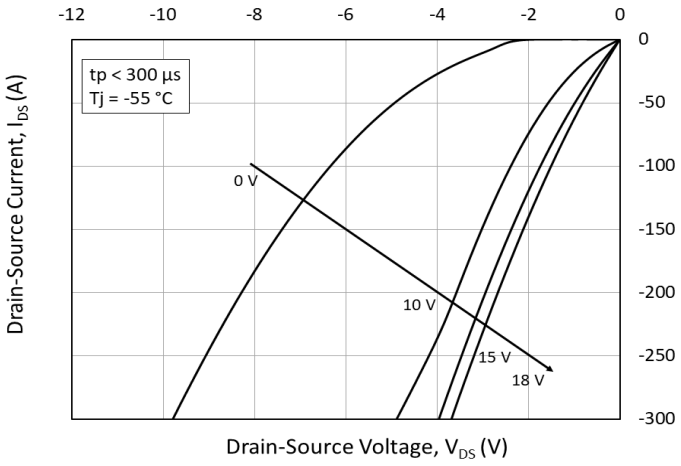

Figure 13. 3rd Quadrant Characteristic at T_{VJ} = -55 °C

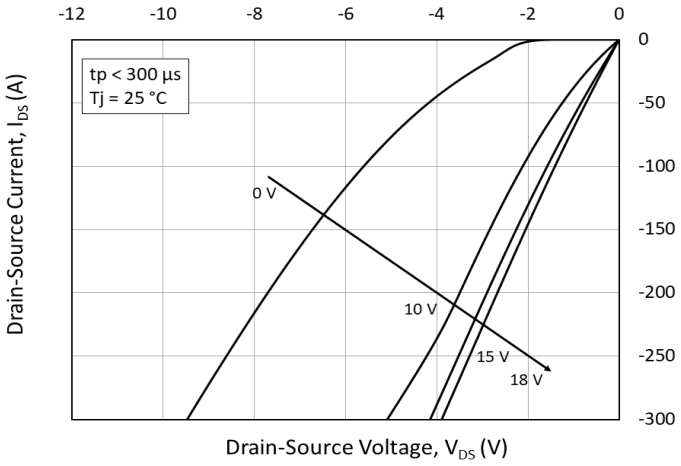

Figure 14. 3rd Quadrant Characteristic at T_{VJ} = 25 °C

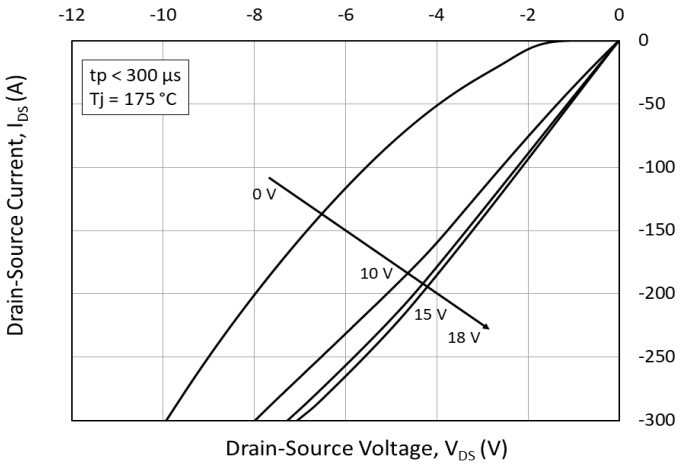

Figure 15. 3rd Quadrant Characteristic at T_{VJ} = 175 °C

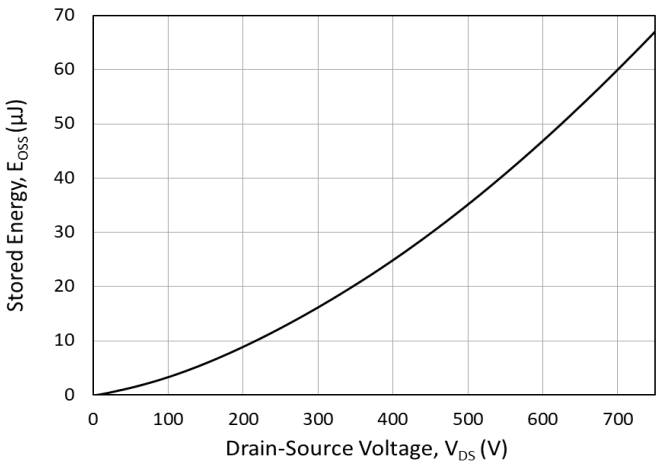

Figure 16. Output Capacitor Stored Energy

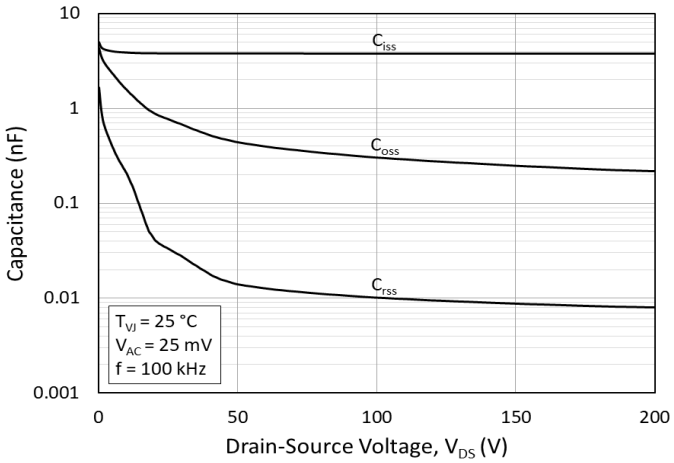

Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

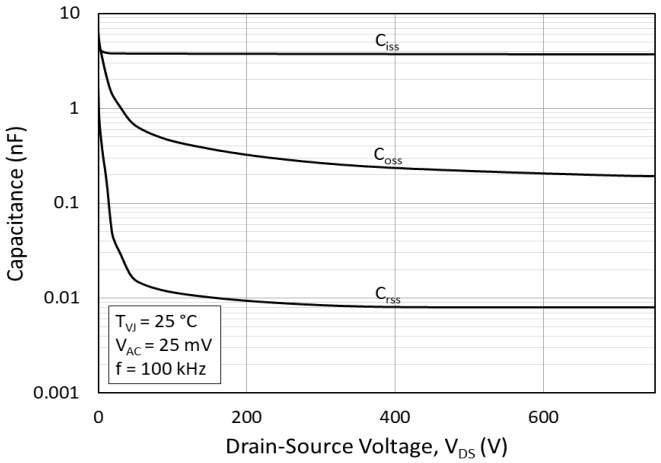

Figure 18. Capacitances vs. Drain-Source Voltage (0-750 V)

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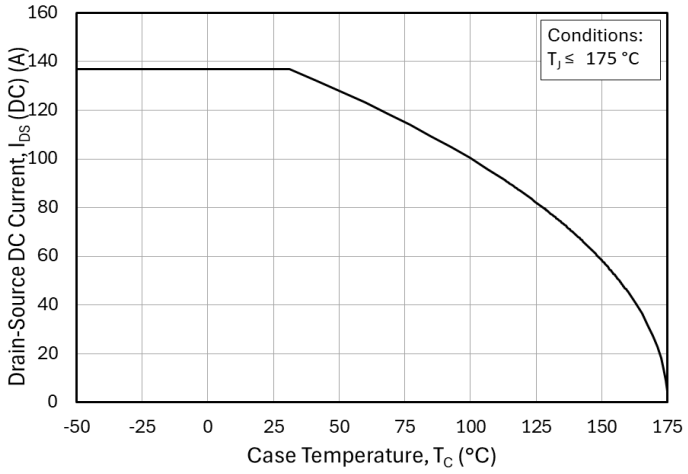

Figure 19. Continuous Drain Current Derating vs. Case Temperature

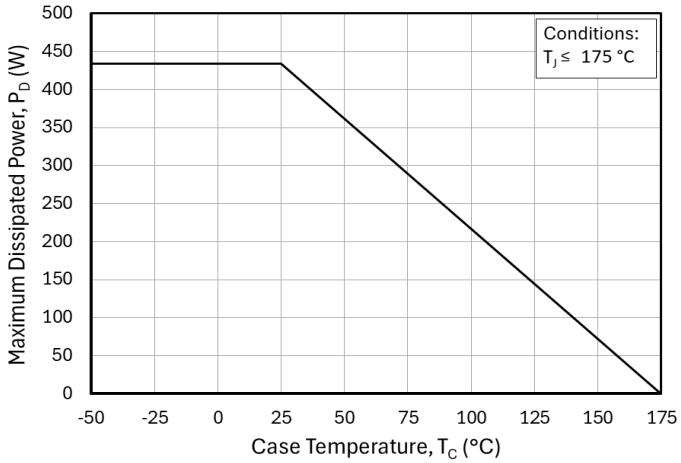

Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

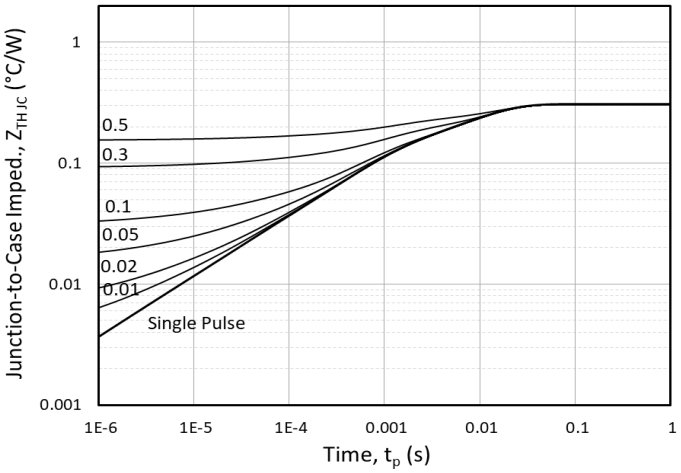

Figure 21. Transient Thermal Impedance (Junction - Case) °C

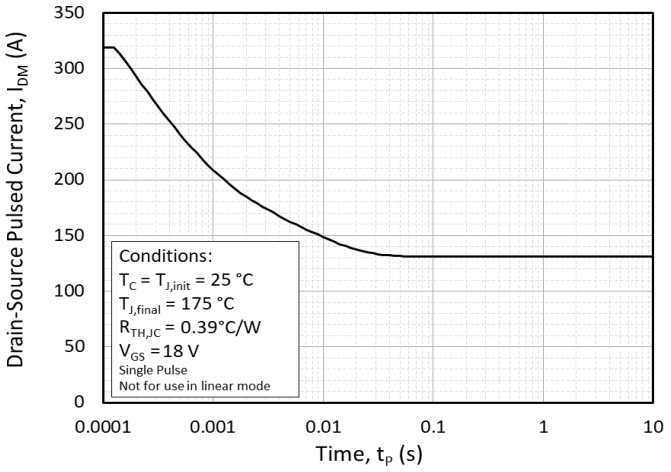

Figure 22. Safe Operating Area

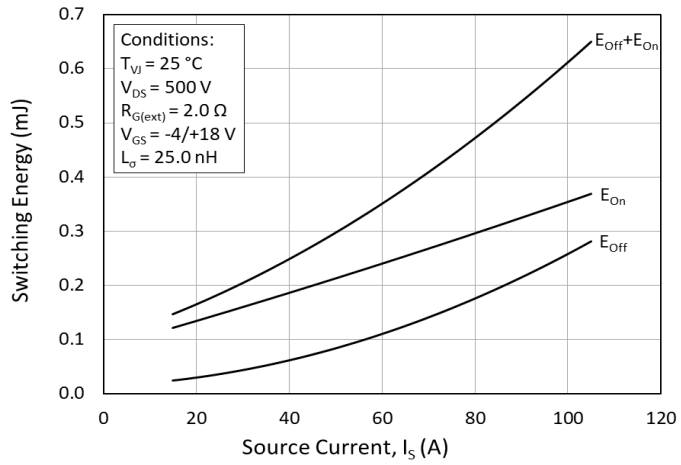

Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 500 V)

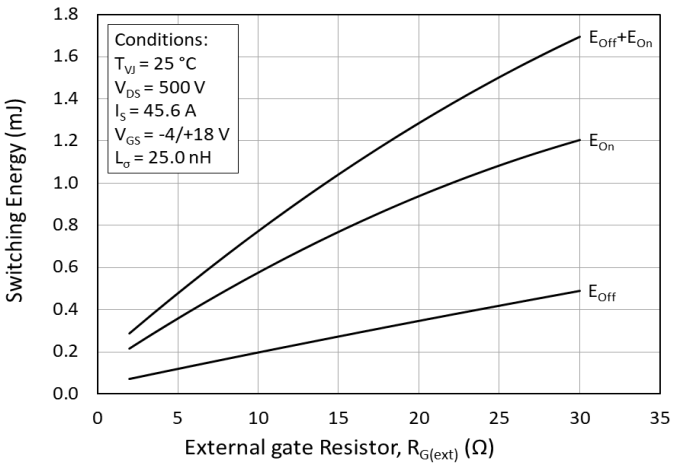

Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

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Typical Performance

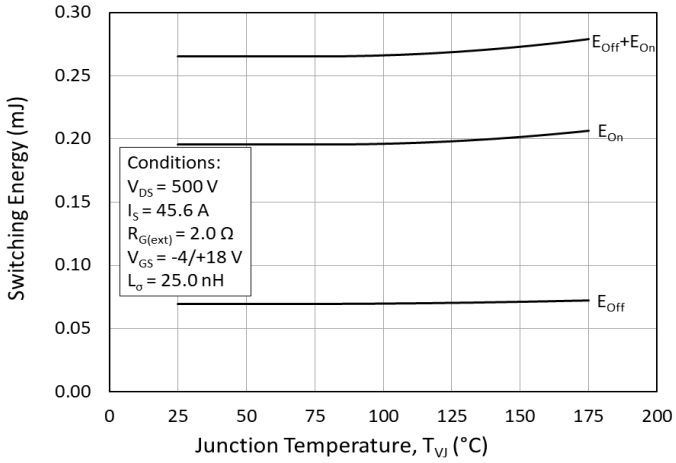

Figure 25. Clamped Inductive Switching Energy vs. Temperature

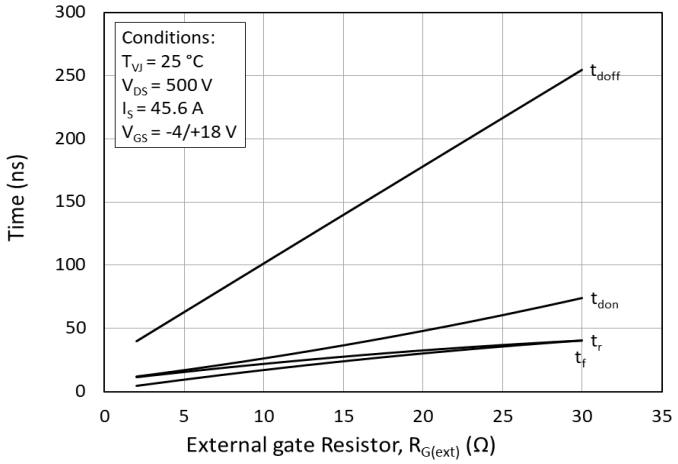

Figure 26. Switching Times vs. $R_{G(ext)}$

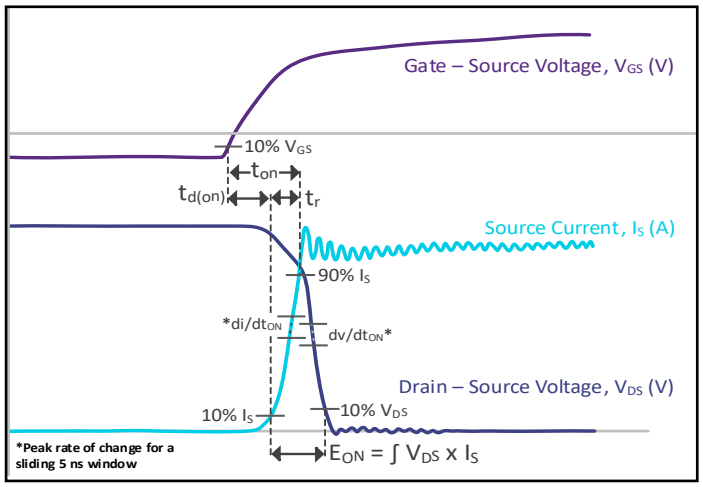

Figure 27. Turn On Switching Time Definition

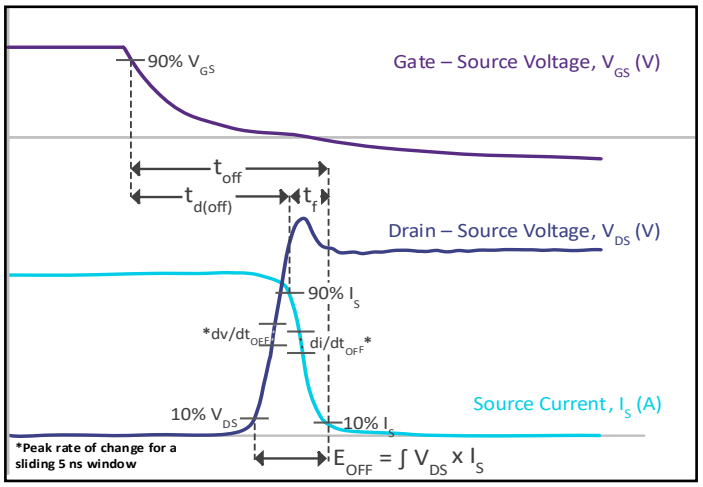

Figure 28. Turn Off Switching Time Definition

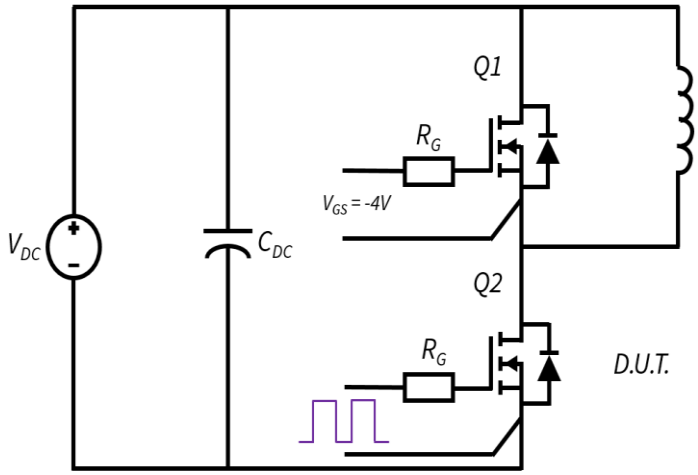

Figure 29. Clamped Inductive MOSFET Switching Waveform Test Circuit

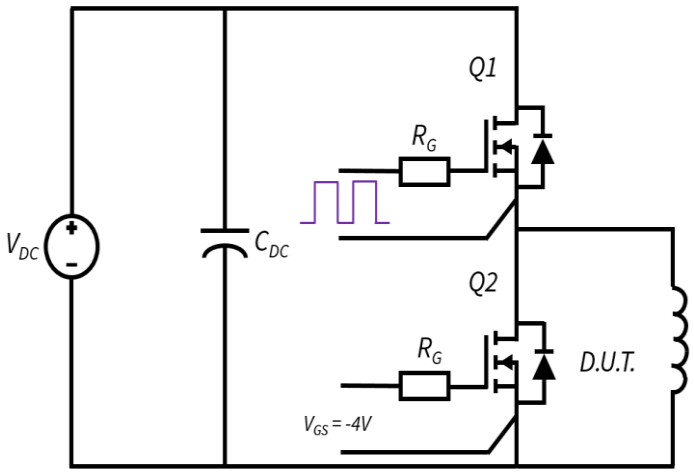

Figure 30. Clamped Inductive Body Diode Switching Waveform Test Circuit

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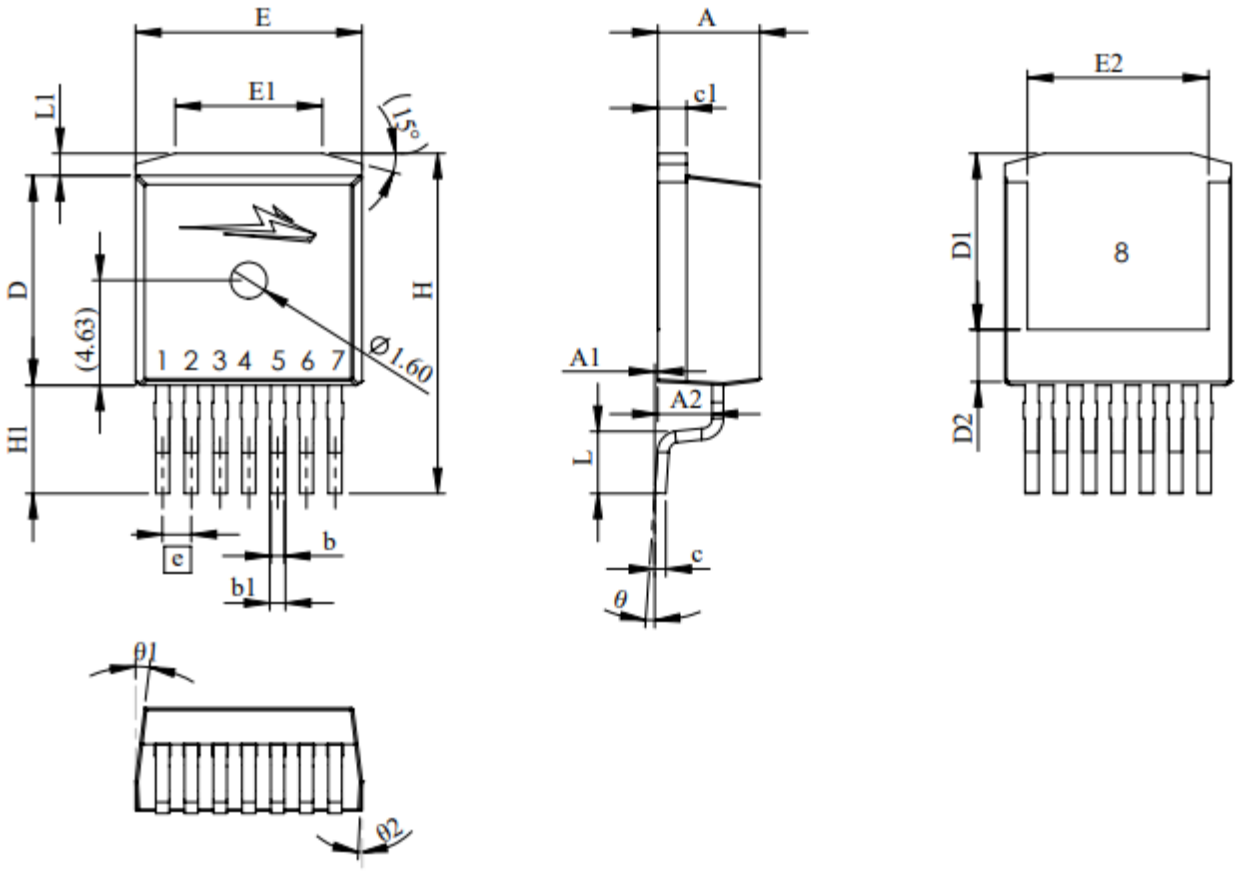
Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	4.30	4.70
A1	0.00	0.25
A2	2.20	2.60
b	0.52	0.72
b1	0.60	0.80
c	0.42	0.62
c1	1.07	1.47
D	9.05	9.45
D1	7.58	7.98
D2	2.05	2.45
E	9.80	10.20
E1	6.30	6.97
E2	7.80	8.20
e	1.27 BSC	
H	14.87	15.27
H1	4.55	4.95
L	2.48	2.88
L1	0.87	1.27
θ	0°	8°
θ1	4°	10°
θ2	0°	6°

1	GATE
2	KELVIN
3	SOURCE
4	
5	
6	
7	
8	DRAIN

NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

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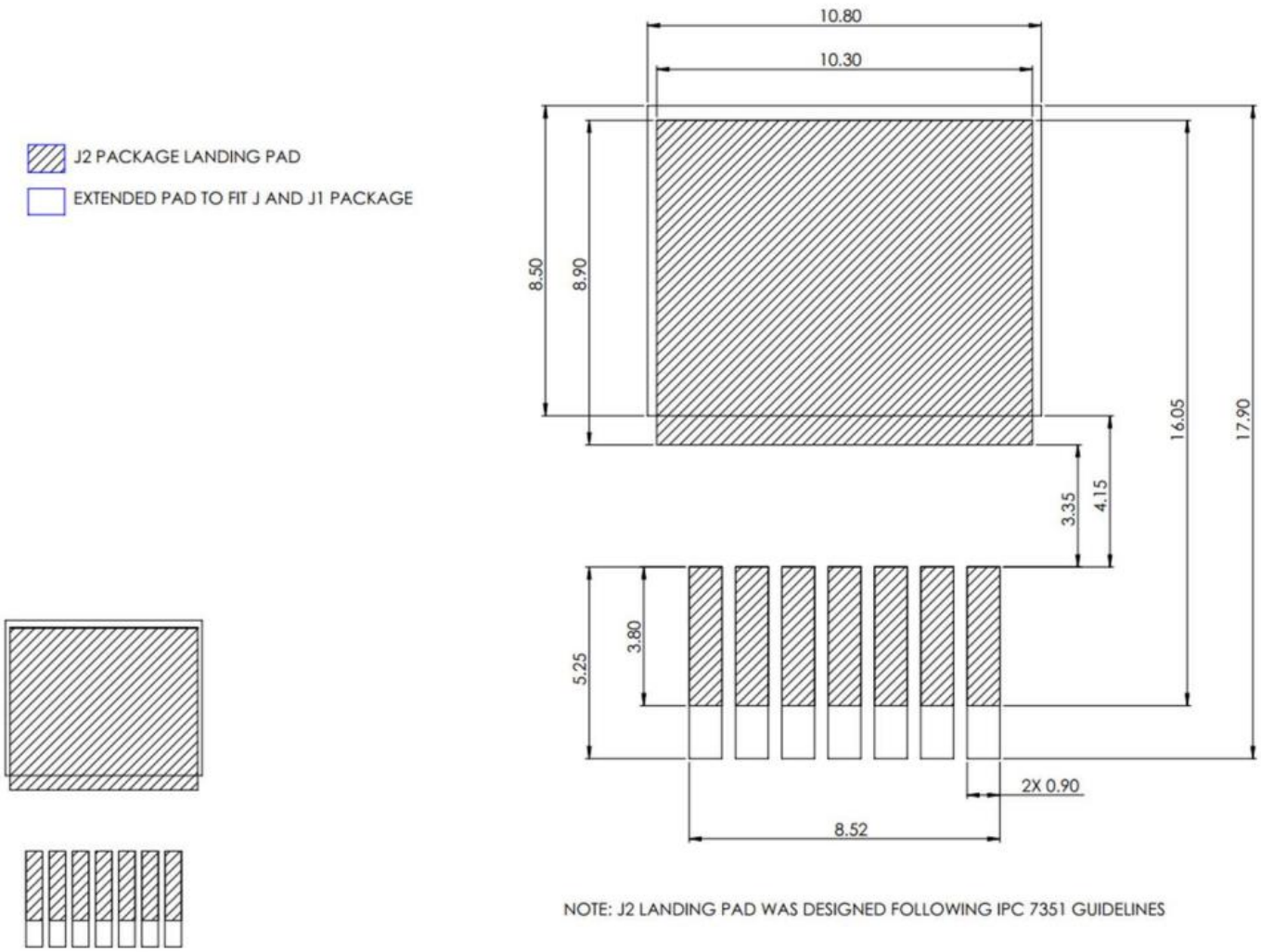
Recommended Solder Pad Layout

All dimensions in mm



NOTE: J2 LANDING PAD WAS DESIGNED FOLLOWING IPC 7351 GUIDELINES

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Revision History

Documents Version	Date of Change	Description of Changes
1	April 2026	Initial Release

Appendix

Appendix Number	Description
A1	The following are recommendations for turning off the MOSFET with 0 V: • Measure the V_{GS} spike accurately using high-CMRR probes and low common mode noise measurements. • For the safe operation of the device, the voltage spike shall remain < 5 V for a time duration of < 40 ns.

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