

C4MS035075J2

Switching Optimized 750V 35mΩ Industrial Silicon Carbide Power MOSFET

Features

- Industry compatible drive voltage 15V...18V/-5V...0V
- Soft body diode with low Vds overshoot and ringing
- Low Temperature Coefficient of RDS(on)
- Improved device capacitance ratio (Ciss/Crss)
- High transient voltage robustness with improved lifetime
- Halogen free, RoHS compliant

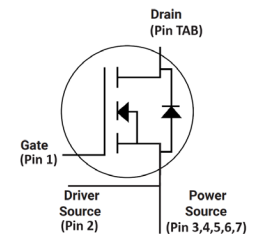
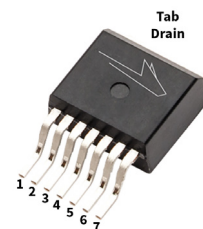
Benefits

- Higher efficiency, lower switching losses and reduced EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system-level cooling requirements

Typical Applications

- Data Center Power Supplies
- EV Chargers
- Solar/ESS
- Motor Control
- Industrial Power Supplies
- High Voltage DC/DC Converters

Package



Orderable Part Number	Package Type	Marking
C4MS035075J2-TR	TO-263-7 XL	C4MS035075J2

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain-Source Voltage	V_{DS}			750	V		
Maximum Gate-Source Voltage	$V_{GS(max)}$	-10		+23			Note 1
DC Continuous Drain Current	I_D		70		A	$V_{GS} = 18\text{ V}, T_C = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Note 2
			50			$V_{GS} = 18\text{ V}, T_C = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	
Pulsed Drain Current	I_{DM}			132		t_{Pmax} limited by T_{Jmax} $V_{GS} = 18\text{ V}, T_C = 25^\circ\text{C}$	
Power Dissipation	P_D		251		W	$T_C = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Note 3
Operating Junction and Storage Temperature	T_J, T_{stg}	-55		+175	$^\circ\text{C}$		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note (1): When applying IPC-9592B or OCP M-CRPS derating standards, a maximum Gate-Source voltage (V_{GS}) of +25V is permissible.

Note (2): Current limit calculated by $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)}) (T_{J(max)} - T_{D(max)})}$

Note (3): $P_D = (T_J - T_C) / R_{th(JC, typ)}$



Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	750			V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	3.9	V	$V_{DS} = V_{GS}, I_D = 5.2\text{ mA}$	Fig. 11
			2.0		V	$V_{DS} = V_{GS}, I_D = 5.2\text{ mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{DS} = 750\text{ V}, V_{GS} = 0\text{ V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 18\text{ V}, V_{DS} = 0\text{ V}$	
$V_{GS(op)}$	Recommended Turn on Gate-Source Voltage		15...18		V		Refer to PRD-09634
	Recommended Turn off Gate-Source Voltage		-5...0				
$R_{DS(on)}$	Drain-Source On-State Resistance		35.0	45.5	m Ω	$V_{GS} = 18\text{ V}, I_D = 18.8\text{ A}$	Fig. 4, 5, 6
			51.5			$V_{GS} = 18\text{ V}, I_D = 18.8\text{ A}, T_J = 175^\circ\text{C}$	
			42.0			$V_{GS} = 15\text{ V}, I_D = 18.8\text{ A}$	
g_{fs}	Transconductance		14		S	$V_{DS} = 20\text{ V}, I_D = 18.8\text{ A}$	Fig. 7
			13			$V_{DS} = 20\text{ V}, I_D = 18.8\text{ A}, T_J = 175^\circ\text{C}$	
$R_{DS(on)Tempco}$	On resistance temperature coefficient		1.47			$V_{GS} = 18\text{ V}, I_D = 18.8\text{ A}$	Note 4
C_{iss}	Input Capacitance		1466		pF	$V_{GS} = 0\text{ V}, V_{DS} = 500\text{ V}$ $f = 100\text{ kHz}$	Fig. 17, 18
C_{oss}	Output Capacitance		95				
C_{rss}	Reverse Transfer Capacitance		3.4				
C_{iss}/C_{rss}	Capacitance Ratio		430			$V_{AC} = 25\text{ mV}$	Note 5
E_{oss}	C_{oss} Stored Energy		16		μJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		124		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0...500\text{ V}$	Note 6
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		198				
E_{on}	Turn-On Switching Energy (Body Diode FWD) $T_J = 25^\circ\text{C}$ $T_J = 175^\circ\text{C}$		54 53		μJ	$V_{DS} = 500\text{ V}, V_{GS} = -4\text{ V}/18\text{ V}$ $I_D = 18.8\text{ A}, R_{G(ext)} = 2\text{ }\Omega, L_\sigma = 25\text{ nH}$	Fig. 25, 27, 29
E_{off}	Turn-Off Switching Energy (Body Diode FWD) $T_J = 25^\circ\text{C}$ $T_J = 175^\circ\text{C}$		26 25				Fig. 25, 28, 29
$t_{d(on)}$	Turn-On Delay Time		8.8		ns	$V_{DD} = 500\text{ V}, V_{GS} = -4\text{ V}/18\text{ V}$ $I_D = 18.8\text{ A}, R_{G(ext)} = 2\text{ }\Omega, L_\sigma = 25\text{ nH}$ Inductive load	Fig. 26, 27, 28, 29
t_r	Rise Time		2.5				
$t_{d(off)}$	Turn-Off Delay Time		19.5				
t_f	Fall Time		10.4				
$R_{G(int)}$	Internal Gate Resistance		2.3		Ω	$f = 1\text{ MHz}$	
Q_{gs}	Gate to Source Charge		18		nC	$V_{DS} = 500\text{ V}, V_{GS} = -4\text{ V}/18\text{ V}$	Fig. 12
Q_{gd}	Gate to Drain Charge		15			$I_D = 18.8\text{ A}$	
Q_g	Total Gate Charge		62			Per IEC60747-8-4	

Note (4): $R_{DS(on)Tempco}$ refers to $R_{DS(on)}$ at 175°C / $R_{DS(on)}$ at 25°C , C4MS 750V product family value

Note (5): Capacitance ratio is a FOM for Partial turn-on immunity PRD-06933, C4MS 750V product family value

Note (6): $C_{o(er)}$ a lumped capacitance that gives the same stored energy as C_{oss} while V_{ds} is rising from 0 to 500 V

$C_{o(tr)}$ a lumped capacitance that gives the same charging time as C_{oss} while V_{ds} is rising from 0 to 500 V



Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	$V_{GS} = -4\text{ V}, I_{SD} = 9.4\text{ A}$	Fig. 8, 9, 10
		4.5		V	$V_{GS} = -4\text{ V}, I_{SD} = 9.4\text{ A}, T_J = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current	37		A	$V_{GS} = -4\text{ V}$	
I_{SM}	Diode Pulse Current		132	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{Jmax}	
t_{rr}	Reverse Recovery Time	8.5		ns	$V_{SD} = 500\text{ V}, V_{GS} = -4\text{ V}, T_J = 175^\circ\text{C}$ $I_S = 18.8\text{ A}, di_F/dt = 12\text{ A/ns}$	Fig. 30
Q_{rr}	Reverse Recovery Charge	253		nC		
I_{RRM}	Peak Reverse Recovery Current	51		A		
E_{RR}	Reverse recovery Energy $T_J = 25^\circ\text{C}$ $T_J = 175^\circ\text{C}$	102 114		μJ	$V_{DS} = 500\text{ V}, V_{GS} = -4\text{ V}/18\text{ V}$ $I_D = 18.8\text{ A}, R_{G(on)} = 2\ \Omega, L_\sigma = 25\text{ nH}$	

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.6		$^\circ\text{C/W}$		

Typical Performance

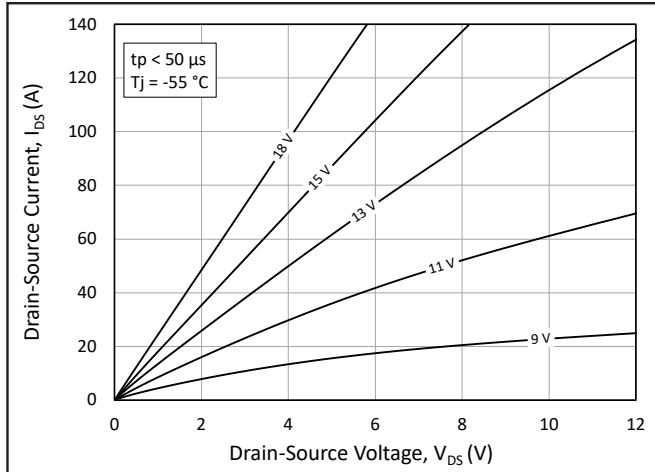


Figure 1. Output Characteristics $T_j = -55^\circ\text{C}$

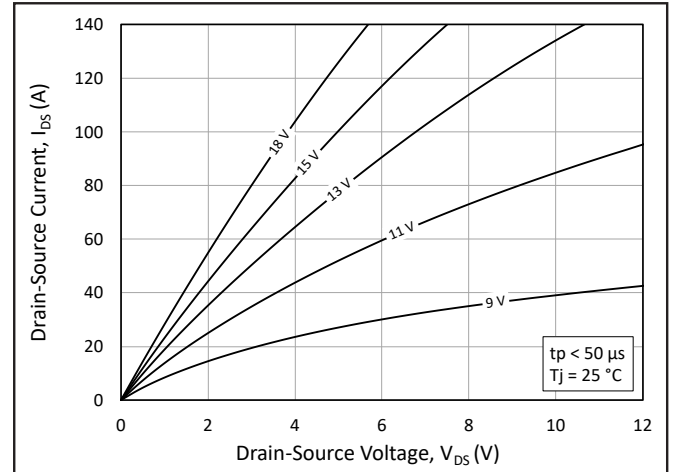


Figure 2. Output Characteristics $T_j = 25^\circ\text{C}$

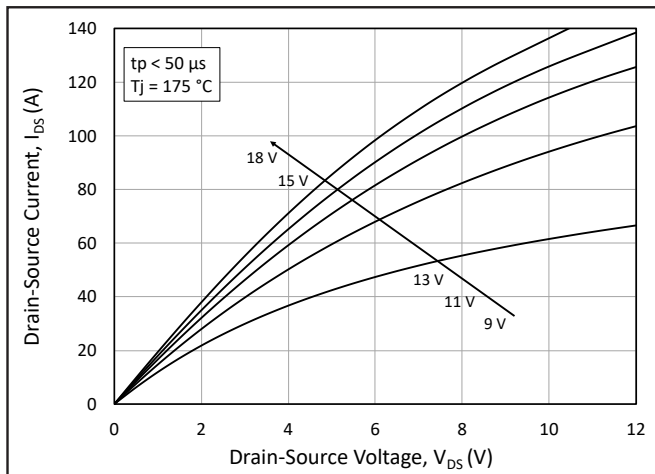


Figure 3. Output Characteristics $T_j = 175^\circ\text{C}$

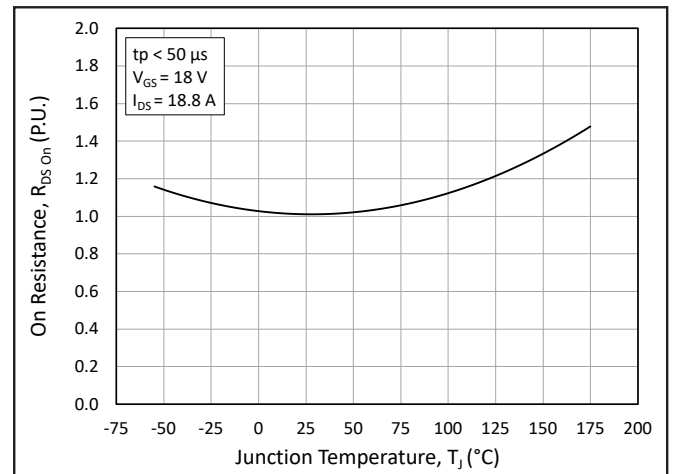


Figure 4. Normalized On-Resistance vs. Temperature

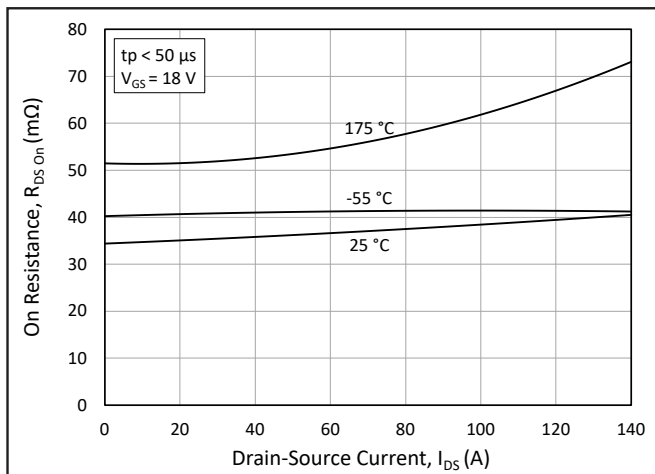


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

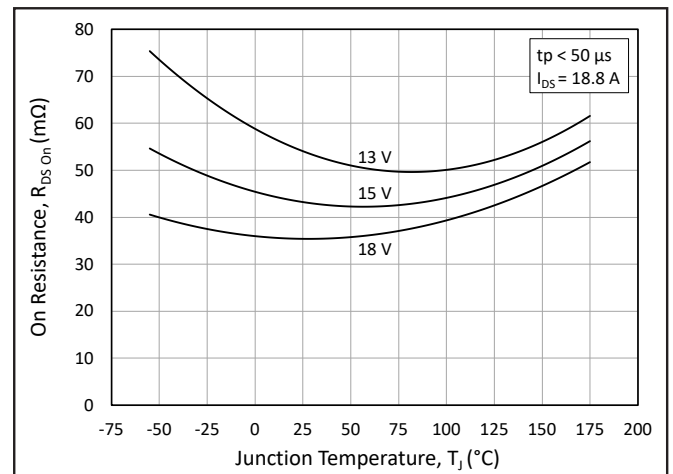


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

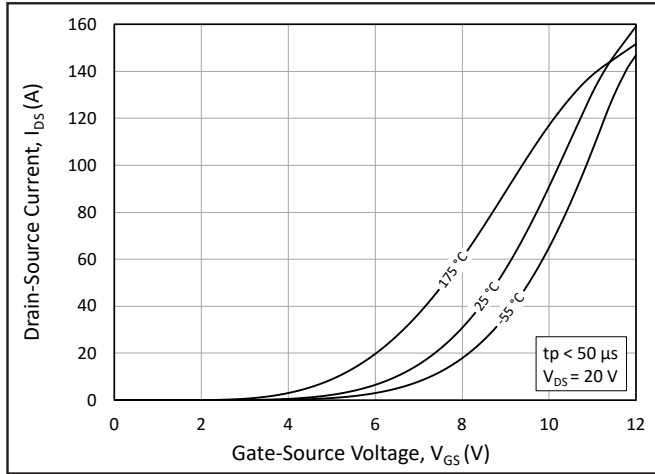


Figure 7. Transfer Characteristic for Various Junction Temperatures

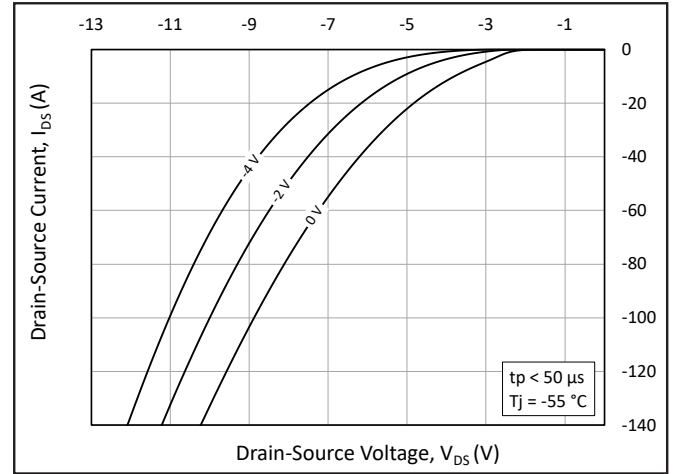


Figure 8. Body Diode Characteristic at -55 °C

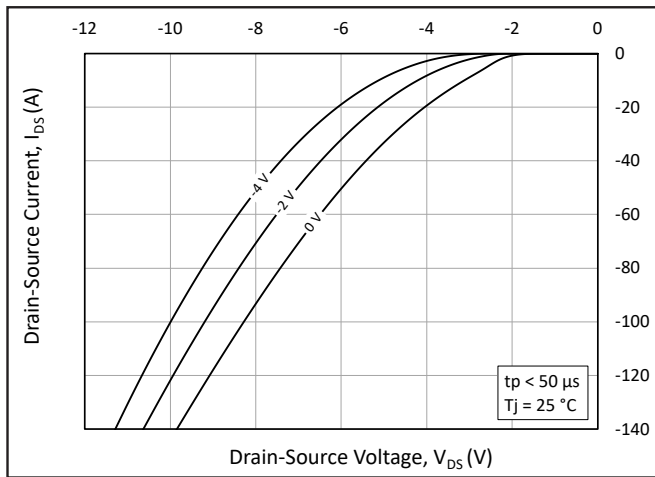


Figure 9. Body Diode Characteristic at 25 °C

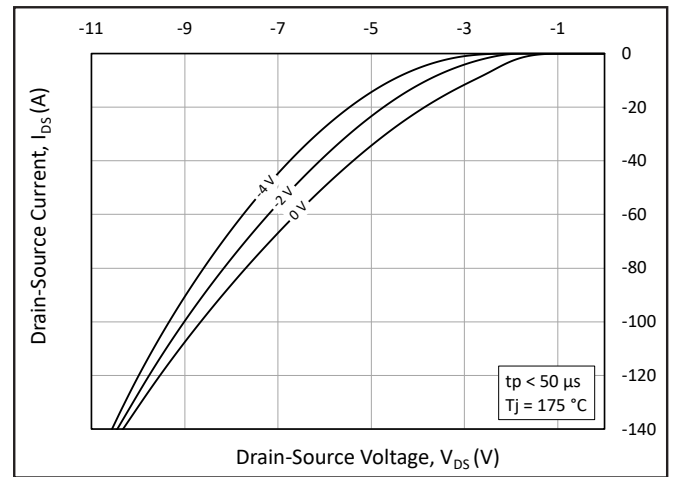


Figure 10. Body Diode Characteristic at 175 °C

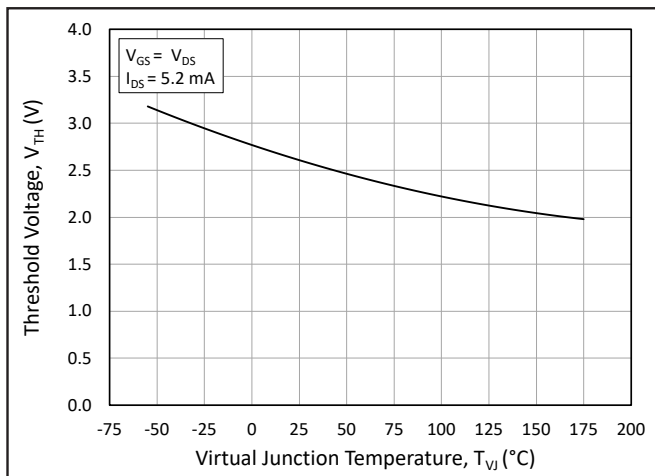


Figure 11. Threshold Voltage vs. Temperature

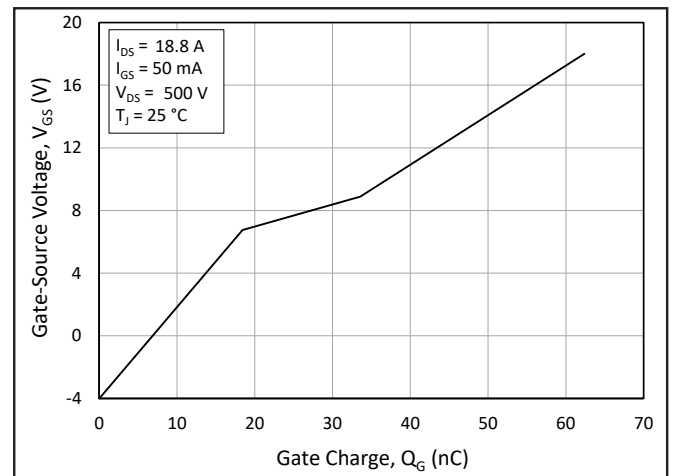


Figure 12. Gate Charge Characteristics

Typical Performance

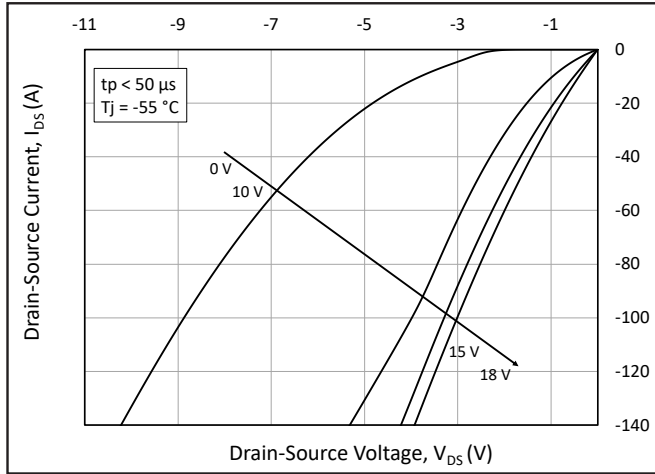


Figure 13. 3rd Quadrant Characteristic at -55°C

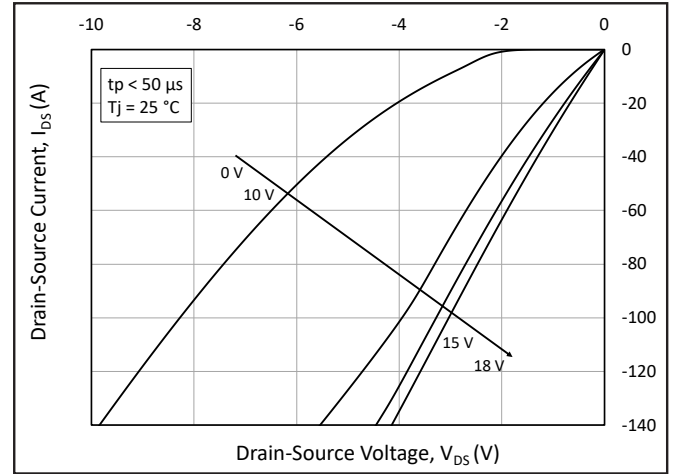


Figure 14. 3rd Quadrant Characteristic at 25°C

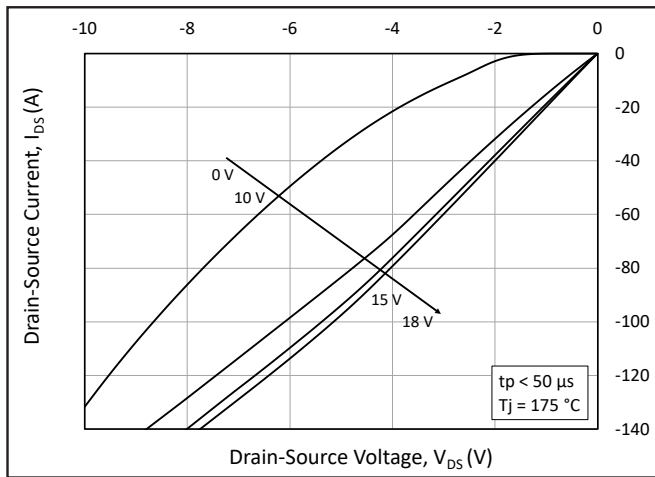


Figure 15. 3rd Quadrant Characteristic at 175°C

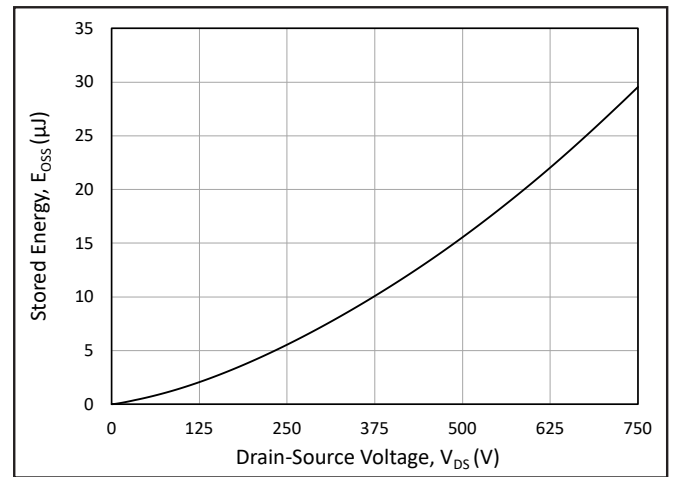


Figure 16. Output Capacitor Stored Energy

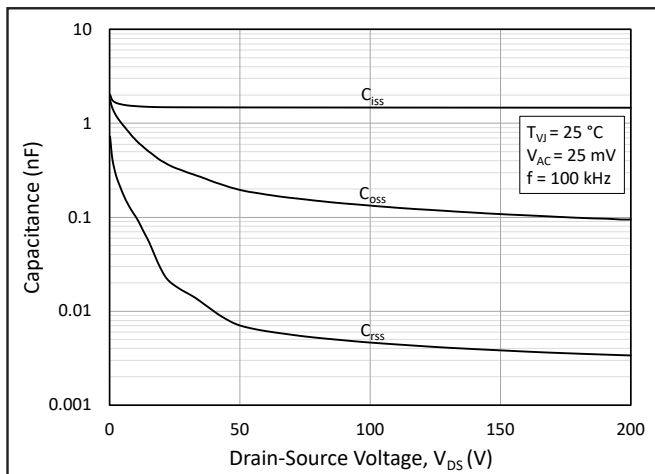


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

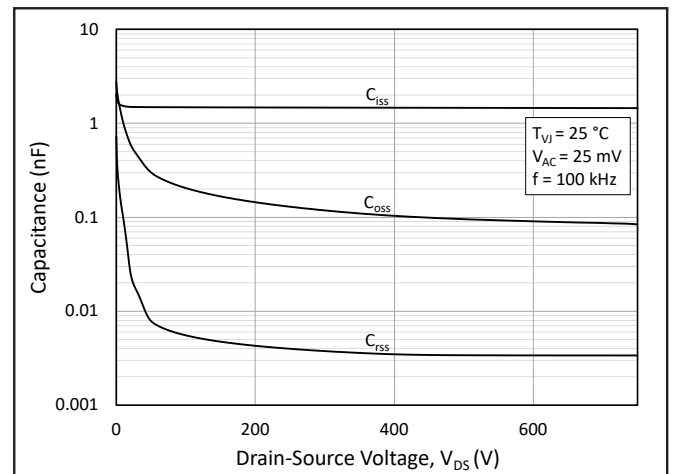


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 750 V)

Typical Performance

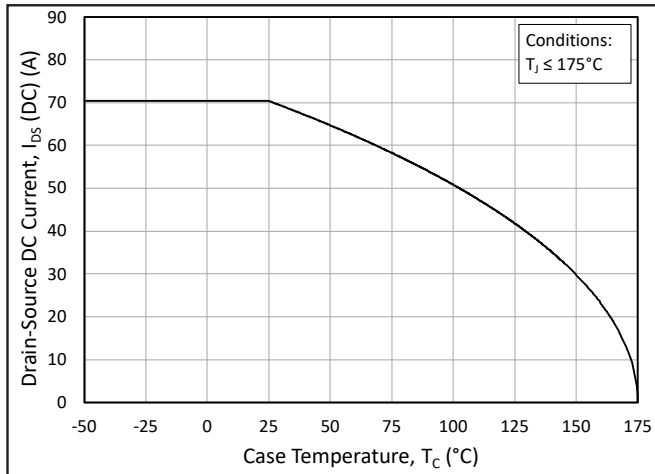


Figure 19. Continuous Drain Current Derating vs. Case Temperature

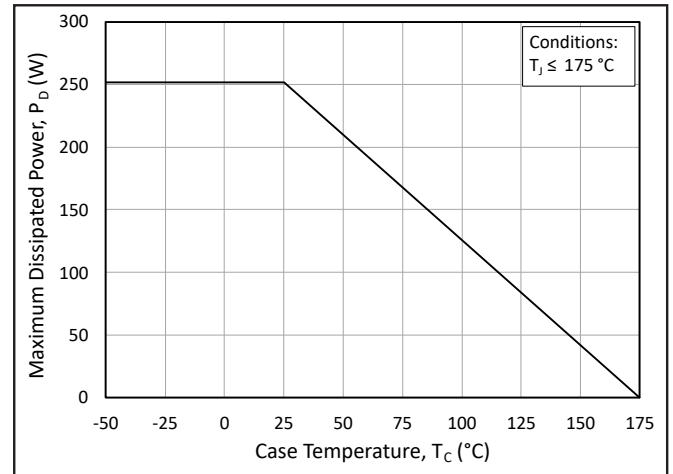


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

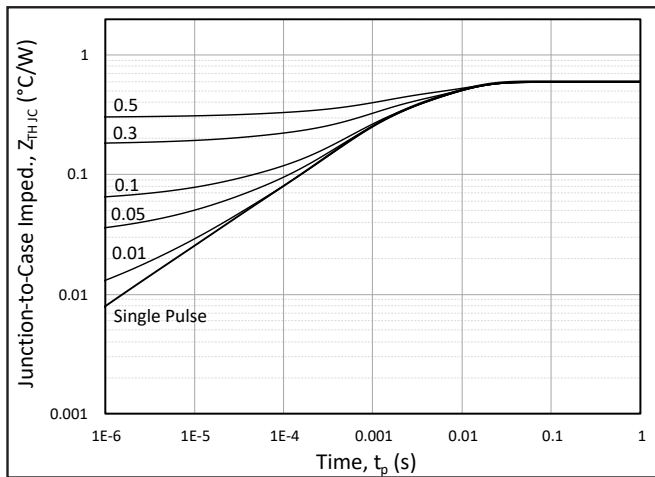


Figure 21. Transient Thermal Impedance (Junction - Case)

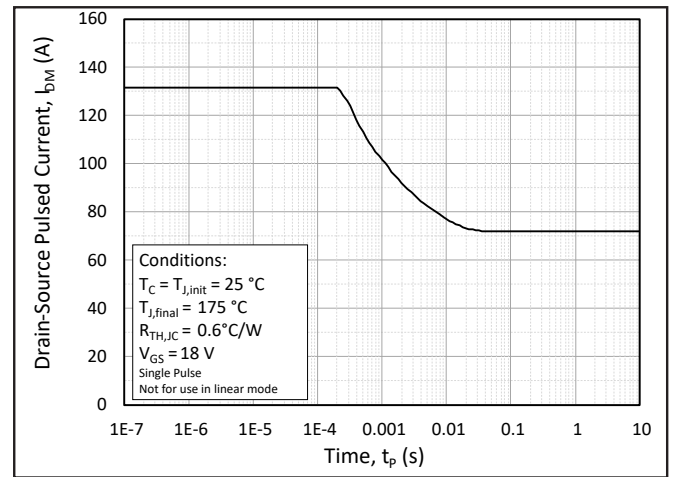


Figure 22. Pulse Current Safe Operating Area

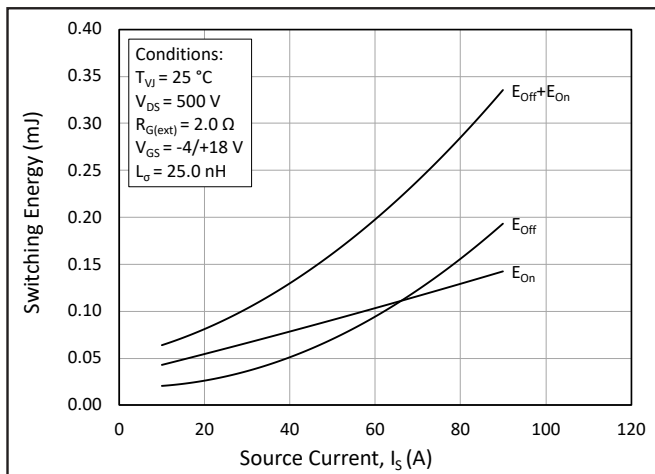


Figure 23. Clamped Inductive Switching Energy vs. Current

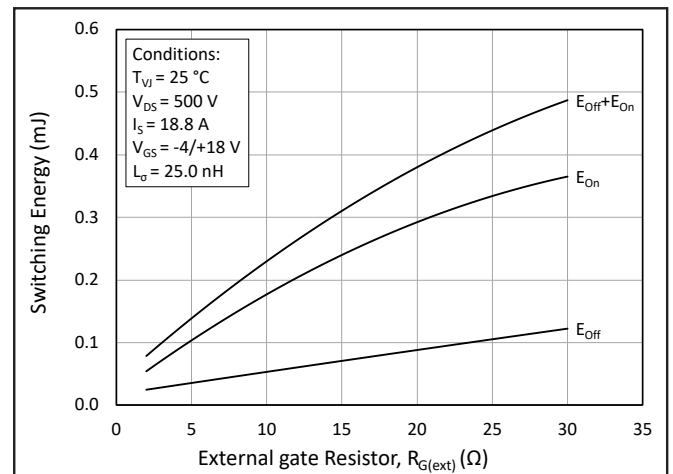


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

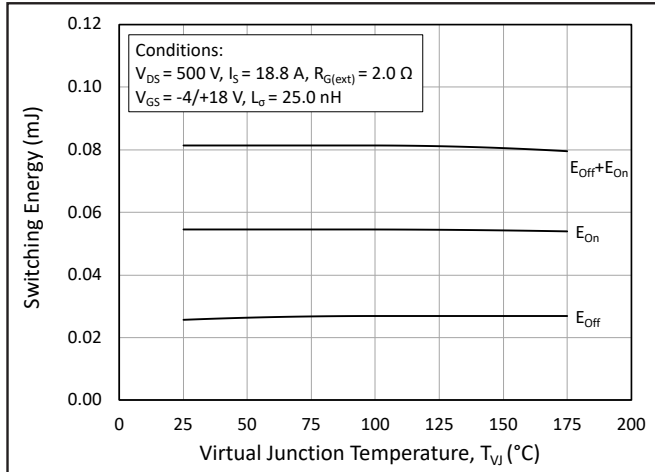


Figure 25. Clamped Inductive Switching Energy vs. Temperature

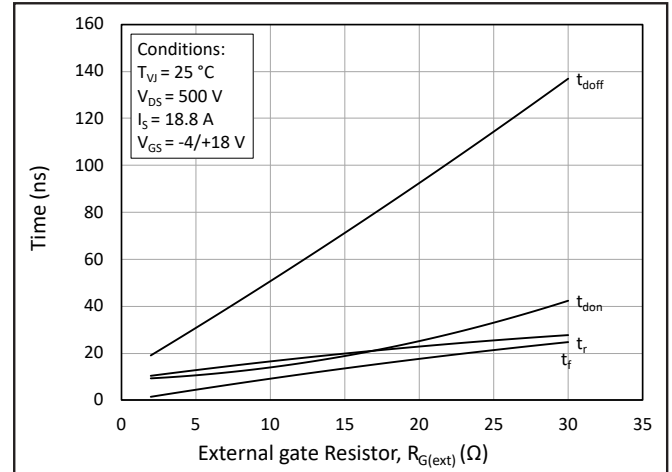


Figure 26. Switching Times vs. $R_{G(ext)}$

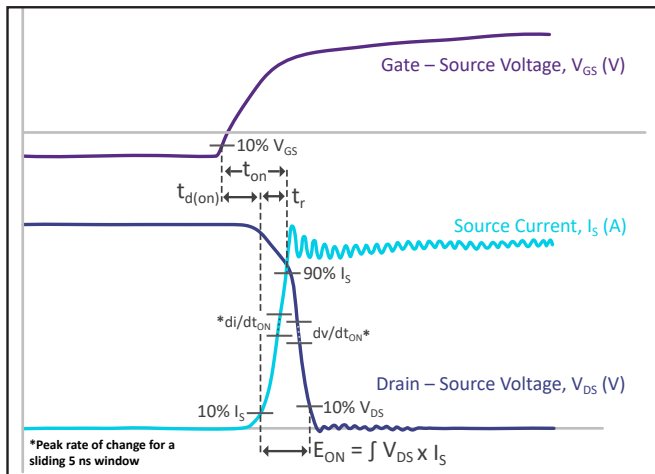


Figure 27. Turn On Switching Times Definition

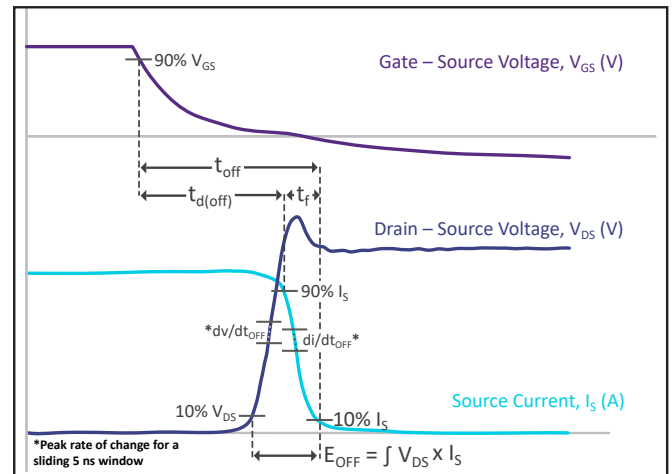


Figure 28. Turn Off Switching Times Definition

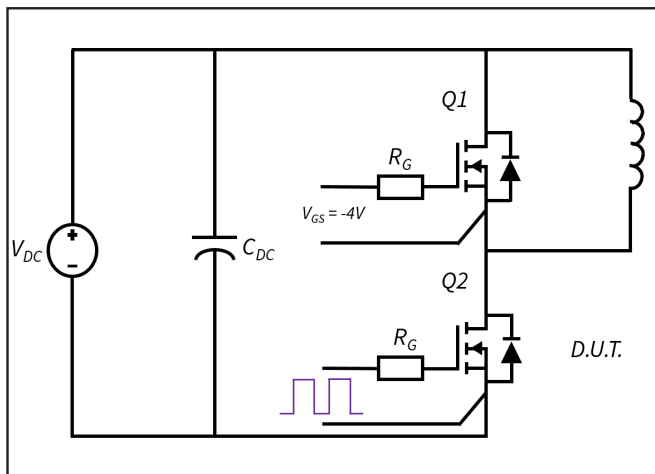


Figure 29. Clamped Inductive MOSFET Switching Waveform Test Circuit

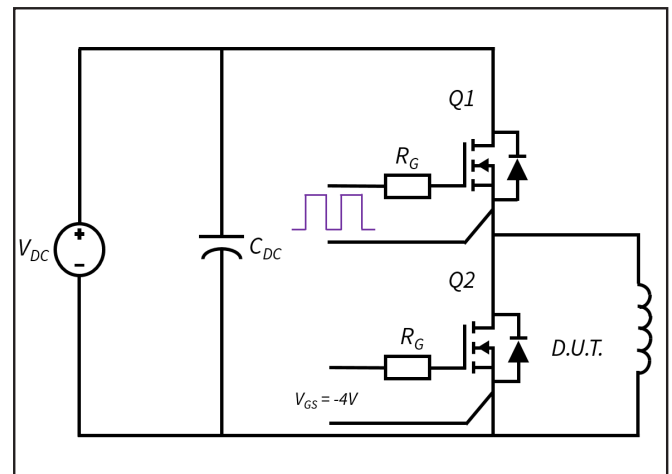
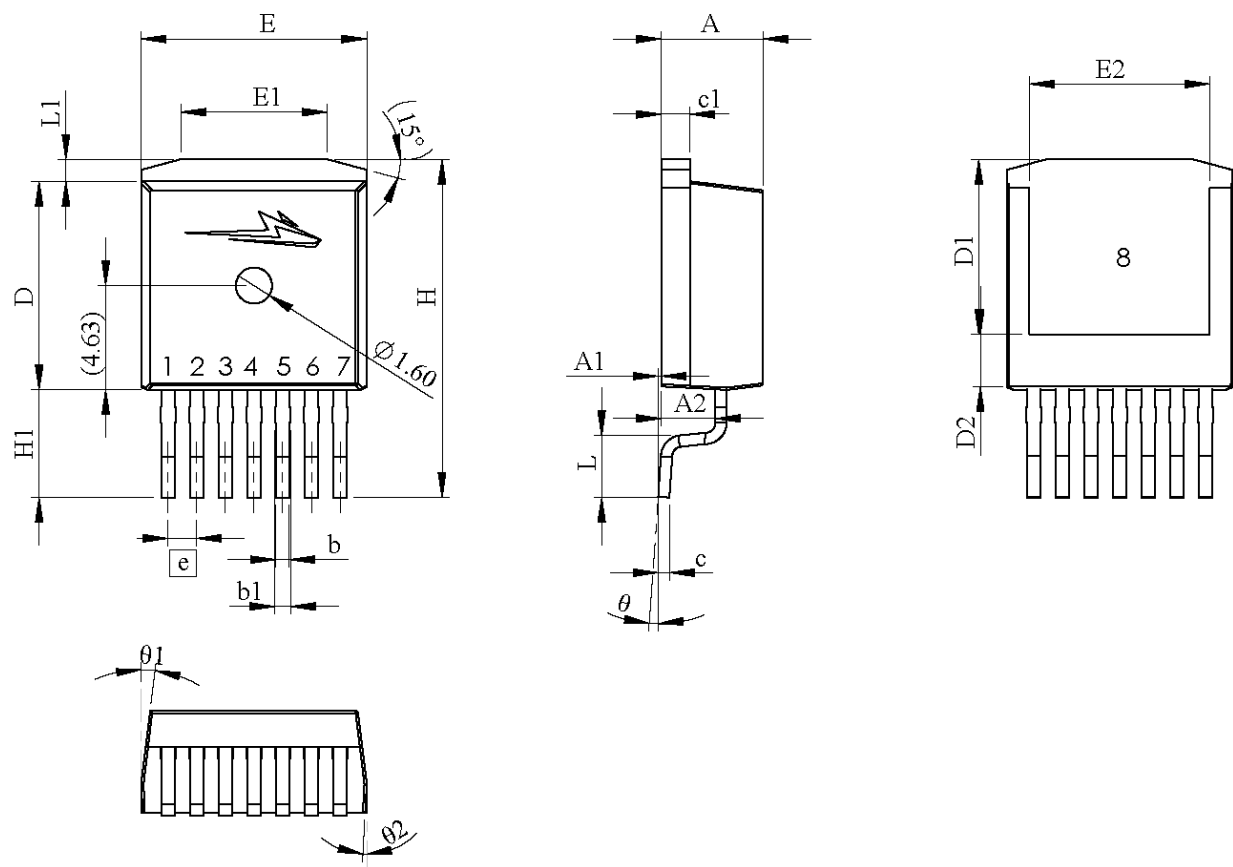


Figure 30. Clamped Inductive Body Diode Switching Waveform Test Circuit



Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	4.30	4.70
A1	0.00	0.25
A2	2.20	2.60
b	0.52	0.72
b1	0.60	0.80
c	0.42	0.62
c1	1.07	1.47
D	9.05	9.45
D1	7.58	7.98
D2	2.05	2.45
E	9.80	10.20
E1	6.30	6.97
E2	7.80	8.20
e	1.27 BSC	
H	14.87	15.27
H1	4.55	4.95
L	2.48	2.88
L1	0.87	1.27
θ	0°	8°
θ1	4°	10°
θ2	0°	6°

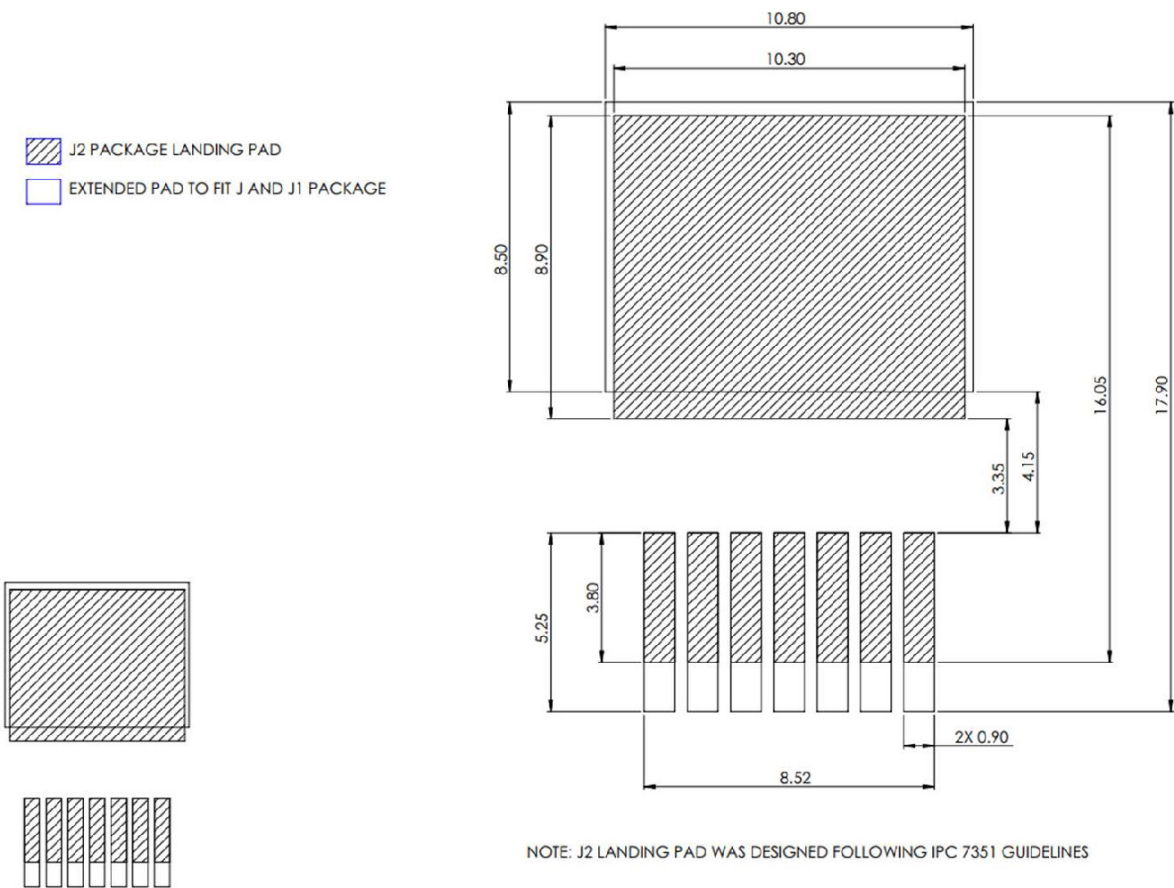
1	GATE
2	KELVIN
3	SOURCE
4	
5	
6	
7	DRAIN
8	

- NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
 2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
 3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
 4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

PRD 07409 Rev No. 01

Recommended Solder Pad Layout

All dimensions in mm





Revision History

Document Version	Date of Change	Description of Changes
1	July 2026	Initial Release

Appendix

Document Version	Description of Changes
A1	The following are recommendations for turning off the MOSFET with 0 V : • Measure the V_{gs} spike accurately using high -CMRR probes and low common mode noise measurements. • For the safe operation of the device, the voltage spike shall remain < 5 V for a time duration of < 40 ns.



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REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

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