C4MS035065L

Switching Optimized 650V 35mΩ Industrial Silicon Carbide Power MOSFET

Features

- Industry compatible drive voltage 15V...18V/-5V...0V
- Soft body diode with low Vds overshoot and ringing
- Low Rds(on) at high operating temperatures
- Improved device capacitance ratio (Ciss/Crss)
- High transient voltage robustness with improved lifetime
- Halogen free, RoHS compliant

Benefits

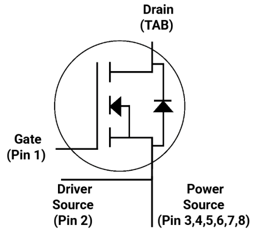
- Higher efficiency, lower switching losses and reduced EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system-level cooling requirements

Typical Applications

- Data Center Power Supplies
- EV Chargers
- Solar/ESS
- Motor Control
- Industrial Power Supplies
- High Voltage DC/DC Converters

Package

Drain Tab



Orderable Part Number	Package Type	Marking
C4MS035065L-TR	TOLL	C4MS035065L

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain–Source Voltage	V_{DS}			650	V		
Transient Drain–Source Voltage	V_{DS}			750	V	<100 h throughout lifetime	Note 1
Maximum Gate–Source Voltage	$V_{GS(max)}$	-10		+23	V		Note 2
DC Continuous Drain Current	I_D		70		A	V_{GS} = 18 V, T_C = 25 °C, T_J ≤175 °C	Note 3
			50		A	V_{GS} = 18 V, T_C = 100 °C, T_J ≤175 °C	
Pulsed Drain Current	I_{DM}			132	A	t_{Pmax} limited by T_{Jmax} V_{GS} = 18 V, T_C = 25 °C	
Power Dissipation	P_D		251		W	T_C = 25 °C, T_J = 175 °C	Note 4
Operating Junction and Storage Temperature	T_J, T_{stg}	-55		+175	°C		
Solder Temperature	T_L			260	°C	According to JEDEC J-STD-020	

Note (1): 100 hours of total accumulated lifetime of the product.

Note (2): When applying IPC-9592B or OCP M-CRPS derating standards, a maximum Gate-Source voltage (V_{GS}) of +25V is permissible.

Note (3): Current limit calculated by $I_{D(max)}=\sqrt{(P_D/R_{DS(typ)}(T_{J(max)},I_{D(max)}))}$

Note (4): $P_D=(T_J-T_C)/R_{th(JC,typ)}$

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Electrical Characteristics (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	3.9	V	V_{DS} = V_{GS}, I_D = 5.2 mA	Fig. 11
			2.0		V	V_{DS} = V_{GS}, I_D = 5.2 mA, T_J = 175 °C	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	µA	V_{DS} = 650 V, V_{GS} = 0 V	
I_{GSS}	Gate–Source Leakage Current		10	250	nA	V_{GS} = 18 V, V_{DS} = 0 V	
$V_{GS(op)}$	Recommended Turn on Gate–Source Voltage		15…18		V		Refer to PRD-09634
	Recommended Turn off Gate–Source Voltage		-5…0				
$R_{DS(on)}$	Drain-Source On–State Resistance		35	45.5	mΩ	V_{GS} = 18 V, I_D = 18.8 A	Fig. 4, 5, 6
			51.5			V_{GS} = 18 V, I_D = 18.8 A, T_J = 175 °C	
			42			V_{GS} = 15 V, I_D = 18.8 A	
g_{fs}	Transconductance		14		S	V_{DS} = 20 V, I_D = 18.8 A	Fig. 7
			13			V_{DS} = 20 V, I_D = 18.8 A, T_J = 175 °C	
$R_{DS(on)Tempco}$	On resistance temperature coefficient		1.47			V_{GS} = 18 V, I_D = 18.8 A	Note 5
C_{iss}	Input Capacitance		1469		pF	V_{GS} = 0 V, V_{DS} = 400 V f = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		102				
C_{rss}	Reverse Transfer Capacitance		3.4				
C_{iss}/C_{rss}	Capacitance Ratio		430				Note 6
E_{oss}	C_{oss} Stored Energy		11		µJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		121		pF	V_{GS} = 0 V, V_{DS} = 0...400 V	Note 7
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		194				
E_{on}	Turn-On Switching Energy (Body Diode FWD) T_J = 25 °C T_J = 175 °C		 33 34		µJ	V_{DS} = 400 V, V_{GS} = -4 V/18 V I_D = 18.8 A, $R_{G(ext)}$ = 2 Ω, $L_σ$ = 17 nH	Fig. 25, 27, 29
E_{off}	Turn-Off Switching Energy (Body Diode FWD) T_J = 25 °C T_J = 175 °C		 22 22				Fig. 25, 28, 29
$t_{d(on)}$	Turn-On Delay Time		9		ns	V_{DD} = 400 V, V_{GS} = -4 V/18 V I_D = 18.8 A, $R_{G(ext)}$ = 2 Ω, $L_σ$ = 17 nH Inductive load	Fig. 26, 27, 28, 29
t_r	Rise Time		3				
$t_{d(off)}$	Turn-Off Delay Time		21				
t_f	Fall Time		10				
$R_{G(int)}$	Internal Gate Resistance		2.3		Ω	f = 1 MHz	
Q_{gs}	Gate to Source Charge		18		nC	V_{DS} = 400 V, V_{GS} = -4 V/18 V I_D = 18.8 A Per IEC60747-8-4	Fig. 12
Q_{gd}	Gate to Drain Charge		15				
Q_g	Total Gate Charge		62				

Note (5): $R_{DS(on)Tempco}$ refers to $R_{DS(on)}$ at 175 C/ $R_{DS(on)}$ at 25C, C4MS 650V product family value

Note (6): Capacitance ratio is a FOM for Partial turn-on immunity PRD-06933, C4MS 650V product family value

Note (7): $C_{o(er)}$, a lumped capacitance that gives the same stored energy as C_{oss} while Vds is rising from 0 to 400 V
$C_{o(tr)}$, a lumped capacitance that gives the same charging time as C_{oss} while Vds is rising from 0 to 400 V

Reverse Diode Characteristics (T$_C$ = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	V_{GS} = -4 V, I_{SD} = 9.4 A	Fig. 8, 9, 10
		4.5		V	V_{GS} = -4 V, I_{SD} = 9.4 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current	38		A	V_{GS} = -4 V	
I_{SM}	Diode Pulse Current		132	A	V_{GS} = -4 V, pulse width t_p limited by T_{Jmax}	
t_{rr}	Reverse Recovery Time	8.2		ns	V_{SD} = 400 V, V_{GS} = -4 V, T_J = 175 °C I_S = 18.8 A, di_F/dt = 9.3 A/ns	Fig. 30
Q_{rr}	Reverse Recovery Charge	235		nC		
I_{RRM}	Peak Reverse Recovery Current	48		A		
E_{RR}	Reverse recovery Energy T_J = 25 °C T_J = 175 °C	 87 98		µJ	V_{DS} = 400 V, V_{GS} = -4 V/18 V I_D = 18.8 A, $R_{G(on)}$ = 2 Ω, $L_σ$ = 17 nH	

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{θJC}$	Thermal Resistance from Junction to Case	0.60		°C/W		

Typical Performance

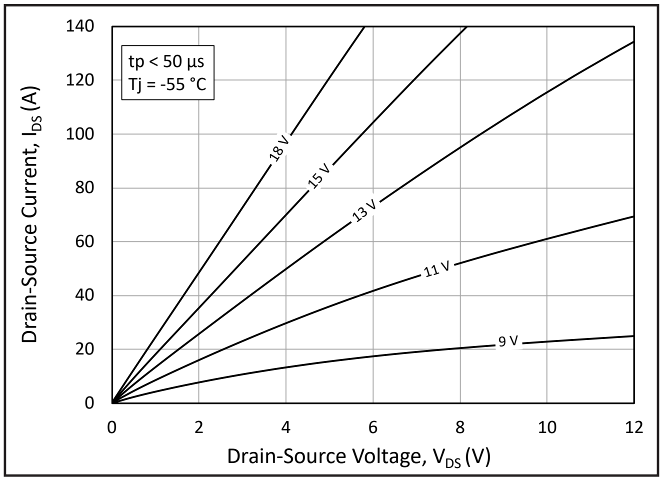


Figure 1. Output Characteristics T_J = -55°C

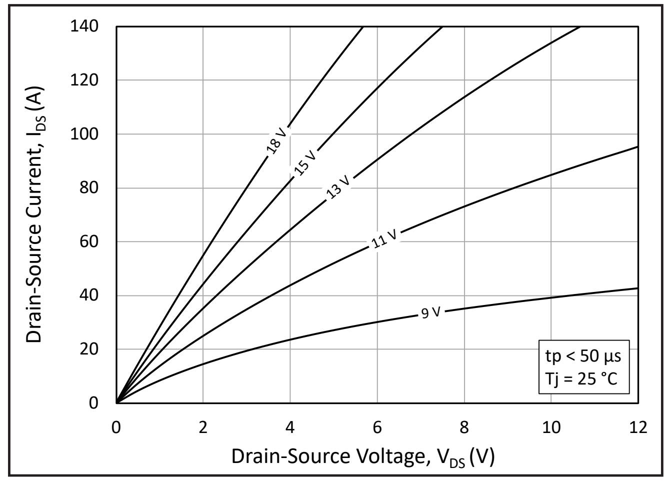


Figure 2. Output Characteristics T_J = 25°C

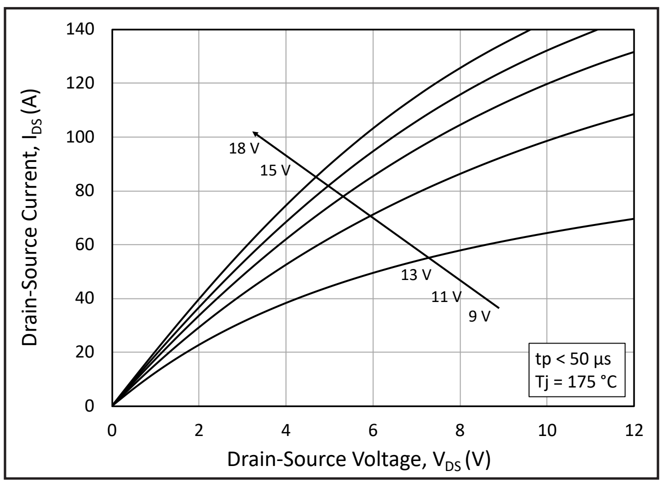


Figure 3. Output Characteristics T_J = 175°C

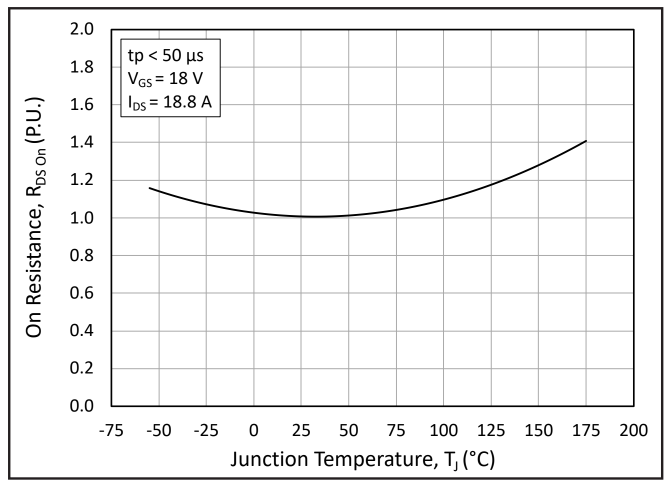


Figure 4. Normalized On-Resistance vs. Temperature

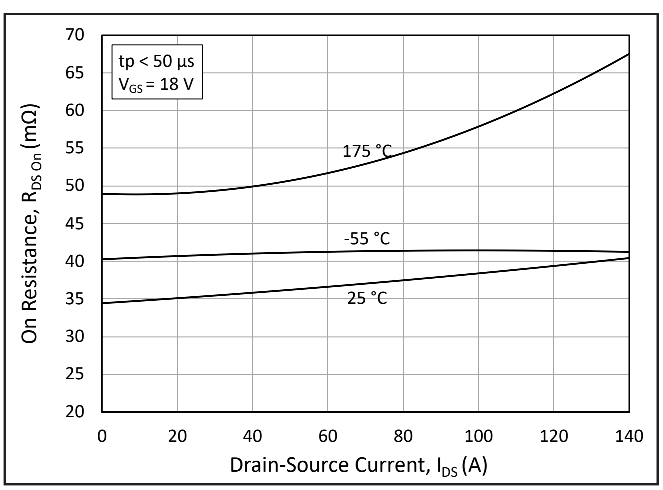


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

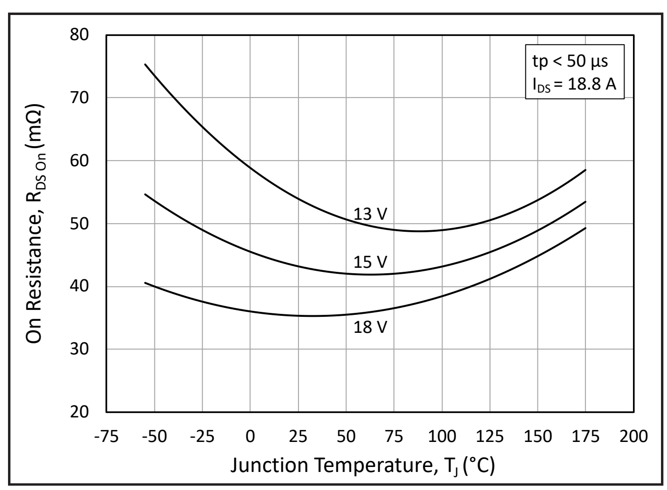


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

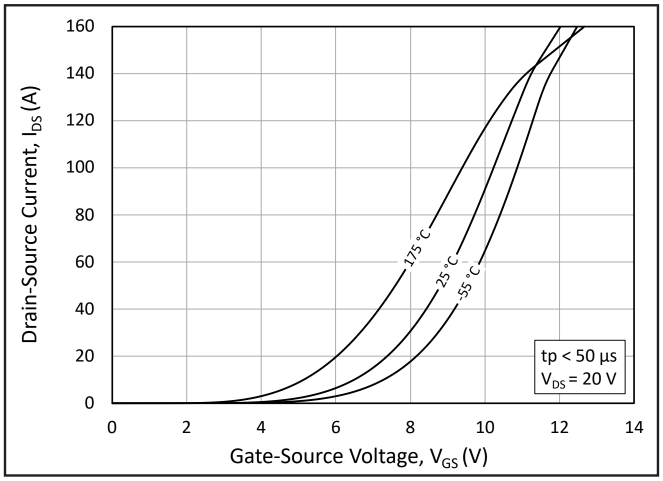


Figure 7. Transfer Characteristic for Various Junction Temperatures

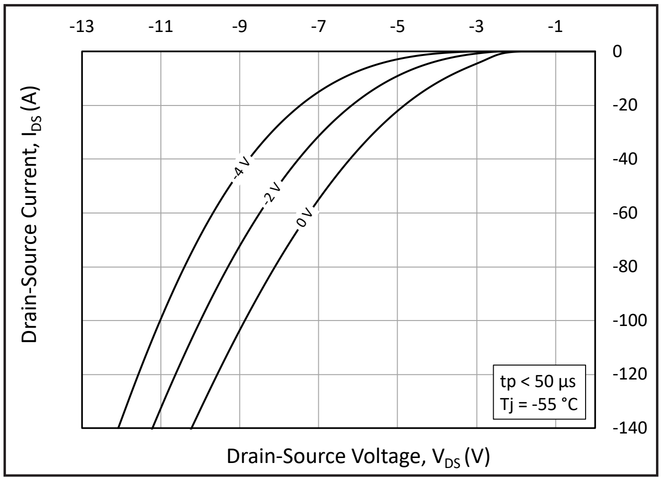


Figure 8. Body Diode Characteristic at -55°C

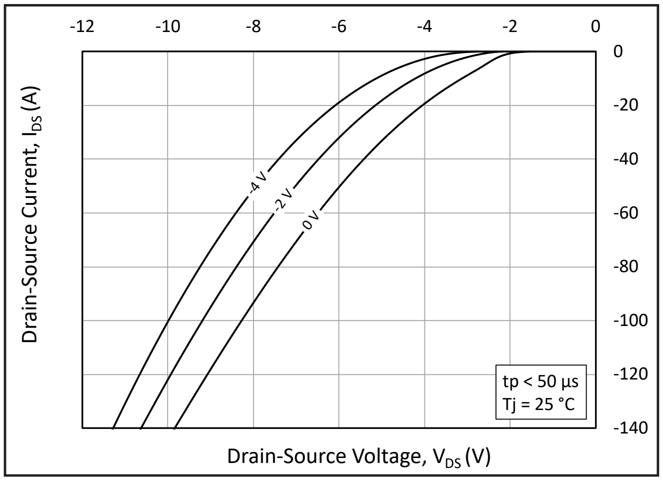


Figure 9. Body Diode Characteristic at 25°C

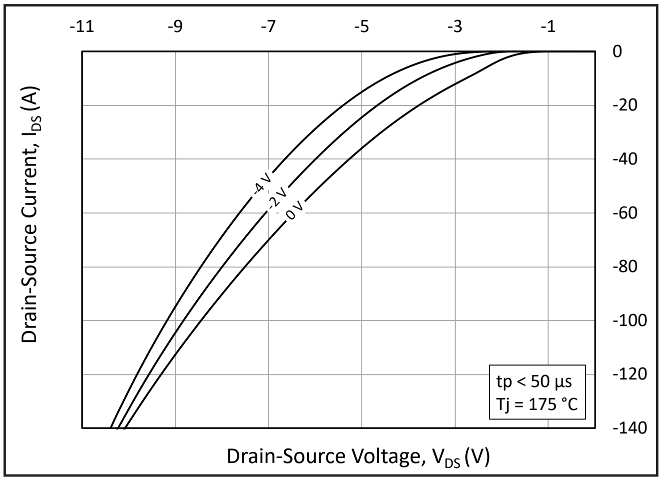


Figure 10. Body Diode Characteristic at 175°C

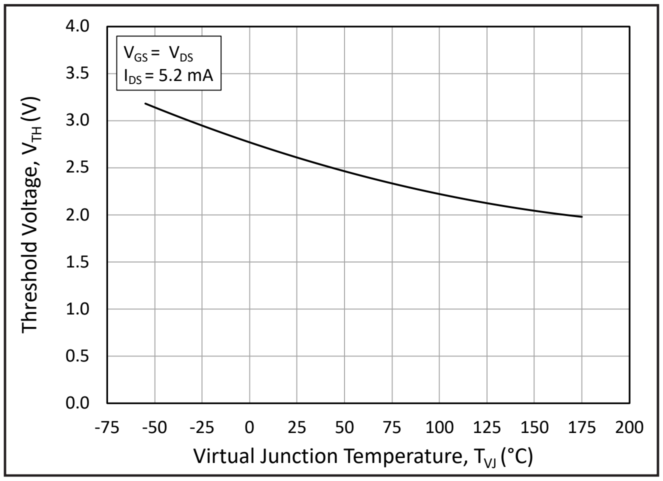


Figure 11. Threshold Voltage vs. Temperature

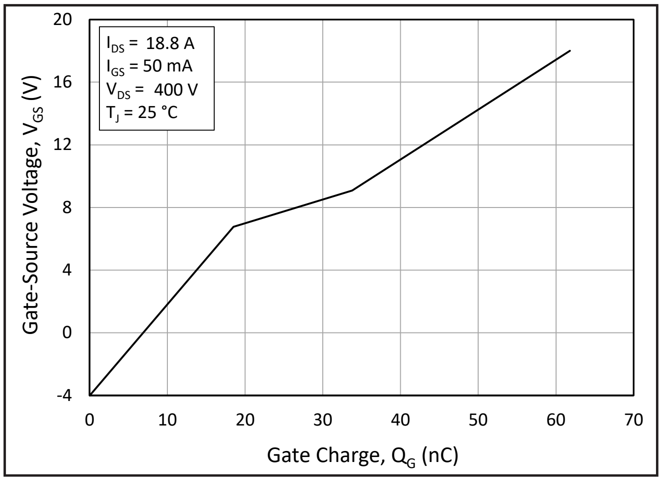


Figure 12. Gate Charge Characteristics

Typical Performance

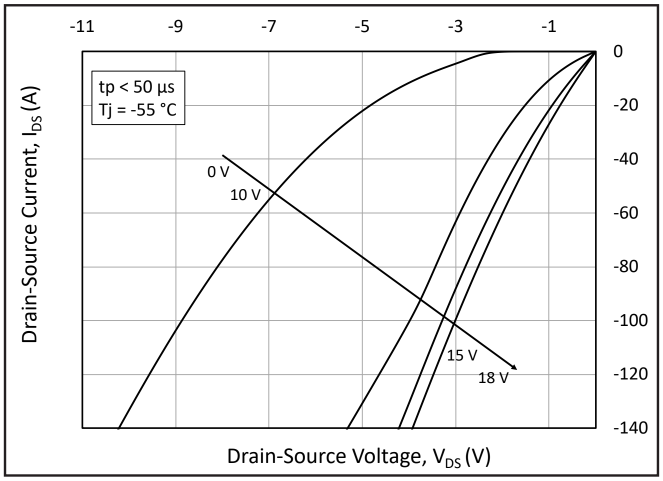


Figure 13. 3rd Quadrant Characteristic at -55°C

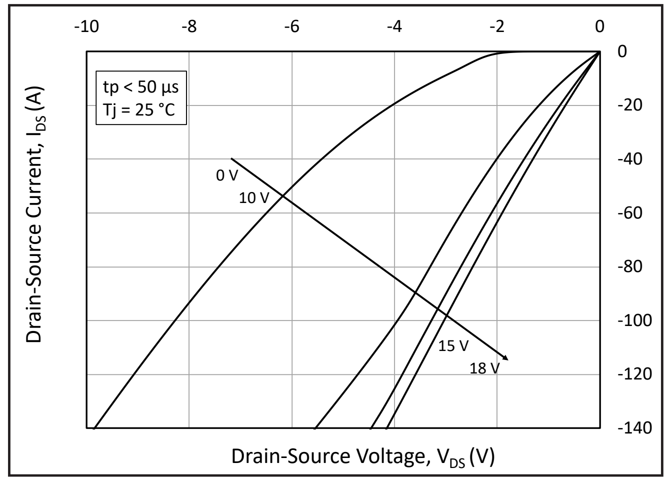


Figure 14. 3rd Quadrant Characteristic at 25°C

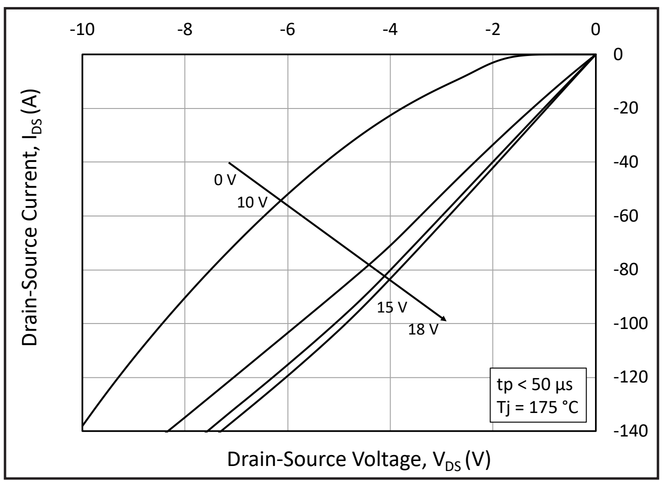


Figure 15. 3rd Quadrant Characteristic at 175°C

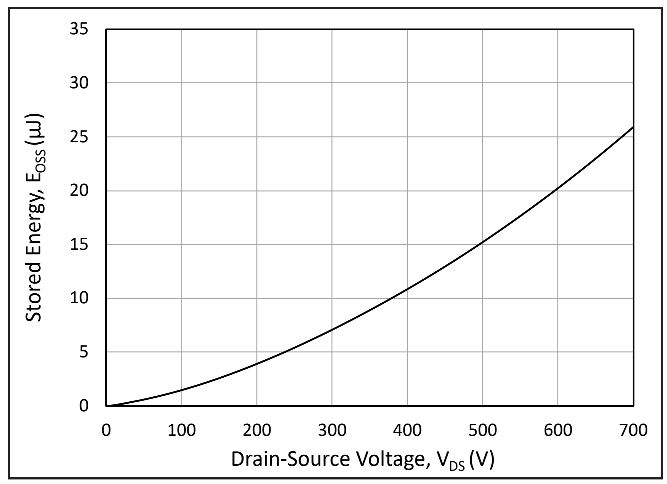


Figure 16. Output Capacitor Stored Energy

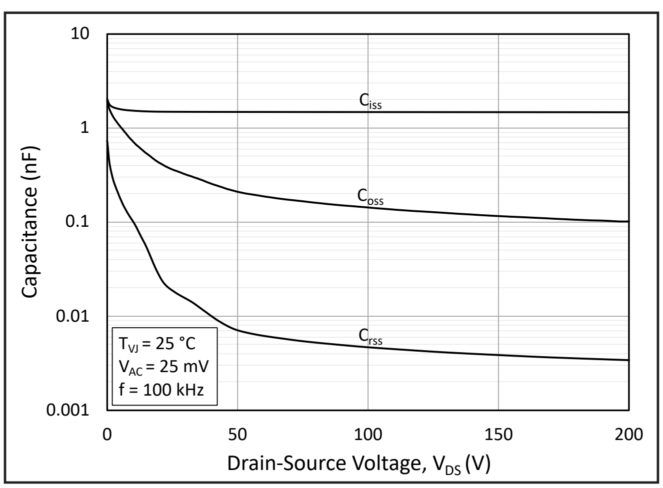


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

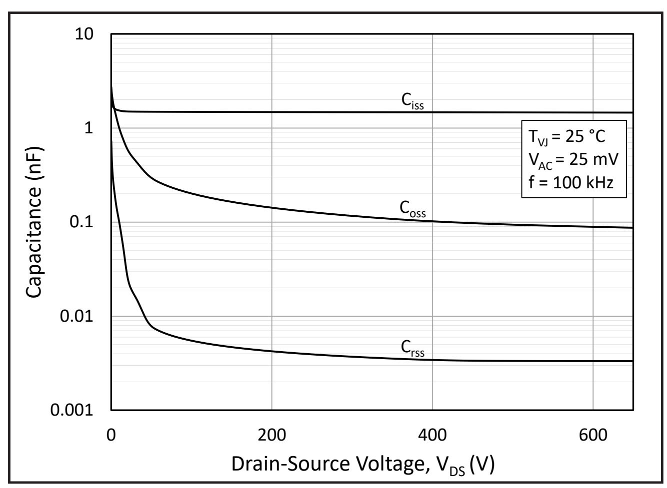


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650 V)

Typical Performance

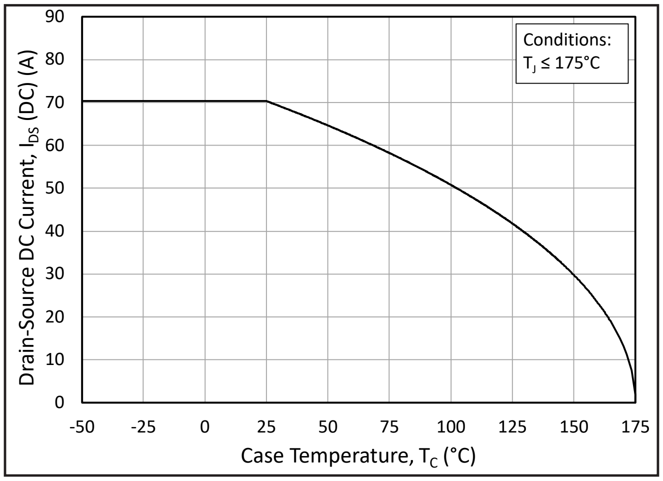


Figure 19. Continuous Drain Current Derating vs. Case Temperature

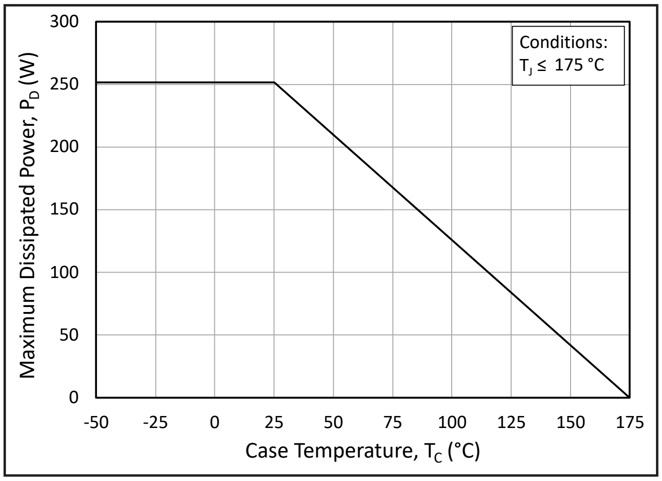


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

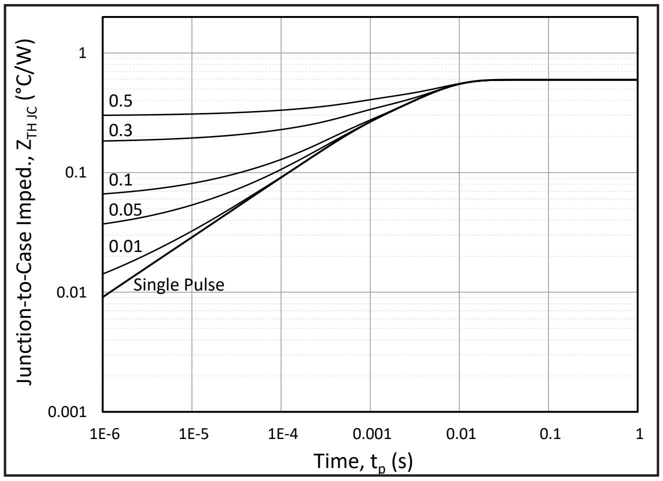


Figure 21. Transient Thermal Impedance (Junction - Case)

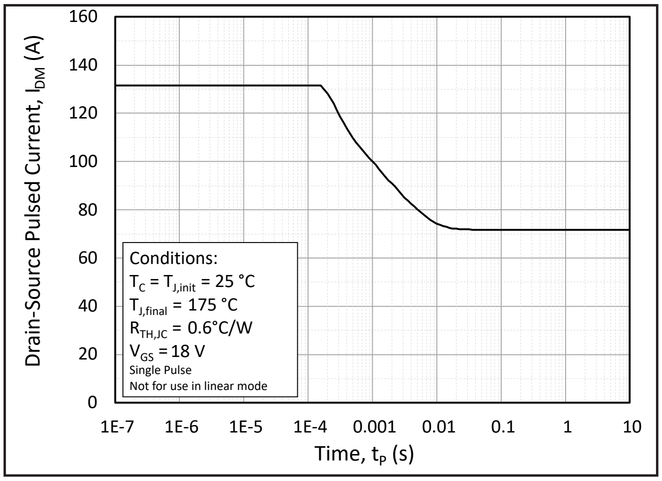


Figure 22. Pulse Current Safe Operating Area

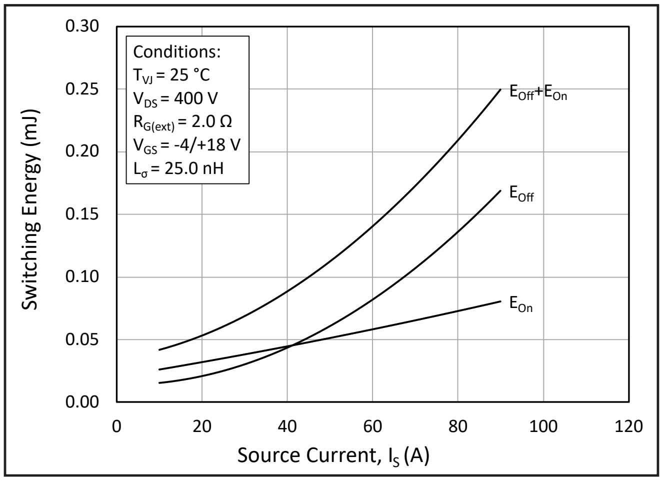


Figure 23. Clamped Inductive Switching Energy vs. Current

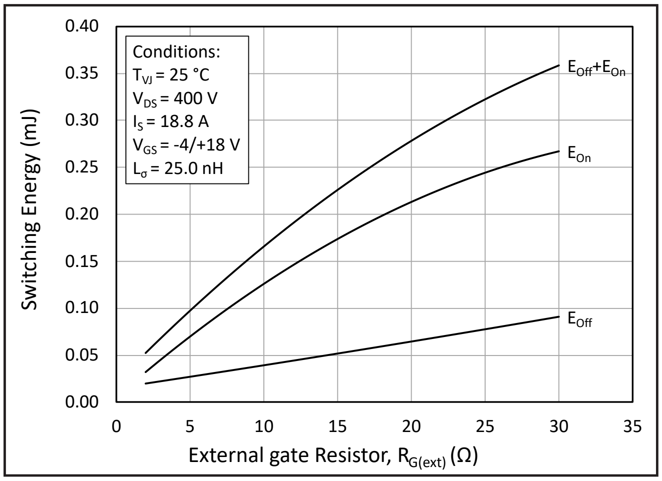


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

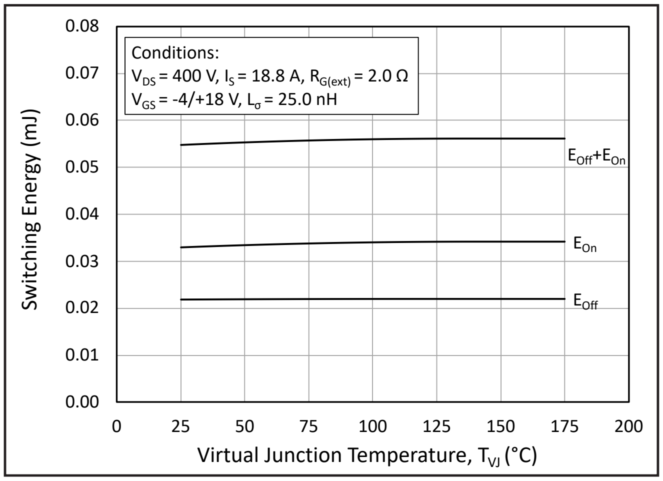


Figure 25. Clamped Inductive Switching Energy vs. Temperature

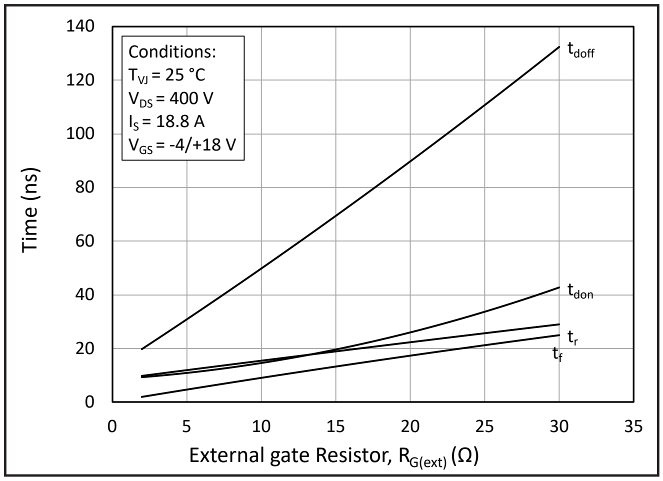


Figure 26. Switching Times vs. $R_{G(ext)}$

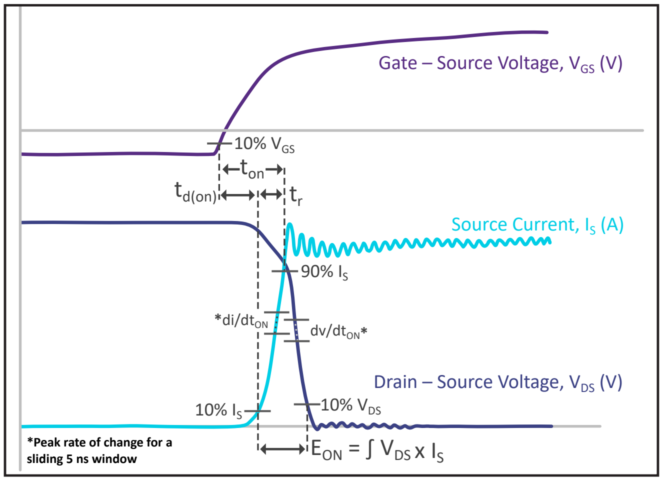


Figure 27. Turn On Switching Times Definition

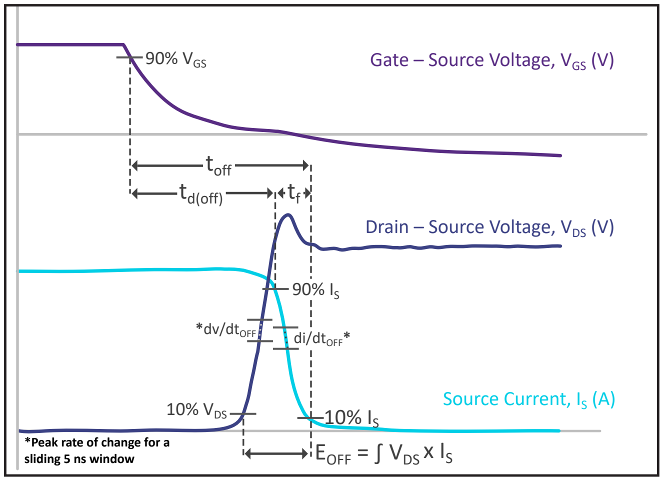


Figure 28. Turn Off Switching Times Definition

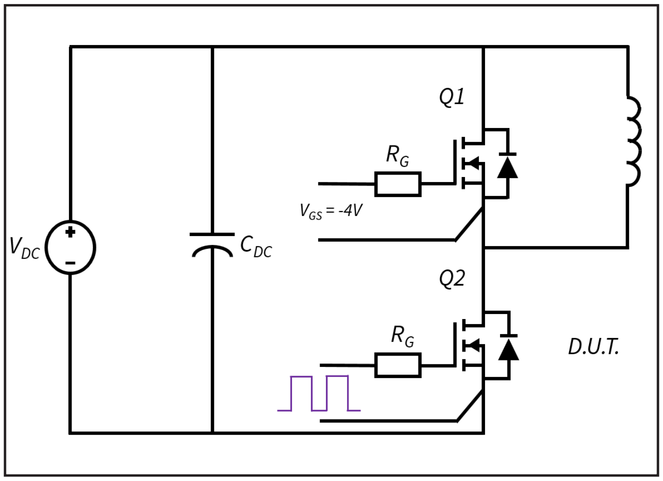


Figure 29. Clamped Inductive MOSFET Switching Waveform Test Circuit

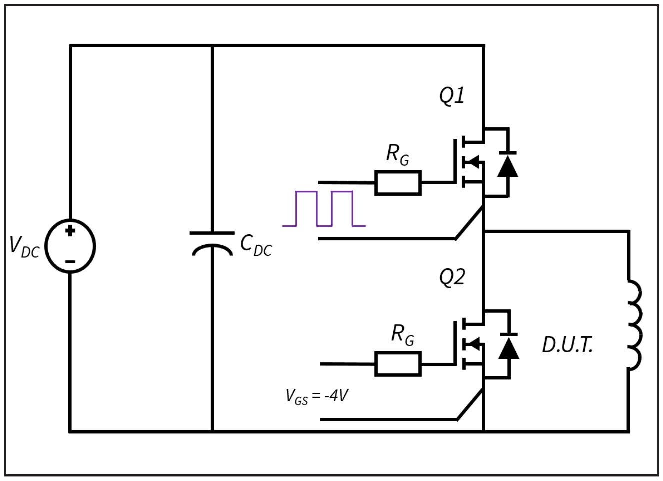
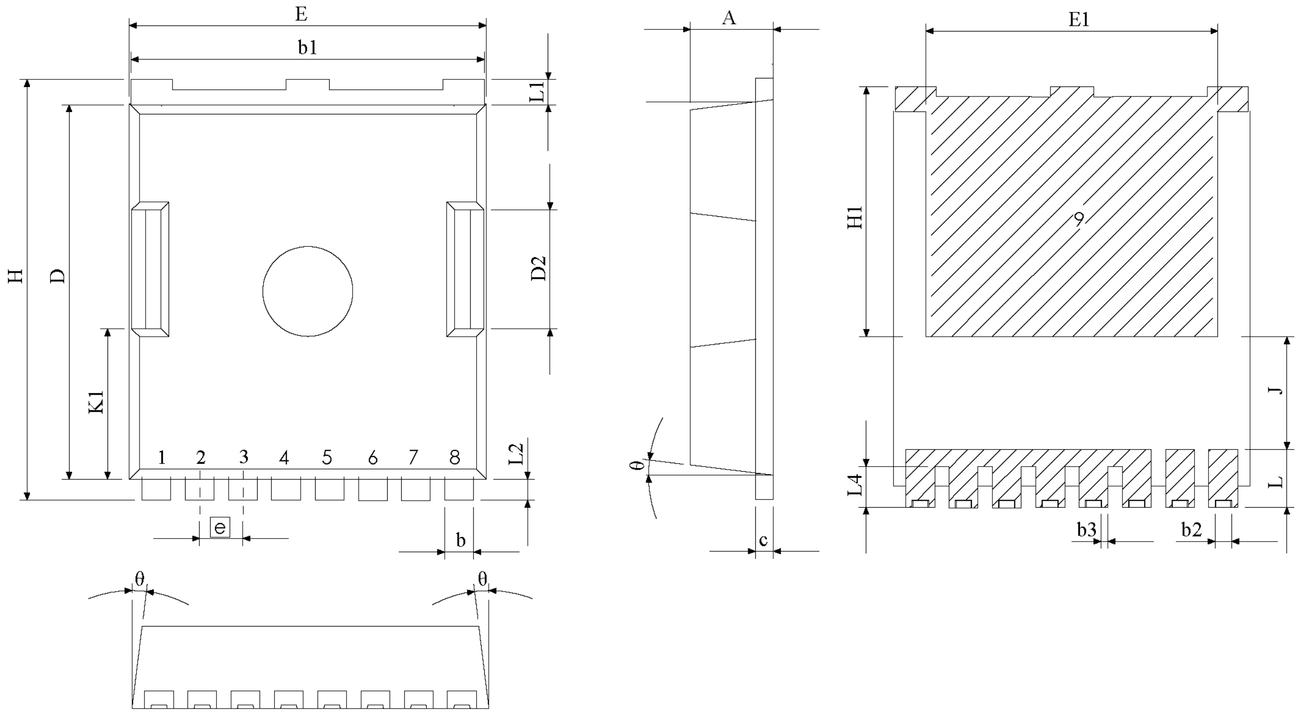


Figure 30. Clamped Inductive Body Diode Switching Waveform Test Circuit

Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
b3	0.07	0.27
c	0.40	0.60
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.10
E1	7.90	8.30
e	1.20 BSC	
H	11.48	11.88
H1	6.75	7.15
J	3.00	3.30
K1	3.98	4.38
L	1.40	1.80
L1	0.60	0.80
L2	0.50	0.70
L4	1.00	1.30
θ	4°	10°

1	GATE
2	KELVIN
3-8	SOURCE
9	DRAIN

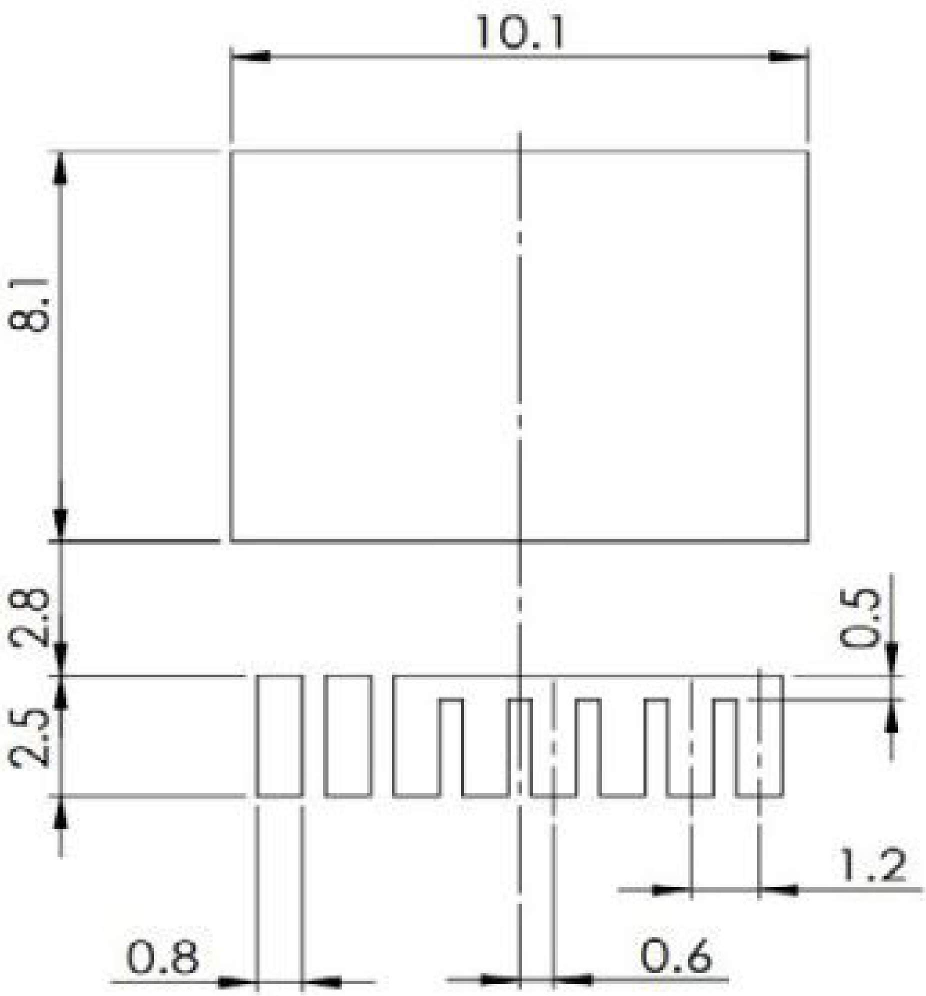
NOTE

1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

PRD-06655 Rev No. 02

Recommended Solder Pad Layout

All dimensions in mm



Revision History

Document Version	Date of Change	Description of Changes
1	June 2026	Initial Release

Appendix

Document Version	Description of Changes
A1	The following are recommendations for turning off the MOSFET with 0 V : • Measure the V_{GS} spike accurately using high -CMRR probes and low common mode noise measurements. • For the safe operation of the device, the voltage spike shall remain < 5 V for a time duration of < 40 ns.

Notes & Disclaimers

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The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Documentation sections of www.wolfspeed.com.

REACh Compliance

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

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