C4MS025075QT

Switching Optimized 750V 25mΩ Silicon Carbide Power MOSFET

Features

- Industry compatible drive voltage 15V...18V/-4V...0V
- Soft body diode with low Vds overshoot and ringing
- Low Rds(on) at high operating temperatures
- Improved device capacitance ratio (Ciss/Crss)
- High transient voltage robustness with improved lifetime
- Halogen free, RoHS compliant

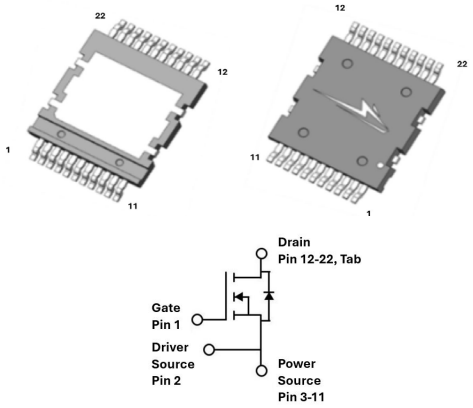
Benefits

- Higher efficiency with lower switching losses and EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system level cooling requirements

Typical Applications

- EV Chargers
- Solar/ESS
- Motor Control
- Industrial Power Supplies
- High Voltage DC/DC Converters

Package



Orderable Part number	Package type	Marking
C4MS025075QT-TR	TSC(QT)	C4MS025075QT

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			750	V		
Transient Drain - Source Voltage				TBD		<100hrs of lifetime	Note 1
Maximum Gate - Source Voltage (Transient)	$V_{GS(max)}$	-10		+23		Transient	Note 2
Operational Turn-On Gate - Source Voltage	$V_{GS(op)}$		+15...+18				Refer to AN PRD-04814
Operational Turn-Off Gate - Source Voltage			-4...0				
DC Continuous Drain Current	I_D		97		A	V_{GS} = 18 V, T_C = 25 °C, T_J ≤175 °C	Note 3
			68			V_{GS} = 18 V, T_C = 100 °C, T_J ≤175 °C	
Pulsed Drain Current	I_{DM}			186		t_{Pmax} limited by T_{jmax} V_{GS} = 18V, T_C = 25 °C	
Power Dissipation	P_D		349		W	T_C = 25°C, T_J = 175 °C	
Operating Junction and Storage Temperature	T_J	-40		+175	°C		Note 4
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note (1): 100 hours of total accumulated lifetime of the product.
Note (2): When applying IPC-9592B derating it is permissible to use Maximum Vgs of +25V
Note (3): Current limit calculated by $I_{D(max)}=\sqrt{(P_D/R_{DS(typ)}/(T_{J(max)},I_{D(max)}))}$
Note(4): $P_D=(T_j-T_c)/R_{th(JC,typ)}$

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Electrical Characteristics (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	750			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2.1	2.6	3.9	V	V_{DS} = V_{GS}, I_D = 7.3 mA	Fig. 11
			2.3		V	V_{DS} = V_{GS}, I_D = 7.3 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	µA	V_{DS} = 750 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 18 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		25	34	mΩ	V_{GS} = 18 V, I_D = 26.7 A	Fig. 4, 5, 6
			37			V_{GS} = 18 V, I_D = 26.7 A, T_J = 175ºC	
			32			V_{GS} = 15 V, I_D = 26.7 A	
g_{fs}	Transconductance		20.1		S	V_{DS} = 20 V, I_D = 26.7 A, T_J = 175ºC	Fig. 7
			20.1			V_{DS} = 20 V, I_D = 26.7 A, T_J = 25ºC	
$R_{DS(on)Tempco}$	On resistance temperature coefficient		1.47			V_{GS} = 18 V, I_D = 26.7 A	Note 4
C_{iss}	Input Capacitance		2328		pF	V_{GS} = 0 V, V_{DS} = 500 V f = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		123				
C_{rss}	Reverse Transfer Capacitance		5				
C_{iss}/C_{rss}	Capacitance Ratio		498				Note 5
E_{oss}	C_{oss} Stored Energy		20		µJ		Fig. 16
$R_{G(int)}$	Internal Gate Resistance		2.9		Ω	f = 1 MHz	
Q_{gs}	Gate to Source Charge		25		nC	V_{DS} = 500 V, V_{GS} = -4 V/18 V I_D = 26.7 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		28				
Q_g	Total Gate Charge		92				

Note (4): $R_{DS(on)Tempco}$ refers to $R_{DS(on)}$ at 25 C/ $R_{DS(on)}$ at 175C
Note (5): Capacitance ratio is a FOM for Partial turn-on immunity PRD-06933, this is a family wide value*

Reverse Diode Characteristics (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	V_{GS} = -4 V, I_{SD} = 13.4 A, T_J = 25 °C	Fig. 8, 9, 10
		4.5		V	V_{GS} = -4 V, I_{SD} = 13.4 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current	67		A	V_{GS} = -4 V, T_C = 25°C	
I_{SM}	Diode Pulse Current		186	A	V_{GS} = -4 V, pulse width t_p limited by T_{jmax} max	

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.43	°C/W		

Typical Performance

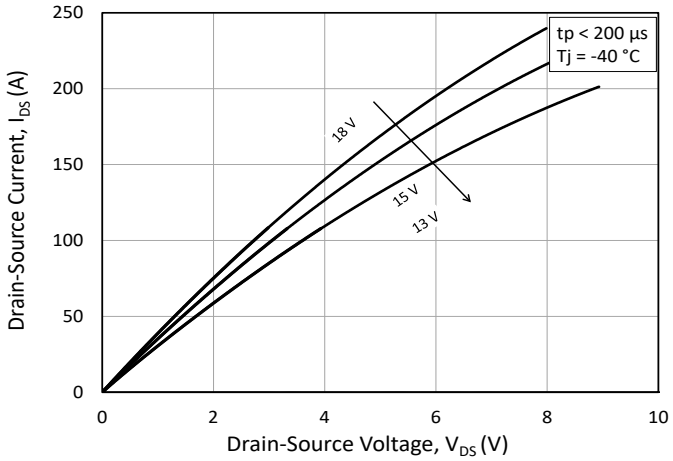


Figure 1. Output Characteristics T_J = -40ºC

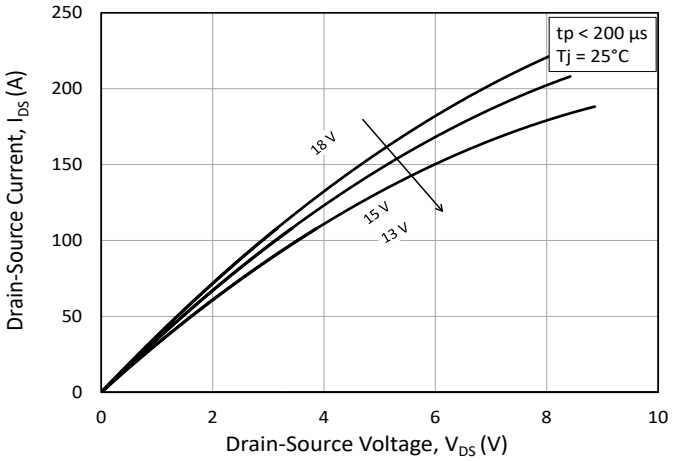


Figure 2. Output Characteristics T_J = 25ºC

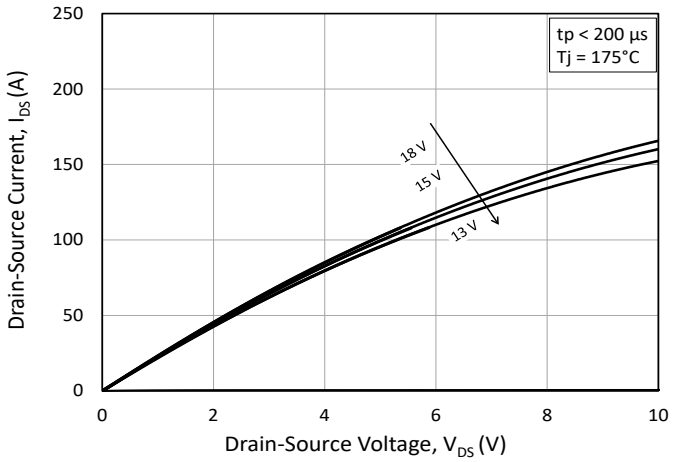


Figure 3. Output Characteristics T_J = 175ºC

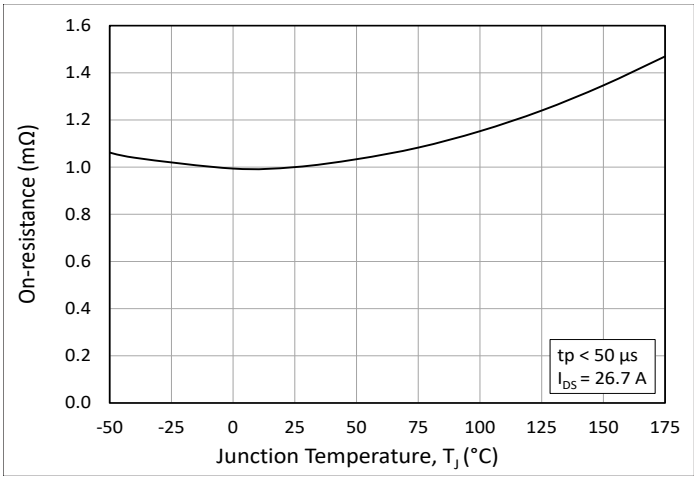


Figure 4. Normalized On-Resistance vs. Temperature

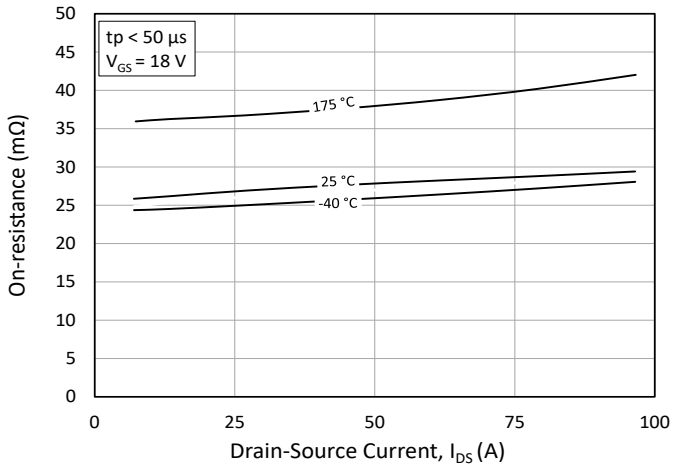


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

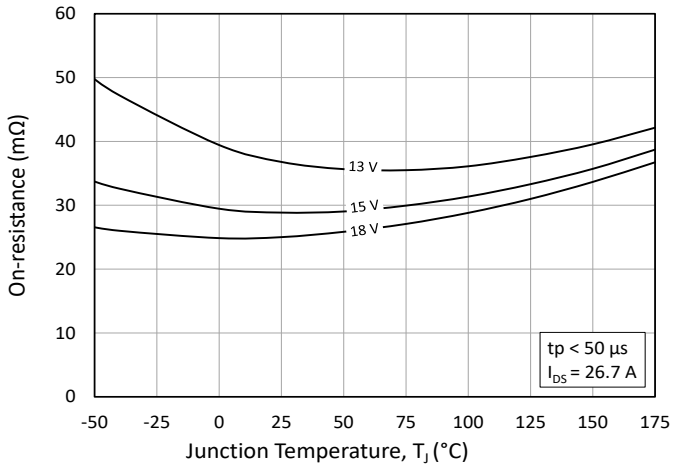


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

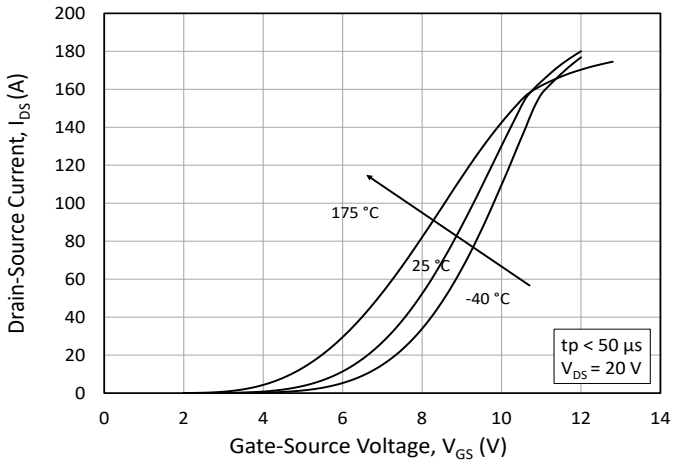


Figure 7. Transfer Characteristic for Various Junction Temperatures

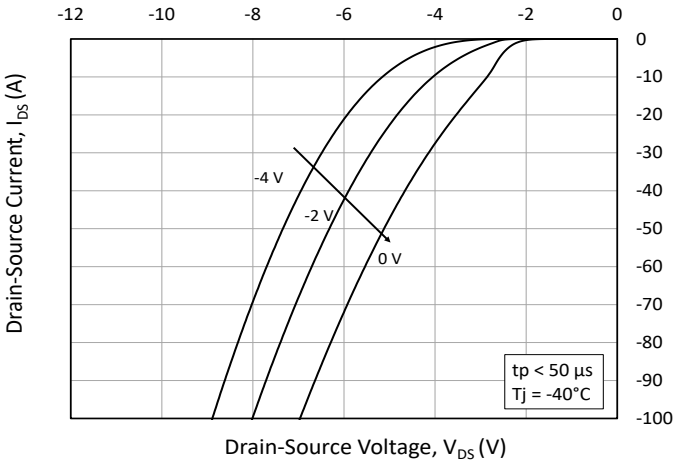


Figure 8. Body Diode Characteristic at -40ºC

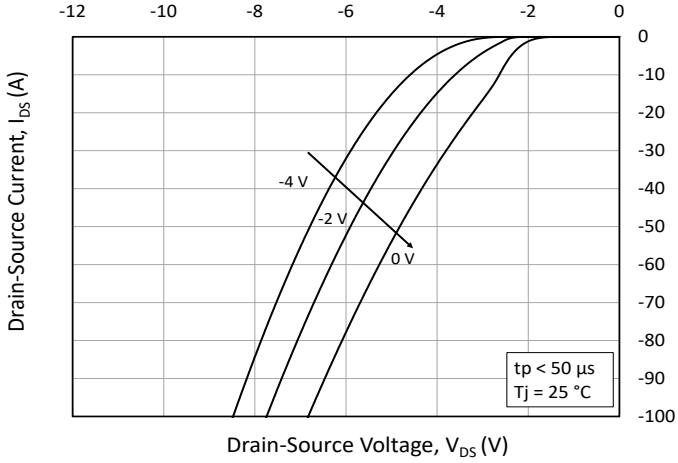


Figure 9. Body Diode Characteristic at 25ºC

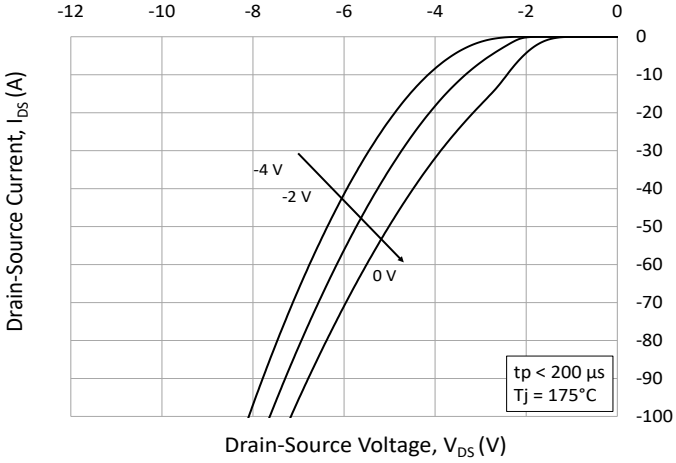


Figure 10. Body Diode Characteristic at 175ºC

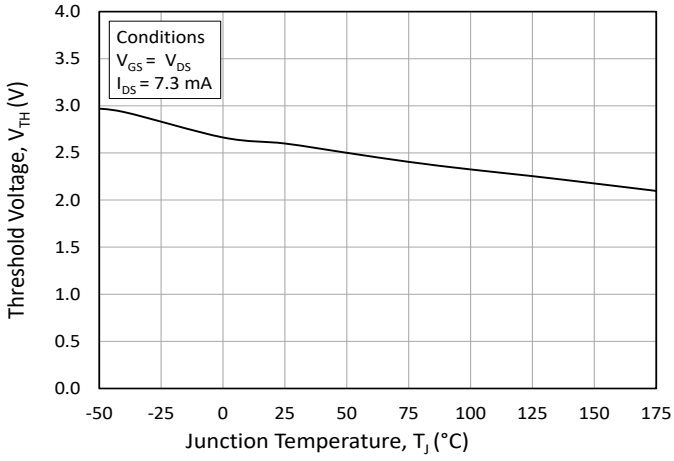


Figure 11. Threshold Voltage vs. Temperature

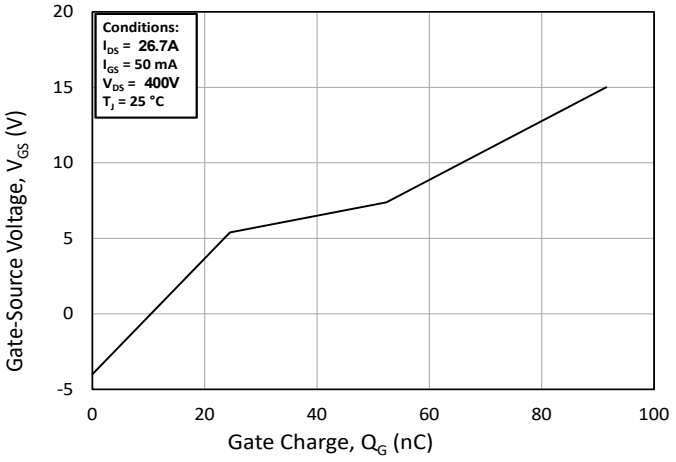


Figure 12. Gate Charge Characteristics

Typical Performance

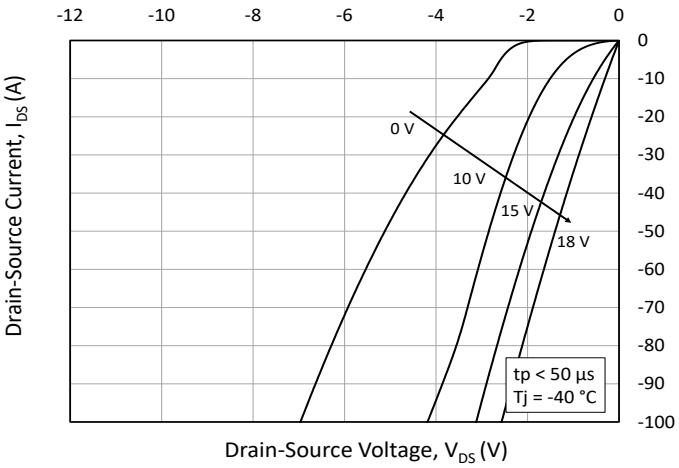


Figure 13. 3rd Quadrant Characteristic at -40ºC

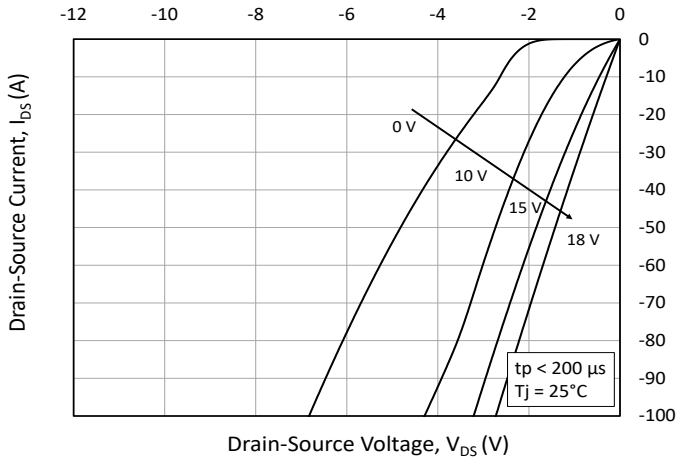


Figure 14. 3rd Quadrant Characteristic at 25ºC

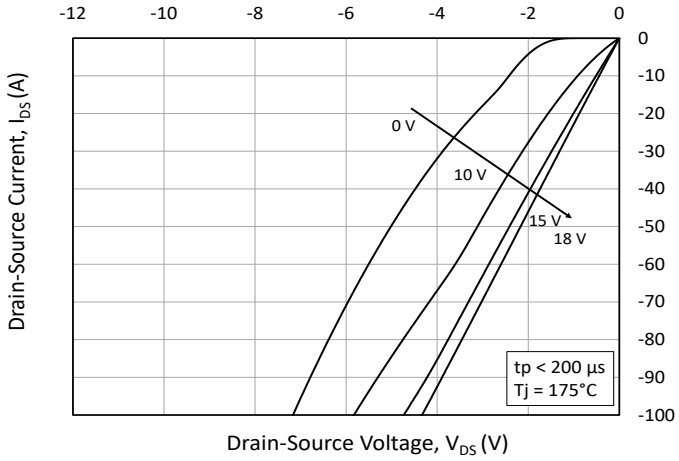


Figure 15. 3rd Quadrant Characteristic at 175ºC

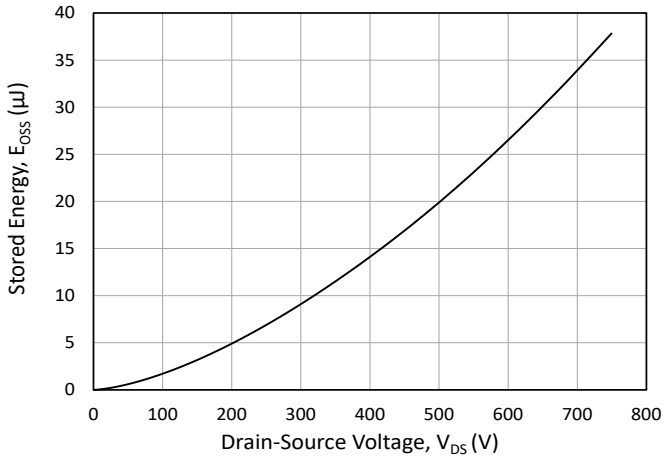


Figure 16. Output Capacitor Stored Energy

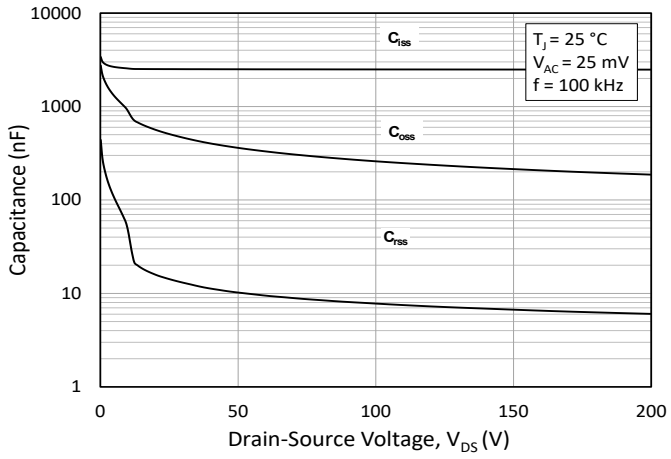


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

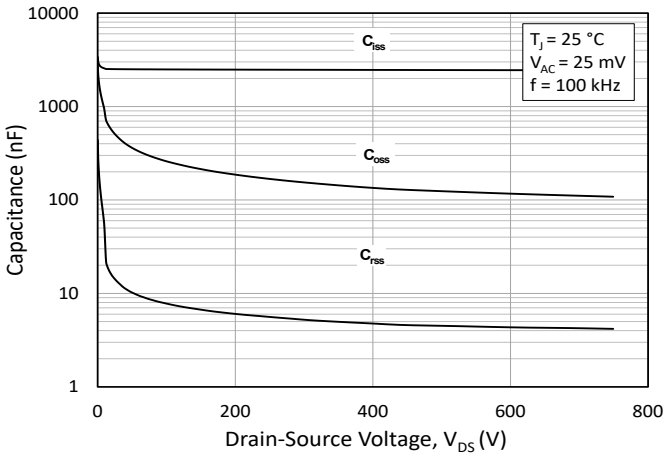
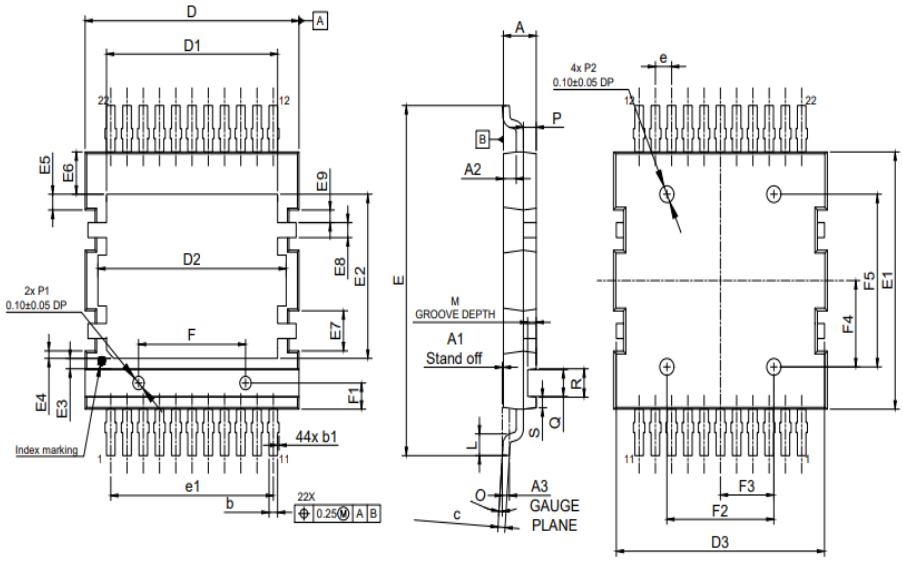
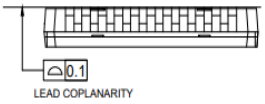


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650 V)

Package Dimensions





SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A	2.25	2.35	E9	0.75	
A1	0.00	0.15	e	1.14	
A2	0.90		e1	11.4	
A3	0.50		F	7.40	7.60
b	0.50	0.70	F1	1.47	1.67
b1	-	0.15	F2	7.40	7.60
c	0.46	0.58	F3	3.65	3.85
D	14.90	15.10	F4	5.07	5.27
D1	12.00		F5	10.24	10.44
D2	13.20		L	1.30	
D3	14.50	14.70	M	0.60	
E	20.81	21.11	N	22	
E1	15.30	15.50	O	0°	8°
E2	9.83		P	0.90	
E3	0.625		P1	0.70	0.90
E4	0.45		P2	0.90	1.10
E5	0.95		Q	1.60	
E6	2.53		R	1.70	
E7	2.40		S	0.631	
E8	0.90				

Revision history

Document Version	Date of release	Description of changes
P1	October 2025	Initial release

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