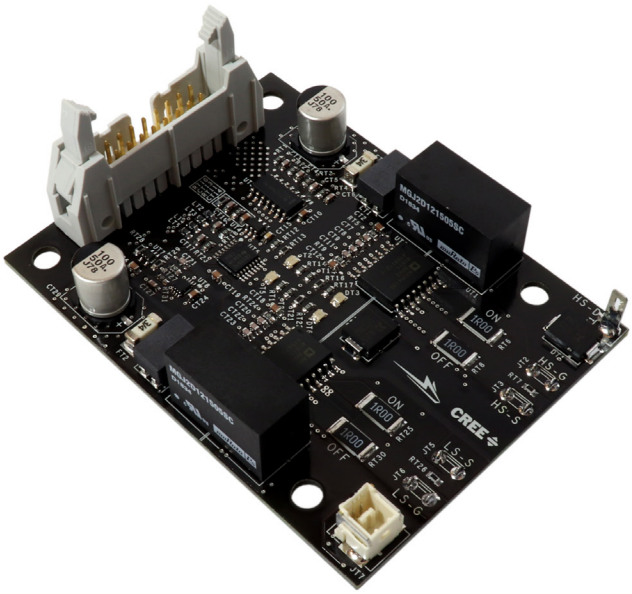
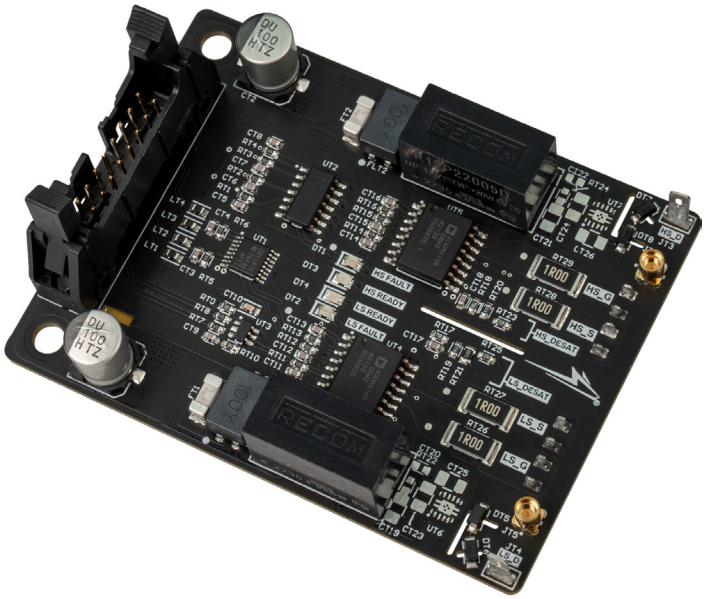
User Guide PRD-09753

Wolfspeed 62 mm Gate Driver User Guide





Part Number	Default V_{GS}	Gate Driver IC	Max. Bus Voltage
CGD1200HB2P-BM2	+20 V / -5 V	Analog Devices ADuM4135	1000 V
CGD1200HB2P-BM3	+15 V / -4 V	Analog Devices ADuM4135	1000 V
CGD1700HB2P-BM2	+20 V / -5 V	Analog Devices ADuM4146C	1500 V
CGD1700HB2P-BM3	+15 V / -4 V	Analog Devices ADuM4146C	1500 V

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DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE BOARD. THERE CAN BE VERY HIGH VOLTAGES PRESENT ON THIS EVALUATION BOARD WHEN CONNECTED TO AN ELECTRICAL SOURCE, AND SOME COMPONENTS ON THIS BOARD CAN REACH TEMPERATURES ABOVE 50˚ CELSIUS. FURTHER, THESE CONDITIONS WILL CONTINUE FOR A SHORT TIME AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED.

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DEATH ▲ SERIOUS INJURY ▲ ELECTROCUTION ▲ ELECTRICAL SHOCK ▲ ELECTRICAL BURNS ▲ SEVERE HEAT BURNS

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请勿在通电情况下接触板子，在操作板子前应使大容量电容器的电荷完全释放。接通电源后，该评估板上通常会存在危险的高电压，板子上一些组件的温度可能超过50摄氏度。此外，移除电源后，上述情况可能会短时持续，直至大容量电容器电量完全释放。

操作板子时应确保遵守正确的安全规程，否则可能会出现下列危险：

死亡 ▲ 严重伤害 ▲ 触电 ▲ 电击 ▲ 电灼伤 ▲ 严重的热烧伤

请在操作本板子前完整阅读本文件。通电时禁止接触板子。所有测试与测量探针或附件必须在板子通电前连接。通电时，禁止使板子处于无人看护状态，且禁止操作板子。必须确保在操作板子前，大容量电容器已释放了所有电量。只有在切断板子电源，且大容量电容器完全放电后，才可更换待测试器件。

警告

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通電している時、ボードに接触するのは禁止です。ボードを処分する前に、大容量のコンデンサーで電力を完全に釈放すべきです。通電してから、ボードにひどく高い電圧が存在している可能性があります。ボードのモジュールの温度は50度以上になるかもしれません。また、電源を切った後、上記の状況がしばらく持続する可能性がありますので、大容量のコンデンサーで電力を完全に釈放するまで待ってください。

ボードを操作するとき、正確な安全ルールを守るのを確保すべきです。さもないと、以下の危険がある可能性があります:

死亡 ▲ 重症 ▲ 感電 ▲ 電撃 ▲ 電気の火傷 ▲ 厳しい火傷

当ボードを操作する前に、完全に当書類をよく読んでください。通電している時にボードに接触する必要がありません。通電する前に必ずすべての試験用のプローブあるいはアクセサリーをつないでください。通電している時に無人監視やボードを操作するのは禁止です。ボードを操作する前に、大容量のコンデンサーで電力を完全に釈放するのを必ず確保してください。ボードの電源を切った後、また大容量のコンデンサーで電力を完全に釈放した後、試験設備を取り換えることができます。

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Wolfspeed 62 mm Gate Driver User Guide

Contents

1. Introduction

The CGD1**2**00HB2P-BM**2**, CGD1**2**00HB2P-BM**3**, CGD1**7**00HB2P-BM**2**, and CGD1**7**00HB2P-BM**3** gate drivers, shown in Figure 1, are dual channel isolated gate drivers optimized for Wolfspeed's 62 mm power modules. The gate drivers are all designed for high-frequency operation and can drive high-performance silicon carbide (SiC) MOSFETs in the 62 mm module package, such as the CAB530M12BM3 shown in Figure 2. All the gate drivers in the 62 mm family feature separate 2 W isolated power supplies and Analog Devices® ADuM4135 or ADuM4146C gate driver integrated circuits (ICs) for independently operating the high- and low-side switch positions of a SiC power module. The designs include input voltage protection, differential inputs for increased noise immunity, soft shutdown, anti-overlap functionality, undervoltage lockout, and overcurrent protection. This user guide provides an overview of the gate driver functions and parameters including connector pinouts and operating guidance.

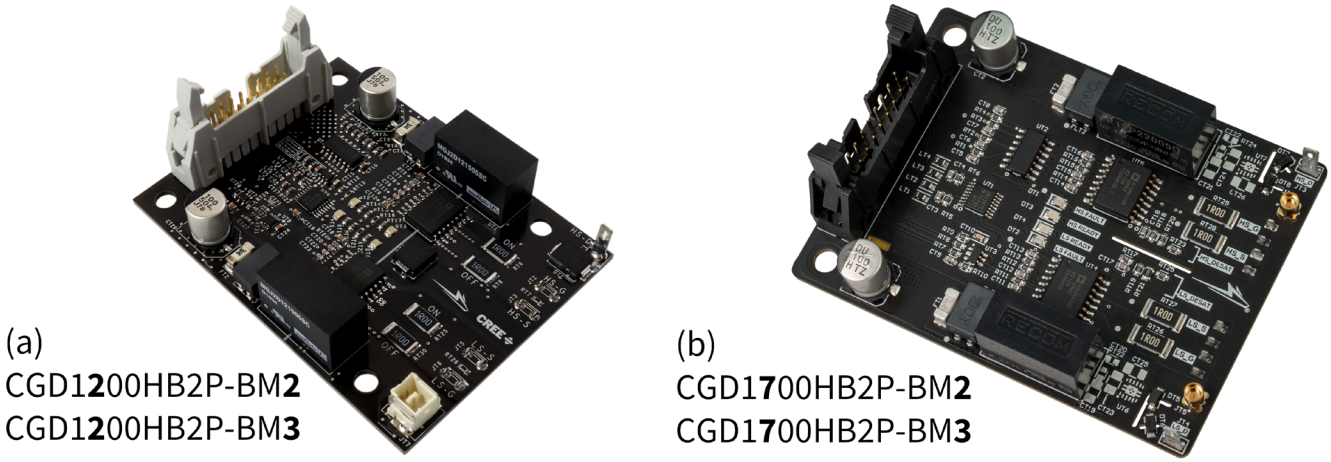

*Figure 1: 62 mm power module gate drivers: (a) CGD1**2**00HB2P-BM2/3 and (b) CGD1**7**00HB2P-BM2/3*

Figure 2: Example Wolfspeed 62 mm power module

1.1 Gate Driver Variations

All the gate drivers in this family are similar, primarily differing on the default output voltages and gate driver ICs employed. For output voltages, the CGD1**2**00HB2P-BM**2** and CGD1**7**00HB2P-BM**2** are both designed for Wolfspeed's Generation 2 (Gen. 2) power devices and therefore have a default output gate-to-source voltage (V_{GS}) of +20 V for turn on and -5 V for turn off. The CGD1**2**00HB2P-BM**3** and CGD1**7**00HB2P-BM**3** are both designed for Wolfspeed's Gen. 3 power devices and therefore have a default output V_{GS} of +15 V for turn on and -4 V for turn off. For gate driver ICs, the CGD1**2**00HB2P-BM**2** and CGD1**2**00HB2P-BM**3** are optimized for 1200 V 62 mm power modules and employ the Analog Device ADuM4135 gate driver IC for bus voltages up to 1000 V. The CGD1**7**00HB2P-BM**2** and CGD1**7**00HB2P-BM**3** are optimized for up to 1700 V 62 mm power modules and employ the Analog Device ADuM4146C gate driver IC for bus voltages up to 1500 V. The differences in gate drivers in the 62 mm gate driver family are summarized in Table 1 and Figure 3.

Table 1: 62 mm gate driver family variations

Part Number	SiC Gen.	Default V_{GS}	Gate Driver IC	Max. Bus Voltage
CGD1200HB2P-BM2	2	+20 V / -5 V	Analog Devices ADuM4135	1000 V
CGD1200HB2P-BM3	3	+15 V / -4 V	Analog Devices ADuM4135	1000 V
CGD1700HB2P-BM2	2	+20 V / -5 V	Analog Devices ADuM4146C	1500 V
CGD1700HB2P-BM3	3	+15 V / -4 V	Analog Devices ADuM4146C	1500 V

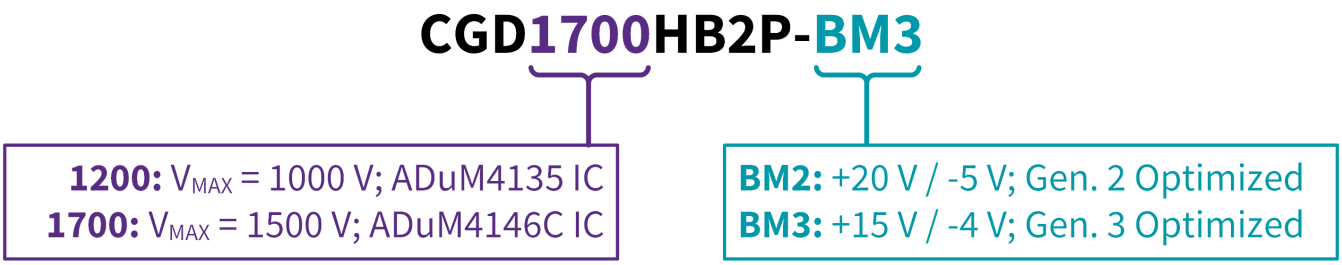

Figure 3: 62 mm gate driver part number descriptions

2. Design Features

The 62 mm power module family of gate drivers includes system benefits such as independent gate resistors and differential signaling in addition to integrated protections such as onboard overcurrent, shoot-through, and reverse polarity protection. The maximum operating parameters of these gate driver designs are shown in Table 2. The full list of electrical parameters are shown in Table 3 for the CGD1**2**00HB2P-BM2/3 gate drivers and Table 4 for the CGD1**7**00HB2P-BM2/3 gate drivers. Renderings of the board assemblies from various views are shown in Figure 4 and Figure 5 for the CGD1**2**00HB2P-BM2/3 and CGD1**7**00HB2P-BM2/3 gate drivers, respectively.

2.1 Maximum Operating Parameters

Table 2: Maximum operating parameters (verified by design)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DC}	-0.5 to 13.2	V
Logic Level Input	V_I	-0.5 to 5.5	
Output Peak Current (T_A = 25 °C)	I_O	±10	A
Output Power Per Channel (T_A = 25 °C)	P_{DRIVE}	2	W
Maximum Switching Frequency (MOSFET & V_{GS} Dependent, See Section 4.7)	f_{SW}	120	kHz
Ambient Operating Temperature	T_{OP}	-40 to 85	°C
Storage Temperature	T_{STG}	-40 to 85	

2.2 Assembly

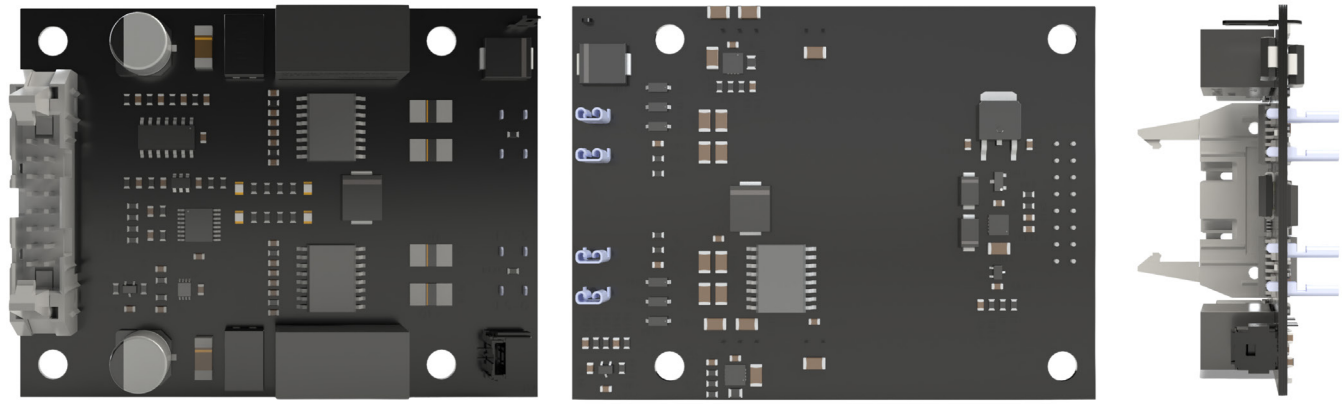

Figure 4: CGD1200HB2P-BM2/3 rending views

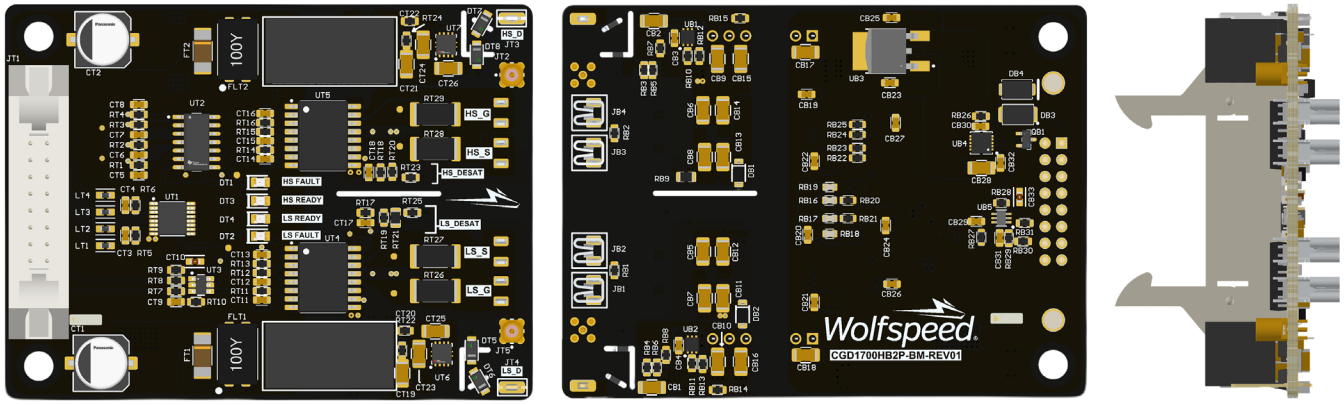

Figure 5: CGD1700HB2P-BM2/3 rendering views

2.3 Electrical Characteristics

*Table 3: Electrical characteristics of CGD1**2**00HB2P-BM2/3 gate drivers (T = 25°C unless otherwise specified)*

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V_{DC}	10.8	12	13.2	V	
Secondary Under Voltage Lockout	V_{UVLO}		11.67	12.25		Turn On, Going High
UVLO Hysteresis	V_{HYS}		0.8			
Over Voltage Clamping	V_{OVLO}	18	20	22		Zenor Diode Voltage
High Level Logic Input Voltage	V_{IH}	3.5		5.5		Single-Ended Inputs (Based on AND Gate Input)
Low Level Logic Input Voltage	V_{IL}	0		1.5		
Diff Input Common Mode Range	V_{IDCM}		±2.5	±7		Differential Inputs
Positive-going input threshold voltage, differential input	V_{IT+}			0.2		$V_{ID} = V_{POS-LINE} - V_{NEG-LINE}$
Negative-going input threshold voltage, differential input	V_{IT-}	-0.2				
High level Output Voltage	$V_{GATE,HIGH}$		+20			CGD1**2**00HB2P-BM**2**
			+15			CGD1**2**00HB2P-BM**3**
Low level Output Voltage	$V_{GATE,LOW}$		-5			CGD1**2**00HB2P-BM**2**
			-4			CGD1**2**00HB2P-BM**3**
Working Isolation Voltage	V_{IOWM}		1000			V_{RMS}
Isolation Capacitance	C_{ISO}		4.9		pF	Per Channel
Common Mode Transient Immunity	CMTI	100			kV/µs	V_{CM} = 1000 V
Output Resistance[1]	$R_{G(IC)-ON}$		0.48	0.98	Ω	Gate Driver Buffer Tested at 1 A
	$R_{G(IC)-OFF}$		0.32	0.63		
External Resistance[2]	$R_{G(EXT)-ON}$		1			External SMD Resistor 2512 (6432 Metric)
	$R_{G(EXT)-OFF}$		1			
Output Rise Time	t_{ON}		174		ns	$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF From 10% to 90%
Output Fall Time	t_{OFF}		157			
Propagation Delay (Turn-Off)	t_{PHL}		108			$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 0 nF From 50% to 50%
Propagation Delay (Turn-On)	t_{PLH}		106			
Over-current Blanking Time	t_{BLANK}		0.6		µs	$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF
Over-current Propagation Delay to FAULT Signal Low	$t_{PD-FAULT}$		0.5	2		Does Not Include Blanking
Soft-Shutdown Time	t_{SS}		3			
Soft-Shutdown Resistance[3]	R_{SS}		10.2	22	Ω	Tested at 250 mA
Miller Clamp Resistance	R_{MC}		1.1	2.75		Tested at 100 mA
Miller Clamp Voltage Threshold	V_{MC}	1.75	2.0	2.25	V	Reference to Source

[1] Output resistance of gate driver integrated circuit (IC).
[2] Additional output resistance is added with surface mount device (SMD) resistors. Separate resistors allow for independent tuning.
[3] Soft-shutdown network will safely turn off the gate if an overcurrent event is detected.

*Table 4: Electrical characteristics of CGD1**7**00HB2P-BM2/3 gate drivers (T = 25°C unless otherwise specified)*

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V_{DC}	10.8	12	13.2	V	
Secondary Under Voltage Lockout	V_{UVLO}		11.5	12		
Secondary UVLO Hysteresis	V_{HYS}		0.06			
Over Voltage Clamping	V_{OVLO}	18	20	22		Zenor Diode Voltage
High Level Logic Input Voltage	V_{IH}	3.5		5.5		Single-Ended Inputs
Low Level Logic Input Voltage	V_{IL}	0		1.5		(Based on AND Gate Input)
Diff Input Common Mode Range	V_{IDCM}		±2.5	±7		Differential Inputs
Positive-going input threshold voltage, differential input	V_{IT+}			0.2		$V_{ID} = V_{POS-LINE} - V_{NEG-LINE}$
Negative-going input threshold voltage, differential input	V_{IT-}	-0.2				
High level Output Voltage	$V_{GATE,HIGH}$		+20			CGD1**7**00HB2P-BM**2**
			+15			CGD1**7**00HB2P-BM**3**
Low level Output Voltage	$V_{GATE,LOW}$		-5			CGD1**7**00HB2P-BM**2**
			-4			CGD1**7**00HB2P-BM**3**
Working Isolation Voltage	V_{IOWM}		1500			V_{RMS}
Isolation Capacitance	C_{ISO}		4.9		pF	Per Channel
Common Mode Transient Immunity	CMTI	100			kV/µs	V_{CM} = 1500 V
Output Resistance[1]	$R_{G(IC)-ON}$		0.48	0.98	Ω	Gate Driver Buffer Tested at 1 A
	$R_{G(IC)-OFF}$		0.47	0.81		
External Resistance[2]	$R_{G(EXT)-ON}$		1			External SMD Resistor 2512 (6432 Metric)
	$R_{G(EXT)-OFF}$		1			
Output Rise Time	t_{ON}		223		ns	$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF From 10% to 90%
Output Fall Time	t_{OFF}		208			
Propagation Delay (Turn-Off)	t_{PHL}		120			$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 0 nF From 50% to 50%
Propagation Delay (Turn-On)	t_{PLH}		125			
Over-current Blanking Time	t_{BLANK}		0.6		µs	$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF
Over-current Propagation Delay to FAULT Signal Low	$t_{PD-FAULT}$		1.3			Does Not Include Blanking
Soft-Shutdown Time	t_{SS}		1.3			$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF
Soft-Shutdown Resistance[3]	R_{SS}		5		Ω	Tested at 25 mA
Miller Clamp Resistance	R_{MC}		1.1	2.75		Tested at 100 mA
Miller Clamp Voltage Threshold	V_{MC}	1.75	2.0	2.25	V	Reference to Source

[1] Output resistance of gate driver integrated circuit (IC).
[2] Additional output resistance is added with surface mount device (SMD) resistors. Separate resistors allow for independent tuning.
[3] Soft-shutdown network will safely turn off the gate if an overcurrent event is detected.

2.4 Block Diagram

A block diagram of the gate drivers in the 62 mm family is shown in Figure 6. Both channels (high- and low-side) include a dedicated isolated DC/DC converter and gate driver integrated circuit (IC) for independent modulation of the respective channels. The gate driver communicates with a controller via differential signaling for both input and feedback signals. The gate driver combines all onboard fault signals (i.e. overcurrent and power faults for both channels) into a single global fault signal which is transmitted to the controller to indicate the board status. The board includes an overcurrent detection circuit, independent turn-on and turn-off resistors and Miller clamp. Some notable interface features on the boards are indicated in Figure 7 and Figure 8 for the CGD1**2**00HB2P-BM2/3 and CGD1**7**00HB2P-BM2/3 gate drivers, respectively.

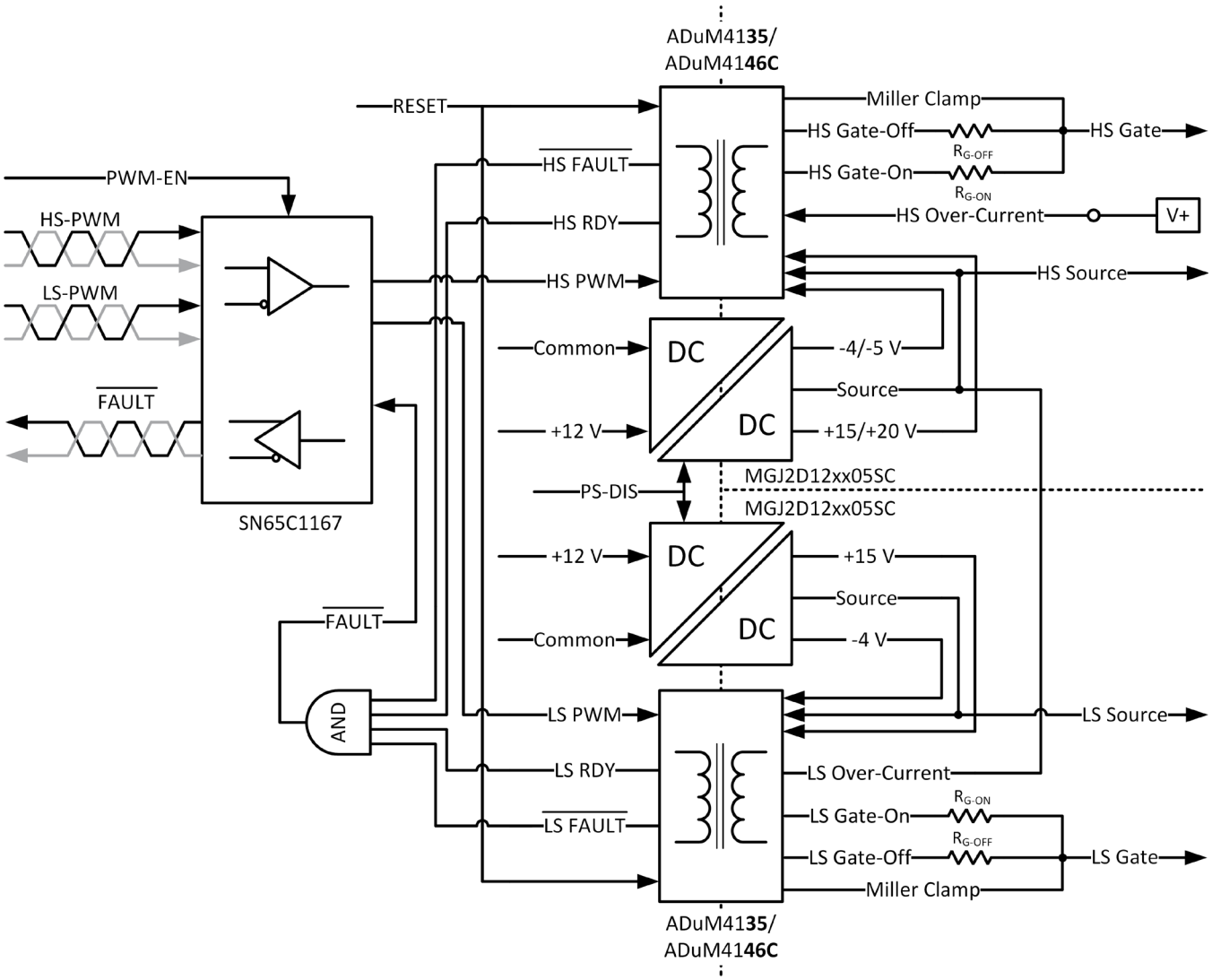

Figure 6: Block diagram of 62 mm gate drivers

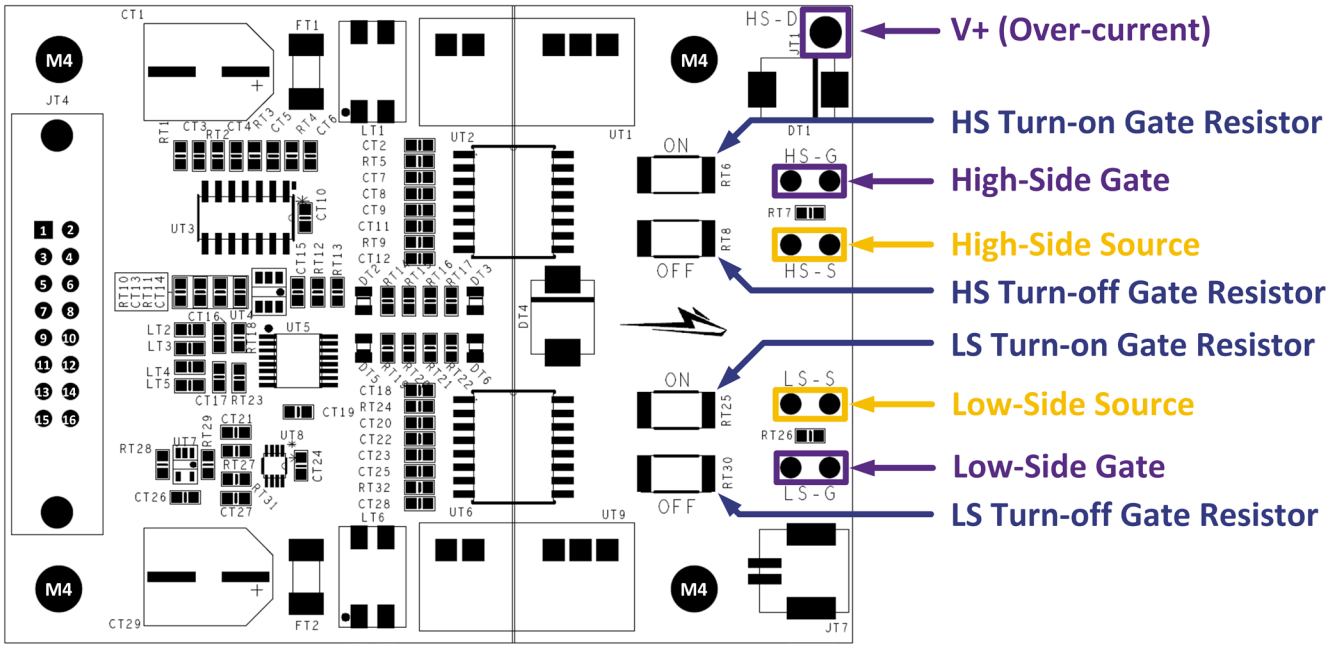

Figure 7: Interface of CGD1200HB2P-BM2/3 gate drivers

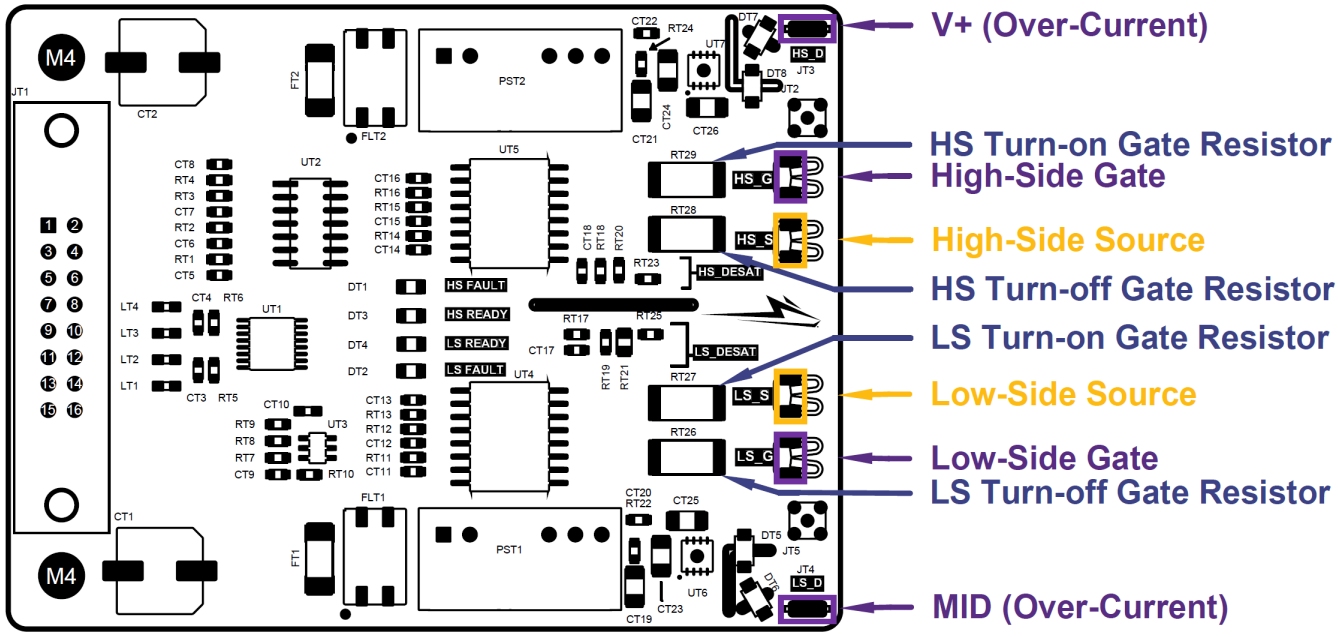

Figure 8: Interface of CGD1700HB2P-BM2/3 gate drivers

3. Inputs/Outputs

The 62 mm gate drivers include multiple connectors for interfacing with the power module and control signals and to perform measurements. This section details the pinouts and functionalities of each of these connectors. An overview of the purpose of each connector is shown in Table 5 and Table 6 for the CGD1200HB2P-BM2/3 and CGD1700HB2P-BM2/3 gate drivers, respectively. The tables also include the corresponding document section numbers to find additional information.

*Table 5: Summary of input/output connectors on CGD1**2**00HB2P-BM2/3*

Ref. Des.	Side	Description	Section
JT1	Top	High-side overcurrent feedback	3.3
JT2	Bottom	High-side gate output	3.2
JT3	Bottom	High-side source output	
JT4	Top	Input signals	3.1
JT5	Bottom	Low-side source output	3.2
JT6	Bottom	Low-side gate output	
JT7	Top	Thermistor feedback **(NOT POPULATED)**	N/A

*Table 6: Summary of input/output connectors on CGD1**7**00HB2P-BM2/3*

Ref. Des.	Side	Description	Section
JT1	Top	Input signals	3.1
JT2	Top	High-side V_{GS} measurement	3.4
JT3	Top	High-side overcurrent feedback	3.3
JT4	Top	Low-side overcurrent feedback	
JT5	Top	Low-side V_{GS} measurement	3.4
JB1	Bottom	Low-side gate output	3.2
JB2	Bottom	Low-side source output	
JB3	Bottom	High-side source output	
JB4	Bottom	High-side gate output	

3.1 Input Connector

The 62 mm gate drivers are intended to operate with differential signaling for improved noise immunity compared to single-ended signaling (see Section 0). All the control and feedback signals with this gate driver are digital and interface through a single input connector (reference designator *JT4 on the* CGD1**2**00HB2P-BM2/3 drivers and *JT1* on the CGD1**7**00HB2P-BM2/3 drivers). The connector orientation and the corresponding pin locations are shown in Figure 9 and Figure 10 for the CGD1**2**00HB2P-BM2/3 and CGD1**7**00HB2P-BM2/3 drivers, respectively. The input connector on the CGD1**2**00HB2P-BM2/3 drivers is part number 71918-116LF manufactured by Amphenol FCI®, and the input connector on the CGD1**7**00HB2P-BM2/3 drivers is part number D3408-6302-AR manufactured by 3M®. The suggested mating parts are listed in Table 7 and are the same for all gate drivers in the 62 mm family.

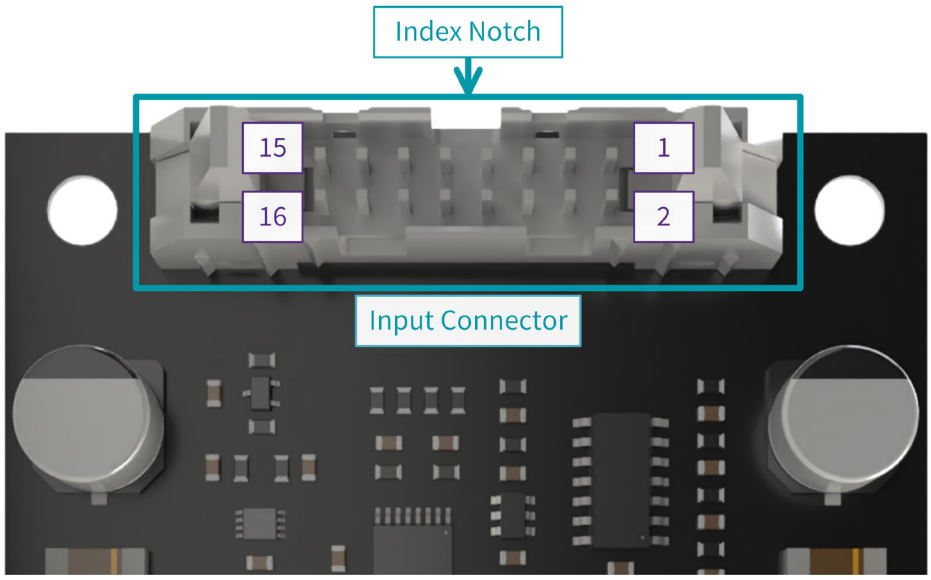

*Figure 9: JT4 input connector orientation and pin locations on CGD1**2**00HB2P-BM2/3*

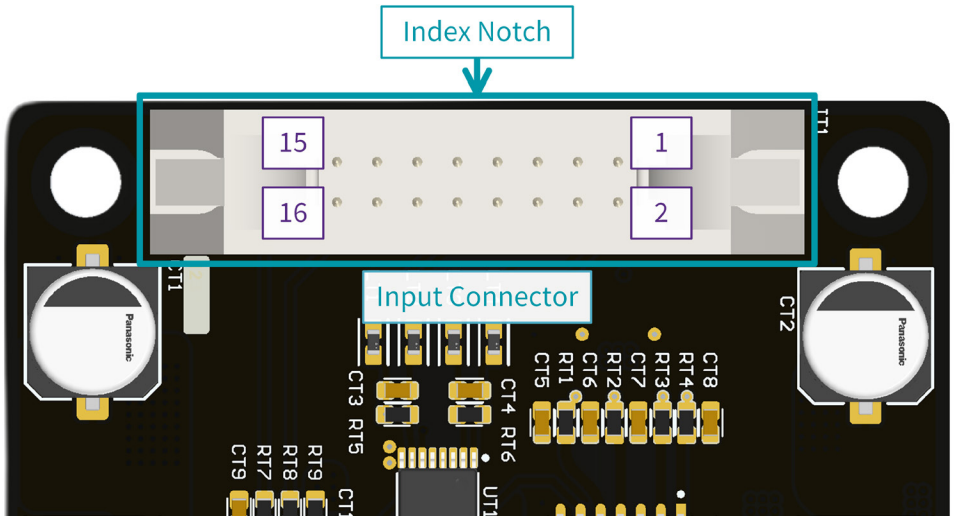

*Figure 10: JT1 input connector orientation and pin locations on CGD1**7**00HB2P-BM2/3*

Table 7: Input connector suggested mating parts

Component	Manufacturer	Part Number	Description
Mating IDC Connector	Sullins Connector Solutions	SBH11-NBPC-D08-SM-BK	16 Position Rectangular Header Connector IDC Gold 28 AWG
Straight Ribbon Cable[1]	3M	HF365/16SF	Flat Ribbon Cable Gray 16 Conductors 0.050" (1.27mm) Flat Cable
Twisted Ribbon Cable[1]	3M	1700/16 100SF	Flat Ribbon Cable Multiple 16 (8 Pair Twisted) Conductors 0.050" (1.27mm)

[1] When using ribbon cable for long connections, it is recommended to use twisted-pair ribbon cable for improved noise immunity.

3.1.1 Pinout

Table 8: Pinout of input connector

Pin	Name	Description
1	VDC	Power supply input pin (+12 V Nominal Input).
2	Common	Common.
3	HS-PWM-P*	Positive line of 5 V differential high-side PWM signal pair. Terminated into 120 Ω.
4	HS-PWM-N*	Negative line of 5 V differential high-side PWM signal pair. Terminated into 120 Ω.
5	LS-PWM-P*	Positive line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω.
6	LS-PWM-N*	Negative line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω.
7	$\overline{\text{FAULT-P}}$*	Positive line of 5 V differential fault condition signal pair. Drive strength 20 mA. A low state on FAULT indicates when a desaturation fault has occurred. The presence of a fault precludes the gate drive output from going high.
8	$\overline{\text{FAULT-N}}$*	Negative line of 5 V differential fault condition signal pair. Drive strength 20 mA.
9	NC	No connect.
10	NC	No connect.
11	$\overline{\text{PS-DIS}}$	Pull down to disable power supply. Pull up or leave floating to enable. Gate and source are connected with 10 kΩ when disabled.
12	Common	Common.
13	PWM-EN	Pull down to disable PWM input logic. Pull up or leave floating to enable. Gate driver output will be held low through turn-off gate resistor if power supplies are enabled.
14	Common	Common.
15	RESET	When a fault exists, bring this pin high for >500 ns to clear the fault.
16	Common	Common.

* Inputs 3-10 are differential pairs.

3.1.2 Signal Descriptions

PWM Signals: High-side and low-side pulse-width modulation (PWM) signals are RS-422 compatible differential inputs. The termination impedance of the differential receiver is 120 Ω. Overlap protection is provided to prevent both the high-side and low-side gates from turning on simultaneously. The overlap protection should not be used as a dead time generator.

$\overline{FAULT}$ Signal: The fault signal is a RS-422 compatible differential output with a maximum drive strength of 20 mA. A high signal (positive line > negative line) means there are no fault conditions for either gate driver channel. This signal will be low if an overcurrent fault or undervoltage-lockout (UVLO) fault condition is detected on either channel. After an overcurrent fault, this signal will latch low until the gate driver is reset via the RESET signal. The presence of a fault precludes the gate drive output from going high. The onboard light-emitting diodes (LEDs) will also indicate the fault condition. See Sections 3.5 and 4.4 for more details.

$\overline{PS\text{-}DIS}$ Signal: The $\overline{PS\text{-}DIS}$ signal disables the output of the isolated DC/DC converters for the two channels. It is a single-ended input that must be pulled low to turn off the power supplies. With the power

supplies disabled, the gate will be help low with a 10 kΩ resistor. This signal can be used for startup sequencing.

PWM-EN: This is a single-ended input that enables the PWM inputs for both channels. When this signal is pulled down, the differential receivers for both channels are disabled and the gates will both be pulled low through $R_{G(EXT)-OFF}$. All protection circuitry and power supplies will continue to operate including $\overline{FAULT}$.

RESET Signal: This is a single-ended input that can be used to clear overcurrent faults on the gate driver. To clear an overcurrent fault, this signal must be commanded high for at least 500 ns. While the signal remains high, the outputs of the gate driver remain disabled. On the gate driver board, this input is held low with a 10 kΩ resistor. This signal resets both channels of the gate driver.

3.2 Output Connectors

The output connectors on the 62 mm gate drivers are four quick-disconnect receptacles designed to attach directly to Wolfspeed 62 mm power modules. An example connection is shown in Figure 11. The power bussing connects directly to the high-ampacity terminals of the module. The high-side and low-side gate driver output connections are isolated from each other and do not share a source connection. The output connectors on the CGD1**2**00HB2P-BM2/3 gate drivers use Keystone Electronics® 3534 receptacles, and the output connectors on the CGD1**7**00HB2P-BM2/3 gate drivers use Keystone Electronics® 3557 receptacles. Figure 12 and Figure 13 show the output connector locations and pinouts for the CGD1**2**00HB2P-BM2/3 and CGD1**7**00HB2P-BM2/3 gate drivers, respectively.

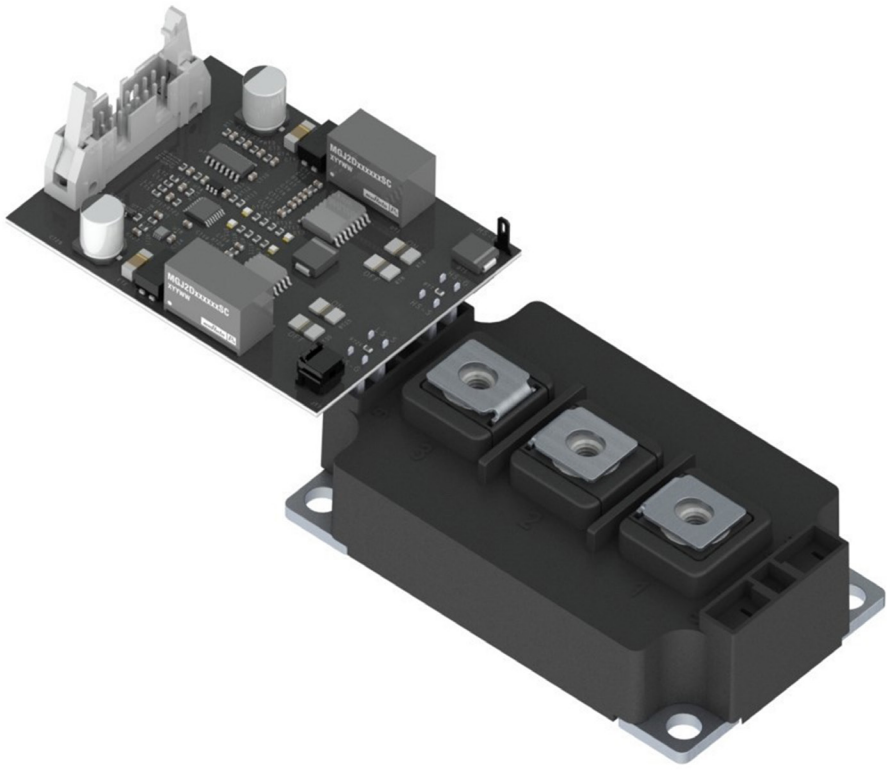

Figure 11: Example 62 mm gate driver attached to a 62 mm power module

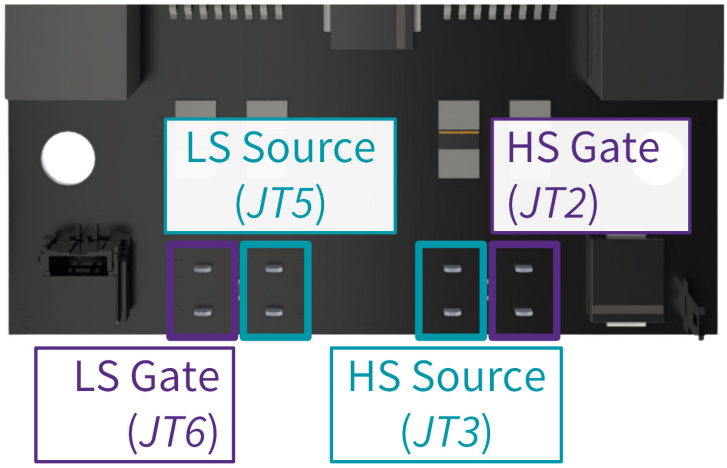

*Figure 12: JT2-3 and JT5-6 output connector orientations and pin locations on CGD1**2**00HB2P-BM2/3 gate drivers*

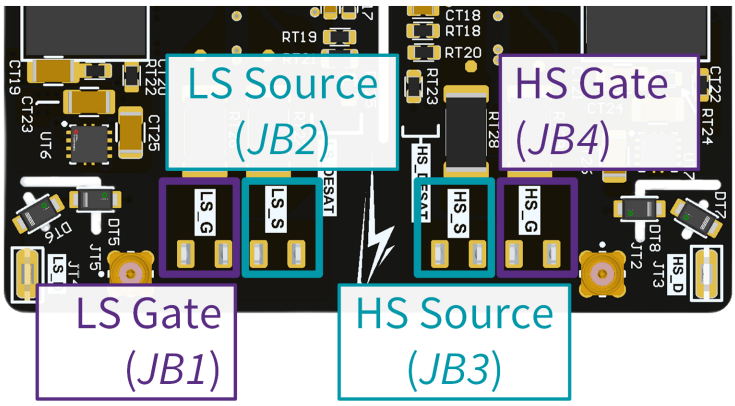

*Figure 13: JB1-4 output connector orientations and pin locations on CGD1**7**00HB2P-BM2/3 gate drivers*

3.3 Overcurrent Feedback Connectors

The desaturation circuits employed on this design for overcurrent protection (see Section 4.4.3) require accurate measurement of the MOSFET drain terminals to identify when the device is conducting high currents, such as when the device output is shorted. The 62 mm gate drivers include connections to attach to the drain terminals for overcurrent protection of each channel. The CGD1**7**00HB2P-BM2/3 gate drivers include a dedicated connector for the low-side overcurrent protection (*JT4*) and the high-side overcurrent protection (*JT3*), as shown in Figure 15. Both connections are 735187-2 connectors manufactured by TE Connectivity. The recommended mating connectors for these are 7-520365-2 or 2-520272-2 which are both manufactured by TE Connectivity. For the best results, a flying wire should be attached to this connector as close as possible to the drain terminal of the corresponding switch position, and the flying wire should be kept as short as possible. The CGD1**2**00HB2P-BM2/3 gate drivers include a dedicated connector for the high-side overcurrent protection (*JT1*) as shown in Figure 14. This connector is also part number 735187-2 manufactured by TE Connectivity with the same recommended mating connectors and flying wire guidance as described above. The low-side overcurrent protection for the CGD1**2**00HB2P-BM2/3 gate drivers does not have a dedicated connector; the low-side overcurrent protection uses the high-side source for the drain measurement, since it is electrically connected to the low-side drain terminal (see Section 6.4 of **PRD-09301** for more information).

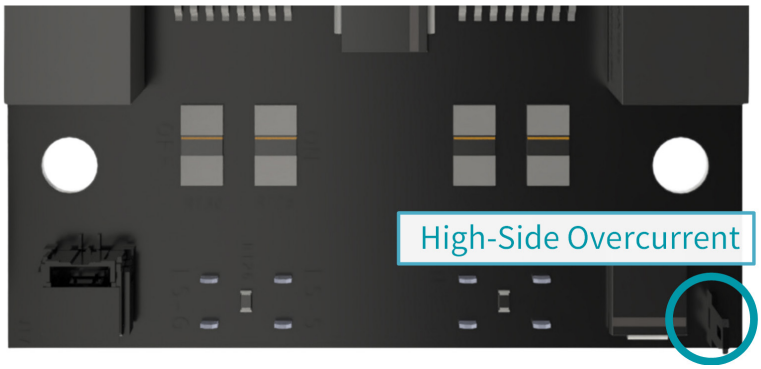

*Figure 14: JT1 high-side overcurrent feedback connector on CGD1**2**00HB2P-BM2/3 gate drivers*

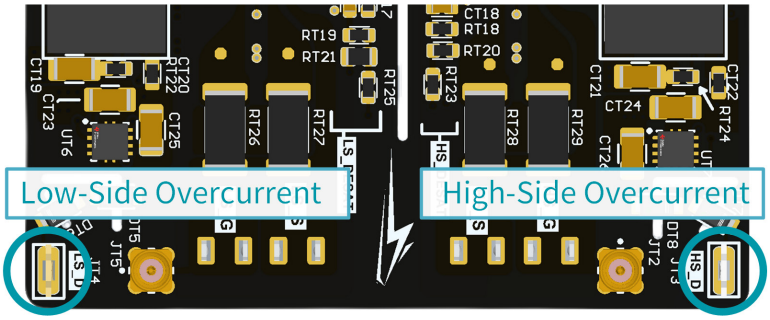

*Figure 15: JT3 and JT4 overcurrent feedback connectors on CGD1**7**00HB2P-BM2/3 gate drivers*

These connectors cannot be left floating as the overcurrent fault will trip immediately when the associated gate is actuated. If bench-top testing of the gate driver is required, it is acceptable to short the connector to the appropriate source to prevent the overcurrent fault from tripping during testing. **Performing this modification will bypass the overcurrent protection**, so the gate driver will no longer be protecting the MOSFET(s).

3.4 Gate-to-Source Voltage Measurement Connectors (CGD1700HB2P-BMx Only)

A high-fidelity gate-to-source voltage measurement (V_{GS}) is critical for many applications such as device characterization, system commissioning, and troubleshooting. The CGD1**7**00HB2P-BM2/3 gate drivers include integrated micro-miniature coaxial (MMCX) connectors for measuring the V_{GS} outputs of the gate driver. Note that the CGD1**2**00HB2P-BM2/3 gate drivers do not include an integrated measurement connector. The pinouts and locations for the measurement connectors on the CGD1**7**00HB2P-BM2/3 gate drivers are shown in Figure 16. A variety of probes can interface directly with these standard MMCX connectors. Wolfspeed recommends performing these measurements with an optically isolated probe such as the Tektronix® IsoVu™ series of probes to ensure high common-mode (CM) rejection during measurements. This is especially critical for the high-side V_{GS} measurement which is referenced to a varying voltage node. In applications where the gate driver is not placed immediately adjacent to the MOSFET gate/source terminals and in applications requiring extremely high fidelity measurements (such as characterization measurements), it is recommended to include a separate V_{GS} probe location right next to the MOSFET. The output connectors of the gate driver includes some parasitic inductance which can obfuscate dynamics occurring at the MOSFET terminals. In characterization measurements, it is critical that the V_{GS} measurement is as close as possible to the MOSFET terminals.

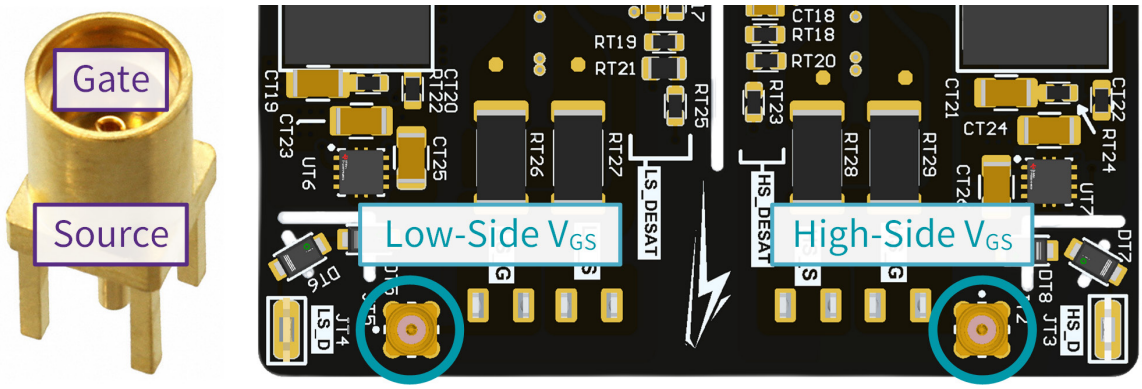

*Figure 16: JT2 and JT3 measurement connector orientations and pins on CGD1**7**00HB2P-BM2/3 gate drivers*

3.5 Status Indicators

The 62 mm gate drivers each include four LEDs to indicate the state of the board. The locations of these LEDs are shown in Figure 17 for the CGD1**2**00HB2P-BM2/3 gate drivers and Figure 18 for the CGD1**7**00HB2P-BM2/3 gate drivers. The functionality of these LEDs is summarized in Table 9. In normal operation, the green READY LEDs will be illuminated, indicating that the gate driver board is functioning as expected. When the system faults due to an overcurrent event, the channel(s) where the fault occurred will illuminate the corresponding red FAULT LED. When the gate driver has an UVLO event, the READY LED of the relevant channel(s) will be extinguished. The status of the gate driver board depending on the LED states is summarized in Table 10.

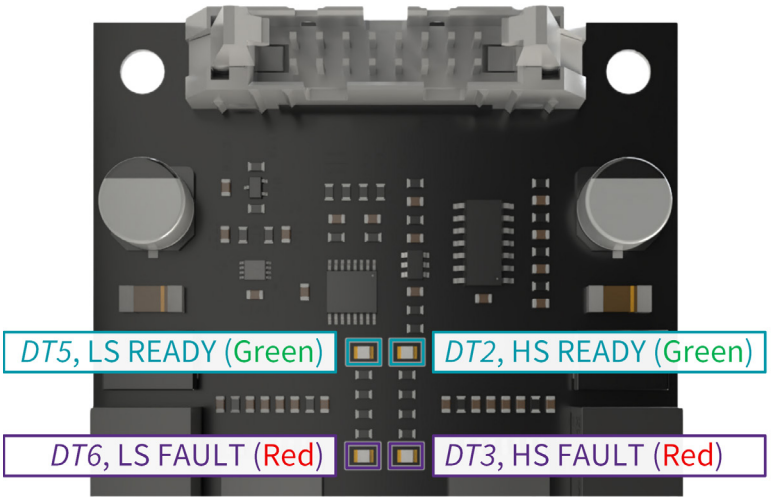

*Figure 17: Status LEDs on CGD1**2**00HB2P-BM2/3 gate drivers*

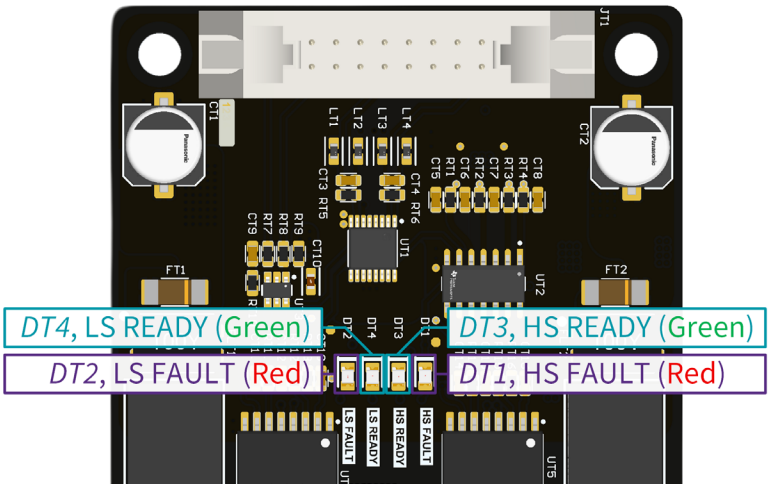

Figure 18: Status LEDs on CGD1700HB2P-BM2/3 gate drivers

Table 9: Status LED descriptions and reference designators

Description	Color	CGD1200HB2P-BM2/3	CGD1700HB2P-BM2/3
Low-Side FAULT	Red	*DT6*	*DT2*
High-Side FAULT	Red	*DT3*	*DT1*
Low-Side READY	Green	*DT5*	*DT4*
High-Side READY	Green	*DT2*	*DT3*

Table 10: Status LED states

READY LED	FAULT LED	Description
1	0	Normal operation. No issues.
0	X	Bad power rail(s). Check input power quality, fuses, component failure, and output short-circuit.
X	1	Overcurrent fault. Clear fault condition and reset gate driver.

1 = LED On | 0 = LED Off | X = Irrelevant

4. Features

The 62 mm family of gate drivers include several design features intended to enable them to efficiently and reliably drive high-performance SiC MOSFETs at high frequencies. These features – which enable higher efficiency, noise immunity, flexibility, and protection – are detailed in this section.

4.1 Independent Gate Resistors

The designs include separate external turn-on ($R_{G(EXT),ON}$) and turn-off ($R_{G(EXT),OFF}$) gate resistors for both channels of the gate driver. The different resistors allow for independent tuning of the turn-on and turn-off switching dynamics. This can be useful for optimizing switching losses while staying within the safe operating bounds. By default, all the 62 mm gate drivers include 1 Ω gate resistors for turn-off and turn-on for both channels, though the resistors can be easily changed to adjust the switching dynamics. The default resistors used are Vishay Dale

CRCW25121R00FKEGHP resistors in a surface-mount 2512 (6432 metric) footprint. To maximize performance, it is recommended to use pulse-rated resistors when replacing/changing the gate resistors. The locations of the gate resistors are shown in Figure 19 and Figure 20 for the CGD1**2**00HB2P-BM2/3 and CGD1**7**00HB2P-BM2/3 gate drivers, respectively. The purpose of each resistor is summarized in Table 11. See **PRD-09301** for more information about independent gate resistor tuning.

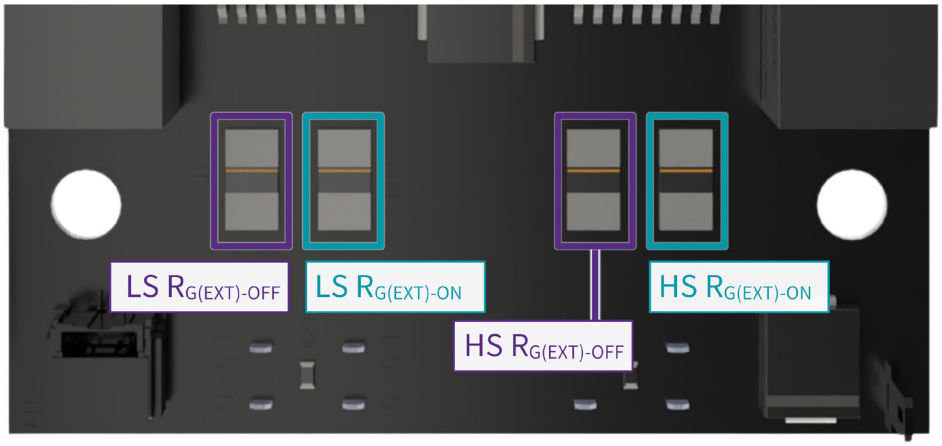

*Figure 19: External turn-on and turn-off gate resistor locations on CGD1**2**00HB2P-BM2/3 gate drivers*

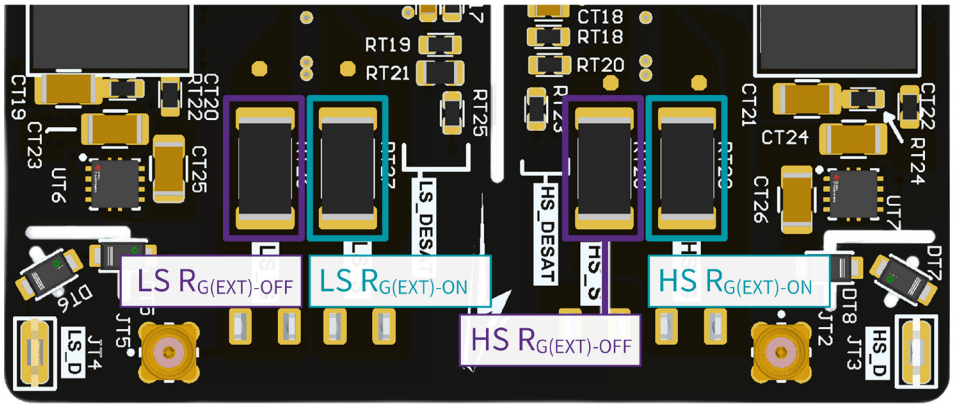

*Figure 20: External turn-on and turn-off gate resistor locations on CGD1**7**00HB2P-BM2/3 gate drivers*

Table 11: External gate resistors descriptions and reference designators

Description	Default	CGD1200HB2P-BM2/3	CGD1700HB2P-BM2/3
Low-Side External Turn-On Resistor	1 Ω	*RT25*	*RT27*
Low-Side External Turn-Off Resistor	1 Ω	*RT30*	*RT26*
High-Side External Turn-On Resistor	1 Ω	*RT6*	*RT29*
High-Side External Turn-Off Resistor	1 Ω	*RT8*	*RT28*

4.2 Differential Signaling

Signal integrity is critical when controlling power devices with a gate driver. A gate driver that is susceptible to the powerful interference generated by power devices can induce a shoot-through condition in the module. The extremely fast turn-on and turn-off times during the switching events in a SiC power system can create electromagnetic interference (EMI) that can easily couple onto the gate control signals. For this reason, differential signaling was adopted instead of standard, single-ended connections between the gate driver and control board. More information about differential signaling compared to single-ended connections is provided in **PRD-09301**.

Differential signaling significantly reduces the impact of radiated noise from the switching events of a power module. A single-ended signal can be converted to a differential signal by transmitting both the original signal and its complement in two closely coupled wires. At the receiver, the two signals are compared in order to reconstruct the original signal. Figure 21 illustrates this principle with an example of induced noise forced onto the cable somewhere between the transmitter and receiver. The noise affects both the original signal and the complement by the same magnitude assuming that the cables are consistently coupled. Thus, when the receiver compares the two signals, the difference is unaffected by the noise induced on the line and the intended original signal is recreated.

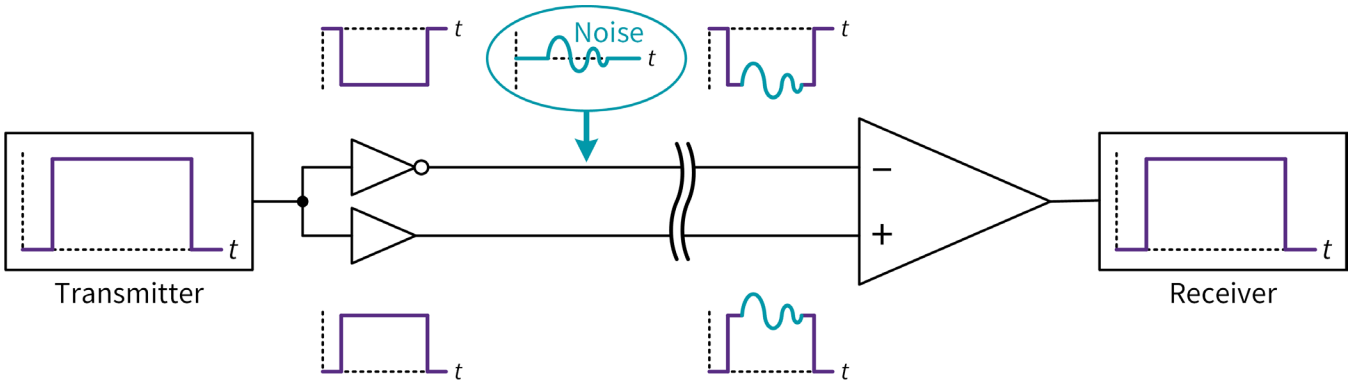

Figure 21: Noise immunity improvement provided by differential signaling

The 62 mm family of gate drivers require differential communication for proper performance. This can be achieved through differential transceivers included directly on a control board or using a single-ended to differential transceiver board. Wolfspeed provides the CGD12HB00D 2-channel differential transceiver companion tool for adding differential signaling to projects. Figure 24 and Figure 25 show example implementations of connecting the CGD12HB00D companion tool to differential gate drivers. For a reference design which adds differential transceivers directly to the control board, see the control board design from the CRD300DA12E-XM3 inverter. The differential circuit implemented on the CGD1**2**00HB2P-BM2/3 gate driver boards is shown in Figure 22, and the implementation on the CGD1**7**00HB2P-BM2/3 gate driver boards is shown in Figure 23.

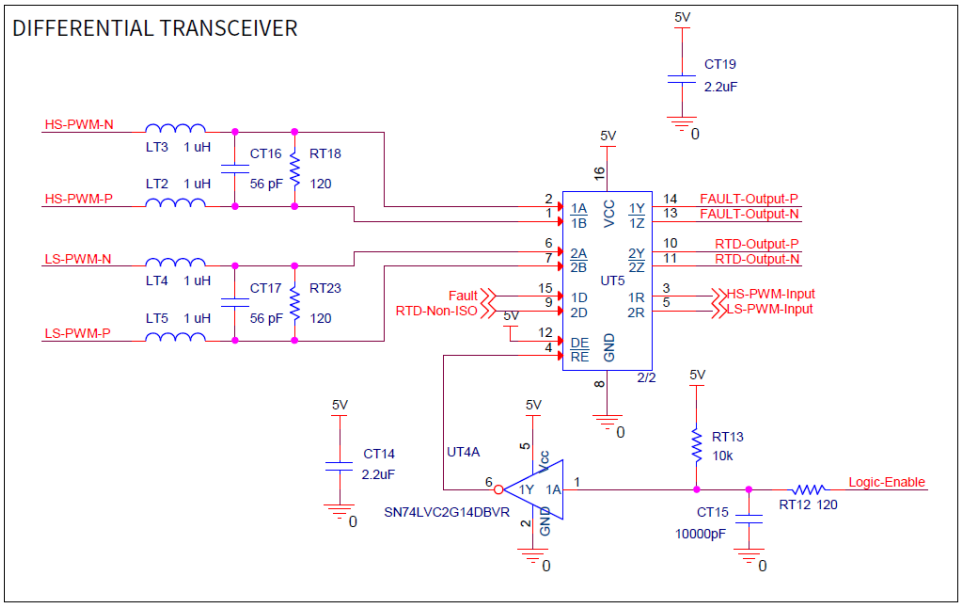

*Figure 22: CGD1**2**00HB2P-BM2/3 differential signaling circuit*

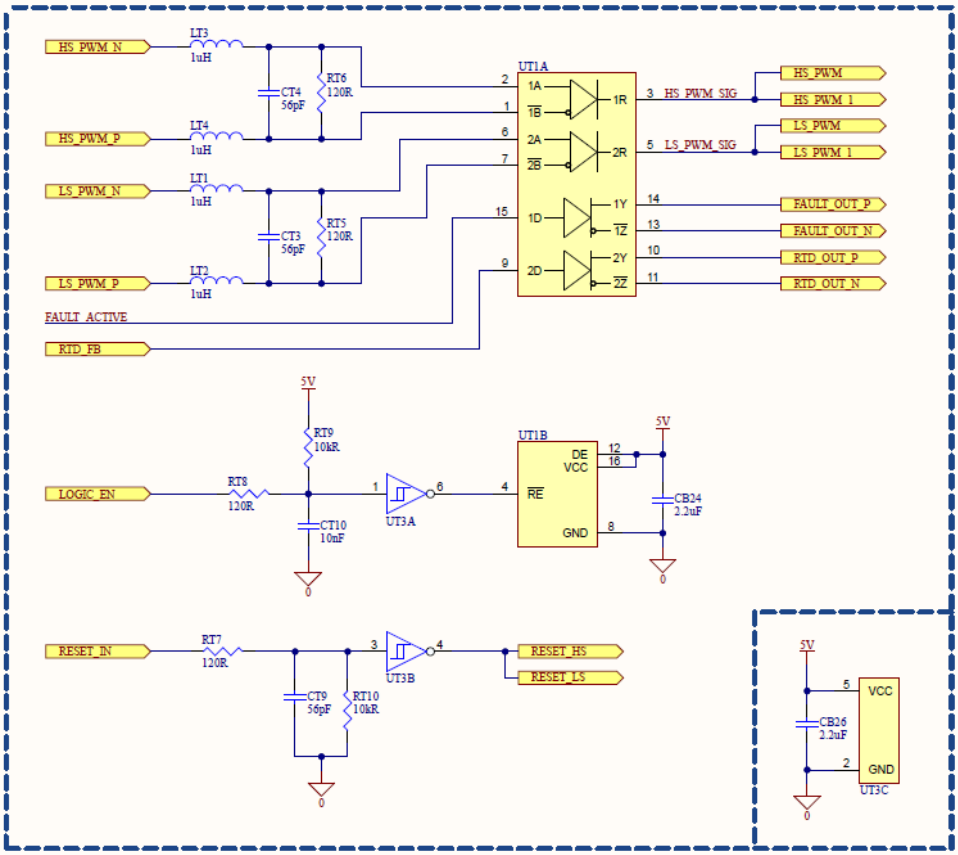

*Figure 23: CGD1**7**00HB2P-BM2/3 differential signaling circuit*

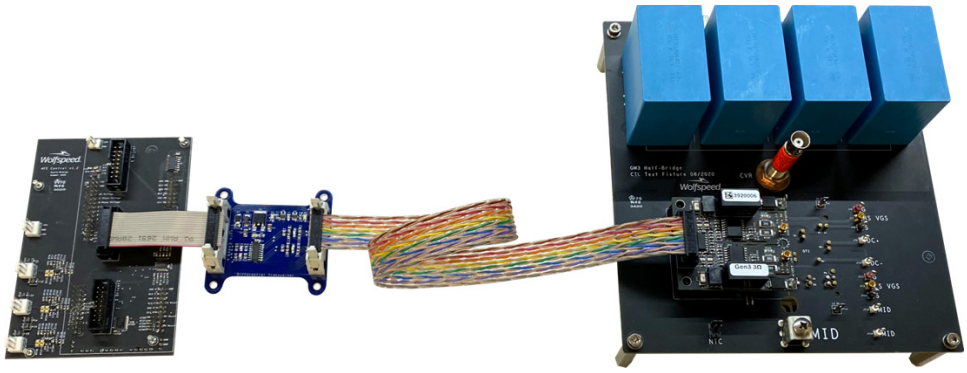

Figure 24: Wolfspeed CDB12HB00D differential transceiver companion board implementation (GM module)

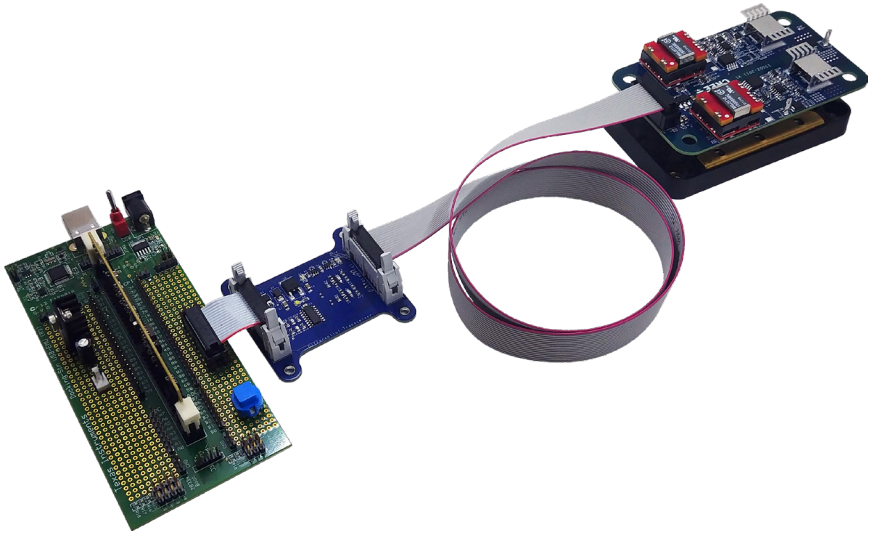

Figure 25: Wolfspeed CDB12HB00D differential transceiver companion board implementation (HM module)

4.3 Adjustable Output Voltages

As discussed in Section 1, the only difference between 62 mm gate drivers within the same voltage node is the output voltage. The gate drivers in the same voltage node use the same printed circuit board layouts but simply vary on which components are populated. The basic power regulation circuitry for all the 62 mm gate drivers is shown in Figure 26, and this section details the differences in power circuit implementations.

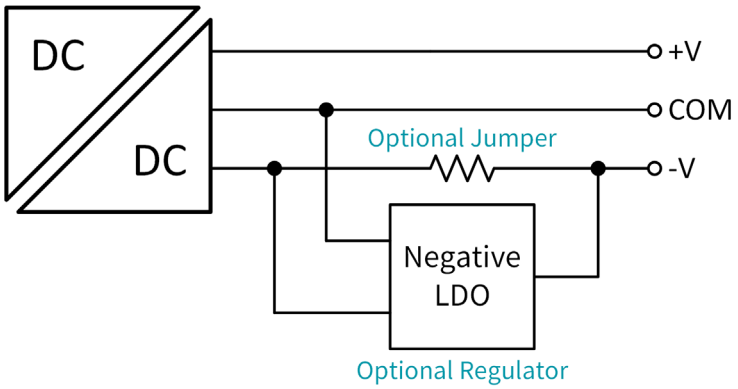

Figure 26: Power regulation circuitry used in all 62 mm gate drivers

4.3.1 Isolated DC/DC Converter

All the variants use an isolated DC/DC converter to serve as the isolation barrier and to generate unregulated voltage rails. The isolated DC/DC converter used in each variant along with the corresponding output voltages are summarized in Table 12. The exact implementation of the isolated DC/DC converter on the CGD1**2**00HB2P-BM2/3 designs is shown in Figure 27 and in Figure 28 for the CGD1**7**00HB2P-BM2/3 designs.

Table 12: Isolated DC/DC converters used for each CGD1700HB2M-UNA variation

Part Number	Isolated DC/DC Converter	DC/DC Converter Voltages
CGD1200HB2P-BM2	Murata MGJ2D122005SC	+20 V / -5 V
CGD1200HB2P-BM3	Murata MGJ2D121505SC	+15 V / -5 V*
CGD1700HB2P-BM2	Murata MGJ2D122005SC	+20 V / -5 V
CGD1700HB2P-BM3	Murata MGJ2D121505SC	+15 V / -5 V*

* Not the final output voltages of the gate driver; the design includes further voltage conditioning

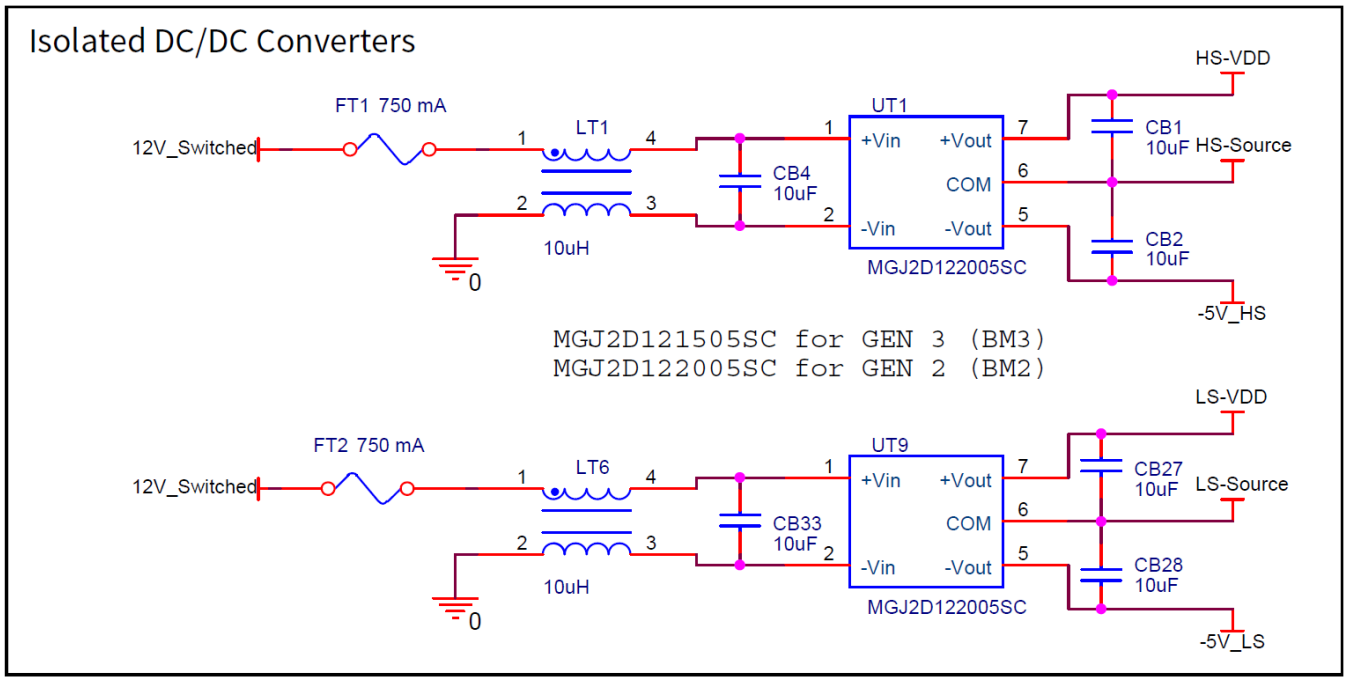

*Figure 27: CGD1**2**00HB2P-BM2/3 isolated power supply circuits*

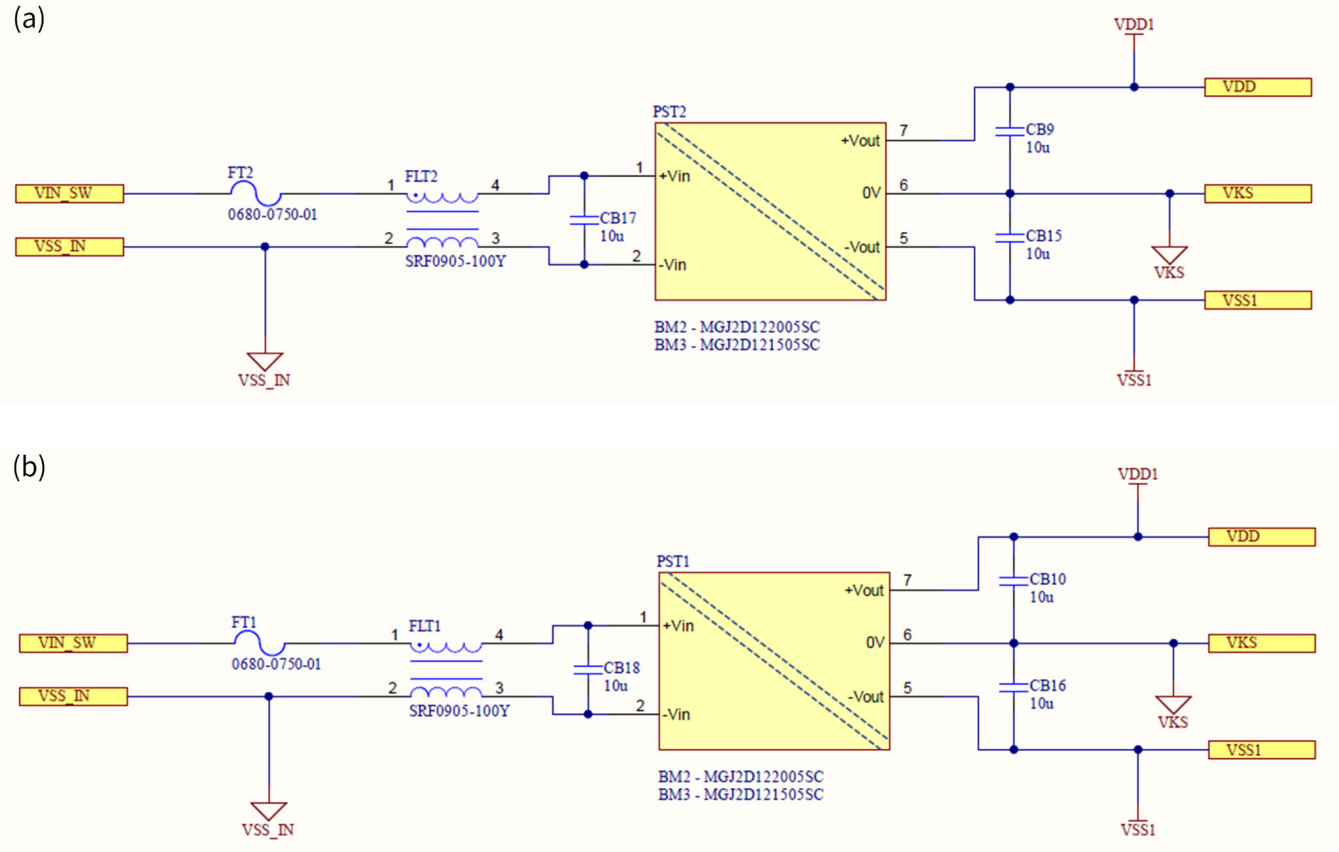

*Figure 28: CGD1**7**00HB2P-BM2/3 isolated power supply circuits: (a) high-side and (b) low-side*

4.3.2 Linear Regulators

For the CGD1x00HB2P-BM**2** variants, the optional jumpers – shown notionally in Figure 26 – are populated and the low dropout (LDO) linear regulators are not populated. In these cases, the isolated DC/DC converter generates the final gate driver output voltages (+20 V / -5 V). For the CGD1x00HB2P-BM**3** variants, the default output voltages of the DC/DC converter (+15 V / -5 V) do not match the turn-off recommended gate driver voltage of the Gen. 3 Wolfspeed devices (-4 V). For these drivers, the optional LDO linear regulators – shown notionally in Figure 26 – are populated and the jumpers are not populated. The regulators are configured to reduce the turn-off voltage to -4 V to create the final gate driver voltages (+15 V / -4 V).

The optional jumpers and regulators implementation for the CGD1**2**00HB2P-BM2/3 gate drivers is shown in Figure 29. The figure is specifically for the CGD1**2**00HB2P-BM**3** gate driver since the optional jumpers **are not** populated and the optional linear regulators **are** populated (indicating a default output voltage of -4 V). The optional jumpers and regulators implementation for the CGD1**7**00HB2P-BM2/3 gate drivers is shown in Figure 30. The figure is specifically for the CGD1**7**00HB2P-BM**2** gate driver since the optional jumpers **are** populated and the optional linear regulators **are not** populated (indicating a default output voltage of -5 V). The populated components for each variation type are shown in Table 13 for the CGD1**2**00HB2P-BM2/3 gate drivers and Table 14 for the CGD1**7**00HB2P-BM2/3 gate drivers. Note that these component values can be modified to create different turn-off output voltages as will be discussed in Section 4.3.4.

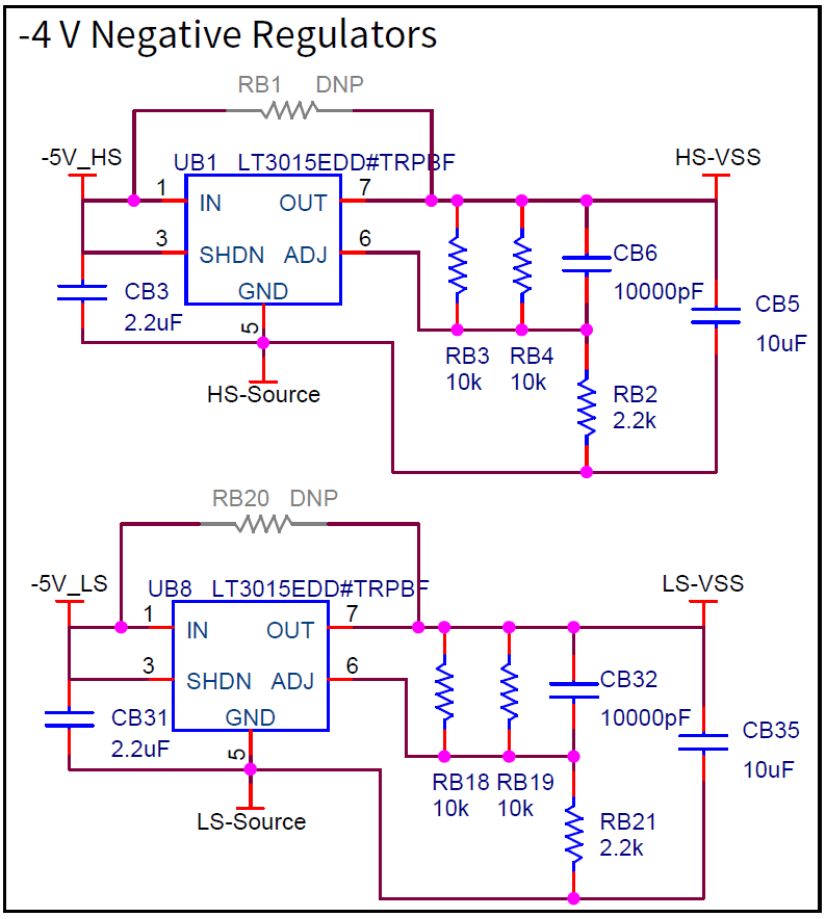

Figure 29: Optional jumpers and negative linear regulator circuits for CGD1**2**00HB2P-BM2/3 gate drivers

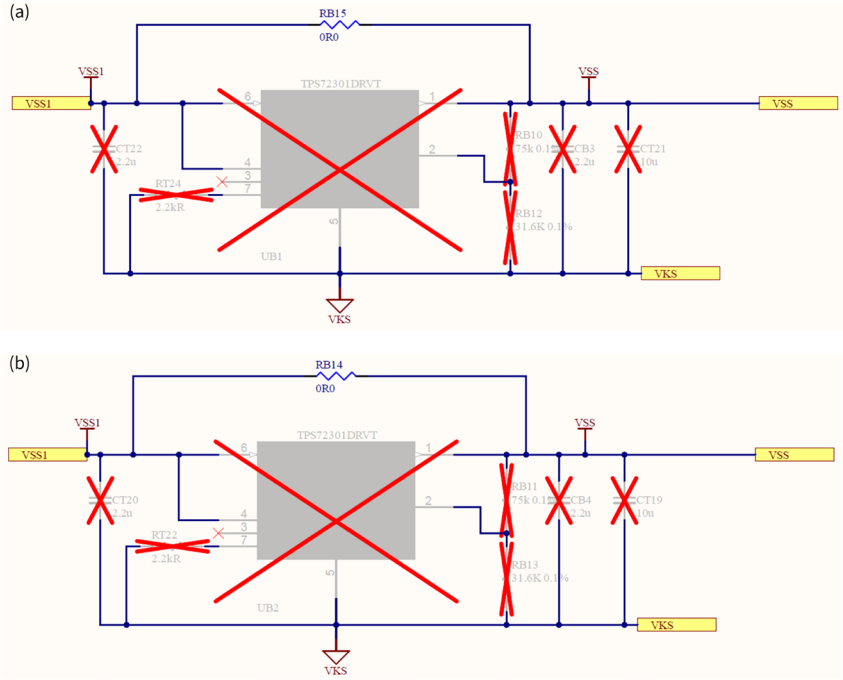

*Figure 30: Optional jumpers and negative linear regulator circuits for CGD1**7**00HB2P-BM2/3 gate drivers*

*Table 13: Populated components on CGD1**2**00HB2P-BM2/3 gate drivers for generating negative bias voltage*

Part Number	UB1 UB8	RB1 RB20	RB3 RB18	RB4 RB19	RB2 RB21	CB3 CB31	CB6 CB32	CB5 CB35
CGD1200HB2P-BM2	DNP	0 Ω	DNP	DNP	DNP	DNP	DNP	DNP
CGD1200HB2P-BM3	Analog Devices LT3015EDD#TRPBF	DNP	10 kΩ	10 kΩ	2.2 kΩ	2.2 µF	10 nF	10 µF

* DNP : Do Not Populate

*Table 14: Populated components on CGD1**7**00HB2P-BM2/3 gate drivers for generating negative bias voltage*

Part Number	UB1 UB2	RB14 RB15	RB10 RB11	RB12 RB13	RT22 RT24	CB3 CB4	CB19 CB21	CT20 CT22
CGD1700HB2P-BM2	DNP	0 Ω	DNP	DNP	DNP	DNP	DNP	DNP
CGD1700HB2P-BM3	Texas Instruments TPS72301DRVT	DNP	75 kΩ	31.6 kΩ	2.2 kΩ	2.2 µF	10 µF	2.2 µF

* DNP : Do Not Populate

4.3.3 Add Negative Voltage Regulation

Since the Gen. 2 variants of the 62 mm gate drivers (CGD1**2**00HB2P-BM**2** and CGD1**7**00HB2P-BM**2**) use the same PCB design as the Gen. 3 model variations (CGD1**2**00HB2P-BM**3** and CGD1**7**00HB2P-BM**3**), the Gen. 2 gate driver variants can be easily modified to add voltage regulation. Some cases where this could be useful include changing the output voltage to evaluate SiC MOSFET performance in other operating conditions or re-purposing the gate driver for a new application (such as supporting newer generations of devices). To add regulation to a Gen. 2 gate driver, simply adjust the components listed in Table 12 to the correct isolated DC/DC converter and adjust the negative bias components in either Table 13 or Table 14 depending on which gate driver is being upgraded. The exact components used for the different variations are included in the bill of materials (BOM) provided on the gate driver website landing pages (CGD1**2**00HB2P-BM**2**, CGD1**2**00HB2P-BM**3**, CGD1**7**00HB2P-BM**2**, or CGD1**7**00HB2P-BM**3**). To change the output voltage to a non-standard output voltage, follow the steps discussed in Section 4.3.4.

4.3.4 Change Output Voltages

In order to change the positive gate driver output voltage or to increase the negative gate driver output voltage magnitude, the isolated DC/DC converters discussed in Section 4.3.1 can be replaced to ones with different output voltages. These DC/DC converters can be swapped with any isolated converter in the same 7-SIP, 5-Lead package footprint. Notably, any DC/DC converter that is used will need to have a suitable isolation rating for the target operating voltage, since the component bridges the gate driver isolation barrier. Recommended DC/DC converters are the Murata MGJ2 series and RECOM RxxP2xxyy series of DC/DC converters.

In order to decrease the negative gate driver output voltage magnitude, the negative linear regulators discussed in Section 4.3.2 can be tuned. Note that this procedure assumes that the gate driver board being modified already includes the negative linear regulators. Therefore, if starting with the CGD1**2**00HB2P-BM**2** or CGD1**7**00HB2P-BM**2** gate driver, first follow the procedure outlined in Section 4.3.3 to add the negative linear

regulators. With the negative linear regulators installed, to change the turn-off voltage, change the feedback resistor network on the negative linear regulator to adjust the voltage using the equation below. Note that the range of the linear regulators is limited by the negative regulator range and the isolated DC/DC converter outputs. The output voltage of the linear regulators can be adjusted between -1.2 V and (V_{DCDC-} + 0.28 V). See the Texas Instruments TPS72301DRVT datasheet for more information. Resistors with tolerances less than or equal to 1% should be used for the best performance.

$$V_{GATE,LOW} = -1.186\ V\left(1 + \frac{R_1}{R_2}\right)$$

$$R_1 + R_2 \approx 100\ k\Omega$$

where

R_1: bias resistor attached between the feedback pin and the output voltage rail [Ω]
R_2: bias resistor attached between the feedback pin and the common rail [Ω]

The calculation for the default circuit configuration of -4 V for Gen. 3 gate drivers is shown below for reference.

$$-1.186\ V\left(1 + \frac{75\ \text{k}\Omega}{31.6\ k\Omega}\right) = -4\ V$$

$$75\ k\Omega + 31.6\ k\Omega = 106.6\ k\Omega \approx 100\ k\Omega$$

The SiC power MOSFETs are not intended to be operated continuously in the linear region, so the user should ensure that the selected voltages are within the safe operating area of the device. Although it is possible to change the output voltage to non-standard voltages, this is not recommended for most applications. This guide is intended to be informative for users testing systems in edge conditions or for evaluating how the system handles faulty conditions. Also, the overcurrent protection circuit blanking time is biased from the output-high voltage rail (see Section 4.4.4), so modifying this voltage can influence the trip timing of the overcurrent protection circuit.

4.4 Faults / Protections

The 62 mm family of gate drivers are protected from input +12 V power quality issues, isolated power supply issues, signal overlap, and overcurrent events. This section discusses these faults in more detail and how to adjust them. Table 15 provides a logic table summary indicating the state of the gate driver outputs depending on the various input signals and/or fault statuses. The UVLO and overcurrent faults of each gate driver channel are combined into a single global fault signal that is transmitted to the controller, as shown in Figure 31 for the CGD1**2**00HB2P-BM2/3 gate drivers and Figure 32 for the CGD1**7**00HB2P-BM2/3 gate drivers.

Table 15: Output logic table depending on inputs and faults

PWM	$\overline{\text{PWM-EN}}$	$\overline{\text{PS-DIS}}$	RESET	Overcurrent/ UVLO	$\overline{\text{FAULT}}$	Output
H	H or Z	H or Z	L	No	H	H
L	H or Z	H or Z	L	No	H	L
X	L	H or Z	L	No	H	L
X	X	L	X	No	L	Z
X	H or Z	H or Z	L	Yes	L	L
X	H or Z	H or Z	H	No	H	L

H = High | L = Low | X = Irrelevant | Z = High Impedance

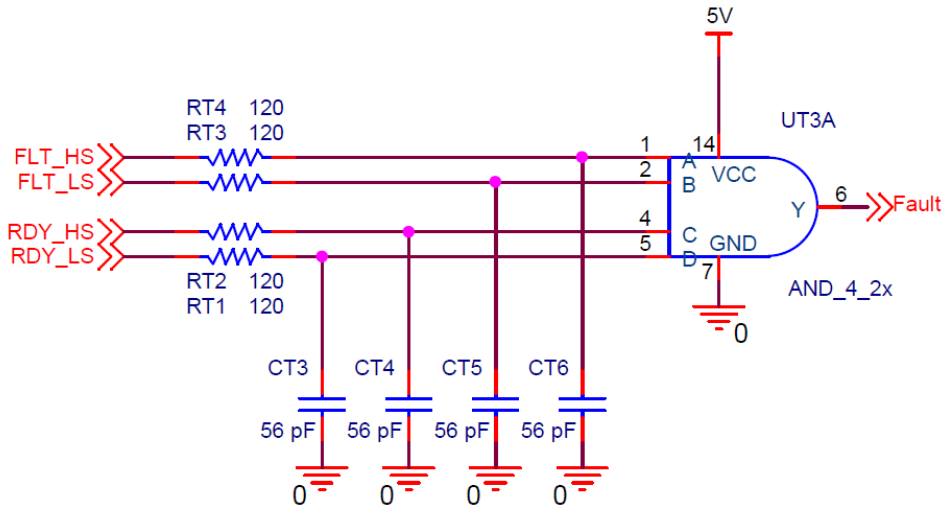

*Figure 31: Fault combination into single global fault signal on CGD1**2**00HB2P-BM2/3 gate drivers*

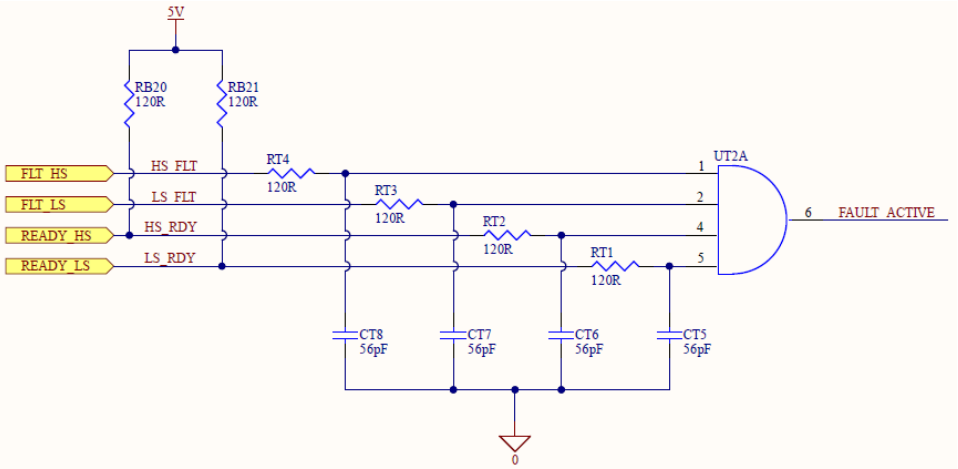

*Figure 32: Fault combination into single global fault signal on CGD1**7**00HB2P-BM2/3 gate drivers*

4.4.1 Input Voltage Protection

The 62 mm family of gate drivers all include overvoltage and reverse voltage protection on the +12 V power input (pin 1) of the input connectors. The implemented overvoltage and reverse voltage protection circuit is shown in Figure 33 for the CGD1**2**00HB2P-BM2/3 gate drivers and Figure 34 for the CGD1**7**00HB2P-BM2/3 gate drivers. The Zener diode protects from input voltage spikes greater than 20 V (nominal) and the P-channel MOSFET protects from the positive and negative voltage polarities being reversed. Incorrect connections should still be avoided when using these gate drivers, though these circuit elements are included to protect the system if it is incorrectly wired.

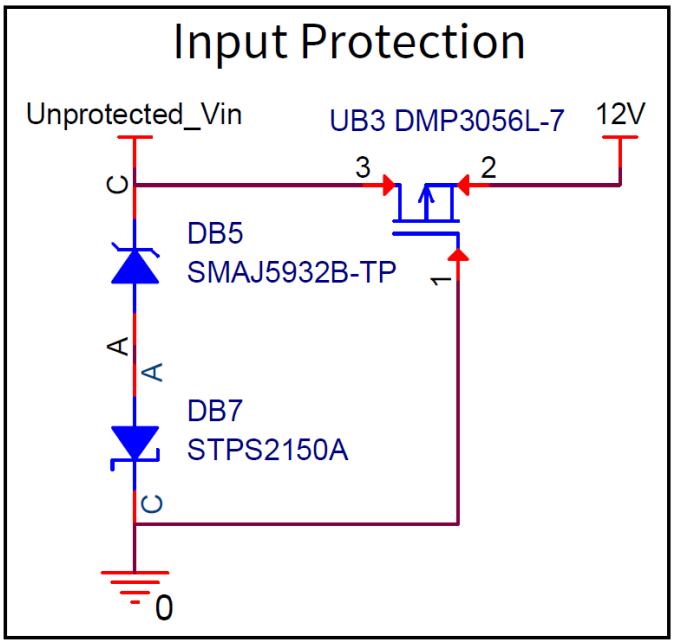

*Figure 33: Input overvoltage and reverse voltage protection circuit on CGD1**2**00HB2P-BM2/3 gate drivers*

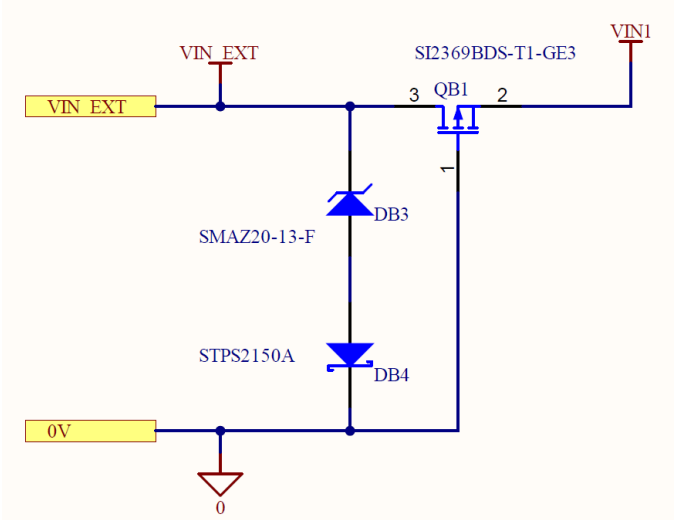

*Figure 34: Input overvoltage and reverse voltage protection circuit on CGD1**7**00HB2P-BM2/3 gate drivers*

The 62 mm gate driver family also includes input overcurrent protection through a power management circuit shown in Figure 35 for the CGD1**2**00HB2P-BM2/3 gate drivers and Figure 36 for the CGD1**7**00HB2P-BM2/3 gate drivers. The protection is implemented with the MP5000A programmable current limit switch manufactured by Monolithic Power Systems Inc.® for all the 62 mm gate drivers, and the power management IC can be enabled/disabled through the $\overline{PS\text{-}DIS}$ signal to remotely power on or off the gate driver. This feature can be useful for system start-up sequencing to avoid many gate drivers simultaneously powering on and potentially causing power rail droop.

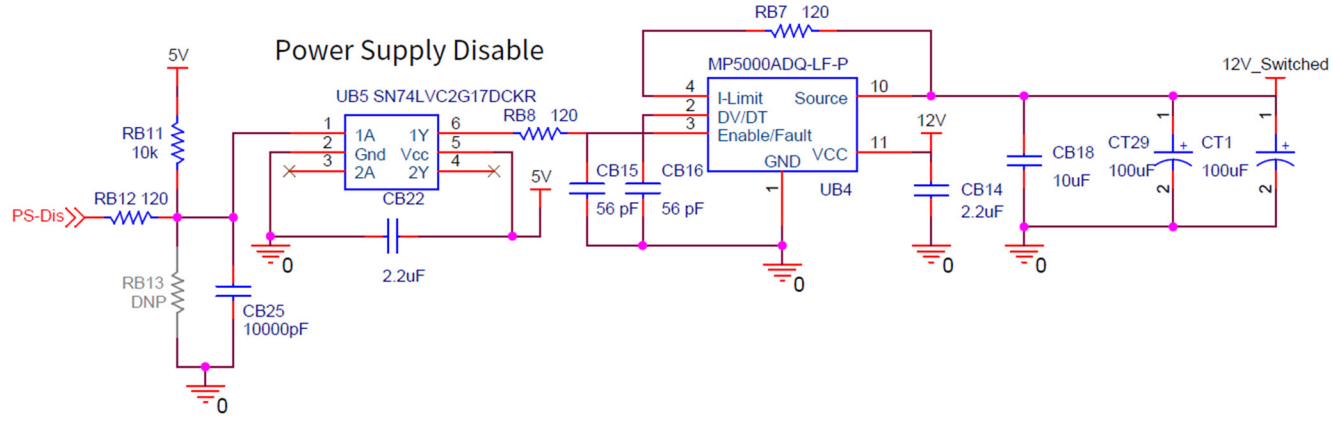

*Figure 35: Inrush current protection and power disable circuit on CGD1**2**00HB2P-BM2/3 gate drivers*

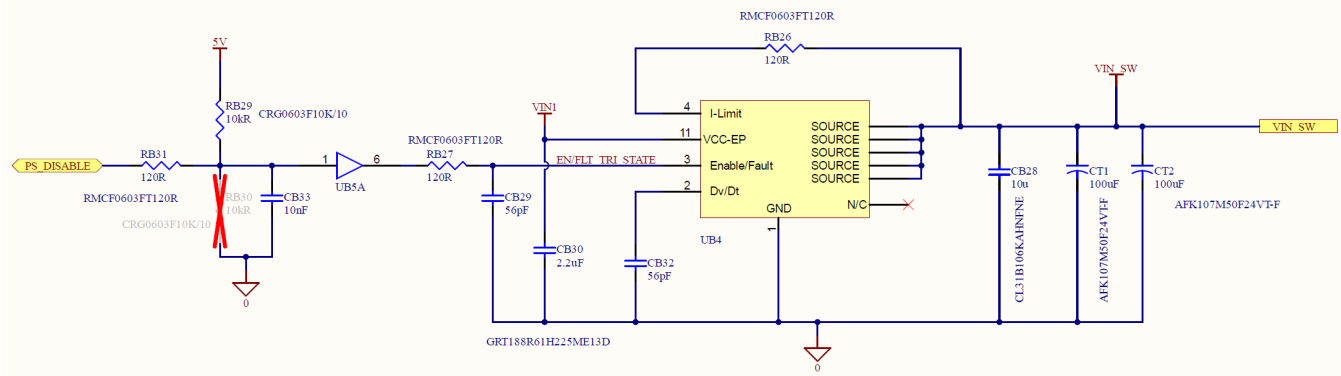

*Figure 36: Inrush current protection and power disable circuit on CGD1**7**00HB2P-BM2/3 gate drivers*

4.4.2 Undervoltage Lockout

The Analog Devices ADuM4135 and ADuM4146C gate driver ICs used on the 62 mm family of gate drivers both feature integrated UVLO. The UVLO circuit detects when the output rails of the isolated DC/DC converter fall below safe operating conditions for the gate driver. A UVLO fault indicates that the potential between the split output voltage rails has fallen below the UVLO active level. The gate for the channel where the fault occurred will be pulled low through $R_{G(EXT)-OFF}$ for the duration of the fault regardless of the PWM input signal. The fault will automatically clear once the potential has risen above the UVLO inactive level. There is hysteresis for this fault to ensure safe operating conditions. The UVLO faults for both channels are combined along with the overcurrent fault in the $\overline{FAULT}$ output signal. When there is no UVLO fault present, a green LED indicates a power good state, as discussed in Section 3.5.

4.4.3 Overcurrent Fault

An overcurrent (OC) fault is an indication of a shoot-through or elevated current event in the SiC power module. The overcurrent protection circuit is implemented through a desaturation (DESAT) circuit which measures the drain-to-source voltage (V_{DS}). The fault will indicate if this voltage has risen above an acceptable current level based on the I_D vs V_{DS} characteristics of the device. When a fault has occurred, the corresponding gate driver channel will be disabled, and the gate will be pulled down through a soft turnoff circuit. The equivalent drain-to-source voltage for a particular overcurrent limit can be configured through onboard resistors. The overcurrent fault is latched upon detection and must be cleared by the user/controller with a high pulse of at least 500 ns on the $RESET$ signal of the gate driver. The CGD1**2**00HB2P-BM2/3 ADuM4135 gate driver ICs with overcurrent protection and output connections are shown in Figure 37 for the high side and Figure 38 for the low side. The CGD1**7**00HB2P-BM2/3 ADuM4146C gate driver ICs with overcurrent protection and output connections are shown in Figure 39 for the high side and Figure 40 for the low side. The various timing and voltage trip levels presented in Table 3 and Section 4.4.4 are defined notionally in the timing diagram shown in Figure 41.

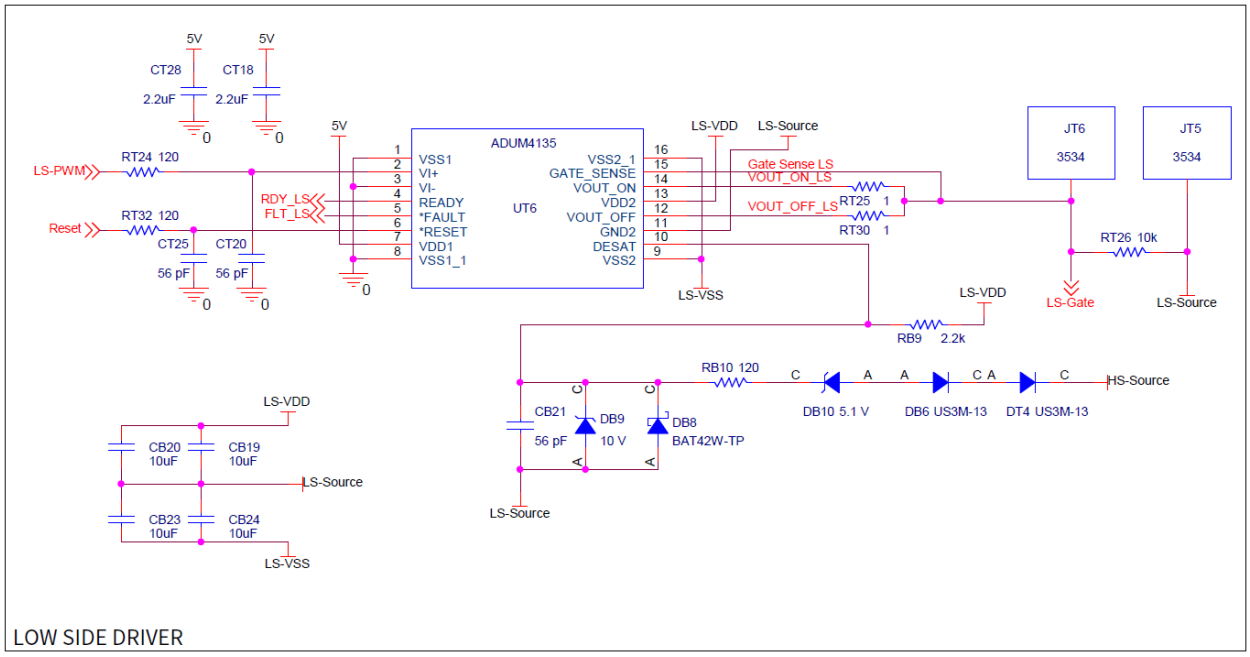

*Figure 37: CGD1**2**00HB2P-BM2/3 low-side gate driver circuit with overcurrent protection*

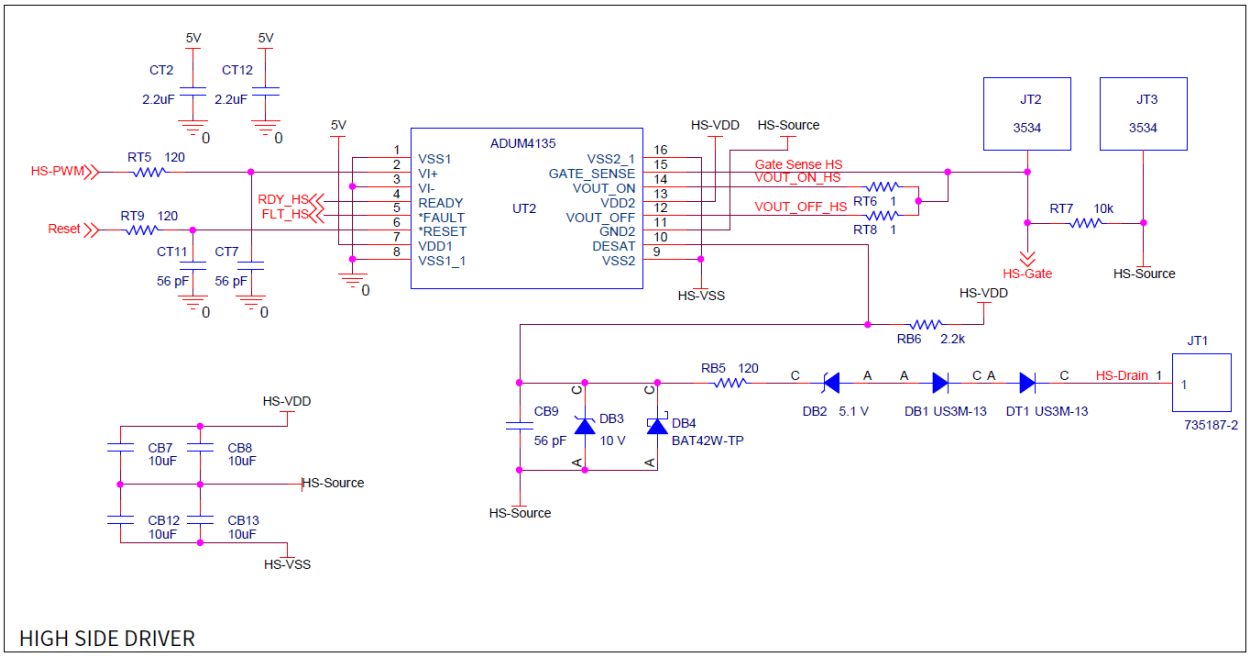

*Figure 38: CGD1**2**00HB2P-BM2/3 high-side gate driver circuit with overcurrent protection*

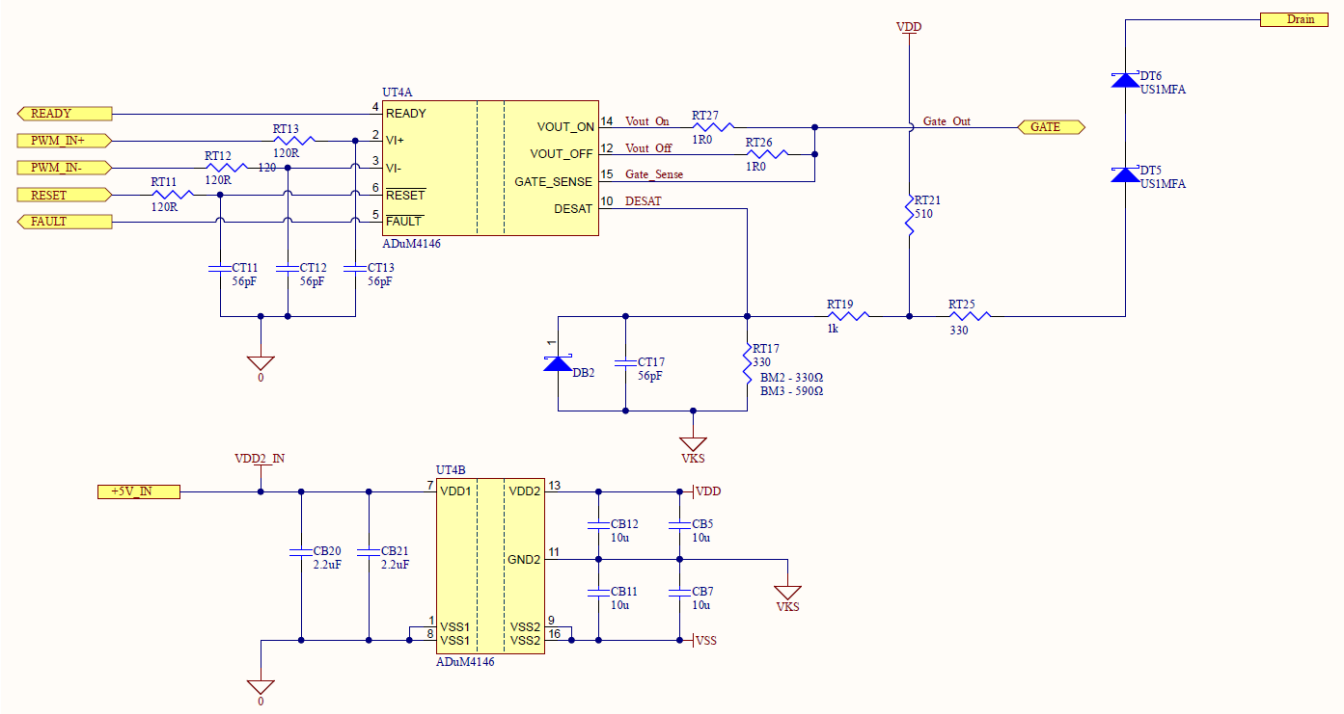

*Figure 39: CGD17**7**00HB2P-BM2/3 low-side gate driver circuit with overcurrent protection*

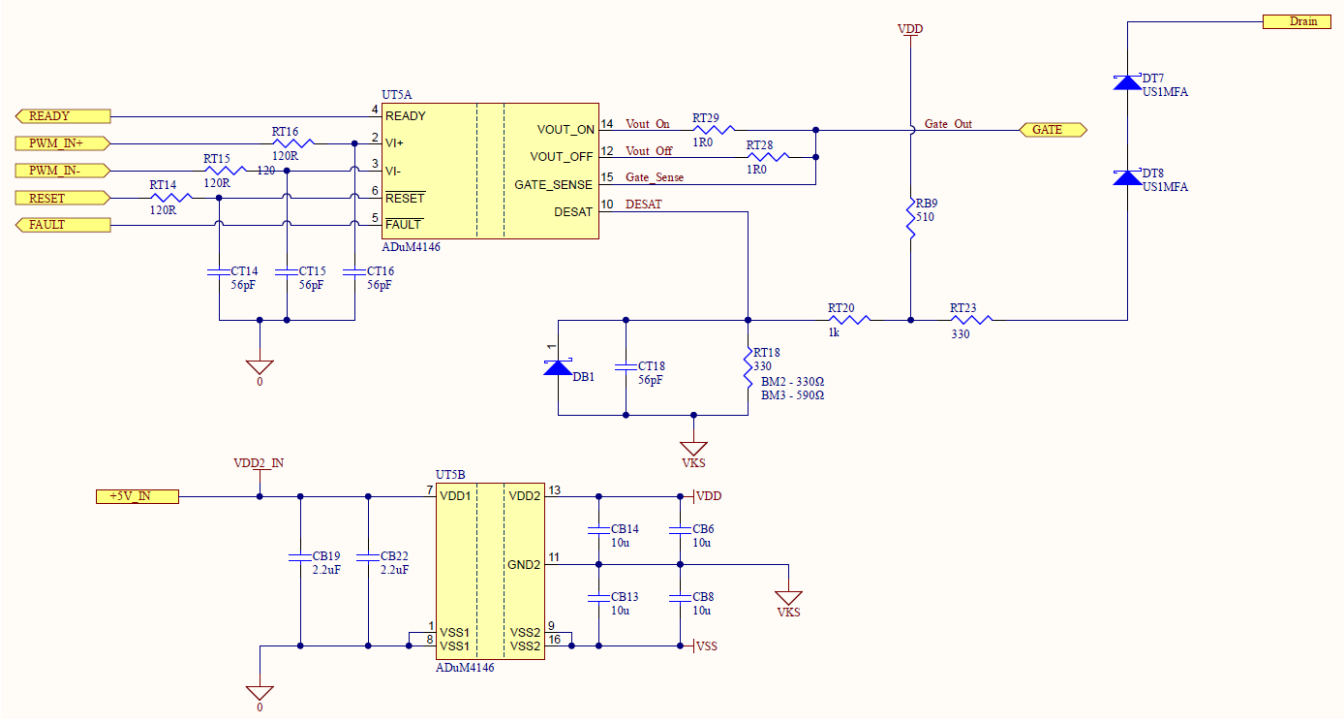

*Figure 40: CGD17**7**00HB2P-BM2/3 high-side gate driver circuit with overcurrent protection*

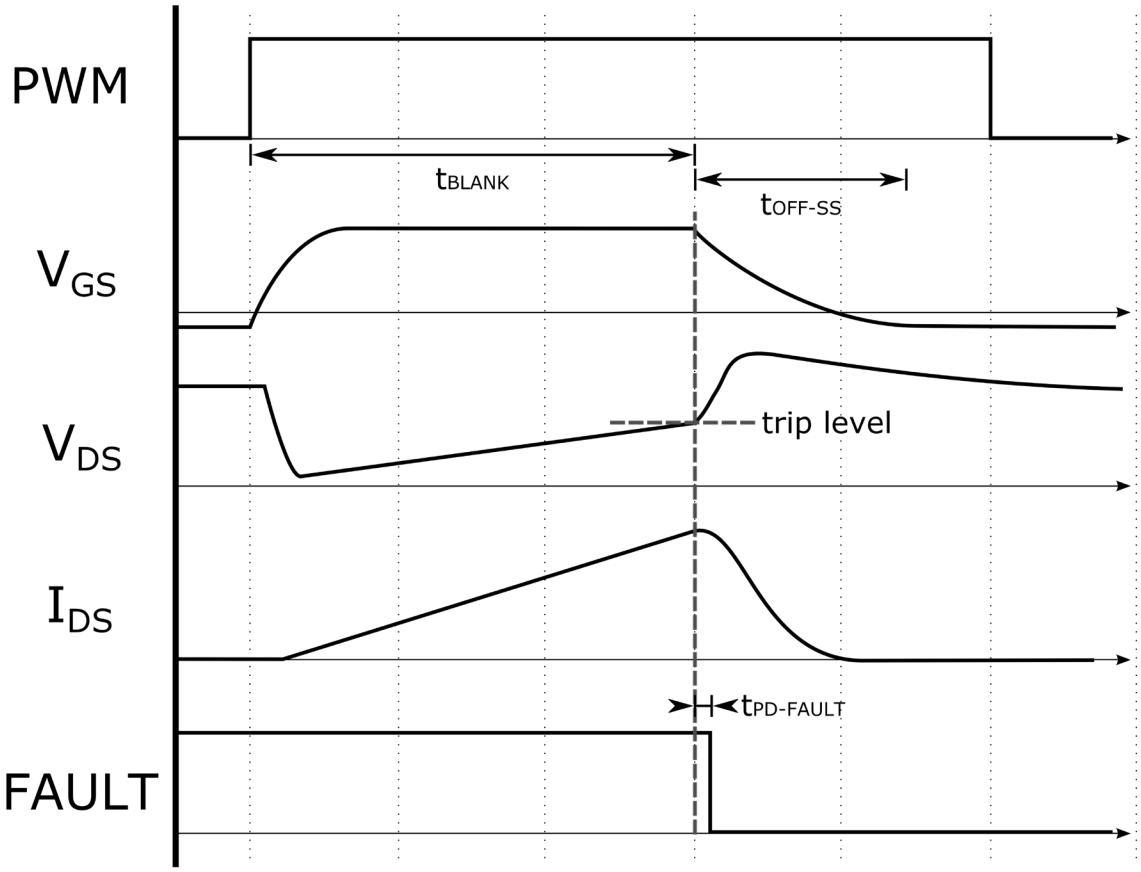

Figure 41: Overcurrent fault timing diagram

4.4.4 Overcurrent Trip Level

The OC fault detection circuits, shown in Section 4.4.3, monitor the on-state V_{DS} across each switch position and trigger a fault condition if the voltage rises above the predefined set level for a predefined amount of time (blanking time) while the device is on. The CGD1**2**00HB2P-BM2/3 and CGD1**7**00HB2P-BM2/3 gate drivers handle overcurrent trip level tuning differently, which are described separately below.

CGD1200HB2P-BM2/3 Overcurrent Trip

The internal comparator trip voltage in the ADuM4135 gate driver IC used on the CGD1**2**00HB2P-BM2/3 gate drivers is 9 V. The circuit is simplified into the notional diagram shown in Figure 42. Considering the forward voltage of the high-voltage blocking diodes and a tunable Zener diode, the over-current trip level is calculated with the following equation:

$$V_{OC-Trip} = 9\,V - V_Z - N_D \cdot V_F$$

where

$V_{OC-Trip}$: target overcurrent trip voltage [V]
V_Z: Zener diode voltage [V]
N_D: number of series high-voltage blocking diodes
V_F: forward voltage of the high-voltage blocking diode(s) [V].

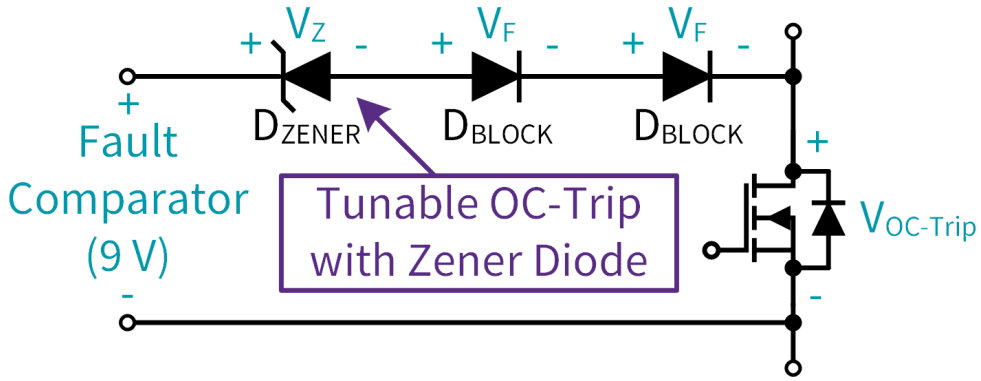

*Figure 42: Notional overcurrent fault circuit on CGD1**2**00HB2P-BM2/3 gate drivers*

To select an appropriate overcurrent trip level, refer to the I_D vs. V_{DS} output characteristic curves in the applicable power module datasheet. As an example, the pulse-current rating of Wolfspeed's CAS530M12BM3 is 1060 A at T_J = 25 °C; therefore, an overcurrent trip point of 1000 A at 25 °C is selected. On the I_D vs. V_{DS} curve, the drain-to-source voltage at the 1000 A operating condition is approximately 2.9 V. Hence, the overcurrent trip voltage, $V_{OC\text{-}Trip}$, should be approximately 2.9 V. Using this value and with the values from the schematic (shown below), the necessary Zener diode voltage, V_Z, can be calculated, as shown below.

$V_{OC-Trip}$: 2.9 V (from the datasheet I_D vs V_{DS} plot of the example module)
N_D: 2 (from gate driver schematic)
V_F: 0.5 (from high-voltage diode datasheet)

$$V_Z = 9\ V - N_D \cdot V_F - V_{OC-Trip} = 9\ V - 2 \cdot 0.5\ V - 2.9\ V = 5.1\ V$$

By default, the CGD1**2**00HB2P-BM2/3 gate drivers are configured with a 2.9 V overcurrent trip voltage using a 5.1 V Zener diode voltage (Nexperia® PDZ5.1BGW). To change the trip value, follow the calculation procedures discussed above to determine the appropriate Zener diode voltage to adopt. The Zener diodes use a SOD123 package such as the PDZ-GW series from Nexperia. The Zener diodes are reference designers *DT3* (high-side) and *DT9* (low-side) on the circuit board.

As discussed in Section 3.3, **the high-side overcurrent connector, *JT1*, cannot be left floating as the overcurrent fault will trip immediately when the high-side gate is actuated**. If bench-top testing of the gate driver is required, it is acceptable to short this connector to the high-side source to prevent the overcurrent fault from tripping. The same phenomenon exists for the low-side, and it is acceptable to short the high-side source (low-side drain) to the low-side source for bench-top testing. An overcurrent fault condition must be acknowledged with the $RESET$ signal to return to normal operation of the gate driver. **Performing this modification will bypass the overcurrent protection**, so the gate driver will no longer be protecting the MOSFET(s).

CGD1700HB2P-BM2/3 Overcurrent Trip

The internal comparator trip voltage in the ADuM4146C gate driver IC used on the CGD1**7**00HB2P-BM2/3 gate drivers is 3.5 V. The circuit is simplified into the notional diagram shown in Figure 43. Referring to this figure, the intermediary voltages V_2 and V_X and the trip resistor, R_X, can be calculated using the following equations:

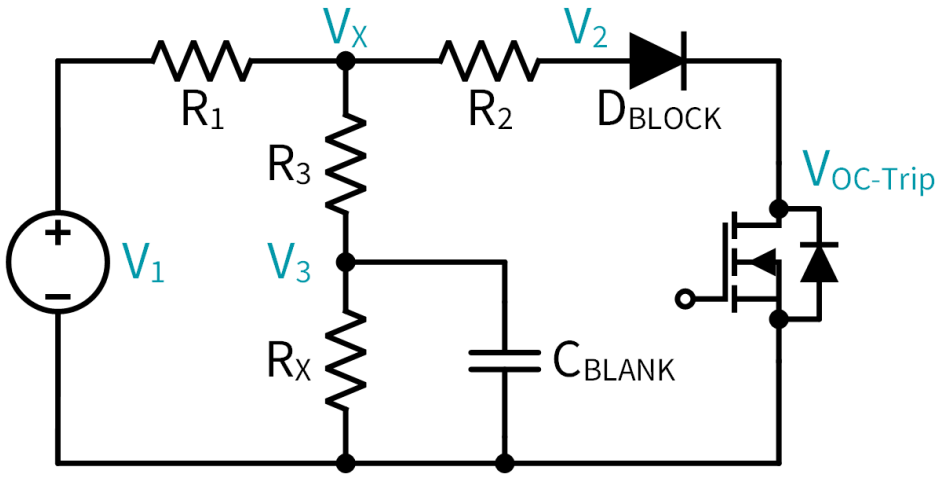

Figure 43: Notional overcurrent fault circuit

$$V_2 = V_{OC-Trip} + N_D \cdot V_F \;\; ; \;\; V_x = \frac{R_2\, R_3\, V_1 + R_1\, R_3\, V_2 + R_1\, R_2\, V_3}{R_1\, R_2 + R_1\, R_3 + R_2\, R_3} \;\; ; \;\; R_X = \frac{V_3 \cdot R_3}{V_X - V_3}$$

where

V_2: intermediate voltage shown in Figure 43 [V]
$V_{OC-Trip}$: target overcurrent trip voltage [V]
N_D: number of series high-voltage blocking diodes
V_F: forward voltage of the high-voltage blocking diode(s) [V]
V_X: intermediate voltage shown in Figure 43 [V]
V_1: source voltage (output-high gate driver voltage) [V]
V_3: internal comparator trip voltage of the gate driver IC [V]
R_1, R_2, R_3: circuit resistor values [Ω]
R_X: resistor value required to trip at the appropriate overcurrent value [Ω].

To select an appropriate overcurrent trip level, refer to the I_D vs. V_{DS} output characteristic curves in the applicable module datasheet. By default, the CGD1**7**00HB2P-BM**3** has an overcurrent trip level of 6.8 V and the CGD1**7**00HB2P-BM**2** has an overcurrent trip level of 16 V. Using the CGD1**7**00HB2P-BM**3** value as an example and with the values from the schematic (shown below), the necessary trip resistor, R_X, can be calculated, as shown below.

$V_{OC-Trip}$: 6.8 V
N_D: 2 (from gate driver schematic)
V_F: 0.5 (from high-voltage diode datasheet)
V_1: 15 V (from gate driver schematic)
V_3: 3.5 V (from the Analog Device ADuM4146C datasheet)
R_1: 510 Ω; R_2: 330 Ω; R_3: 1 kΩ (from gate driver schematic)

$$V_2 = 6.8\,V + 2 * \; 0.5\,V \rightarrow \boldsymbol{V_2 = 7.8\,V}$$

$$V_x = \frac{330\ \Omega * 1000\ \Omega * 15\ V + 510\ \Omega * 1000\ \Omega * 7.8\ V + 510\ \Omega * 330\ \Omega * 3.5V}{510\ \Omega * 330\ \Omega + 510\ \Omega * 1000\ \Omega + 330\ \Omega * 1000\ \Omega} \rightarrow \boldsymbol{V_x = 9.44\ V}$$

$$R_x = \frac{3.5\ V * 1000\ \Omega}{9.44\ V - 3.5\ V} = \frac{3500}{5.94} \rightarrow \mathbf{R_x = 590\ \Omega}$$

By default, the CGD1**7**00HB2P-BM**3** gate driver is therefore configured with a 590 Ω resistor for R_x. To change the trip value, follow the calculation procedures discussed above. As discussed in Section 3.3, **the overcurrent connectors, *JT3* and *JT4*, cannot be left floating as the overcurrent fault will trip immediately when the gate is actuated**. If bench-top testing of the gate driver is required, it is acceptable to short the connector to the appropriate source to prevent the overcurrent fault from tripping. **Performing this modification will disable the overcurrent protection.**

4.4.5 Miller Clamp

When a switch position is in the off state, high *dV/dt* in other switch positions can cause current flow through the Miller capacitance of a MOSFET and ultimately induce noise into the gate. To prevent false turn-on of the device, it is important that the gate driver has a low-impedance to the turn-off voltage when the device is off to ensure the gate of the MOSFET is held low. The Analog Devices ADuM4135 and ADuM4146C gate driver ICs employed in these designs feature an integrated Miller clamp circuit. When the gate voltage drops below a ~2 V internal reference, the Miller clamp latch is engaged, which is a low-impedance connection to the output-low voltage rail. In this configuration, the external turn-off resistor still controls the turn-off dynamics, and the gate driver has a low-impedance connection to dissipate Miller charge even when a high-valued turn-off resistor is employed.

4.4.6 Interlock Protection

In a half-bridge circuit, commanding both channels on simultaneously short-circuits the bus and can cause extreme currents. While the overcurrent protection circuit discussed in 4.4.3 can prevent catastrophic damage, these gate drivers also include circuitry intended to prevent both channels from being commanded on simultaneously. This interlock protection, also commonly referred to as shoot-through or anti-overlap protection, applies an XOR logic gate to the two input signals, preventing either output from going high if both signals are commanded on simultaneously, as shown in Table 16. This can help with noise rejection if noise causes one of the commanded signals to flip and it can help prevent issues from a faulty controller. Notably, this protection should not be relied upon for generating dead time. The interlock protection on the CGD1**2**00HB2P-BM2/3 gate drivers is implemented with discrete logic gates as shown in Figure 44. The interlock protection on the CGD1**7**00HB2P-BM2/3 gate drivers is implemented using the integrated protection in the Analog Devices ADuM4146C gate driver IC.

Table 16: Interlock protection logic table

HS PWM	LS PWM	$V_{GS,HS}$	$V_{GS,LS}$
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

H = High | L = Low

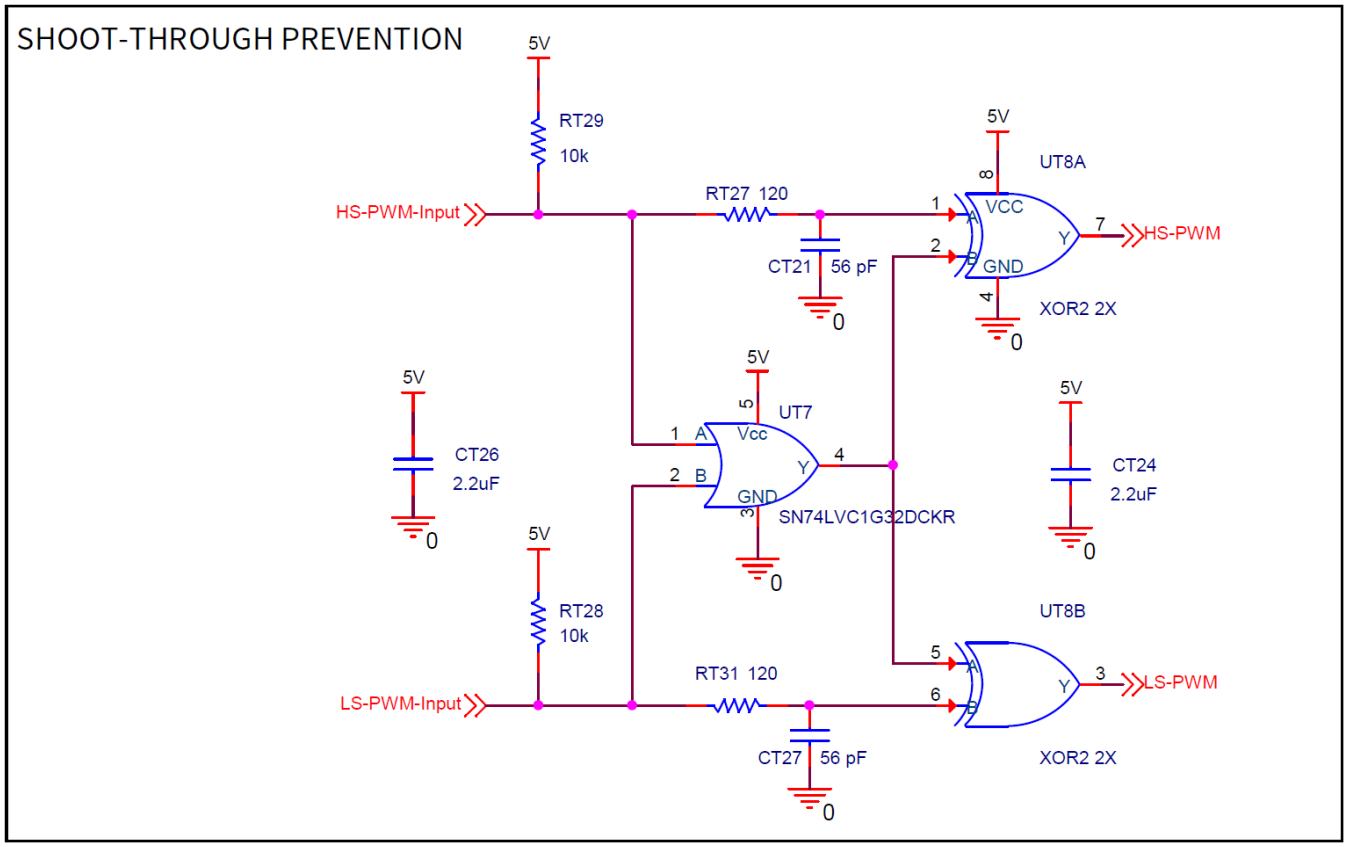

Figure 44: Interlock protection circuit on CGD1200HB2P-BM2/3 gate drivers using discrete logic gates

4.5 Soft Shutdown

When an overcurrent fault occurs, hard turn-off of the device (i.e. turning the device off normally) can induce large voltage overshoots due to the enormous *di/dt* event. To ensure the device voltage does not exceed the safe operating area, the Analog Devices ADuM4135 and ADuM4146C ICs used on the 62 mm gate drivers include an integrated soft shutdown feature. When the overcurrent fault is detected, a secondary N-channel MOSFET is used to shutdown the device. The second MOSFET has a resistance higher than the normal turn-off MOSFET. Using this approach turns the power device off in a controlled manner to reduce the chance of an overvoltage spike.

4.6 Timing Definitions

Table 3 provides various timing parameters to indicate the propagation delays of the gate driver. These timing parameters are shown visually in Figure 45 for the gate signals.

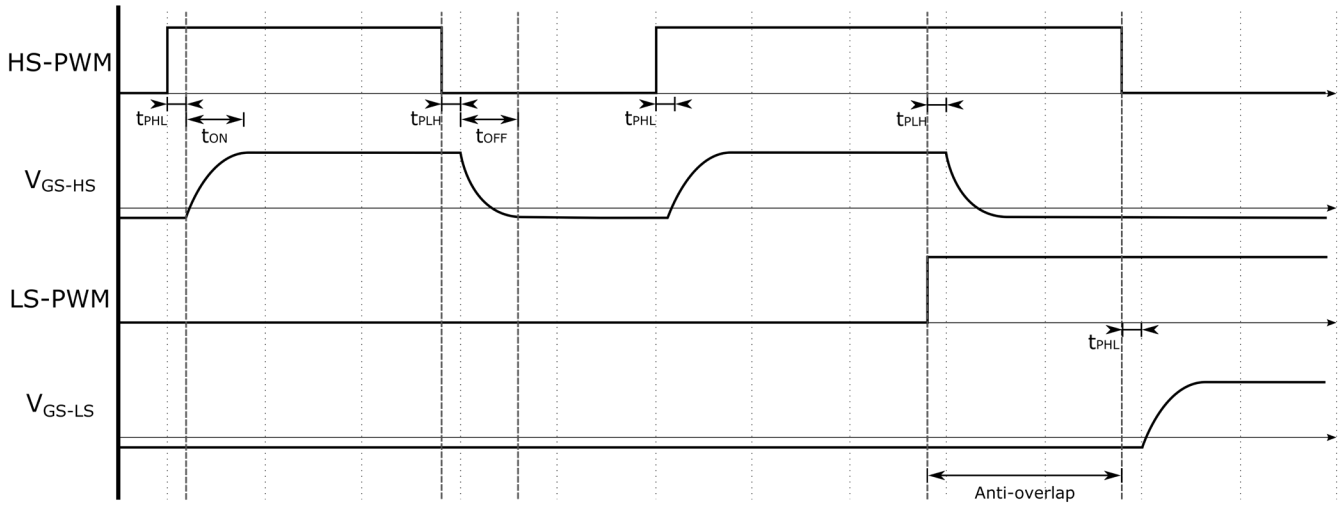

Figure 45: Gate timing diagram

4.7 Power Estimates

The gate driver power required to drive a switch position at a target switching frequency is calculated using the equation below. The gate charge is dependent on the datasheet of the MOSFET being driven. Once the required gate driver power is calculated, the necessary input power can be calculated from the efficiency curves on the datasheet of the applicable power supply. This calculation is for one channel of the gate driver.

$$P_{SW} = Q_G \cdot f_{SW} \cdot \Delta V_{PS}$$

where

P_{SW}: per channel gate driver power [W]
Q_G: total gate charge [C]
f_{SW}: switching frequency [Hz]
ΔV_{PS}: difference in isolated power supply voltage rails ($V_{PS,HIGH}$ – $V_{PS,LOW}$) [V]

This calculation can be manipulated to determine the theoretical maximum switching frequency possible with a gate driver and MOSFET combination (with some margin). Note that the calculated maximum switching frequency is not always achievable or practical in the target application depending on rise/fall times, deadtime, and parasitic inductance/capacitance. This calculation is often most critical in applications using high ampacity power modules or high switching frequencies. This value serves as the theoretical maximum based on the gate driver components. Thermal performance of the ADuM4135 and ADuM4146C gate driver ICs must also be considered when pushing to elevated switching frequencies. At very high switching frequencies, refer to the ADuM4135 and ADuM4146C datasheets for more information about estimating the temperature of the gate driver IC. An example calculation for the CAS350M12BM3 power module and CGD1200HB2P-BM3 gate driver is demonstrated below, and Table 17 shows example calculations for all the 62mm gate drivers.

P_{SW}: 2 W (rated output power of the isolated power supplies on the gate driver)
Q_G: 844 nC (provided in CAS350M12BM3 datasheet)
$V_{PS,HIGH}$: 15 V (default positive output voltage of the CGD1200HB2P-BM3)
$V_{PS,LOW}$: -4 V (default negative output voltage of the CGD1200HB2P-BM3)
ΔV_{PS}: 19 V ($V_{PS,HIGH} - V_{PS,LOW}$)

$$f_{SW} \leq \frac{2\ W}{844\ nC \cdot 19\ V} \rightarrow f_{sw} \leq 105.7\ kHz$$

Table 17: Maximum switching frequency calculations for 62 mm gates drivers

Gate Driver	Power Module	ΔV_{PS}	Q_G	$f_{SW,MAX}$*
CGD1**2**00HB2P-BM**2**	CAS300M12BM2	25 V	1025 nC	70 kHz
CGD1**2**00HB2P-BM**3**	CAS350M12BM3	19 V	844 nC	120 kHz
CGD1**7**00HB2P-BM**2**	CAS300M17BM2	25 V	1076 nC	70 kHz
CGD1**7**00HB2P-BM**3**	CAS310M17BM3	19 V	996 nC	100 kHz

* $f_{SW,MAX}$ includes margin in the calculation

5. Dimensions

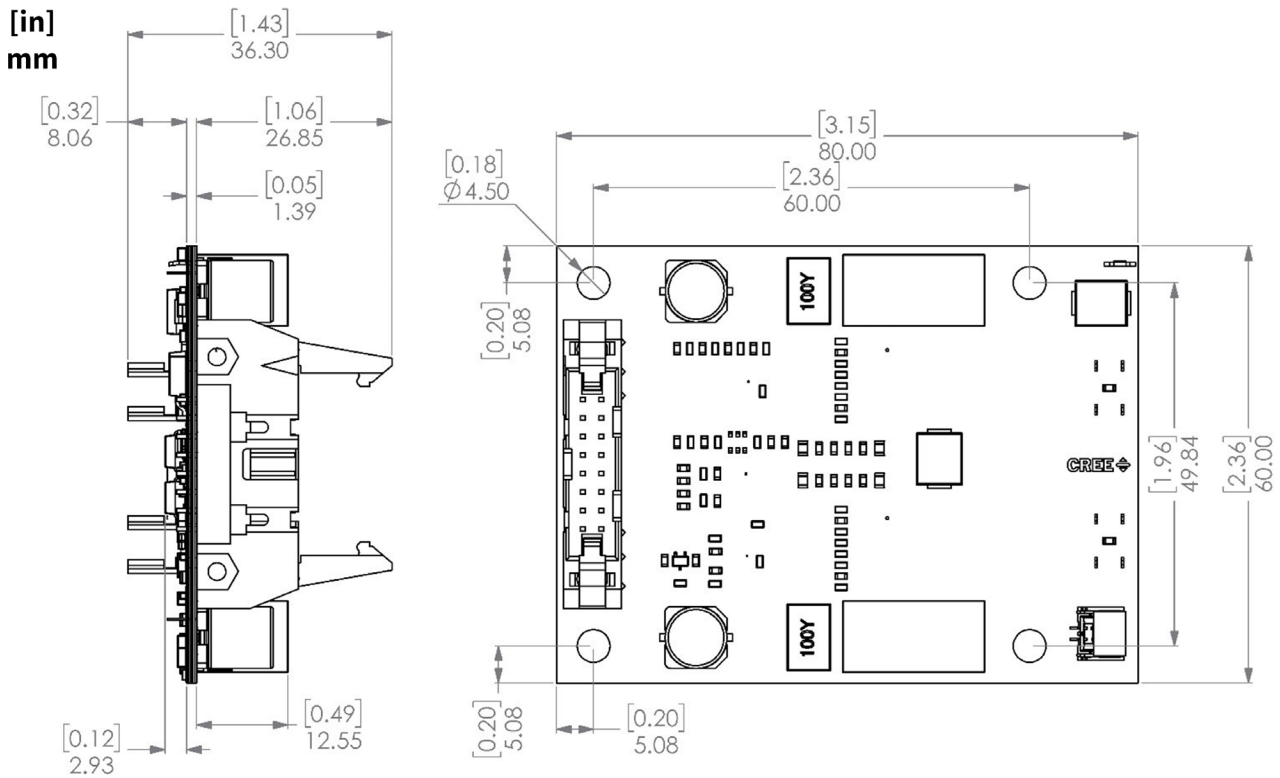

*Figure 46: Dimensions of the CGD1**2**00HB2P-BM2/3 gate drivers*

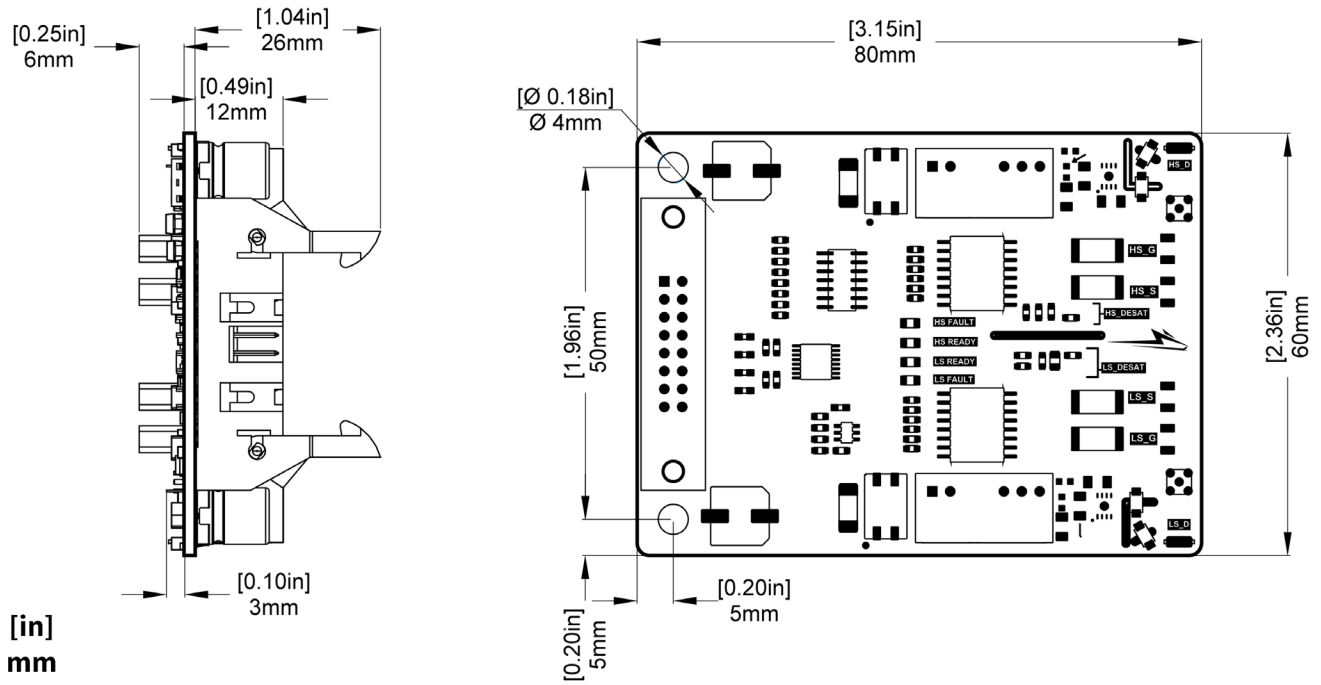

*Figure 47: Dimensions of the CGD17**7**00HB2P-BM2/3 gate drivers*

6. Supporting Links and Tools

The following links provide additional information about gate drivers, Wolfspeed 62 mm SiC power modules, and design tools for using the devices. Please navigate to the landing page for these gate driver designs for additional links and support.

6.1 Evaluation Tools and Support

- 62 mm Power Modules
- CGD1200HB2P-BM2: Evaluation Gate Driver Tool Optimized for the 1200 V BM2 Module Platform
- CGD1200HB2P-BM3: Evaluation Gate Driver Tool Optimized for the BM3 Module Platform
- CGD1700HB2P-BM2: Evaluation Gate Driver Tool Optimized for the 1700 V BM2 Module Platform
- CGD1700HB2P-BM3: Evaluation Gate Driver Tool Optimized for the 1700 V BM3 Module Platform
- KIT-CRD-CIL12N-BM: Dynamic Characterization Evaluation Tool Optimized for the 62mm (BM) Module Platform
- KIT-CRD-CIL17N-BM: Dynamic Characterization Evaluation Tool Optimized for the 1700 V 62 mm (BM) Module Platform
- SpeedVal™: Modular Evaluation Platform
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum
- All Wolfspeed Gate Drivers

6.2 Dual Channel Gate Driver Board

- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

6.3 Application Notes

- PRD-09301: Gate Driver Design for SiC Power Modules
- PRD-04814: Design Options for Wolfspeed Silicon Carbide MOSFET Gate Bias Power Supplies

Revision History

Date	Revision	Changes
February 2026	1	Initial release.

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