

# C4MV060065T

## 650V 60mΩ VGS Optimized Silicon Carbide Power MOSFET N-Channel Enhancement Mode

### Features

- Industry compatible drive voltage +15V..18V
- Industry standard Top Side Cooled (TSC) package
- High power dissipation capability
- Optimized package with separate driver source pin
- High-speed switching with low capacitances
- Soft body diode to minimize voltage overshoots
- Halogen free, RoHS compliant

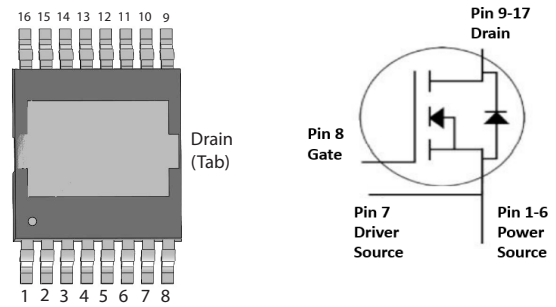
### Benefits

- Compatible with industry standard gate drivers
- Increase power density
- Reduce cooling requirements
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Increase system switching frequency

### Applications

- EV Chargers
- Solar/ESS
- Motor Control
- Industrial Power Supplies
- High Voltage DC/DC Converters

### Package



Orderable Part Number	Package	Marking
C4MV060065T-TR	TOLT (TSC)	C4MV060065T

### Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	$V_{DS}$			650	V	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage (Transient)	$V_{GS}$	-10		+23		Transient	Refer to PRD-04814
DC Continuous Drain Current	$I_D$		36		A	$V_{GS} = 18\text{V}, T_c = 25^\circ\text{C}, T_j \leq 175^\circ\text{C}$	Fig 19 Note 1
			26			$V_{GS} = 18\text{V}, T_c = 100^\circ\text{C}, T_j \leq 175^\circ\text{C}$	
Pulsed Drain Current	$I_{DM}$			93		$t_{pmax}$ limited by $T_{jmax}$ $V_{GS} = 18\text{V}, T_c = 25^\circ\text{C}$	Fig 22
Power Dissipation	$P_D$		153		W	$T_c = 25^\circ\text{C}, T_j = 175^\circ\text{C}$	Fig 20
Operating Junction and Storage Temperature	$T_j, T_{stg}$	-55		175	°C		
Solder Temperature	$T_L$			260		According to JEDEC J-STD-020	

Note (1): Verified by Design

Electrical Characteristics ( $T_c = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.6	3.8		$V_{DS} = V_{GS}, I_D = 3.67\ \text{mA}$	Fig. 11
			2.2			$V_{DS} = V_{GS}, I_D = 3.67\ \text{mA}, T_J = 175^\circ\text{C}$	
$I_{DSS}$	Zero Gate Voltage Drain Current		1	50	$\mu\text{A}$	$V_{DS} = 650\ \text{V}, V_{GS} = 0\ \text{V}$	
$I_{GSS}$	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 18\ \text{V}, V_{DS} = 0\ \text{V}$	
$V_{GS(op)}$	Recommended Turn On Gate-Source Voltage		+15..+18		V		Refer to PRD-09634
	Recommended Turn Off Gate-Source Voltage		-5..0				
$R_{DS(on)}$	Drain-Source On-State Resistance		60	78	m $\Omega$	$V_{GS} = 18\ \text{V}, I_D = 13.4\ \text{A}$	Fig. 4, 5, 6
			102			$V_{GS} = 18\ \text{V}, I_D = 13.4\ \text{A}, T_J = 175^\circ\text{C}$	
			70			$V_{GS} = 15\ \text{V}, I_D = 13.4\ \text{A}$	
$g_{fs}$	Transconductance		10		S	$V_{DS} = 20\ \text{V}, I_{DS} = 13.4\ \text{A}$	Fig. 7
			10			$V_{DS} = 20\ \text{V}, I_{DS} = 13.4\ \text{A}, T_J = 175^\circ\text{C}$	
$C_{iss}$	Input Capacitance		1068		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V to } 400\ \text{V}$ $f = 100\ \text{kHz}$ $V_{AC} = 25\ \text{mV}$	Fig. 17, 18
$C_{oss}$	Output Capacitance		85				
$C_{rss}$	Reverse Transfer Capacitance		8				
$E_{oss}$	$C_{oss}$ Stored Energy		8		$\mu\text{J}$		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		106		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0 \dots 400\ \text{V}$	Note: 2
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		146				
$E_{oN}$	Turn-On Switching Energy (MOSFET FWD)		24		$\mu\text{J}$	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/18\ \text{V}, I_D = 13.4\ \text{A},$ $R_{G(ext)} = 2\ \Omega, L = 63\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode	
$E_{oFF}$	Turn-Off Switching Energy (MOSFET FWD)		13				
$t_{d(on)}$	Turn-On Delay Time		8		ns	$V_{DD} = 400\ \text{V}, V_{GS} = -4\ \text{V}/18\ \text{V}$ $I_D = 13.4\ \text{A}, R_{G(ext)} = 2\ \Omega,$ Timing relative to $V_{DS}$ Inductive load	
$t_r$	Rise Time		3				
$t_{d(off)}$	Turn-Off Delay Time		18				
$t_f$	Fall Time		9				
$R_{G(int)}$	Internal Gate Resistance		2.6		$\Omega$	$f = 1\ \text{MHz}$	
$Q_{gs}$	Gate to Source Charge		11		nC	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/18\ \text{V}$ $I_D = 13.4\ \text{A}$ Per IEC60747-8-4 pg 21	Fig. 12
$Q_{gd}$	Gate to Drain Charge		15				
$Q_g$	Total Gate Charge		44				

Note (2):  $C_{o(er)}$ , a lumped capacitance that gives same stored energy as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 400V

$C_{o(tr)}$ , a lumped capacitance that gives same charging time as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 400V

Reverse Diode Characteristics ( $T_c = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$V_{SD}$	Diode Forward Voltage	4.9		V	$V_{GS} = -4\text{ V}, I_{SD} = 6.7\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.2			$V_{GS} = -4\text{ V}, I_{SD} = 6.7\text{ A}, T_J = 175^\circ\text{C}$	
$I_S$	Continuous Diode Forward Current		25	A	$V_{GS} = -4\text{ V}, T_C = 25^\circ\text{C}$	
$I_{SM}$	Diode pulse Current		93		$V_{GS} = -4\text{ V}$ , pulse width $t_p$ limited by $T_{Jmax}$	
$t_{rr}$	Reverse Recovery time	9		ns	$V_{GS} = -4\text{ V}, I_{SD} = 13.4\text{ A}, V_R = 400\text{ V}$ $dif/dt = 7167\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
$Q_{rr}$	Reverse Recovery Charge	239		nC		
$I_{rrm}$	Peak Reverse Recovery Current	42		A		
$t_{rr}$	Reverse Recovery time	106		ns	$V_{GS} = -4\text{ V}, I_{SD} = 13.4\text{ A}, V_R = 400\text{ V}$ $dif/dt = 970\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
$Q_{rr}$	Reverse Recovery Charge	281		nC		
$I_{rrm}$	Peak Reverse Recovery Current	8		A		

## Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.75	$^\circ\text{C}/\text{W}$		Fig. 21



Typical Performance

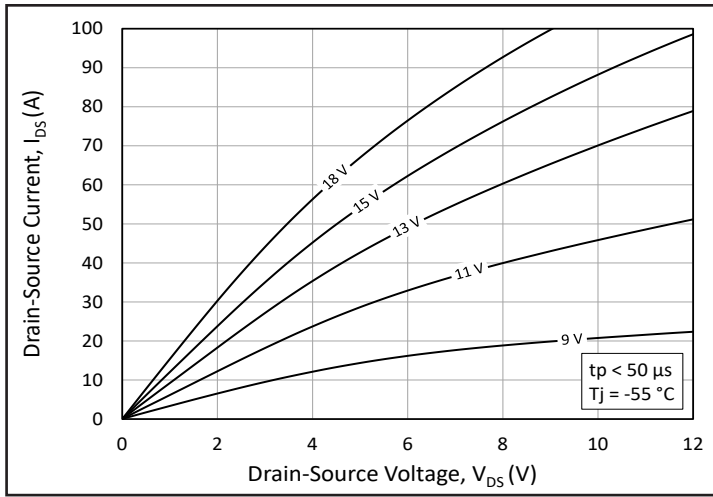


Figure 1. Output Characteristics  $T_j = -55\text{ }^\circ\text{C}$

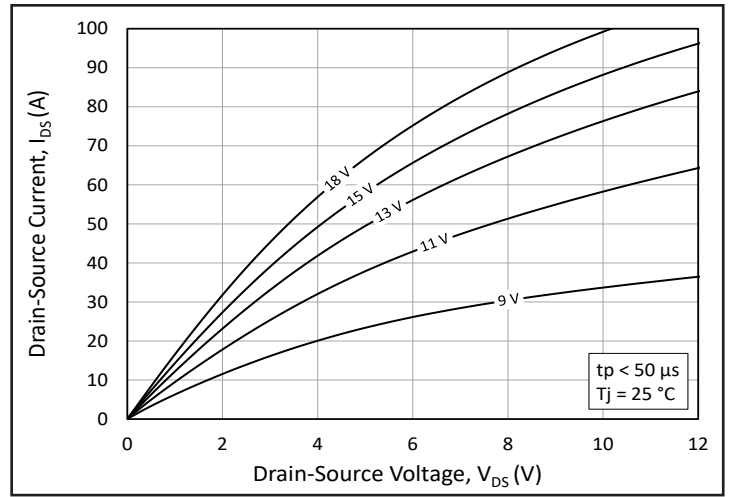


Figure 2. Output Characteristics  $T_j = 25\text{ }^\circ\text{C}$

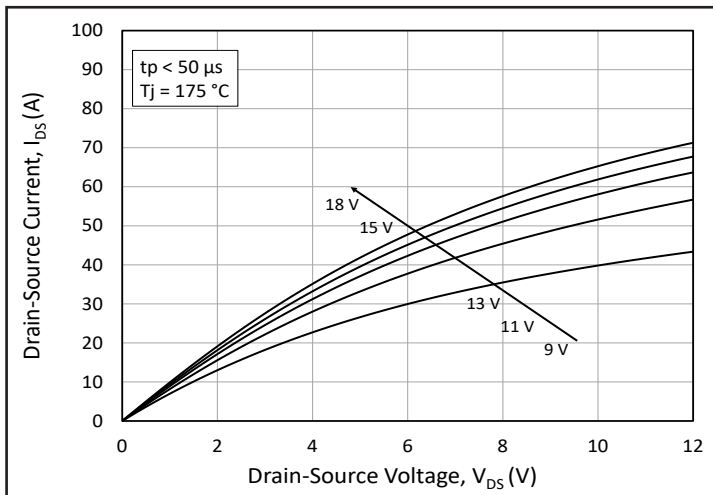


Figure 3. Output Characteristics  $T_j = 175\text{ }^\circ\text{C}$

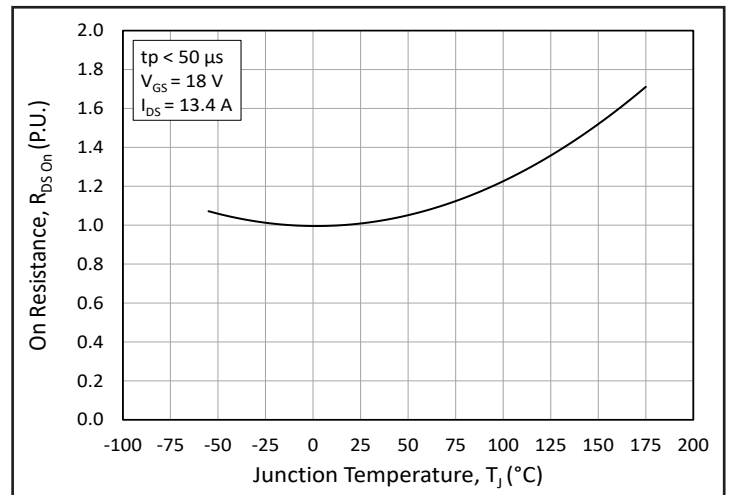


Figure 4. Normalized On-Resistance vs. Temperature

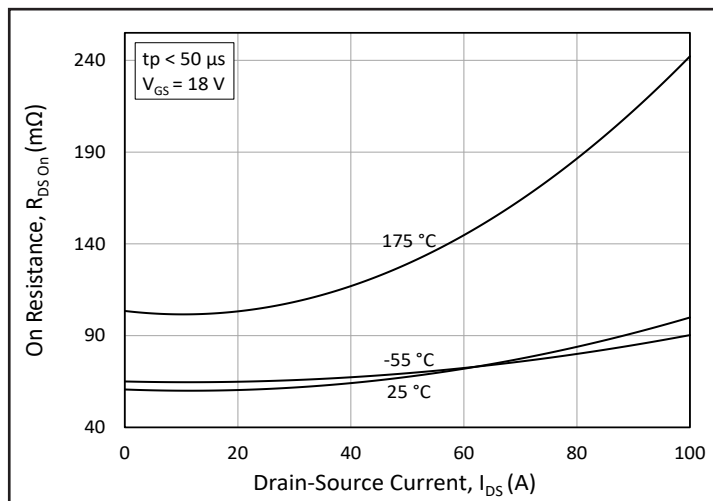


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

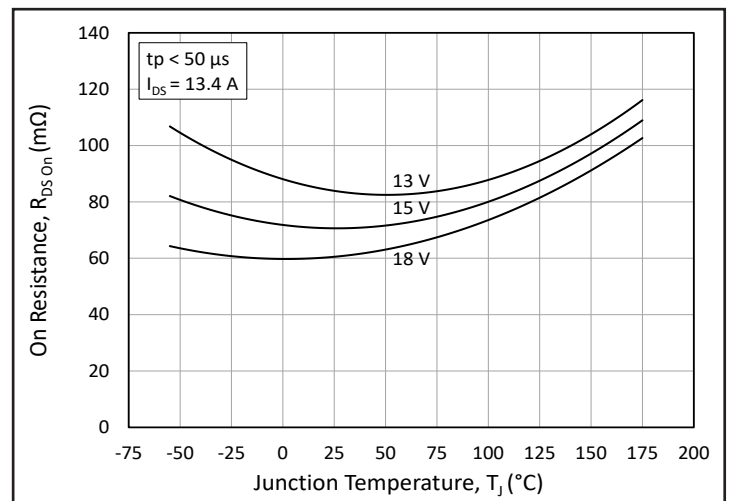


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

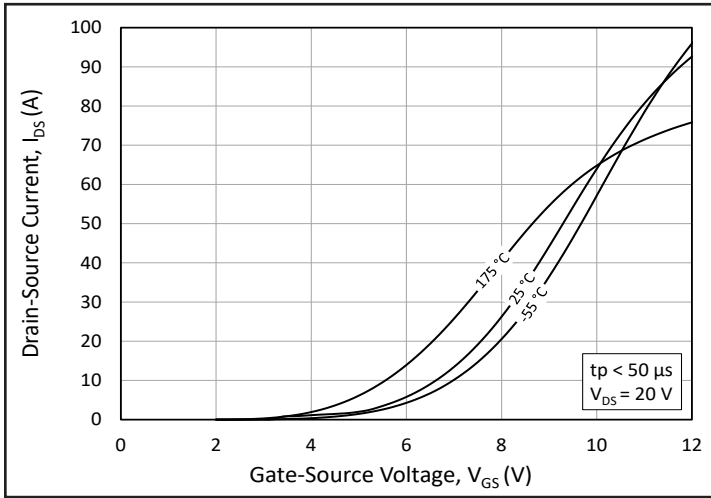


Figure 7. Transfer Characteristic for Various Junction Temperatures

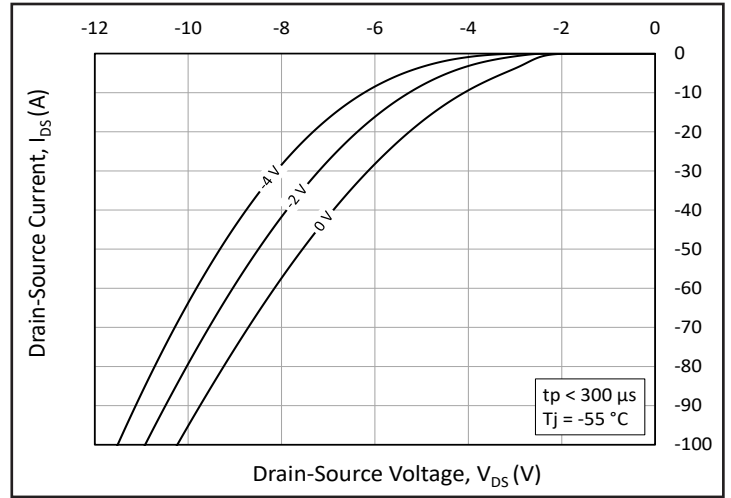


Figure 8. Body Diode Characteristic at -55 °C

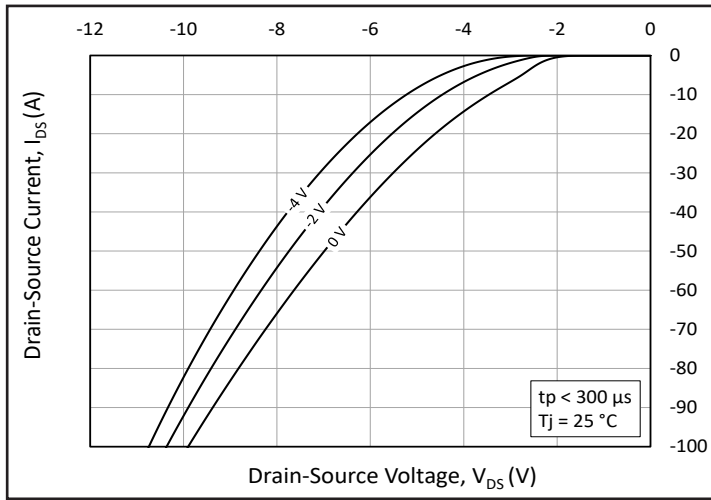


Figure 9. Body Diode Characteristic at 25 °C

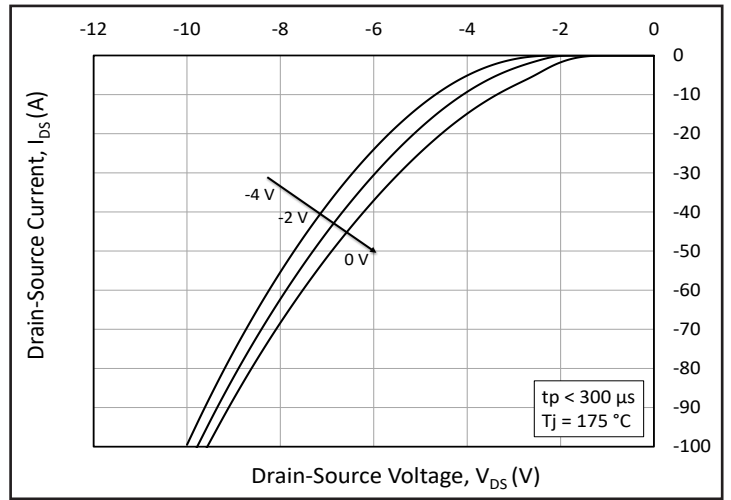


Figure 10. Body Diode Characteristic at 175 °C

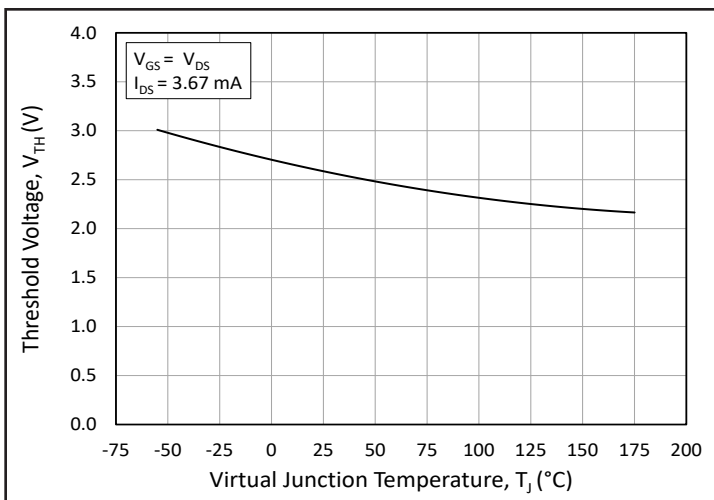


Figure 11. Threshold Voltage vs. Temperature

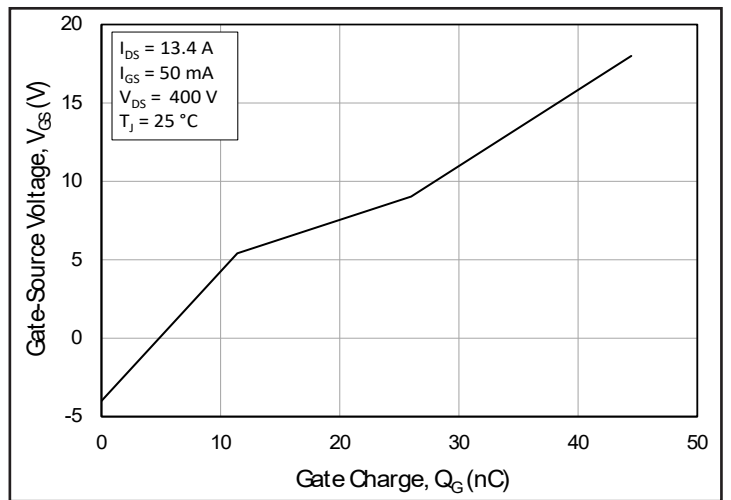


Figure 12. Gate Charge Characteristics

Typical Performance

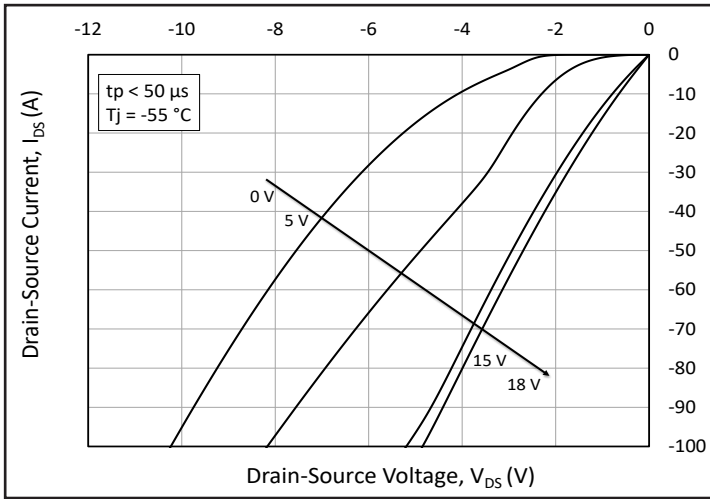


Figure 13. 3rd Quadrant Characteristic at -55 °C

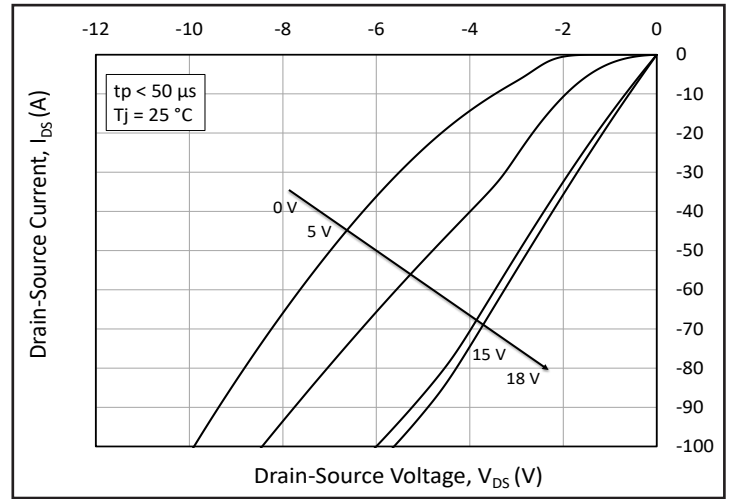


Figure 14. 3rd Quadrant Characteristic at 25 °C

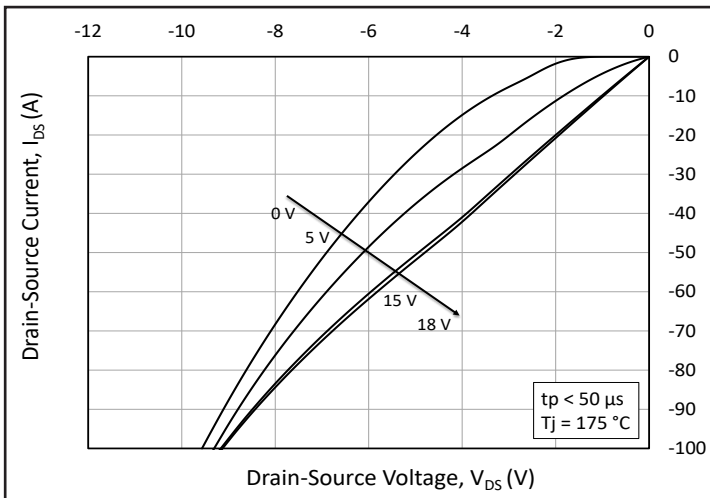


Figure 15. 3rd Quadrant Characteristic at 175 °C

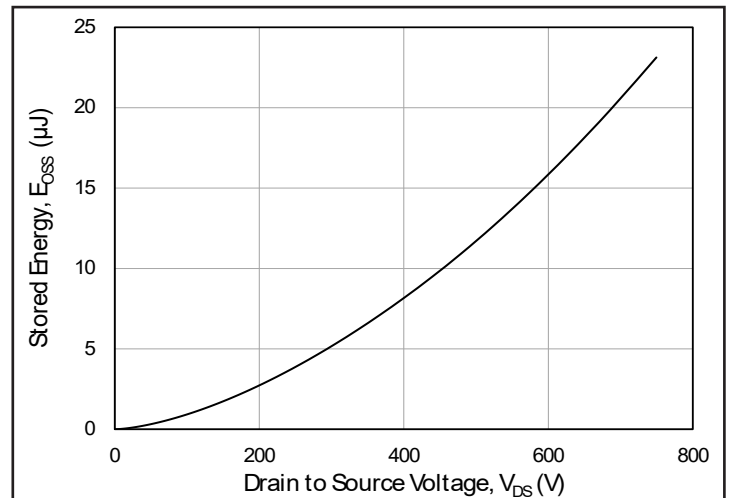


Figure 16. Output Capacitor Stored Energy

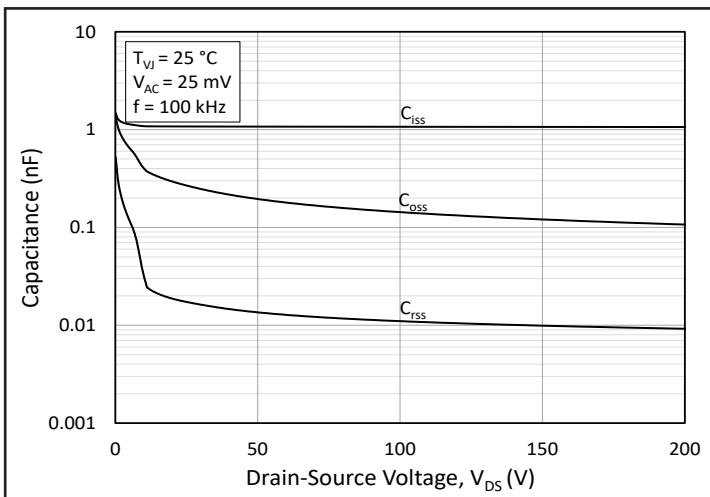


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

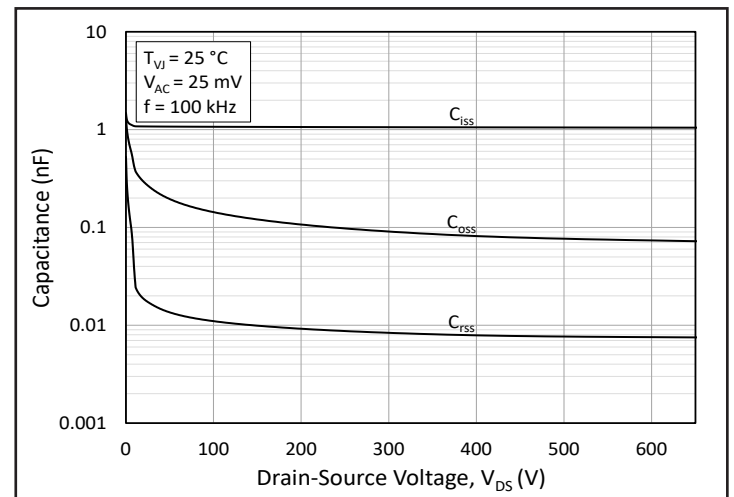


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)



Typical Performance

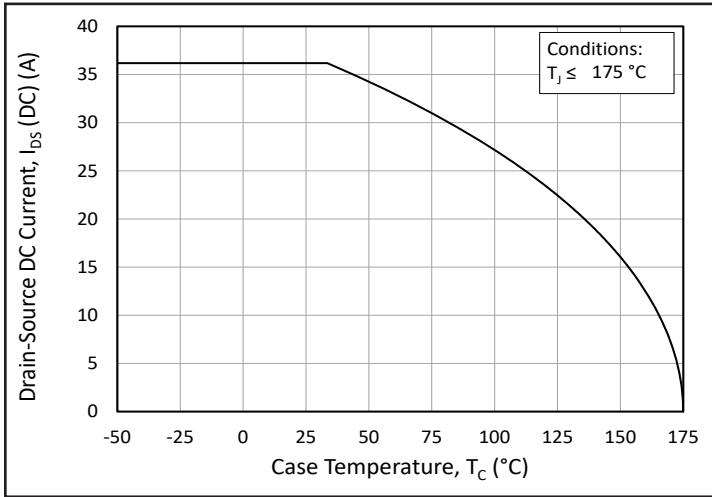


Figure 19. Continuous Drain Current Derating vs. Case Temperature

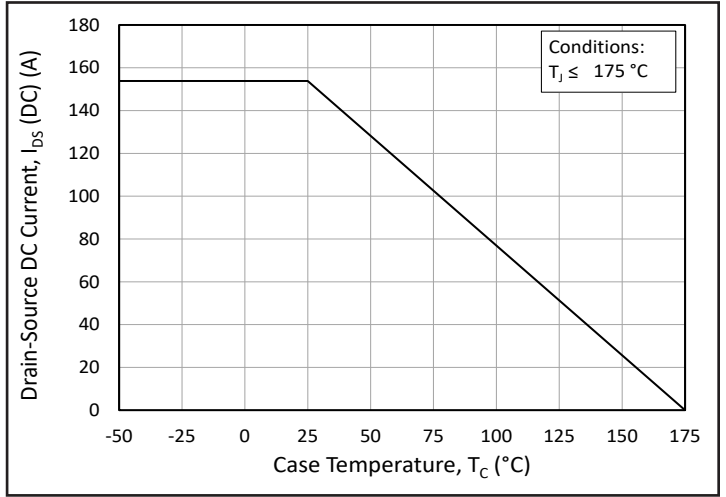


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

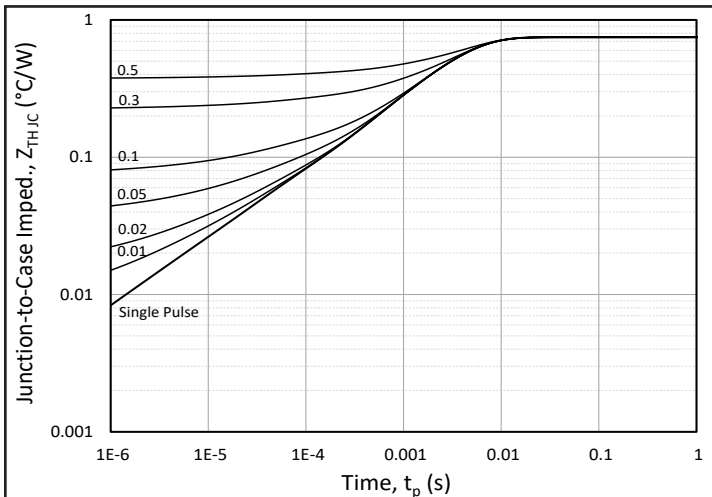


Figure 21. Transient Thermal Impedance (Junction - Case)

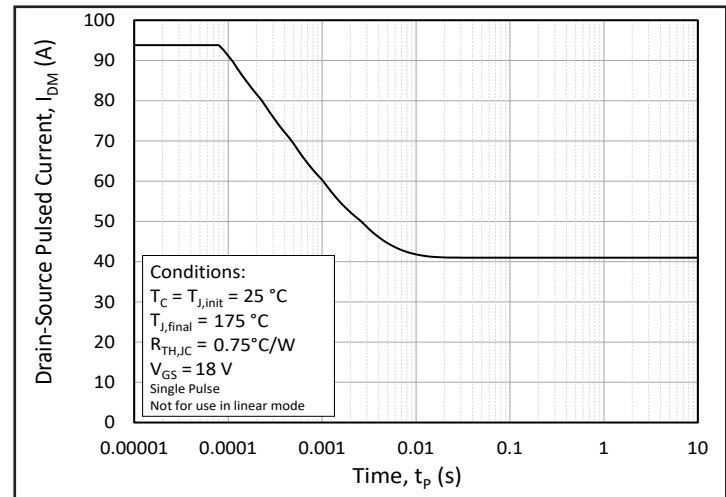


Figure 22. Safe Operating Area

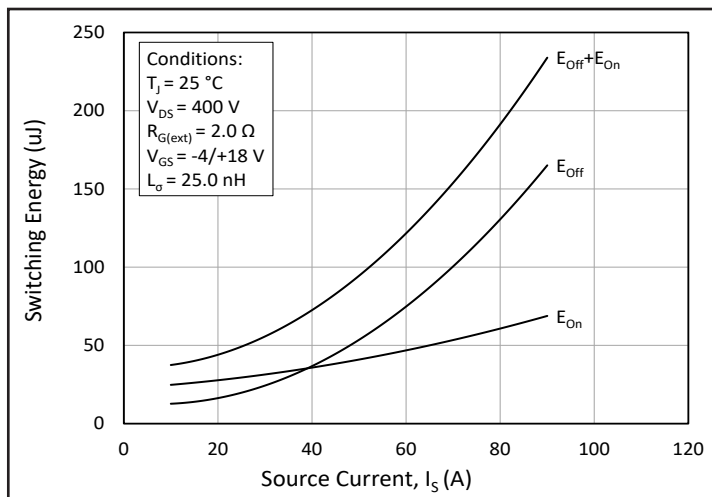


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 400V$ )

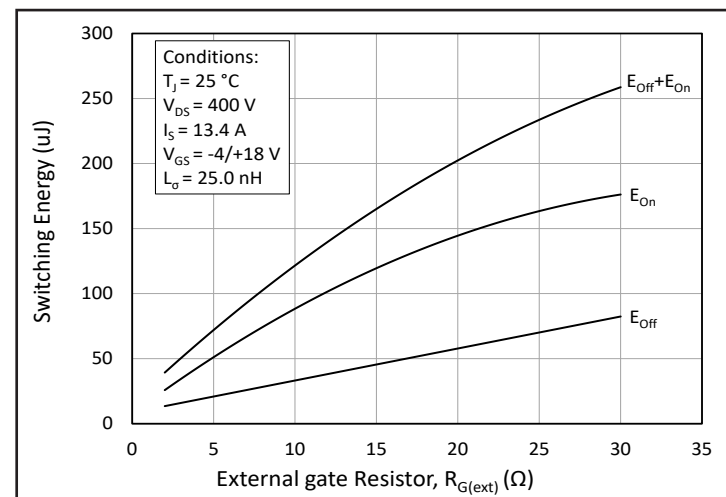


Figure 24. Clamped Inductive Switching Energy vs.  $R_{G(ext)}$



Typical Performance

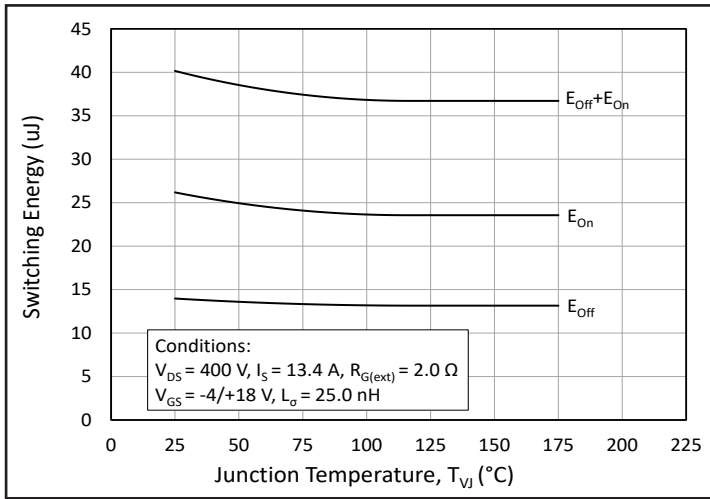


Figure 25. Clamped Inductive Switching Energy vs. Temperature

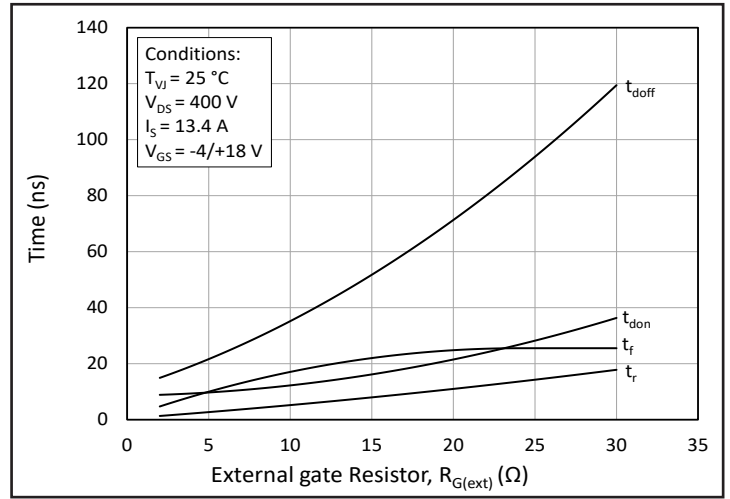


Figure 26. Switching Times vs.  $R_{G(ext)}$

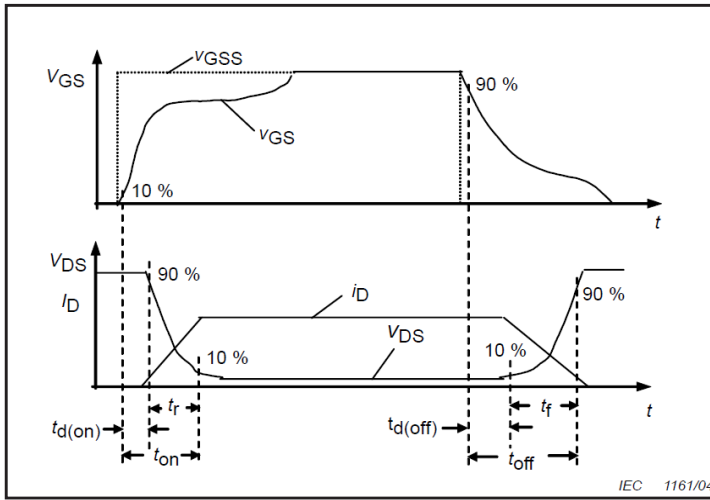


Figure 27. Switching Times Definition

## Test Circuit Schematic

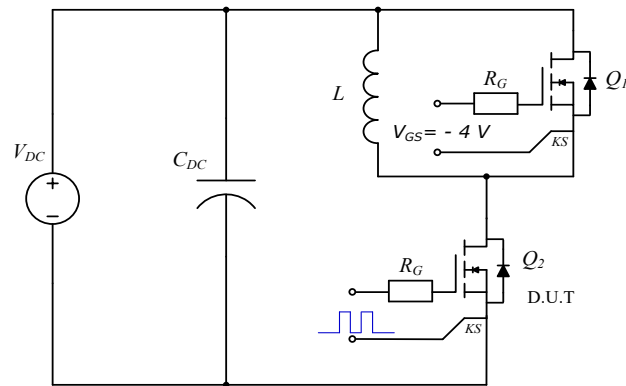
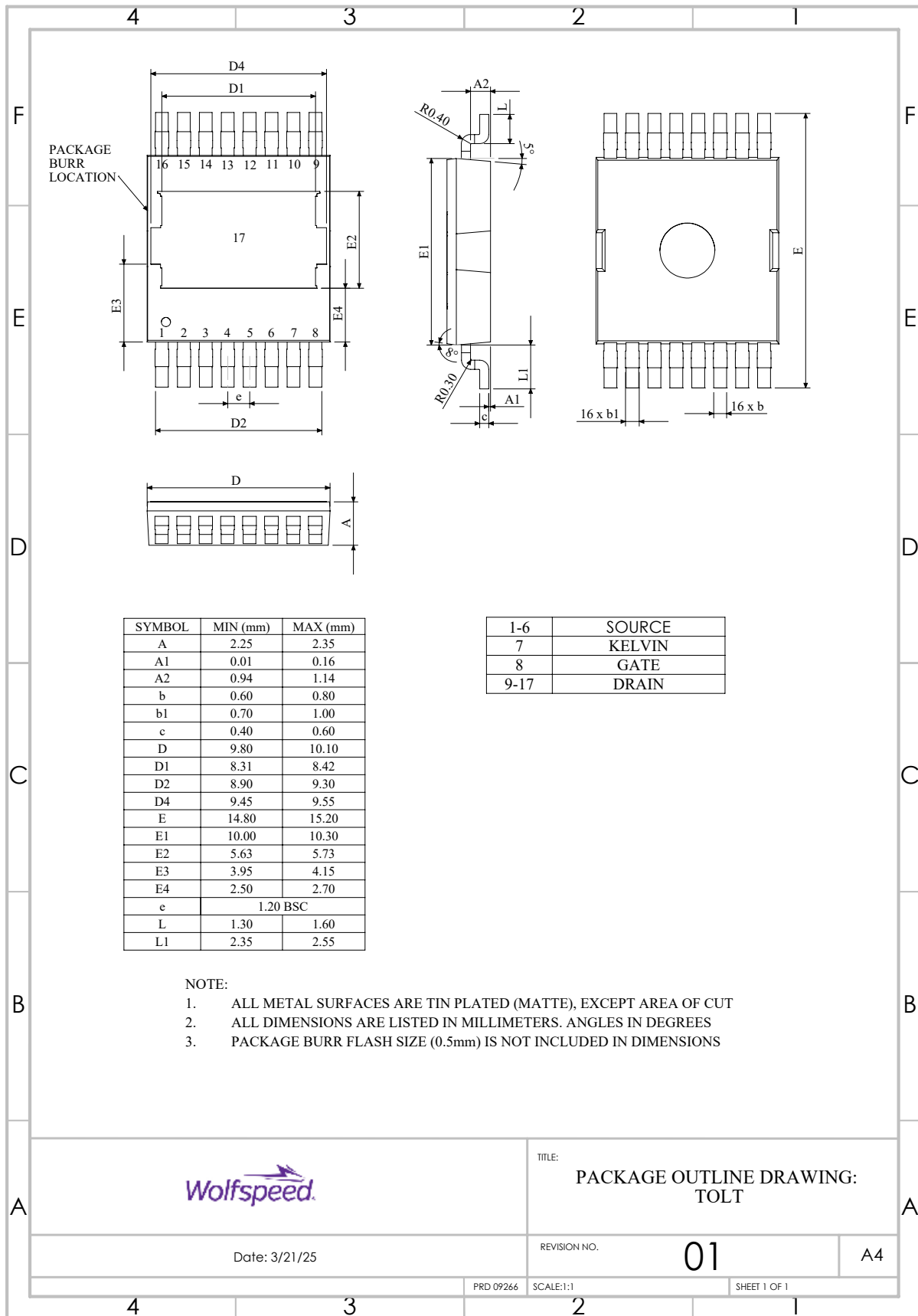


Figure 28. Clamped Inductive Switching  
Waveform Test Circuit

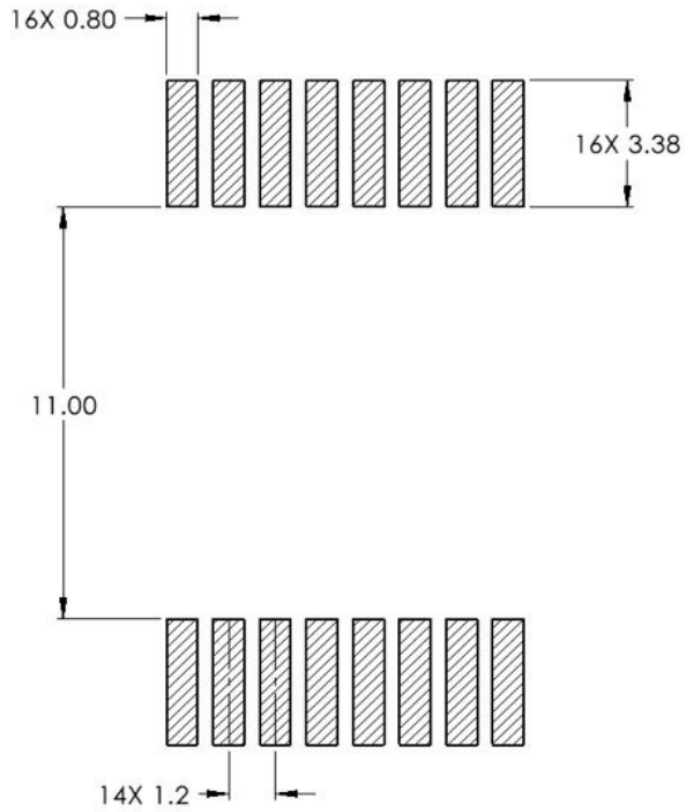
Package Dimensions





### Recommended Solder Pad Layout

All dimensions in mm





Revision history

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Document Version	Date of release	Description of changes
1	January 2026	Initial release



## Notes & Disclaimer

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