User Guide **PRD-09623**

CRD200DA23N-GMA Three-Phase Inverter User Guide

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CRD200DA23N-GMA Three-Phase Inverter User Guide

Contents

1. Introduction

This user guide provides an overview of the Wolfspeed CRD200DA23N-GMA 200 kW three-phase inverter reference design including key system specifications, sub-system functional descriptions, performance test data, and mechanical assembly. The CRD200DA23N-GMA design, shown in Figure 1, was developed to provide power electronics engineers with a hardware evaluation platform and reference design files to support early design-in activities of the 2.3 kV Wolfspeed WolfPACK™ baseplate-less power module platform. In conjunction with this user guide, the complete suite of reference design files including schematics, printed circuit board (PCB) layout, Gerber files, bill of materials (BOM), and 3D mechanical files are available for download from the CRD200DA23N-GMA landing page on the Wolfspeed website.

Figure 1: CRD200DA23N-GMA three-phase inverter

The CRD200DA23N-GMA is an easy-to-use, flexible power stage designed around the CAB5R0A23GM4T (2300 V / 5 mΩ) Wolfspeed WolfPACK half-bridge power module. This module, shown in Figure 2, utilizes Wolfspeed's 2.3 kV node to enable 1500 V bus operation with a simple two-level topology, without requiring the complexity of a three-level topology. The module utilizes Wolfspeed's 4th generation technology which features improved switching performance and a softer body diode compared to previous generations. The modules include pre-applied phase-changing thermal interface material (TIM) for strong thermal performance and easy system-level integration.

Figure 2: CAB5R0A23GM4T, 2300 V, 5 mΩ half-bridge power module

A high-level overview of the design is shown in the block diagram shown in Figure 3. The design features series-stacked capacitors to enable higher DC-bus voltages. The mid-point of the series-stacked capacitors can be used to attach the neutral of the load and for using a split rail input power supply. This design intends to provide everything needed to quickly evaluate performance out of the box while also providing the resources to expand its capabilities to suit target end-application needs. To this end, integrated into this design is DC-bus capacitance with low-inductance power planes, gate drivers, and thermal management. The design includes three half-bridge power modules to create the three output phases and integrated voltage feedback measurements. An integrated general-purpose controller is included with baseline firmware pre-installed for immediate use, though the controller firmware can easily be upgraded for customization or improvement purposes. The design also includes onboard gate drivers which communicate via differential signaling, integrated desaturation overcurrent protection, and integrated power module thermistor feedback for monitoring substrate temperature.

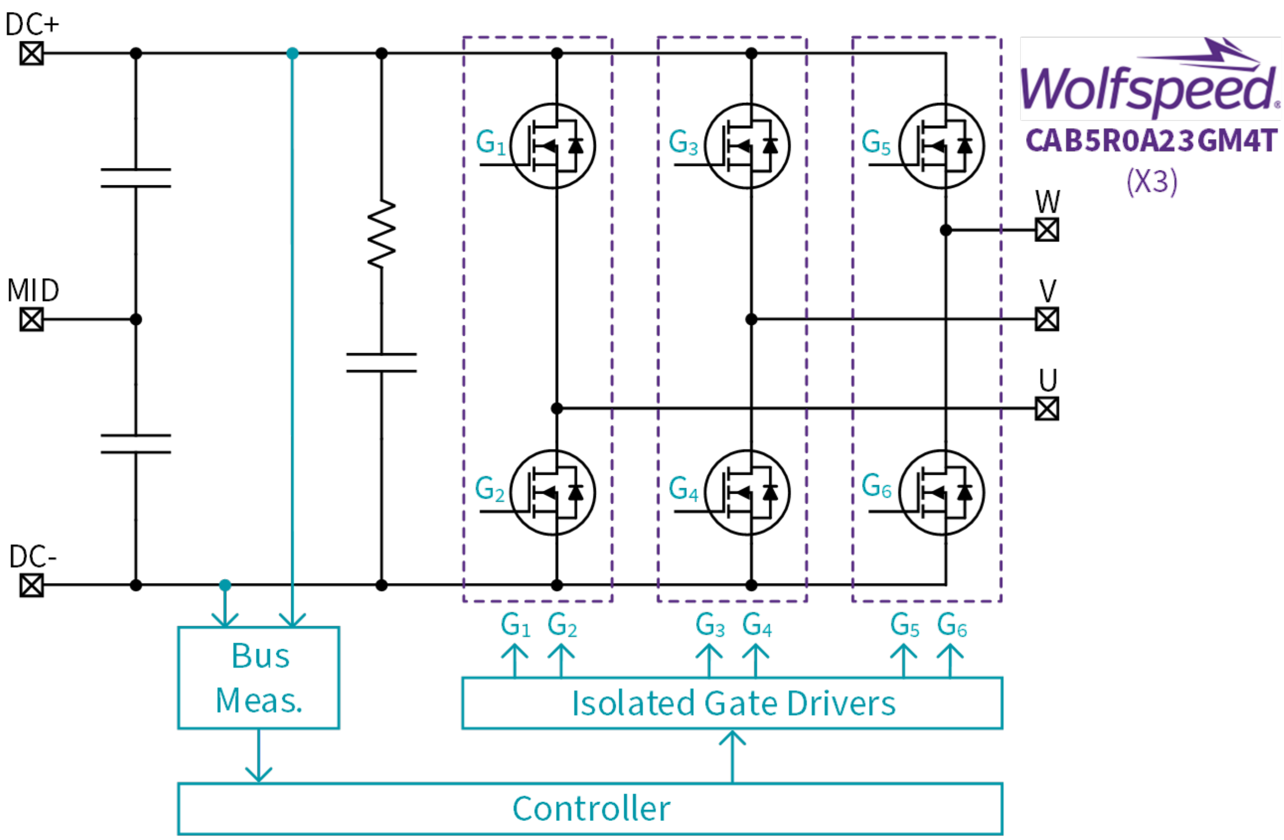

Figure 3: CRD200DA23N-GMA block diagram

By default, the CRD200DA23N-GMA is designed to be evaluated as a simple three-phase inverter topology, but the flexibility of the generic power stage makes it simple to adapt to other applications. As such, the design is ideal for evaluating or scaling up to higher power levels in industrial motor drives, power supplies, and renewable energy applications, or as the bi-directional active front end (AFE) stage for energy storage applications.

2. Design Features

This section highlights the design features of the CRD200DA23N-GMA design including key system specifications, a description of the various functional circuit groups, and a general input/output (I/O) pinout definitions.

2.1 Key System Specifications

- Three CAB5R0A23GM4T (2300 V / 5 mΩ) Wolfspeed WolfPACK half-bridge power modules
- General purpose controller (Texas Instruments® LAUNCHXL-F28379D) with customizable firmware
- Isolated temperature measurement included on the module substrates for temperature monitoring
- Isolated CAN communication for real-time monitoring and adjustments
- Separate turn-on and turn-off gate resistors for switching loss optimization
- DC bus and phase voltage measurement circuitry
- Integrated desaturation overcurrent protection on all switch positions
- Detailed characterization of the thermal solution for improved simulation predictions
- Integrated gate measurement connectors for easy system troubleshooting and evaluation

Table 1: CRD200DA23N-GMA ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output Power	P_{OUT}	—	—	200	kW
DC Bus Voltage	V_{DC}	—	1500	—	V
Output Phase Current	I_{OUT}	—	—	167	A_{RMS}
Switching Frequency[1]	f_{sw}	—	20	50	kHz
Thermal Resistance, Junction-to-Ambient[1]	$R_{th,ja}$	—	0.343	—	°C/W

[1] Refer to Section 5 for more information

2.2 Subsystem Functional Groups

The various subsystem functional groups of this reference design are shown from the top and side profile views in Figure 4 and Figure 6, respectively. A brief description of each of the labeled subsystems is provided in Table 2 with further details about each of the subsystems described in Section 2.3.

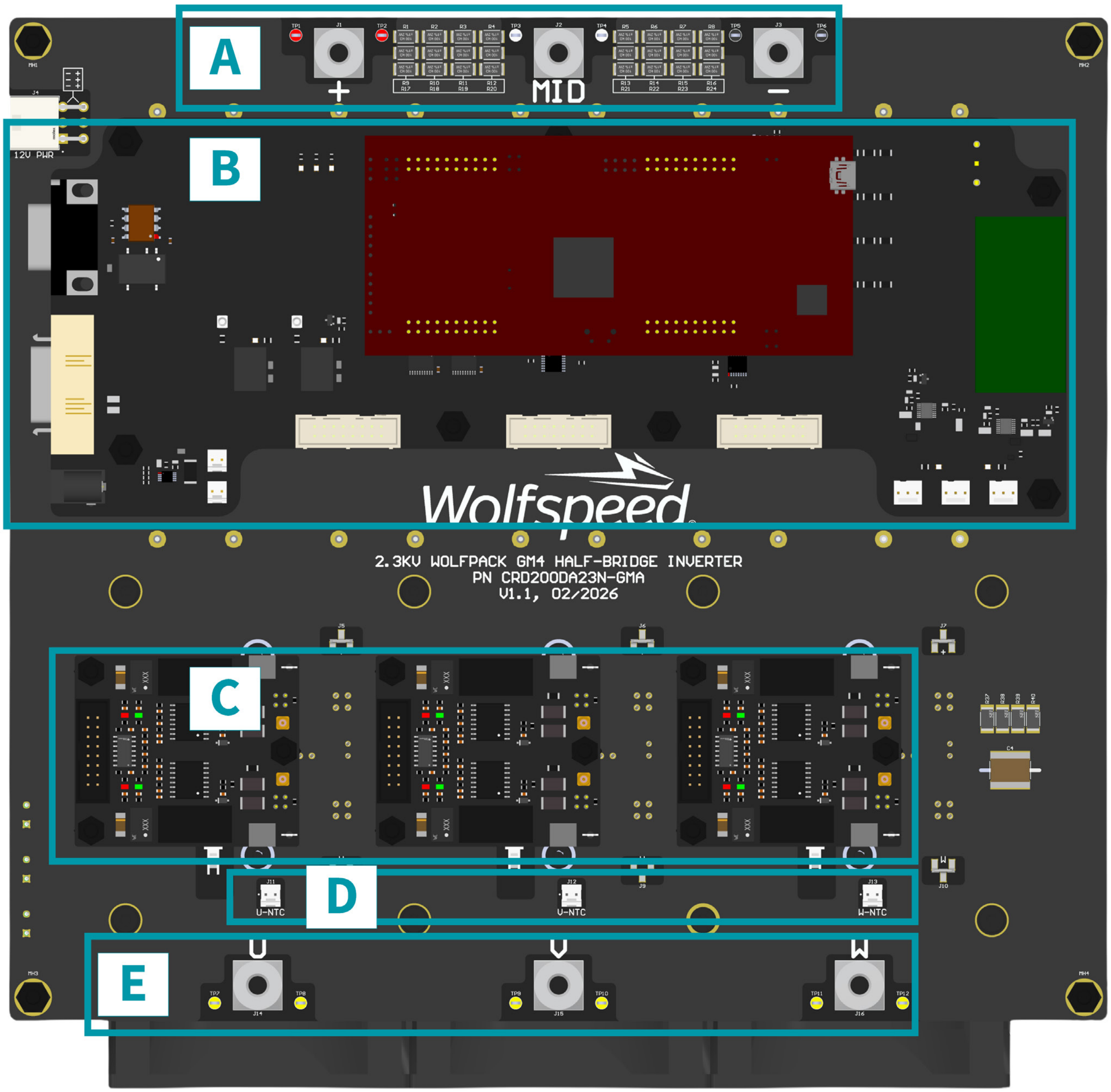

Figure 4: CRD200DA23N-GMA top view

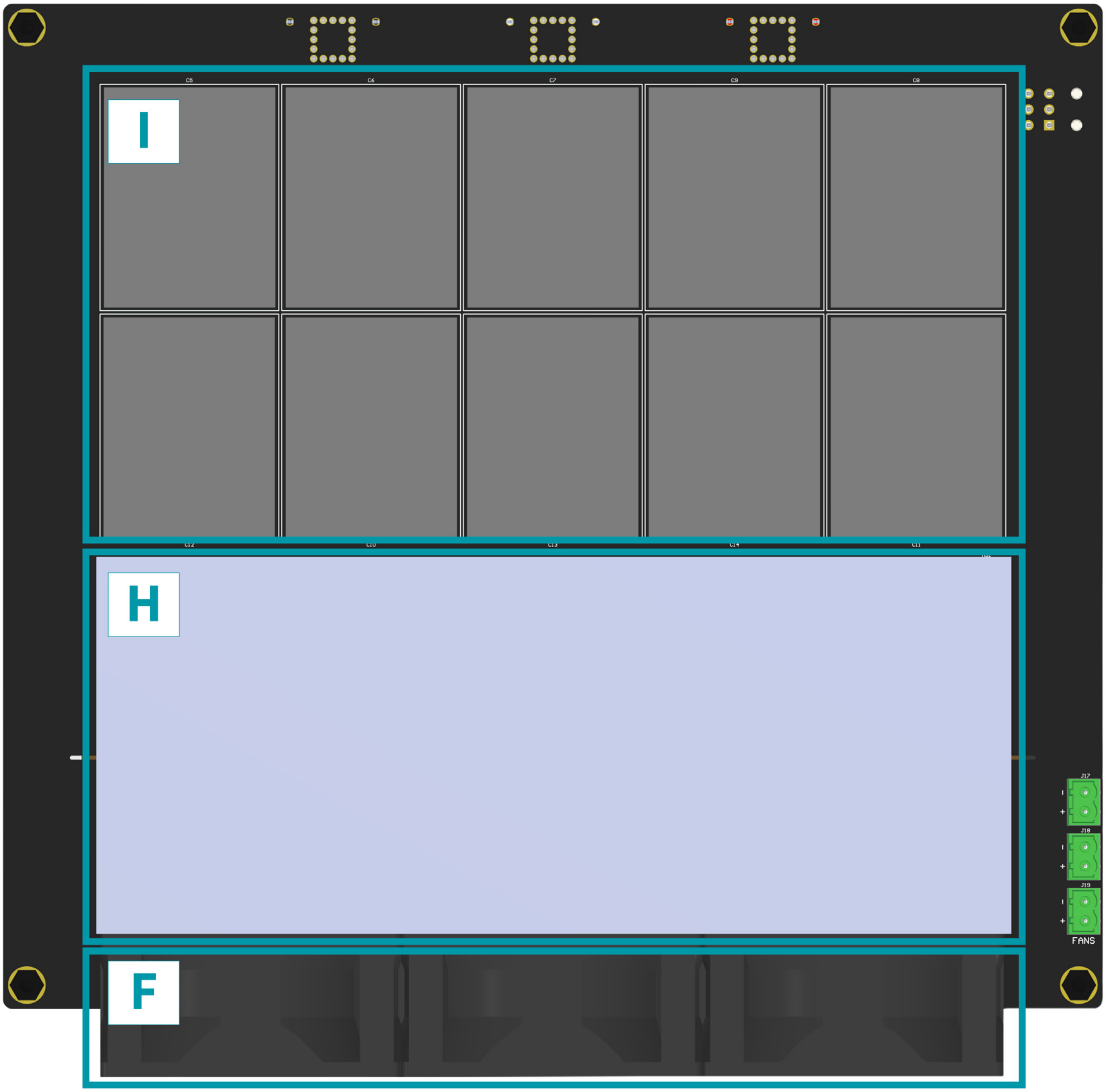

Figure 5: CRD200DA23N-GMA bottom view

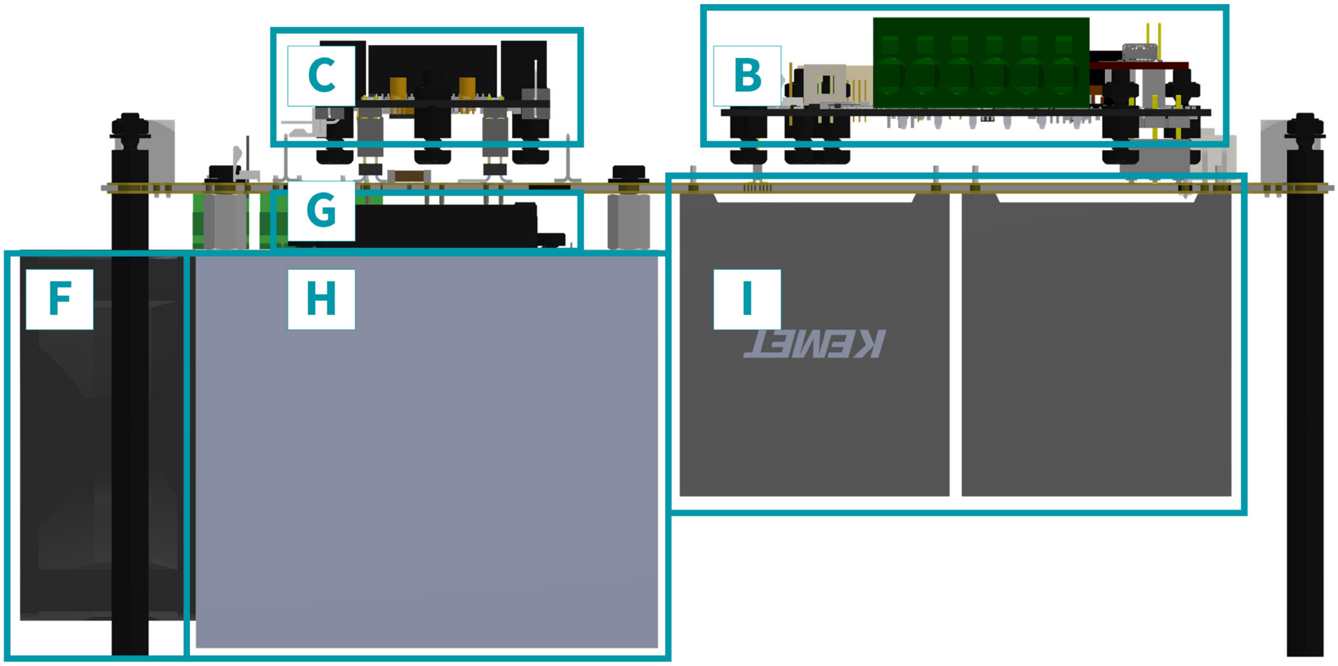

Figure 6: CRD200DA23N-GMA side view

Table 2: Subsystem functional group descriptions

Label	Description
A	Input DC Power Terminals
B	Controller
C	Gate Drivers
D	Thermistor Connectors
E	Output AC Power Terminals
F	Cooling Fans
G	CAB5R0A23GM4T Power Modules
H	Air-Cooled Heat Sink
I	DC-Link Capacitors

2.3 Control Board

This design leverages the controller printed circuit board (PCB) from the CRD300DA12E-XM3 three-phase inverter reference design. This enables customers who have experience with that design to easily adapt any custom firmware to this design. The control board, shown in Figure 4, uses the Texas Instruments (TI) LAUNCHXL-F28379D LaunchPad™ development kit for gate driver control and feedback monitoring. The design files for this control board are available for download on the CRD300DA12E-XM3 landing page. A summary of the various elements on the control board are provided in Table 3, and more information about the controller and modifying the firmware is presented in Section 4. Several of the input/output connectors discussed throughout Section 2 are located on this control board.

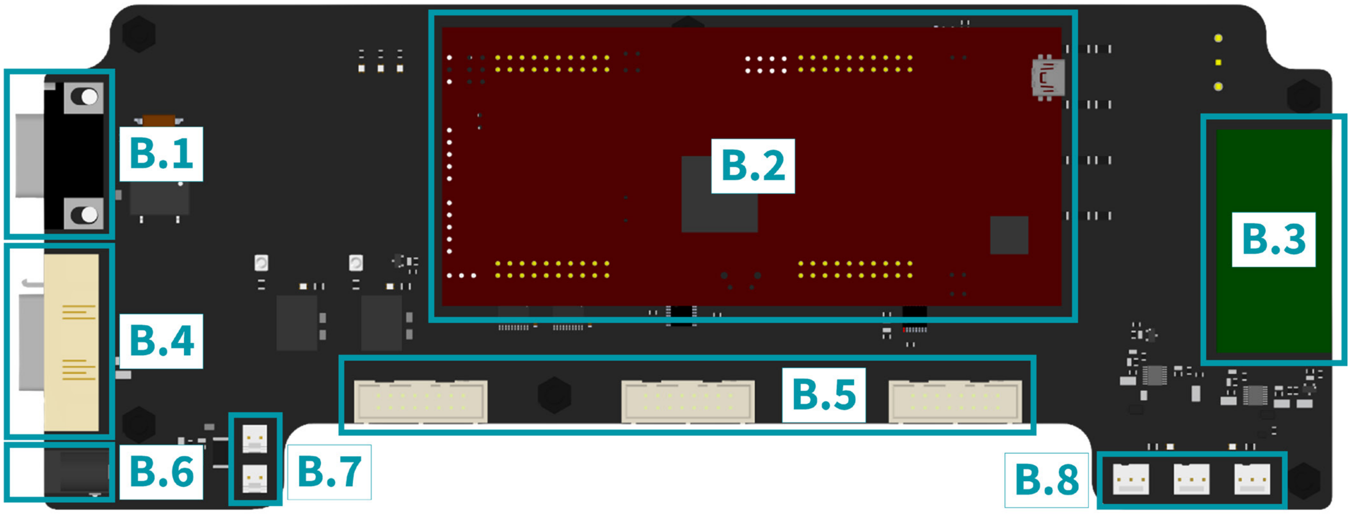

Figure 7: Controller PCB top view

Table 3: Controller PCB subsystem descriptions

Label	Description
B.1	CAN Communication Port
B.2	TI LaunchPad Controller
B.3	Phase Voltage Feedback
B.4	Auxiliary Communication/Feedback
B.5	Differential Gate Driver Signals
B.6	Controller Input Power
B.7	Output +12 V Power
B.8	Current Measurement Feedback

2.4 Input/Output Pinout

This design features a variety of ports for connecting external sensors, controlling external hardware, and communicating directly with the onboard controller. Each of these interfaces will be discussed in the later sections of this document. This section provides a quick reference to the pinouts of the various ports.

2.4.1 High Power Terminals

The high-power input DC bus and output phase connections, shown in Figure 8, are made through Würth Elektronik® 7461059 terminals. These terminals are attached to the PCB through a press-fit process and require no solder for the PCB connection. The terminals include internal M6 threads to support mounting high-power wires or bus bars directly to the terminals using M6 screws.

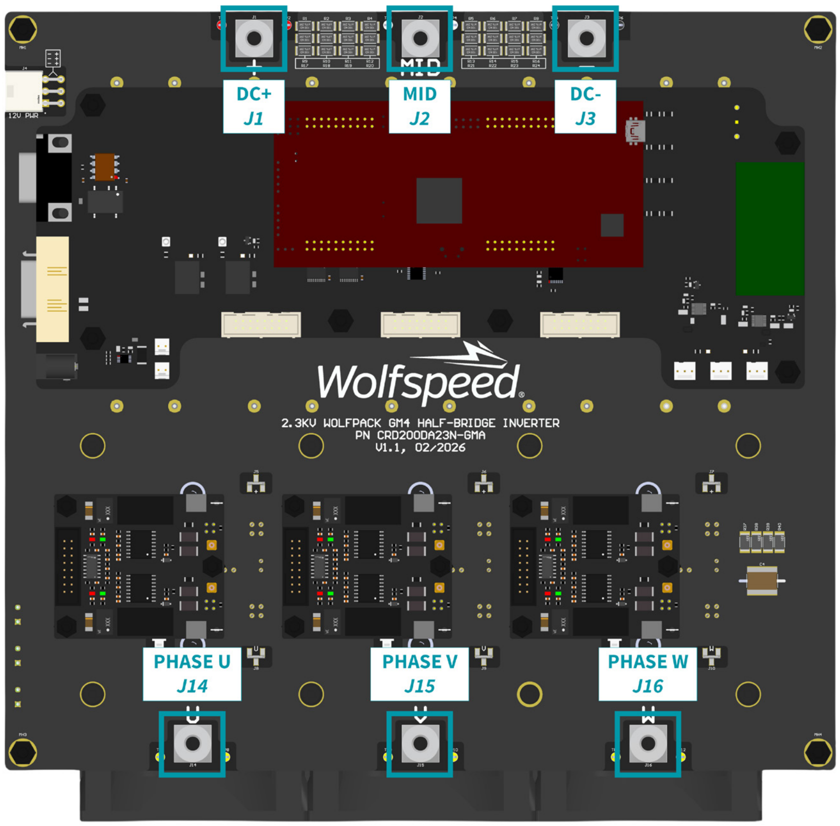

Figure 8: High-power terminal locations

2.4.2 Voltage Feedback Connector Pinout

The design includes circuitry to measure the output phase voltages using differential inputs. These measurements do not have the bandwidth to measure high-frequency drain-to-source voltage switching dynamics but can be useful for low-frequency voltage measurements such as after a filter element. The voltage feedback uses a Phoenix Contact® 1719231 connector with the pinout shown in Figure 9, and the corresponding pin functionalities are shown in Table 4. Wires can be inserted directly into this connector, so no mating connector is required. A narrow tool such as a small screwdriver can be inserted into the upper square opening and pushed in to open the spring-loaded contact to allow the wire end to be inserted into the lower circular opening. The plus and minus inputs are differential allowing for measurement on a floating voltage rail. The signals are stepped down to a low voltage by a voltage divider so that the measurement can be performed by the onboard controller. The corresponding voltage conditioning circuit is discussed further in Section 3.5.

Figure 9: Voltage feedback connector pinout (control board J7)

Table 4: Voltage feedback connector (control board J7) pin functionalities

Pin #	Signal	Description
1	U+	Positive differential Phase U voltage feedback
2	U-	Negative differential Phase U voltage feedback
3	V+	Positive differential Phase V voltage feedback
4	V-	Negative differential Phase V voltage feedback
5	W+	Positive differential Phase W voltage feedback
6	W-	Negative differential Phase W voltage feedback

Note that the signals appear as A, B, and C on the silkscreen instead of U, V, and W.

2.4.3 Controller Power Connector Pinout

The controller board is powered from an external +12V supply. The power is applied through a CUI Devices® PJ-102AH barrel connector (*J11* on the control board) with the pinout shown in Figure 10. The recommended mating connector is CUI Devices PP3-002A. The control board can be power using a wall power adapter with a mating barrel jack connector such as the Phihong® PSAA30R-120-R wall adapter.

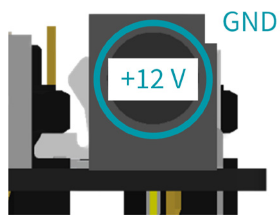

Figure 10: Controller power connector pinout (control board J11)

2.4.4 Fan Power Connector Pinouts

The attached heat sink includes three separate fans for air-cooling the reference design (see Section 5.1). Each of these fans requires a maximum power of approximately 70 W for a total requirement of 210 W. Since this power requirement exceeds the rating of the barrel jack connector discussed in Section 2.4.3, this design includes a second input power connector which is separate from the control board. The connector, which is mounted on the power stage PCB, is 0039301062 manufactured by Molex® with the pinout shown in Figure 11. Recommended power supply units (PSUs) for applying 12 V to this connector are the Bel Power Solutions® SDI300G-12-U-P219 and the Mean Well® GST280A12-C6P which are rated for 288 W and 252 W, respectively. Both these PSUs include the proper mating connector by default.

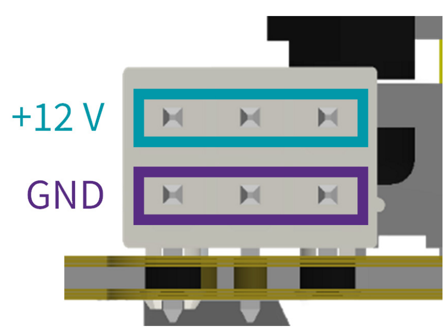

Figure 11: Fan input power connector pinout (J4)

Each fan connects to the PCB through a Phoenix Contact® 1755736 connector mounted to the bottom of the PCB as shown in Figure 12 (*J17-J19*). These connectors are connected through the PCB to the *J4* input power connector. Though this +12 V voltage rail and corresponding GND are routed on the same PCB as the power stage, there is sufficient creepage and clearance distance between the power stage and these low-voltage connections. The fans are already connected by default when the unit is shipped. The mating connector is Phoenix Contact 1754449, and each fan has a dedicated connector.

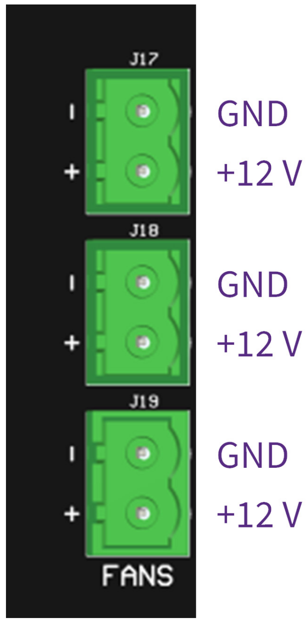

Figure 12: Output fan power connector pinout (J17-J19, bottom side)

2.4.5 CAN Port Pinout

The isolated Controller Area Network (CAN) port is a standard male DB9 connector (Amphenol® L717SDE09PA4CH4RC309) with the pinout shown in Figure 13 and descriptions shown in Table 5. This CAN port can be mated with any standard DB9 female connector and is intended to be used with a CAN adapter such as the PEAK System® PCAN-USB Pro FD or National Instruments® USB-8473. Notably, the controller board includes two CAN channels, A and B. Either CAN channel can be used to control or monitor this design; however, only CANA includes isolation. The CANB channel is not isolated, so it requires an isolated CAN adapter for communication. The *J9* CAN port connector is attached to **CANA**, whereas the *J10* auxiliary connector is attached to CANB.

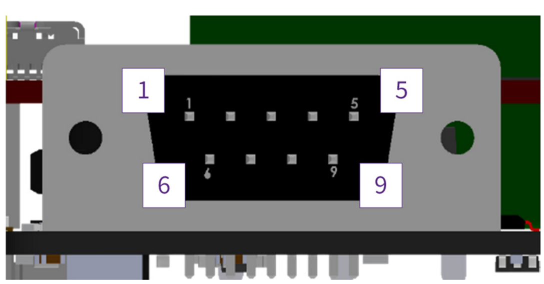

*Figure 13: CAN port connector pinout (control board J9 attached to **CANA**)*

Table 5: CAN port pinout (control board J9 attached to **CANA**)

Pin #	Name	Type	Description
1	NC0	—	No Connect
2	CANA_L	Digital (I/O)	Isolated CAN Port A Low
3	V-	Power	Isolated Ground
4	NC1	—	No Connect
5	SHLD	Power	Isolated Ground
6	O(V-)	—	No Connect
7	CANA_H	Digital (I/O)	Isolated CAN Port A High
8	NC2	—	No Connect
9	V+	Power	Isolated +5V Power

I = Input | O = Output

2.4.6 Auxiliary Controller Connector Pinout

The control board includes an auxiliary connector for connecting spare/extra peripherals. This connector includes pin attachments for a fourth current sensor, a second CAN interface (**CANB** which is not isolated), and encoder ports. The connector is 10226-55G3PC manufactured by 3M® and is a standard Mini D ribbon connector. The connector pinout and descriptions are shown in Figure 4 and Table 6, respectively.

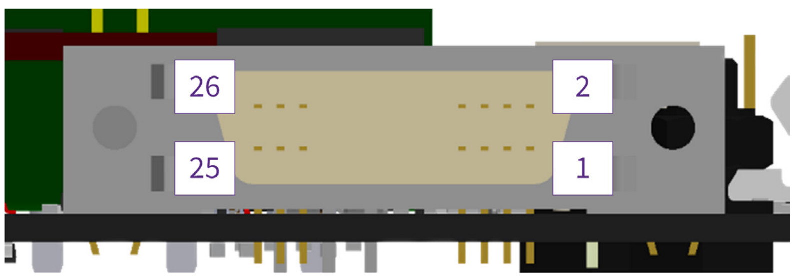

Figure 14: Auxiliary controller connector pinout (control board J10)

Table 6: Auxiliary controller connector pinout (control board J10)

Pin #	Name	Type	Description
1	CANB_L	Digital (I/O)	Isolated CAN Port B Low
2	CANB_H	Digital (I/O)	Isolated CAN Port B High
3	GND	Power	Controller Ground
4	GND	Power	Controller Ground
5	GND	Power	Controller Ground
6	IEXT-M	Analog (I)	External Current Sensor Signal
7	-15V	Power	External Current Sensor Power -15 V
8	+15V	Power	External Current Sensor Power +15 V
9	GND	Power	Controller Ground
10	+3V3	Power	+3.3 V Power Supply Output
11	GND	Power	Controller Ground
12	+5V	Power	+5 V Power Supply Output
13	GND	Power	Controller Ground

Pin #	Name	Type	Description
14	QEA_A	Digital (I)	Quadrature Encoder Port A Input A
15	GND	Power	Controller Ground
16	QEA_B	Digital (I)	Quadrature Encoder Port A Input B
17	GND	Power	Controller Ground
18	QEA_I	Digital (I)	Quadrature Encoder Port A Input I
19	GND	Power	Controller Ground
20	+5V	Digital (I)	+5 V Power Supply Output
21	GND	Power	Controller Ground
22	QEB_A	Digital (I)	Quadrature Encoder Port B Input A
23	GND	Power	Controller Ground
24	QEB_B	Digital (I)	Quadrature Encoder Port B Input B
25	GND	Power	Controller Ground
26	QEB_I	Digital (I)	Quadrature Encoder Port B Input I

I = Input | O = Output

2.4.7 Thermistor Connector Pinouts

The design includes connectors which are directly attached to the integrated power module thermistors. These thermistors are included in the power modules to monitor the module substrate temperatures. Each module has external terminals to measure the corresponding thermistor resistance, as shown in Figure 15. The PCB connectors, *J11-J13*, are attached to these module thermistor terminals and provide an easy method to perform a measurement of the thermistor resistances and therefore its corresponding temperature. These connectors are 640456-2 manufactured by TE Connectivity®, and the recommended mating connectors are 0022012027 connectors manufactured by Molex (with Molex 0008500113 pins). These connectors can be directly measured with any isolated measurement circuit to determine the thermistor resistance; by default, the connectors are attached to the thermistor feedback pins of the attached CGD1700HB2M-UNA gate drivers (see Section 3.2) as shown notionally in Figure 16 (along with the connector pinouts). The gate drivers encode the resistance to an isolated duty cycle which can be read directly by the controller. See Section 3.6 regarding the thermistor duty cycle encoding.

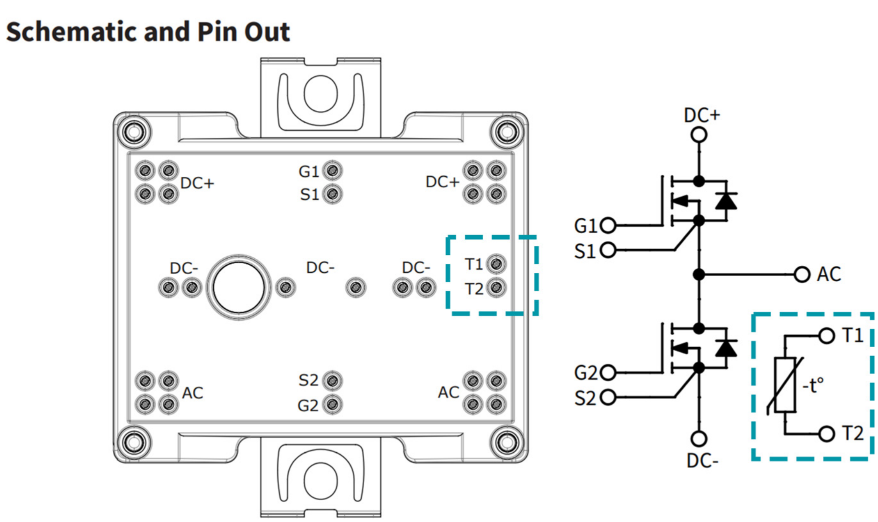

Figure 15: Integrated power module thermistor terminals

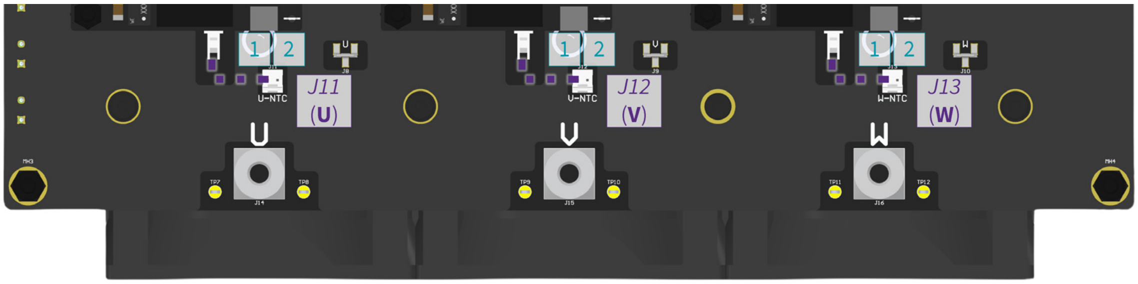

Figure 16: Thermistor connector pinouts and connections (J11-J13)

Note that in the hardware update from Version 1.0 (indicated on the silkscreen by “V1.0, 11/2024”) to Version 1.1 (indicated on the silkscreen by “V1.1, 02/2026”), the thermistor connectors moved slightly to avoid interference with the additional heat sink mounting holes discussed in Section 5.1. No electrical functionality changed when moving the thermistor connectors.

2.4.8 Gate Driver Signal Connector Pinouts

The control board has three outputs, shown in Figure 17, for driving the three gate drivers included on this design (see Section 3.2 for more information about the gate drivers). The input pinouts of the gate drivers are described in Table 7. The high-frequency signals are all transmitted differentially for improved noise immunity (see Section 3.2). By default, the design ships with ribbon cables connecting the controller outputs to the corresponding gate driver inputs. These ribbon cables only transmit low-voltage control signals (so the cables do not include any high-voltage signals) but should be routed away from high-voltage wires such as the DESAT cables (see Section 2.4.9). Note that the controller was designed to support a variety of gate drivers, so some of the gate driver control features in the controller PCB schematic are not valid for the CGD1700HB2M-UNA gate drivers used in this design. Refer to **PRD-06992** for more information about the CGD1700HB2M-UNA gate drivers.

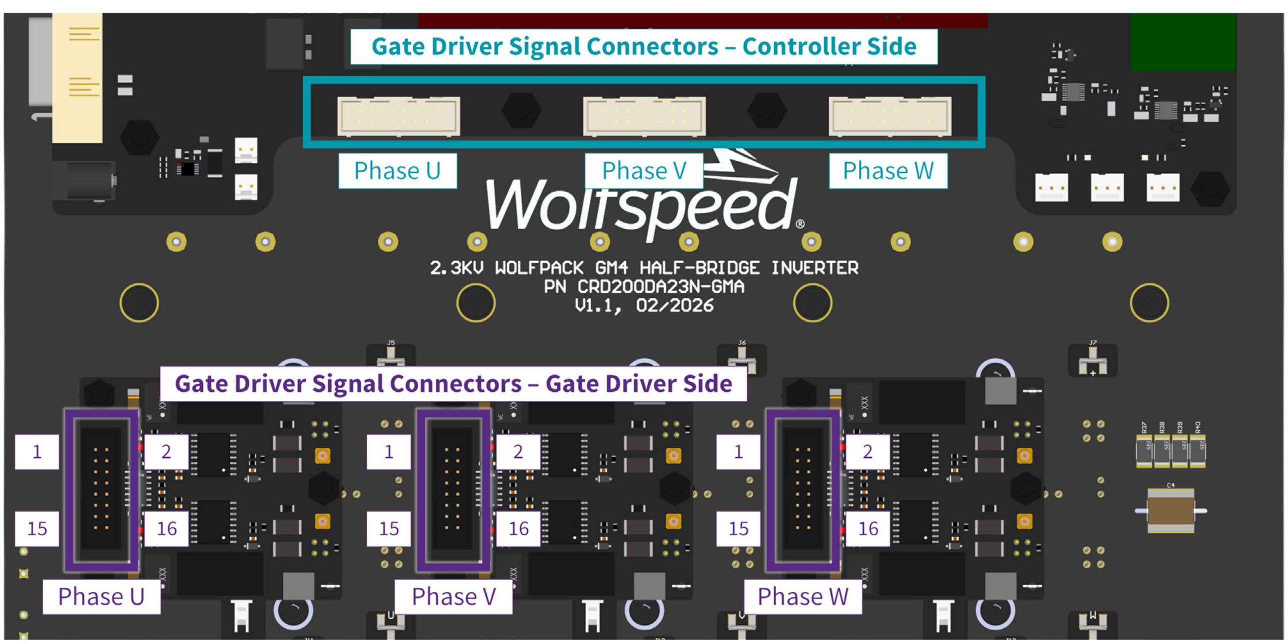

Figure 17: Gate driver connector locations and pinouts

Table 7: Pinout of gate driver input connectors

Pin	Name	Description
1	VDC	Power supply input pin (+12 V Nominal Input).
2	Common	Common.
3	HS-PWM-P*	Positive line of 5 V differential high-side PWM signal pair. Terminated into 120 Ω.
4	HS-PWM-N*	Negative line of 5 V differential high-side PWM signal pair. Terminated into 120 Ω.
5	LS-PWM-P*	Positive line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω.
6	LS-PWM-N*	Negative line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω.
7	$\overline{\text{FAULT}}$-P*	Positive line of 5 V differential fault condition signal pair. Drive strength 20 mA. A low state on FAULT indicates when a desaturation fault has occurred. The presence of a fault precludes the gate drive output from going high.
8	$\overline{\text{FAULT}}$-N*	Negative line of 5 V differential fault condition signal pair. Drive strength 20 mA.
9	THERM-P*	Positive line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA. Temperature measurement is encoded via duty cycle.
10	THERM-N*	Negative line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA. Temperature measurement is encoded via duty cycle.
11	NC	No connect.
12	Common	Common.
13	No	No connect.
14	Common	Common.
15	$\overline{\text{RESET}}$/EN	Pull up or leave floating to enable the gate driver. Onboard 10 kΩ pull up. When a fault exists, bring this pin low for >1000 ns to clear the fault on the rising edge.
16	Common	Common.

* Inputs 3-10 are differential pairs.

2.4.9 Overcurrent Protection Pinouts

The gate drivers used in this design feature overcurrent protection in the form of a desaturation, commonly referred to as a DESAT, circuit which monitors the drain-to-source voltage (V_{DS}) of each switch position to check for increased on-state voltage due to high current flowing through the channel of the device. More information about this circuit is provided in Section 3.2.2. To connect the gate driver DESAT circuits with the MOSFET drain terminals, the CRD200DA23N-GMA includes spade connectors which connect to the drain terminal of each power module switch position. The locations of these spade connectors are shown in Figure 18. By default, these spade connectors are attached with a flying wire to the DESAT spade connectors on the CGD1700HB2M-UNA gate drivers, as shown in Figure 18. Note that these wires can be floating at the full bus voltage during inverter operation. The spade connectors on the CRD200DA23N-GMA board are 4928 manufactured by Keystone Electronics®. The recommended mating connector is 0190050001 manufactured by Molex. On the CGD1700HB2M-UNA gate drivers, the connector is 735187-2 manufactured by TE Connectivity, and the recommended mating connectors for these are 7-520365-2 or 2-520272-2 which are both manufactured by TE Connectivity. These connections cannot be left floating on the gate drivers, since it will immediately trip an overcurrent fault when left floating.

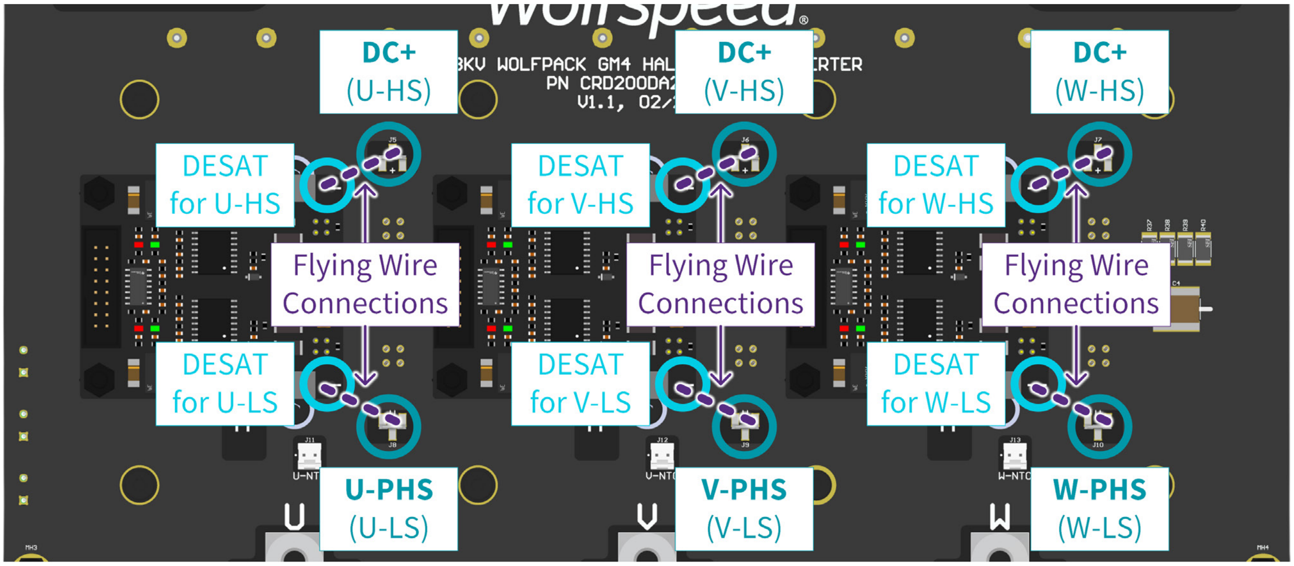

Figure 18: DESAT connection locations

2.4.10 Spare +12 V Connector Pinouts

The control board includes two connectors, *J12-J13*, for powering +12 V auxiliary equipment. These connectors are 640456-2 manufactured by TE Connectivity, and the recommended mating connectors are 1375820-2 manufactured by TE Connectivity. The pinouts for these connectors are shown in Figure 19. These connectors can be used to drive any always-on +12 V peripherals. For example, these outputs can be used to operate a fan to cool external equipment. Notably, these outputs are powered from the input controller power connector (see Section 2.4.3), so these connectors do not have the drive strength to operate the integrated heat sink fans which require significantly more power. These connectors should only be used to drive low-power peripherals. By default, these connectors are not attached to anything.

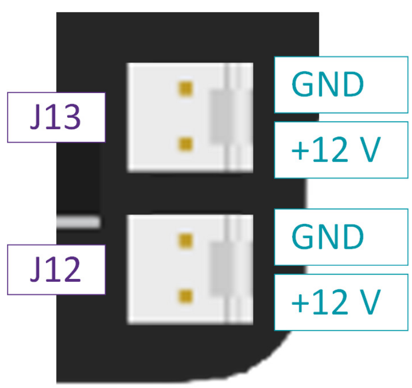

Figure 19: Spare +12 V power connector pinouts

2.4.11 Current Sensor Connector Pinouts

In its default configuration, this design does not include integrated current sensors. However, the board includes provisions to add external current sensors. The connectors, *J4-J6*, on the control board allow adding one or more external current sensors. These connectors each include +15 V and -15 V voltage rails for biasing the current sensor and a feedback measurement pin with the pinouts shown in Figure 20. These connectors are

0022232031 manufactured by Molex and the recommended mating connectors are 0022013037 manufactured by Molex. These inputs are intended to operate with closed-loop current transducers such as the LEM® LF 510-S current sensors. Using current output signals – as opposed to voltage output signals – is preferred for better immunity against electrical noise injected into the wiring between the sensor and the controller. Closed-loop transducers have higher accuracy and lower temperature drift compared to open-loop transducers. The current signals are filtered and scaled and then sensed as a voltage signal by analog-to-digital converters (ADCs) on the controller. The peak primary current corresponds to a 0-3 V signal centered at 1.5 V at the ADC input. The controller features a DC/DC converter to provide the bipolar ±15 V power required for the sensors. Provisions for a fourth current sensor are available on the control board for an external sensor to measure an additional current using the auxiliary connector (see Section 2.4.6). The corresponding current conditioning circuits are discussed in further detail in Section 3.4.

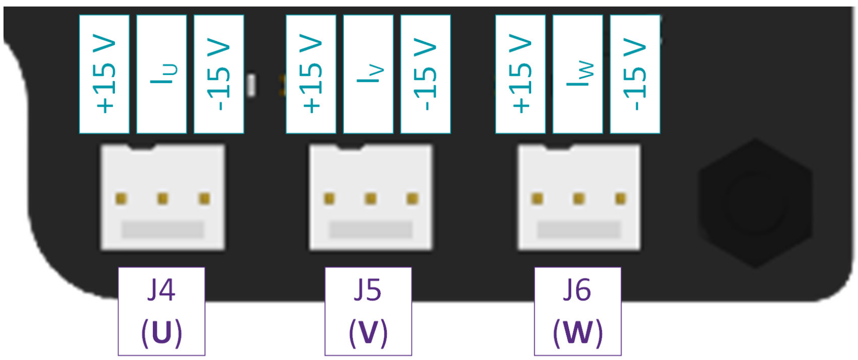

Figure 20: Current sensor connector pinouts (control board J4-J6)

3. System Description

CAUTION

IT IS NOT NECESSARY FOR YOU TO TOUCH THE BOARD WHILE IT IS ENERGIZED. WHEN DEVICES ARE BEING ATTACHED FOR TESTING, THE BOARD MUST BE DISCONNECTED FROM THE ELECTRICAL SOURCE AND ALL BULK CAPACITORS MUST BE FULLY DISCHARGED.

SOME COMPONENTS ON THE BOARD REACH TEMPERATURES ABOVE 50° CELSIUS. THESE CONDITIONS WILL CONTINUE AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED. DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE BOARD.

PLEASE ENSURE THAT APPROPRIATE SAFETY PROCEDURES ARE FOLLOWED WHEN OPERATING THIS BOARD AS SERIOUS INJURY, INCLUDING DEATH BY ELECTROCUTION OR SERIOUS INJURY BY ELECTRICAL SHOCK OR ELECTRICAL BURNS, CAN OCCUR IF YOU DO NOT FOLLOW PROPER SAFETY PRECAUTIONS.

警告

通电时不必接触板子。连接器件进行测试时，必须切断板子电源，且大容量电容器必须释放完所有电荷。

板子上一些组件的温度可能超过50摄氏度。移除电源后，上述情况可能会短暂持续，直至大容量电容器完全释放电荷。通电时禁止触摸板子，应在大容量电容器完全释放电荷后，再操作电路板。

请确保在操作电路板时已经遵守了正确的安全规程，否则可能会造成严重伤害，包括触电死亡、电击伤害、或电灼伤。，大容量电容器已释放了所有电量。只有在切断板子电源，且大容量电容器完全放电后，才可更换待测试器件。

警告

通電している時にボードに接触する必要がありません。設備をつないで試験する時、必ずボードの電源を切ってください。また、大容量のコンデンサーで電力を完全に釈放してください。

ボードのモジュールの温度は50度以上になるかもしれません。電源を切った後、上記の状況がしばらく持続する可能性がありますので、大容量のコンデンサーで電力を完全に釈放するまで待ってください。通電している時にボードに接触するのは禁止です。大容量のコンデンサーで電力をまだ完全に釈放していない時、ボードを操作しないでください。

ボードを操作している時、正確な安全ルールを守っているのを確保してください。さもなければ、感電、電撃、厳しい火傷などの死傷が出る可能性があります。

3.1 Power Stage

The power stage of this design uses two-series stacked sets of five 65 µF low-inductance capacitors each in parallel to form a total of 162.5 µF of DC-link capacitance. The capacitors used are KEMET® C4AQQEW5650A3BJ film capacitors with a voltage rating of 1.1 kV. The series-stacked arrangement increases the bus voltage rating to 2.2 kV. The capacitors are charged through the input DC terminals (see Section 2.4.1) and connect directly to the DC+ and DC- terminals of the power modules using low-inductance interleaved copper pours. The DC-link capacitor circuitry and the connections to the power module are shown in schematic in Figure 21. The PCB used in this design features interleaved DC+ and DC- copper layers to increase the flux cancellation between layers and reduce the inductance between the capacitors and the power module input pins. The interleaved layers are indicated in the notional PCB stack-up shown in Table 10, which shows the signals/planes on each circuit board layer in the area around the DC bus.

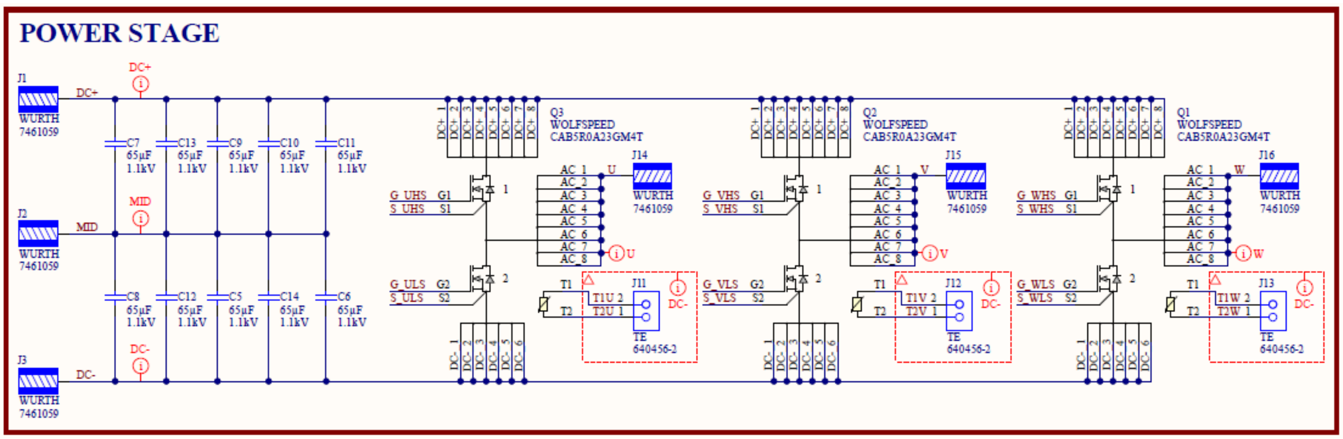

Figure 21: Power stage circuitry (bulk capacitors and power modules)

Table 8: DC bus PCB layer stack-up

Layer #	Primary Signals
1	DC+/MID
2	DC-
3	DC+
4	DC-
5	DC+
6	DC-

For voltage balancing between the series-stacked capacitors and to ensure the DC-bus safely discharges after shutdown, the design includes balancing/bleed resistors. These resistors discharge the bus to less than 50 V in under 2.5 minutes when the input voltage is removed from the system. These resistors are connected to the DC bus at all times to ensure the bus is always depleted after system shutdown. The balance/bleed resistors circuit is shown in Figure 22.

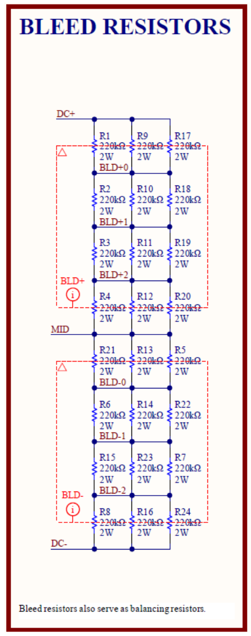

Figure 22: Balance/bleed resistors circuit

3.2 Gate Drivers

The CRD200DA23N-GMA inverter uses three CGD1700HB2M-UNA gate drivers, shown in Figure 23, to independently drive the three onboard power modules. These gate drivers use the Texas Instruments UCC21710 gate driver integrated circuit (IC) and are rated up to a DC-bus voltage of 1500 V. By default, these gate drivers use 0 Ω external turn-on and turn-off resistors ($R_{G(EXT),ON}$ and $R_{G(EXT),OFF}$). For users wanting to evaluate the performance with different gate resistors, the gate resistors can be easily changed on the gate driver board. The resistors are standard 2512 (6432 metric) footprint resistors. The default resistors are Vishay Dale® CRCW25120000Z0EGHP. To maximize performance, it is recommended to use pulse-rated resistors when replacing/changing the gate resistors. See **PRD-06992** for more information about the CGD1700HB2M-UNA gate driver and changing the gate resistors.

Figure 23: CGD1700HB2M-UNA gate driver

These gate drivers use Wolfspeed's standard universal gate driver footprint and communication, so other gate drivers (with suitable isolation ratings) from Wolfspeed or gate driver partners can also be evaluated in this design. A list of Wolfspeed and partner gate drivers are available here. The gate driver schematic section for this design is shown in Figure 24. These CGD1700HB2M-UNA gate drivers have three non-standard changes which would need to be considered if adopting a different gate driver. First, as mentioned previously, these gate drivers are configured with 0 Ω gate resistors, whereas the standard CGD1700HB2M-UNA gate driver includes 1 Ω gate resistors by default. Second, the output connectors on these gate drivers are taller than the standard output connectors to ensure a reliable connection to the power stage. The added height ensures that the gate drivers make good connection to the power PCB, even through the acrylic sheet employed on this design. The updated connectors are ESQ-102-12-G-D connectors manufactured by Samtec®; though the mating connector is still Samtec TSM-102-01-SMDV for these updated connectors. Third, the blanking capacitors on the gate drivers, *CT19* and *CT20*, were increased from 56 pF to 120 pF to accommodate the CAB5R0A23GM4T power module and the high DC-bus voltage.

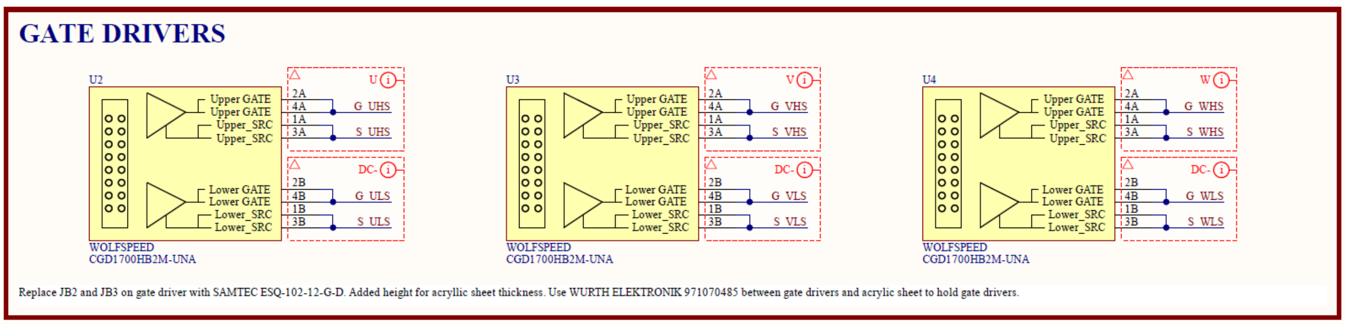

Figure 24: Independent CGD1700HB2M-UNA gate drivers

3.2.1 Differential Signaling

The gate drivers communicate with the controller through differential signaling for improved noise immunity compared to traditional single-ended communication. Differential signaling significantly reduces the impact of radiated noise from the switching events of a power module. A single-ended signal can be converted to a differential signal by transmitting both the original signal and its complement in two closely coupled wires. At the receiver, the two signals are compared in order to reconstruct the original signal. Figure 25 illustrates this principle with an example of induced noise forced onto the cable somewhere between the transmitter and receiver. The noise affects both the original signal and the complement by the same magnitude assuming that the cables are consistently coupled. Thus, when the receiver compares the two signals, the difference is unaffected by the noise induced on the line and the intended original signal is created. As discussed in Section 2.4.8, the gate drivers are connected to the controller with ribbon cables by default when the unit is shipped. Though the signals have improved noise immunity due to the differential signaling, the connection should still be kept as short as possible to further improve the noise immunity.

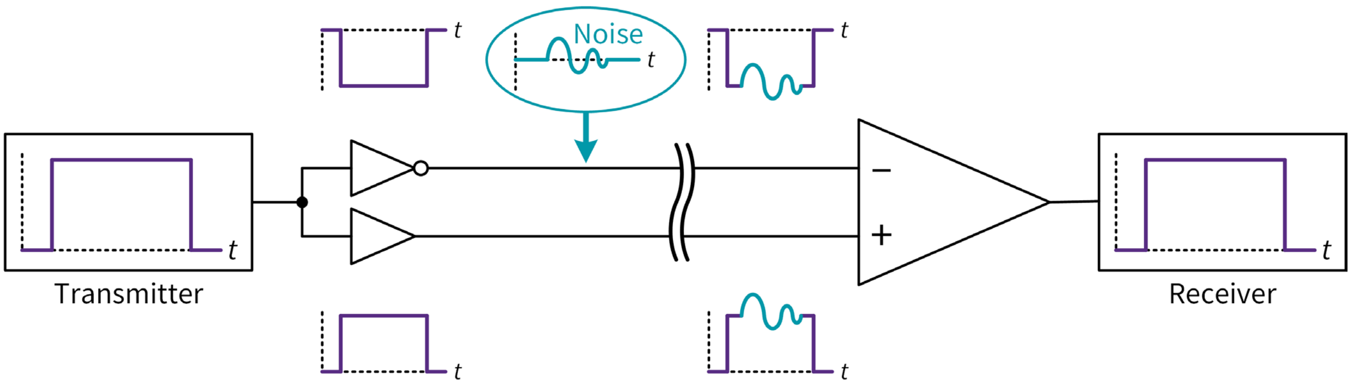

Figure 25: Noise immunity improvement provided by differential signaling

3.2.2 Overcurrent Protection

As discussed in Section 2.4.9, the CGD1700HB2M-UNA gate drivers include integrated overcurrent protection in the form of a DESAT circuit. Flying wires are used to connect the drain terminal of each switch position to the corresponding gate driver channel, as shown in Figure 18; The spade terminal net connections are shown in Figure 26. The DESAT circuit monitors the drain-to-source voltage (V_{DS}) of the relevant switch position to check for increased on-state voltage due to high current flowing through the channel of the device. An elevated VDS when the device is turned on indicates that the device is conducted excessive current, often in the form of a shoot-through or short circuit event. The DESAT circuit monitors for this voltage and systematically shuts down the channel when a fault occurs. For more information about the integrated DESAT circuit on the CGD1700HB2M-UNA, see the gate driver user guide (**PRD-06992**) and for more information about DESAT implementations in general, see **PRD-09301**.

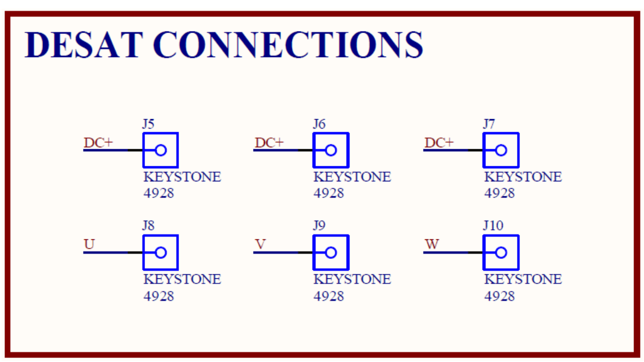

Figure 26: Spade connections for attaching the MOSFET drain terminals to the gate driver DESAT circuit

When an overcurrent event occurs on one or more of the switch positions, the tripped gate driver will engage a soft-turnoff feature to turn off the tripped device in a controlled manner. The faulted switch position will indicate the fault by illuminating a red fault LED on the gate driver PCB and will transmit a fault signal to the controller. The default firmware (see Section 4.1) will quickly disable all the other gate drivers using the C2000 trip zone hardware functionality. All the gate drivers will be held off until the faulted gate driver is reset. Note that without proper firmware implementation, only the tripped gate driver(s) will turn off after a fault condition. If an operator customizes the firmware, it is important to keep functionality which quickly detects faults in one or more gate driver(s) and safely disables the remaining drivers.

3.3 Snubber Circuits

The high *dV/dt* achievable with SiC MOSFETs is attractive in many applications since it leads to reduced switching losses and higher switching frequencies. However, it can introduce overshoot into the drain-to-source voltage of the semiconductor. In many designs with low-inductance PCB layout, the slight voltage overshoot is not an issue in the system assembly. However, in some designs – especially when operating a device close to its rated blocking voltage – the voltage overshoot can be problematic because it can lead to exceeding the safe-operating-area (SOA) of the device. By default, the CRD200DA23N-GMA includes several provisions to limit V_{DS} overshoot on the device which are listed below.

- *Wolfspeed's Generation 4 MOSFETs* include a softer body diode which significantly reduces V_{DS} overshoot due to the improved reverse recovery performance
- *Interleaved DC+ and DC- Layers* which achieve flux cancellation
- *Wide Copper Pours* which increase the cross-sectional areas
- Compact Power Loop with DC-link capacitors close to the modules which reduces the power loop area

These features together minimize the PCB inductance of the design and reduce the device V_{DS} overshoots. Even with these features, some customers still prefer to use snubber elements to further reduce the risk of overshoot and ringing. The CRD200DA23N-GMA includes a resistor-capacitor (RC) snubber circuit placed very close to the power module terminals to create a dissipative shunt path for high-frequency energy. When sized appropriately, an RC snubber can reduce a power module's maximum overshoot voltage and damp oscillatory ringing. Figure 27 shows the influence on device V_{DS} of a CAB5R0A23GM4T half-bridge power module in an Analog Devices® LTspice® double-pulse test (DPT) simulation. The simulation was performed at a bus voltage of 1500 V and a load current of 167 A. The introduction of the snubber elements reduces both the overshoot and the oscillations significantly. For more information about the DPT simulation for evaluating performance in different operating conditions, visit https://www.wolfspeed.com/tools-and-support/power/ltspice-and-plecs-models/.

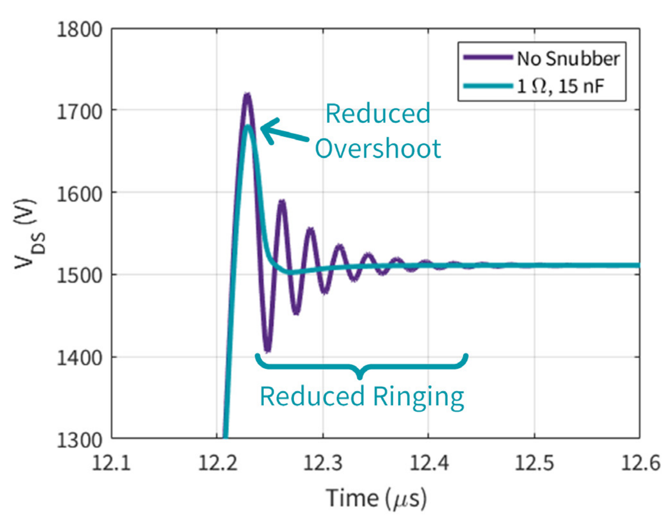

Figure 27: Simulation comparison with and without a snubber circuit

For the most effective RC snubber implementation, the snubber components need to be placed physically close to the terminals of the power module to limit the inductance between the MOSFETs and the snubber circuit elements. This design uses four individual RC snubber circuits so that each power module can have snubber elements close to its power terminals. The RC snubber schematics are shown in Figure 28, and the PCB layout implementations are shown in Figure 29. For best performance, the snubber elements are symmetrically placed equidistant from the power modules, and the snubber capacitors include a slot underneath for increase creepage distance. If snubber customization is required, the snubber uses standard 2512 (6432 metric) footprint resistors and 3640 (9110 metric) footprint capacitors. These can be easily swapped for alternative components with the same package footprint. Notably, if adopting alternative snubber components, the capacitors should have a voltage rating greater than the peak V_{DS} overshoot of the device, and the resistors should have suitable power rating to dissipate the high frequency energy shunted through the snubber.

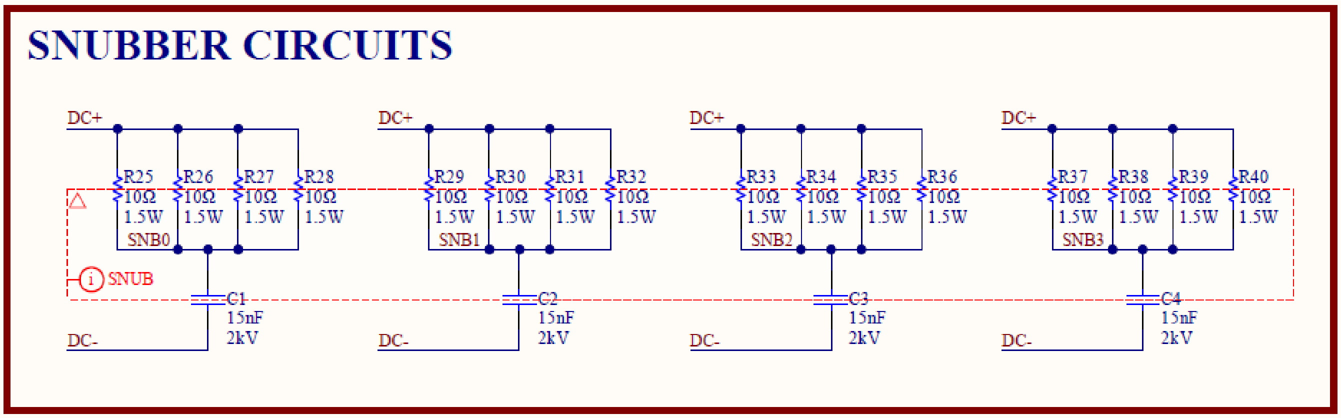

Figure 28: RC snubber circuit

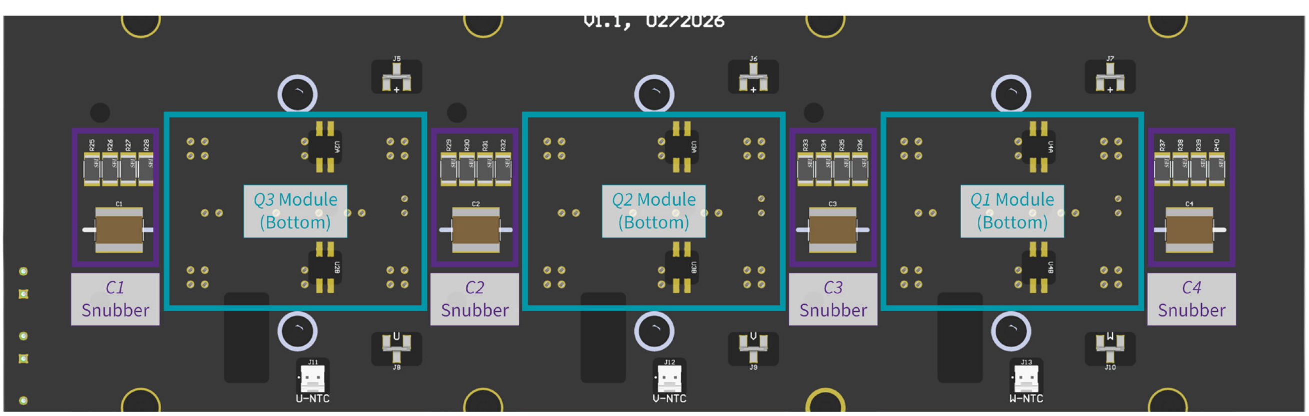

Figure 29: RC snubber circuit locations with respect to the power modules

3.4 Current Sensing

As discussed in Section 2.4.11, the design includes connections to attach an external closed-loop current transducer such as the LEM LF 510-S current sensor. By default, there are no integrated current sensors on the CRD200DA23N-GMA, though it was designed to easily attach sensors through the connectors *J4-J6* on the control board (for the AC measurements) and through *J10* on the control board (for the DC measurement). The conditioning circuits for measuring the AC current sensors are shown in Figure 30, and the conditioning circuit for measuring the DC current sensor is shown in Figure 31. This circuit was originally designed for use with the LEM LF 510-S current sensors, so by default the circuit is configured such that a ±800 A peak current corresponds to a 0-3 V signal centered at 1.5 V at the ADC input. The operational amplifier feedback circuitry can easily be modified to support other sensor gains and dynamic ranges. The controller features a DC/DC converter to provide the bipolar ±15 V power required for the sensors.

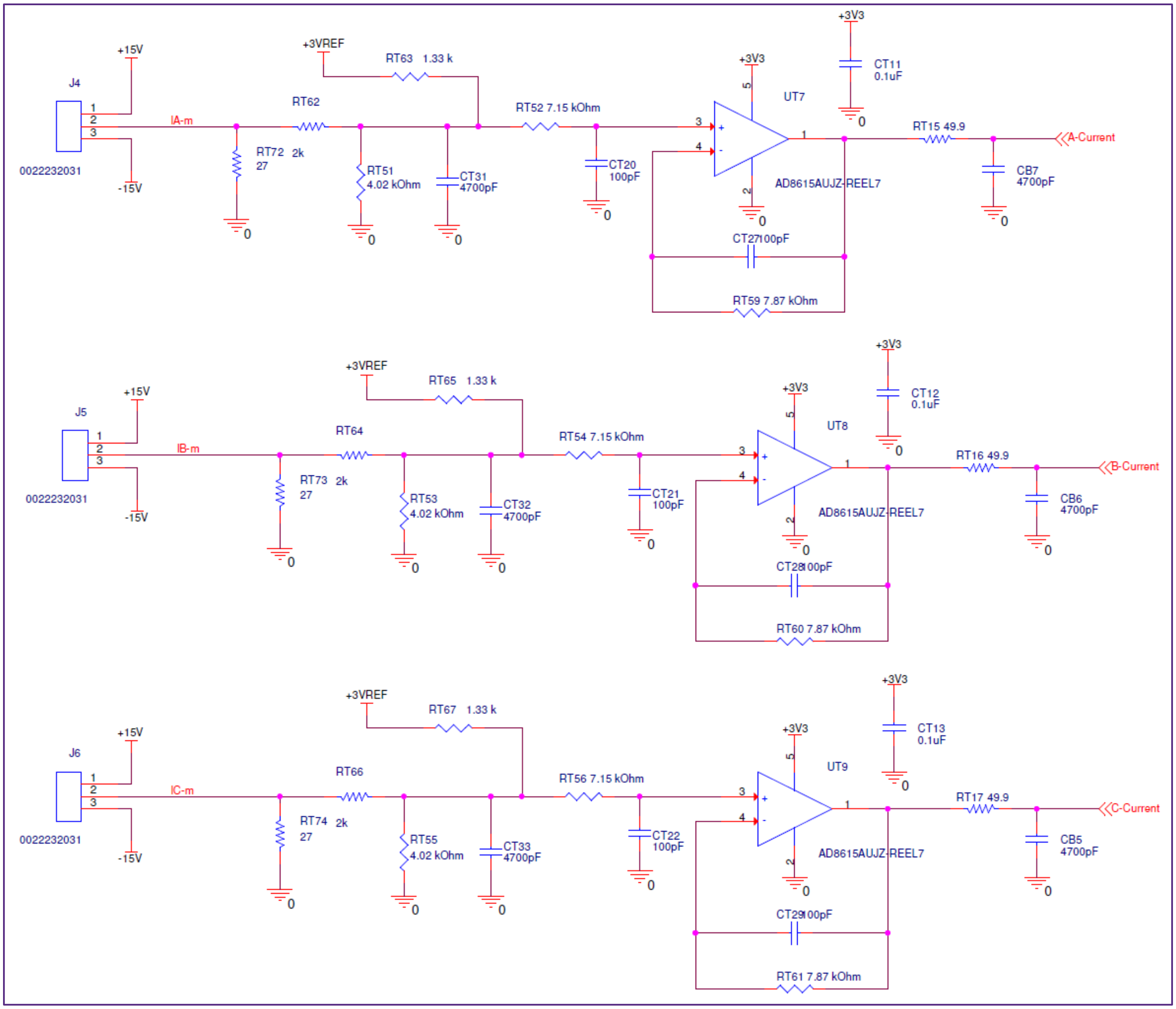

Figure 30: AC current conditioning circuit on the control board

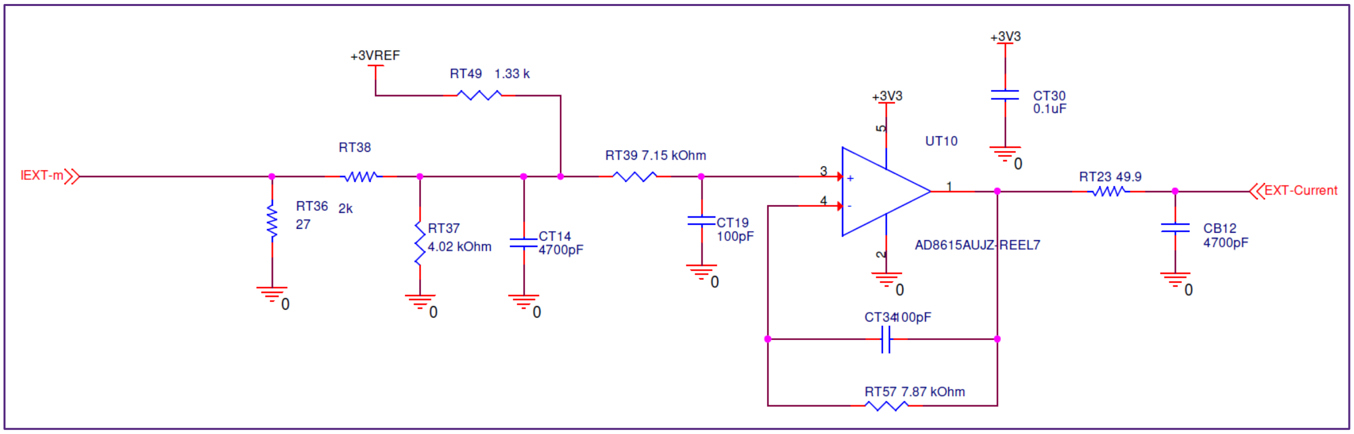

Figure 31: DC current conditioning circuit on the control board

3.5 Voltage Sensing

The controller board includes provisions to measure AC voltages through the *J7* connector on the control PCB (see Section 2.4.2). The "+" and "-" inputs for each phase are differential inputs to support floating voltage measurements. As shown in the conditioning circuit in Figure 32, the voltage inputs are scaled down by a voltage divider and filtered to a low voltage that can be sensed by the controller. A ±1500 V input is scaled down to 0-3 V centered at 1.5 V for a 0 V input. The voltage sense measurements are brought in as high-voltage signals without pre-scaling for better noise immunity. Any noise injected onto the high voltage signal will create negligible noise on the final signal compared to transmitting the signal pre-scaled to a low voltage 0-5 V signal. Compared to the default control board on the CRD300DA12E-XM3, the voltage conditioning circuit on this design is modified slightly to be optimized for the expected voltages of this reference design. The resistors *RT29*, *RT75*, and *RT96* were changed from 1.8 kΩ to 1 kΩ, as shown in Figure 32, to expand the dynamic measuring range of the circuit in order to support measuring voltages up to the full bus voltage. Notably, the voltage measurement circuitry does not have the bandwidth to measure V_{DS} dynamics such as *dV/dt* and overshoot. To capture those performance metrics, an oscilloscope would still be required. This circuit is more suitable for measuring low-frequency voltages.

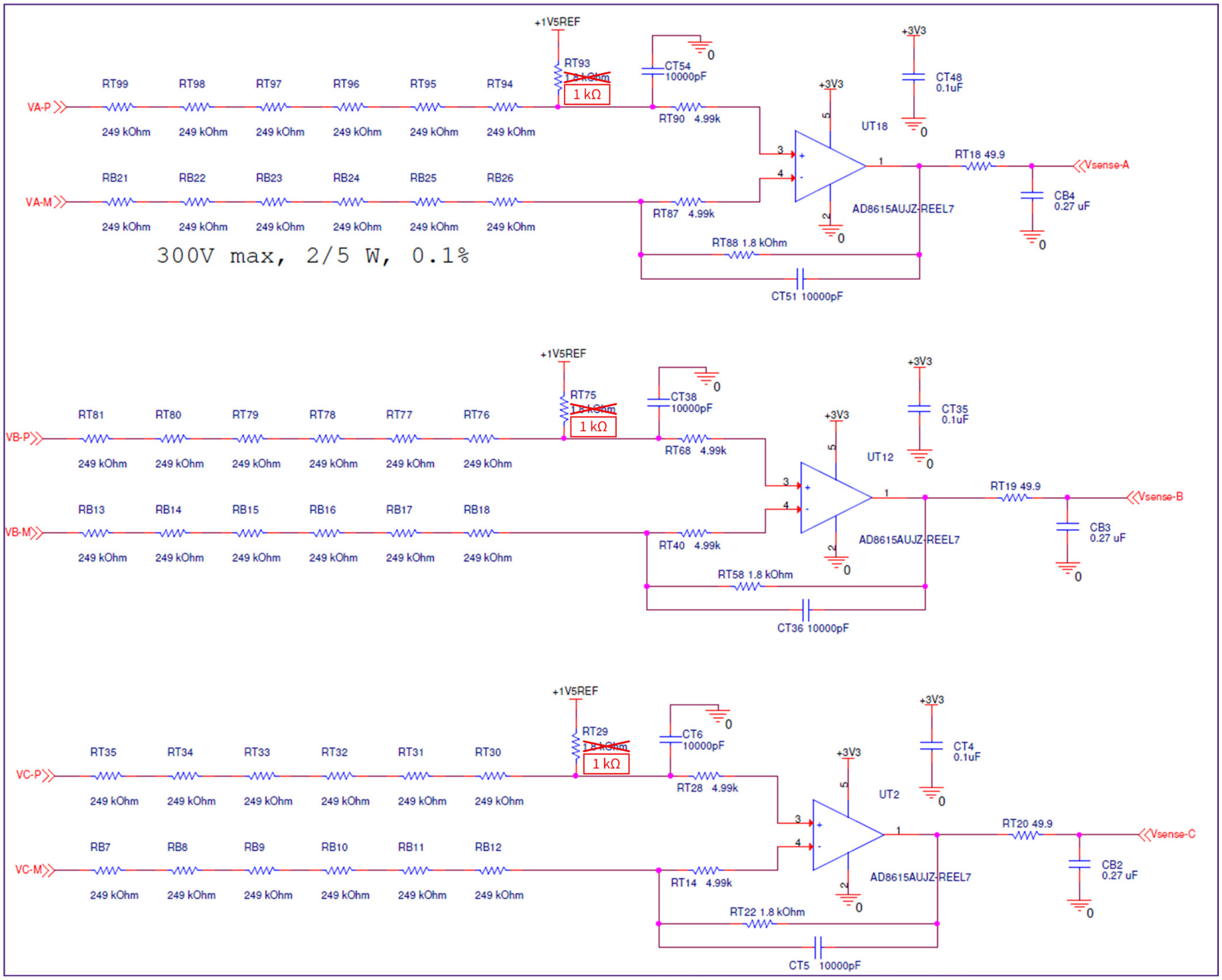

Figure 32: AC voltage conditioning circuit on the control board

The DC bus voltage is measured using *J8* on the controller PCB. This connector is mounted to the underside of the control PCB and plugs directly into the *U1A* connector on the power stage of the PCB. This connector is not easily accessible to a user since it is a board-to-board connector, so a dedicated pinout was not presented in Section 2.4. Similar to the AC voltage measurements, the DC bus voltage signal is scaled to a 0-3 V ADC voltage using the circuit shown in Figure 33. Compared to the default control board on the CRD300DA12E-XM3 reference design, the voltage conditioning circuit is modified slightly to be optimized for the expected voltages of this reference design. The resistor *RT4* was changed from 3.74 kΩ to 1.5 kΩ, as shown in Figure 33, to expand the dynamic measuring range of the circuit in order to support measuring voltages up to the full bus voltage.

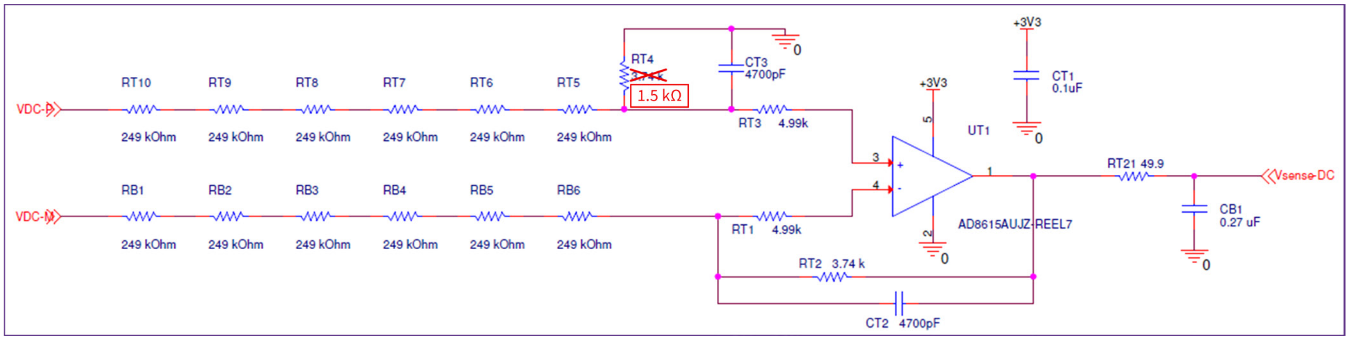

Figure 33: DC voltage conditioning circuit on the control board

3.6 Temperature Sensing

As discussed in Section 2.4.7, this design includes connectors which directly attach to the integrated thermistor in each of the three half-bridge power modules included in this reference design. By default, these connectors are attached to the CGD1700HB2M-UNA thermistor measurement connector (see Figure 16). The CGD1700HB2M-UNA converts the thermistor resistance to a variable duty cycle ranging from 10% to 88% and operating with a 400 kHz carrier frequency. With the default firmware, the controller measures the duty cycle using the Enhanced Capture module of the C2000 controller, and the measured duty cycle is converted to its equivalent temperature using

$$T_{MOD} = 949{,}897d^5 - 3{,}424{,}700.89d^4 + 4{,}910{,}895.93d^3 - 3{,}500{,}349.15d^2 + 1{,}240{,}060.64d - 174{,}939.94$$

where

T_{MOD}: power module thermistor temperature [K]

d: measured duty cycle [unitless, 0-1].

Note that the power module thermistors are representative of the power module case temperature, not the die junction temperature (see PRD-08376 for more details). The design also includes an integrated thermistor on the PCB for measuring the ambient board temperature. The conditioning circuit for this measurement is shown in Figure 34. The ambient temperature is measured with a simple ADC and converted to its equivalent temperature using

$$T_{PCB} = \frac{1}{0.000256 \cdot \ln\left(\frac{4504.1}{ADC} - 1\right) + 0.003354}$$

where

T_{PCB}: power module thermistor temperature [K]

ADC: measured ADC register value [unitless, 0-4095].

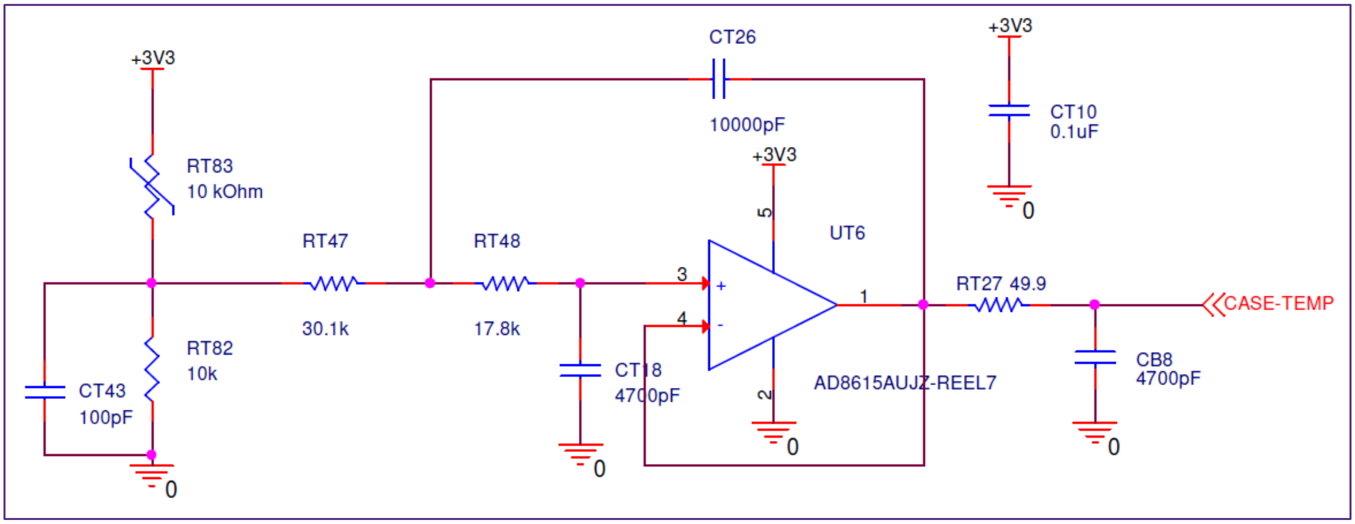

Figure 34: Ambient temperature conditioning circuit

3.7 Position Sensing

Through the auxiliary connector on the control board, *J10* (see Section 2.4.6), the controller can measure up to two external encoders for determining rotational position. These pins attach directly to the LaunchPad controller and utilize the built in quadrature inputs on the controller. The default firmware on the controller (see Section 4.1) does not include functionality to read the encoder by default, though this can be added later by an end user.

3.8 Metrology

This design includes a variety of test points and probe connection points to measure various signals on the board in order to evaluate the design and test various control schemes. To measure the gate signals, each of the three CGD1700HB2M-UNA gate drivers includes a dedicated MMCX connector for the high- and low-side output channels to measure the high- and low-side gate-to-source voltages (V_{GS}), respectively. These measurements can be used to evaluate the power module or control scheme performance. These are standard MMCX connectors intended to be monitored directly with an oscilloscope probe. Notably, during system operation, the gate measurements can float at the full bus voltage. Therefore, the gate measurements should not be monitored using single-ended oscilloscope probes due to the safety risks of high-voltage potentials being applied to the oscilloscope reference. It is recommended to perform these gate measurements with high-isolation probes such as the Tektronix® IsoVu™ series of probes.

The design also includes several through-hole test points to measure the power stage voltages. These test points are in the physical locations indicated in Figure 35 and are connected to the signals shown in Figure 36 and Table 9. The test points can be used to perform measurements of the output phase voltages and/or the DC-bus voltage. Ensure that a probe and/or meter with suitable voltage dynamic range is used when performing measurements on these test points since these test points can be higher than the bus voltage for short durations.

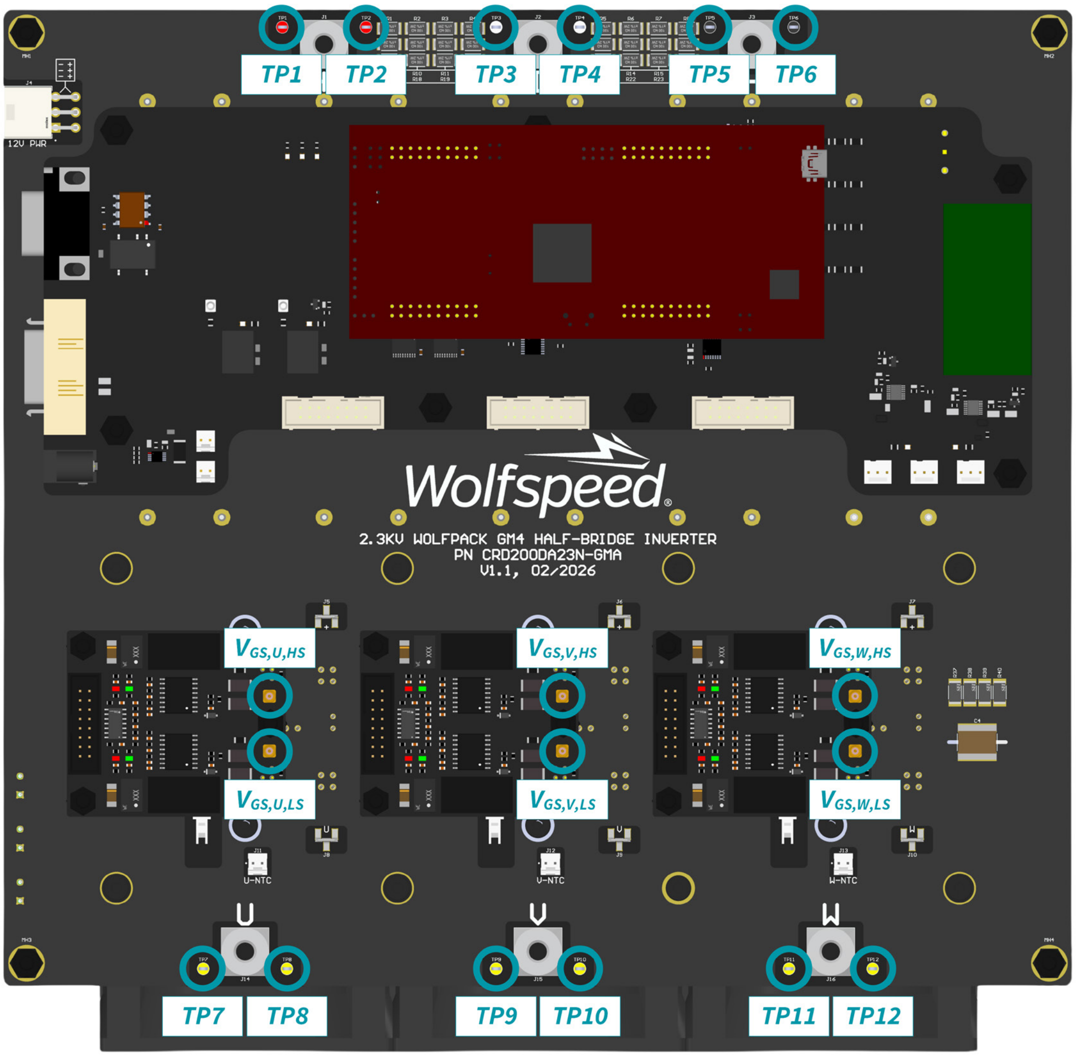

Figure 35: Power stage test point locations and gate driver MMCX connectors

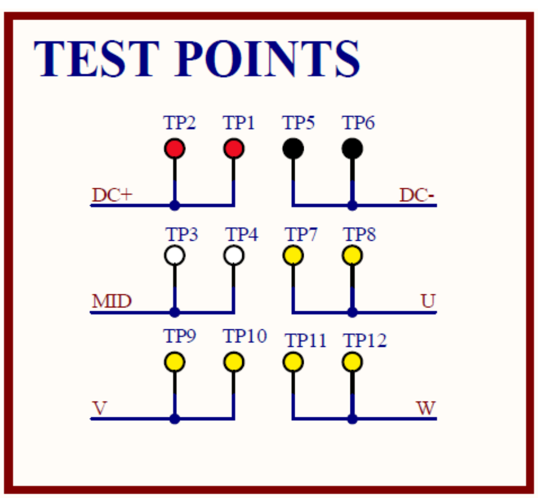

Figure 36: Power stage test points

Table 9: Power stage test point descriptions

Designator	Signal	Color	Description
TP1	DC+	Red	Positive DC-bus voltage
TP2			
TP3	MID	White	Series-stacked DC-bus capacitors mid-point
TP4			
TP5	DC-	Black	Negative DC-bus voltage
TP6			
TP7	U	Yellow	Output phase U voltage
TP8			
TP9	V	Yellow	Output phase V voltage
TP10			
TP11	W	Yellow	Output phase W voltage
TP12			

4. Controller and Firmware

The controller stage of the CRD200DA23N-GMA inverter system was designed around the F28379D LaunchPad™ (LAUNCHXL-F28379D) from the Texas Instruments (TI) C2000™ family of real-time microcontrollers. The LaunchPad, shown in Figure 37, plugs directly into the controller PCB as shown in Figure 7. The on-board isolated XDS100v2 USB-to-JTAG debug probe is a convenient interface to run and debug firmware without additional hardware by connecting a USB-Mini-B cable between *CON1* and a host computer. More information about running firmware is provided in the next section. While the CRD200DA23N-GMA inverter was exclusively tested with the F28379D LauchPad, theoretically, any microcontroller daughter card with an equivalent pinout could be used.

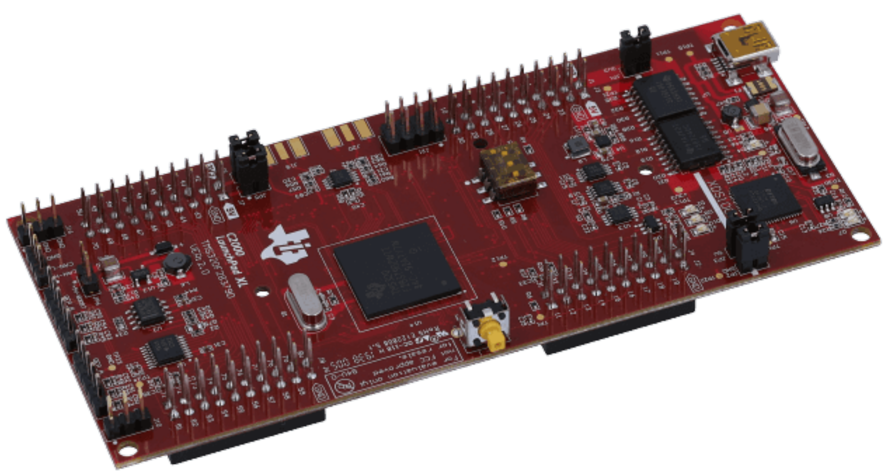

Figure 37: Texas Instruments F28379D LaunchPad

4.1 Firmware

The CRD200DA23N-GMA firmware is provided as a Code Composer Studio™ (CCS) project. The project was developed and tested with CCS version 12.8.1, so this version or newer is recommended to build and run this project. If not installed, download and install CCS from the TI website. The CCS User's Guide provides more details about CCS installation and use.

The software project was also developed and built with TI's C2000Ware to provide device-specific drivers and libraries. C2000Ware version 5.03.00.00 was used for development and testing, so this version or newer is recommended. C2000Ware is a separate installation from CCS, so if not installed, download and install C2000Ware from the TI website. Once the required software is installed, the following instructions can be used to import and run the provided CRD200DA23N-GMA firmware CCS project. To import the project into CCS, click **Project → Import CCS Projects** and browse to the local directory where the downloaded project was saved *<Local Directory>\CRD200DA23N-GMA* and click **Select Folder**. Verify the CRD25DA12N-FMC Firmware project was discovered and click **Finish**. Once properly imported, the project should look like Figure 38.

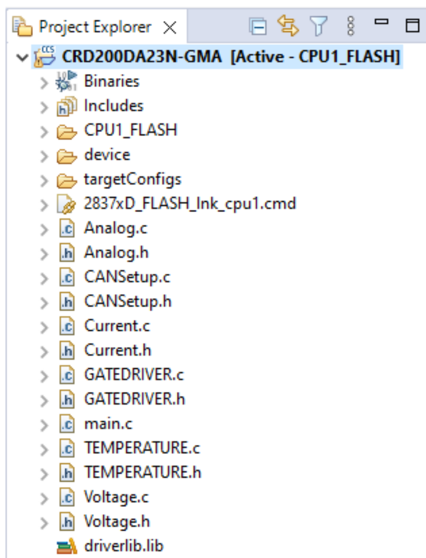

Figure 38: CRD200DA23N-GMA firmware CCS project explorer view

The default build configuration is *CPU1_FLASH* with the linker command file *2837xD_FLASH_link_cpu1.cmd* specified to run the program from Flash memory and the *TMS320F28379D.ccxml* target configuration file to use the on-board XDS100v2 USB Debug Probe on the F28379D LaunchPad. The parent folder contains all the hardware-specific source files to run the design including the drivers for current, voltage, and temperature sensing, along with the CAN communication protocol.

To build the project, click **Project → Build Project** or click on the **Build** icon button on the toolbar. Monitor the **Console** pane to confirm the project was successfully built without any errors. Address any errors listed in the **Problems** pane, if they occur. If there are no errors, go to **Run → Debug** or click on the **Debug** icon to launch a debug session. Once the debug session is launched, the program will be halted at the start of main(). Go to **Run → Resume** or click the **Resume** icon to start running the code. Add desired variables to the **Expressions** pane and click the **Continuous Refresh** icon to continuously monitor them during the debug session.

4.2 CAN Communication GUI

In addition to the open-loop three-phase sine pulse width modulation (SPWM) control law being executed by the code, a CAN communication protocol is also operating in the background to provide the ability to manipulate the parameters of the open-loop control from a host computer using the Wolfspeed provided GUI. Once downloaded and extracted, run the *GMA Inverter CAN Interface.exe* file where the *Communication Setup* dialog shown in Figure 39 will appear.

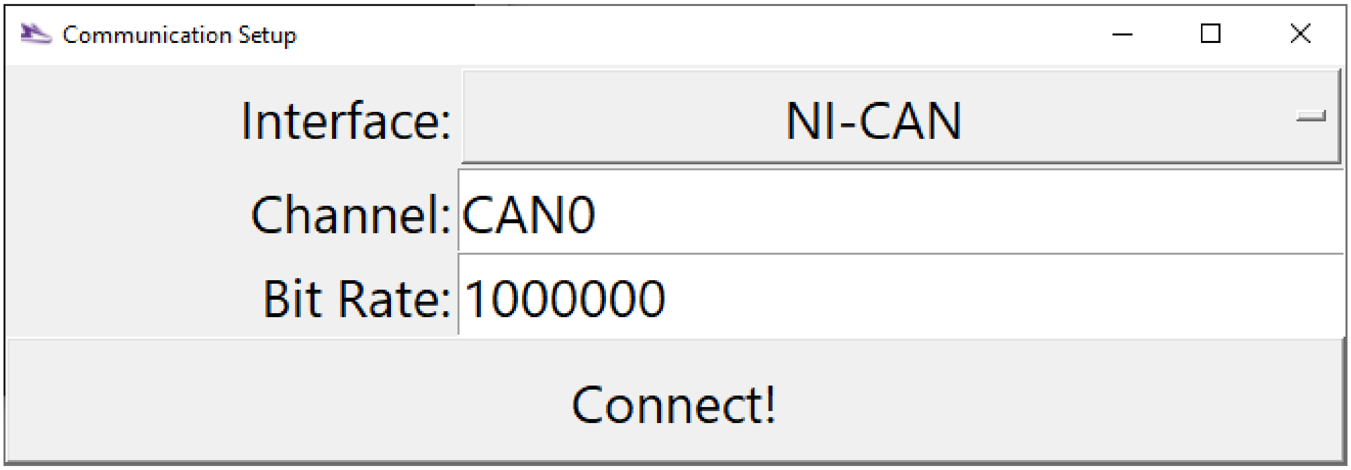

Figure 39: Communication setup dialog window

Click on the drop-down menu to select the proper **Interface** and input the correct settings for **Channel** and **Bit Rate** as determined by the CAN hardware adapter being used. The CAN GUI can interface with the controller using CANA or CANB (see Sections 2.4.5-2.4.6 for more details), though it is recommended to use **CANA**. The **CANA** channel includes integrated isolation and a DB9 connector which can directly connect to many CAN adapters. The GUI was built using the python-can library which provides support for various hardware adapters. A full list of CAN Interface Modules suppored by this library along with the configuration settings can be found at https://python-can.readthedocs.io/en/stable/. Wolfspeed validated system operation at power with two CAN adapters which are summarized in Table 10 along with the associated configuration settings. For best performance, Wolfspeed recommends using one of these adapters when evaluating the CRD200DA23N-GMA hardware. Once communication is established by clicking **Connect!**, the *GMA Inverter CAN Interface* GUI control window will appear as shown in Figure 40. A command window will also show a log of the raw CAN packets that are sent and received on the CAN bus. If there is an invalid packet, a warning will be printed, and the errors will be displayed in this window. By default, the CAN packets are transmitted and encoded/decoded in code approximately once every second.

Table 10: Recommended CAN adapters

Recommended CAN Adapters	Interface	Bit Rate
PEAK System PCAN-USB Pro FD	PCAN_USBBUS**x**[1]	1000000
National Instruments USB-8473	CAN**x**[1]	1000000

[1] : **x** is 0 or 1 depending on the configuration; recommended to try both numbers during initial setup

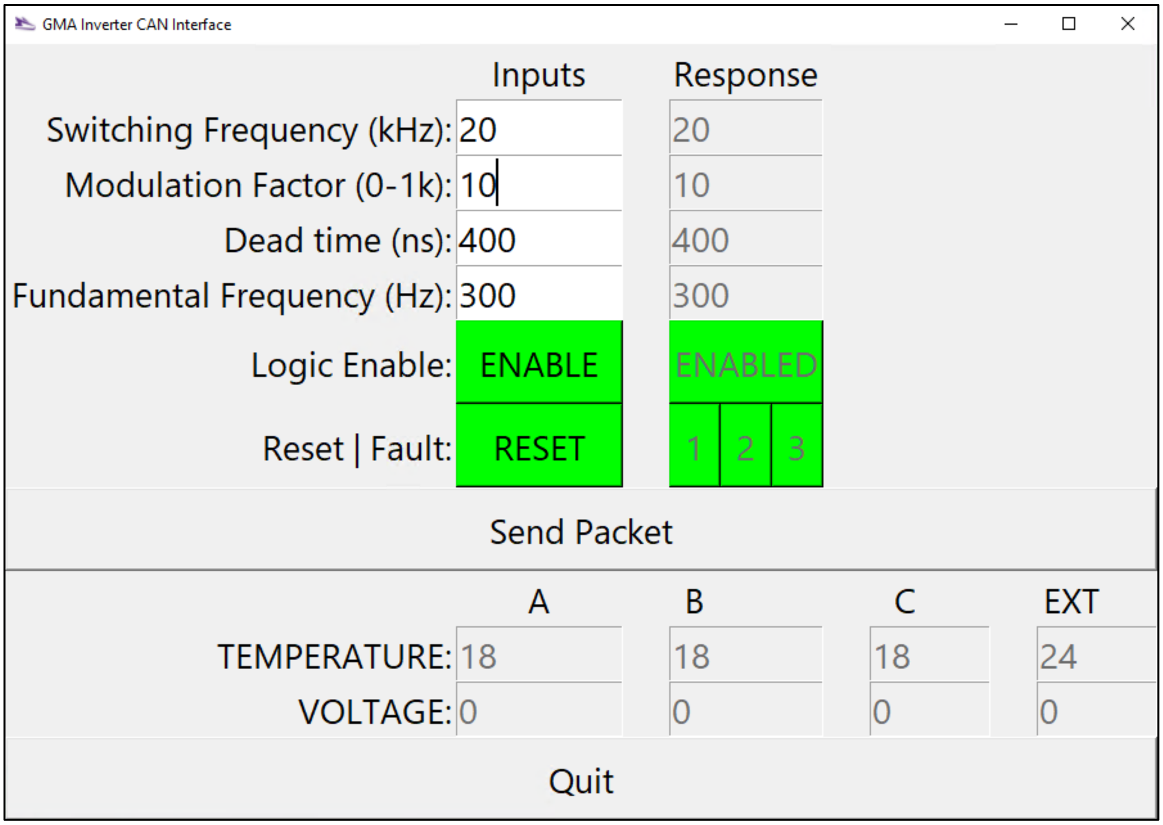

Figure 40: FMC inverter CAN interface GUI

The GUI control panel provides **Inputs** fields that consist of four numerical inputs and two toggle buttons. Pressing the **Send Packet** button sends a new CAN packet with the populated values of each input field. A description of each Inputs field is given below.

Switching Frequency field is the frequency of the output PWM in kHz. The default value is 20 = 20 kHz. The input range is 1 – 50.

Modulation Factor field is the modulation factor (depth) of the reference sinusoidal wave for the output PWM, scaled by a factor of 1000. The default value is 10 = 0.01 MF. The input range is 0 – 1000.

Dead time field is the dead time between the complementary high-side and low-side switch position PWM for each bridge-leg in nanoseconds (ns). The default value is 400 = 400 ns dead time. The input range is 100 – 2000.

Fundamental Frequency field is the fundamental frequency of the reference sinusoidal wave in Hz. The default value is 300 = 300 Hz. The input range is 1 – 500.

Logic Enable toggle-button enables and disables the PWM logic of all six switch positions. By default, the logic is disabled, so the toggle-button is highlighted red. When enabled, the toggle-button will turn green.

Reset toggle-button allows the user to reset one or more overcurrent faults. When a fault occurs, all the PWM signals are disabled by the controller and the corresponding phase(s) will appear as red in the

Fault response field. After the fault is identified, a user should first clear the issue causing the fault and update the inverter operating values (disable logic, set modulation factor low, etc.) to values suitable for re-starting the inverter. When the inverter is in a safe state to re-start, the user should toggle the Reset button so that it appears as red and send the CAN packet. Upon receiving the reset command, the controller will apply the proper signal sequence to reset the fault(s) on the gate drivers. The Reset button will automatically toggle back to green after the command is sent.

Response field displays the values contained in the most recent packet sent from the controller, indicating the status of each control parameter or confirming values were properly updated after a new input packet was sent.

Also included in the information sent by the controller in each packet are the feedback values for the measured power module thermistor temperatures (°C), phase feedback voltages (V), onboard thermistor temperature (°C), and bus voltage (V). The onboard thermistor temperature and bus voltage appear in the (EXT) column. Pressing the Quit button will close the GUI.

5. Performance

During development, Wolfspeed performed several measurements to characterize the thermal behavior of this reference design and to evaluate its performance at various operating conditions. This section details the measured characterization of the CRD200DA23N-GMA.

5.1 Heat Sink

The thermal performance of the module and system is influenced by its ability to reject heat from the device junction to its ambient environment. The baseplate-less design of the Wolfspeed CAB5R0A23GM4T already reduces the device thermal impedance compared to a similarly sized power modules since less material (i.e. baseplate) is present in the thermal path. To further maintain thermal integrity, this design uses the Fischer Elektronik® LA HB 9 100 12 heatsink, shown in Figure 41, with a 135 CFM integrated axial fan to cool the power modules. This heat sink is air-cooled. This design demonstrates one of the core advantages of adopting power modules with higher voltage ratings. Due to the elevated voltage, even an air-cooled design using only a two-level topology is able to achieve high power levels. Notably, the fans used in this design are loud; **operators should wear hearing protection when these fans are operating.** By default, the heat sink includes no mounting holes. Several holes were drilled and tapped into the heat sink to enable mounting the power modules to the heat sink and to mount the heat sink to the PCB. The placement of these holes is shown in the mechanical drawing in Figure 58.

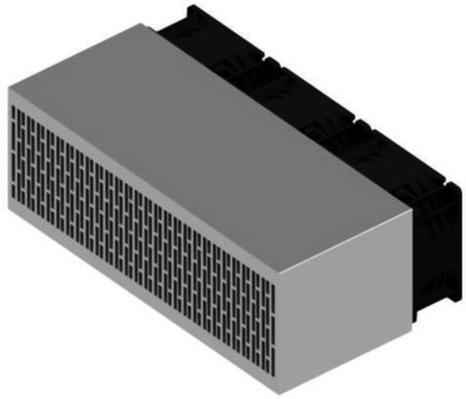

Figure 41: Fischer Elektronik LA HB 9 100 12 heatsink used in this design

When shipped, the heat sink is floating with respect to any voltage potentials, as shown in the schematic for the heat sink in Figure 42. The heat sink was floating for all the Wolfspeed characterization testing. For operators wanting to connect the heat sink to a potential such as ground, a screw with a wire/ring-terminal combination can be added to the heat sink. Version 1.0 of the hardware (indicated on the PCB silkscreen as “V1.0, 11/2024”) included four mounting holes in the corners of the heat sink to mount it to the PCB. In most cases, this provided sufficient clamping force to the thick PCB, though it could introduce inconsistencies if the PCB ever bowed or flexed. To improve the consistency in the manufactured assemblies, four additional holes were added to both the heat sink and PCB to improve the mounting interface in hardware Version 1.1 (indicated on the PCB silkscreen as “V1.1, 02/2026).

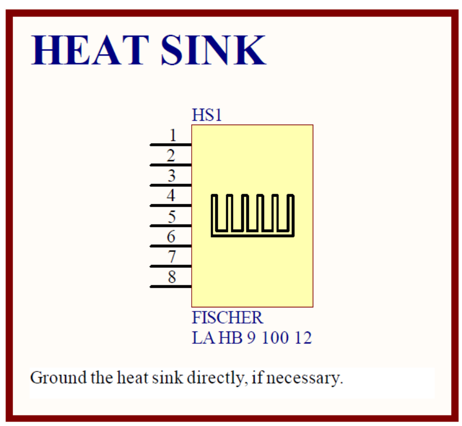

Figure 42: Schematic of the PCB heat sink connections

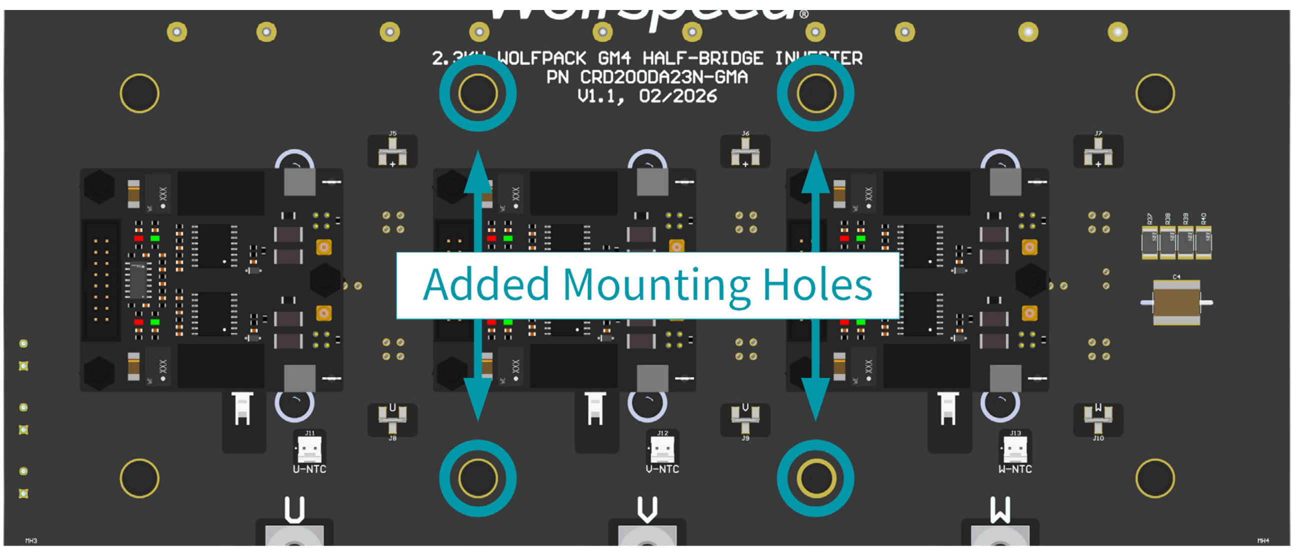

Figure 43: Heat sink & PCB holes added to hardware V1.1

The junction-to-heatsink thermal impedance, Z_{th}, for the power module is provided in the device datasheet. However, to evaluate the thermal performance of this reference design, the thermal impedance of the heatsink was also characterized. Characterizing the heatsink within the system was performed using a Siemens® Simcenter POWERT3ster™, which is an all-in-one thermal evaluation instrument to determine the thermal impedance of devices and applications. The single pulse transient thermal impedance measurements of the module, heatsink, and the combination of the two is shown in Figure 44. Note that these measurements are for a single switch position of the power module.

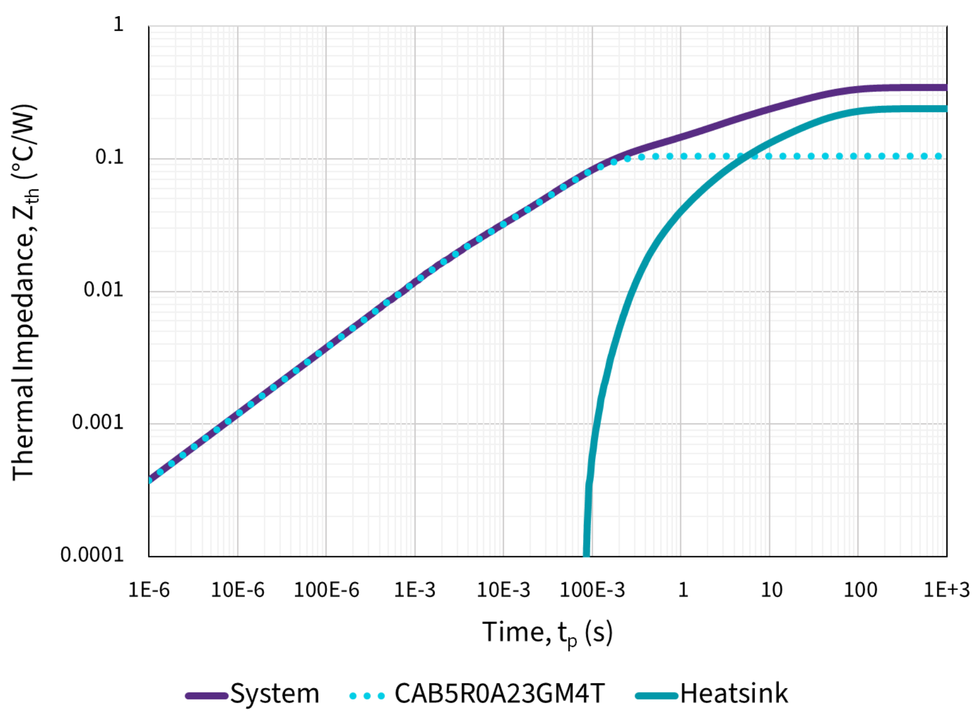

Figure 44: Transient thermal impedance measurements

The resulting junction-to-ambient thermal resistance, $R_{th,ja}$, for the entire system is 0.343 °C/W. From the device datasheet, the module junction-to-heatsink, $R_{th,jhs}$, is 0.105 °C/W. Note that this value already includes the pre-applied TIM layer. Therefore, the contribution of the heatsink to the overall, $R_{th,ja}$, is approximately 0.238 °C/W. The extracted 4th order Cauer network of the heatsink performance is shown in Figure 45. This thermal network can be used in tandem with the PLECS® model of the Wolfspeed CAB5R0A23GM4T to simulate this reference design. This is discussed in more detail in Section 5.3.

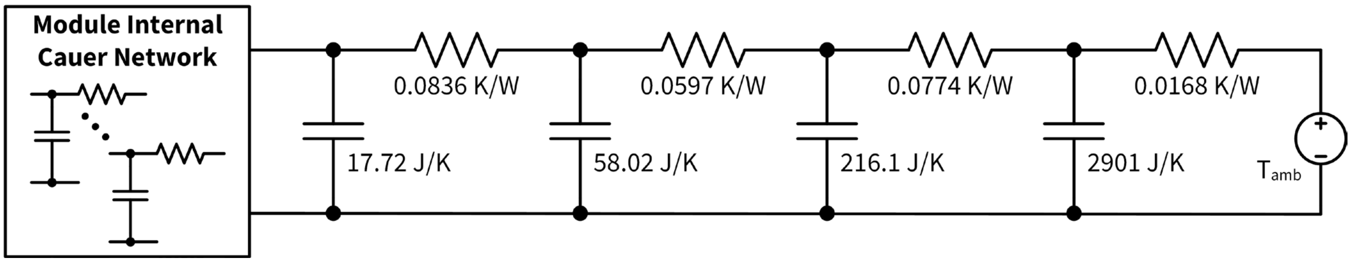

Figure 45: Heat sink 4th order equivalent Cauer network

As discussed in Section 2.4.4, the fans are powered from a dedicated +12 V power supply that plugs into *J4* on this design. The power supply is included with the shipment of this reference design. Each fan plugs into the PCB through the dedicated connectors on the bottom-side of the PCB, *J17-J19*. To achieve the expected performance of this reference design, the power supply must be connected and powered on, and each of the fans must be plugged into accordingly. Before testing the performance of this inverter, check that all these connections are in place and that all three fans are blowing air as expected. Additionally, ensure there is sufficient space around the heat sink and fans for air to blow across the heat sink for proper cooling.

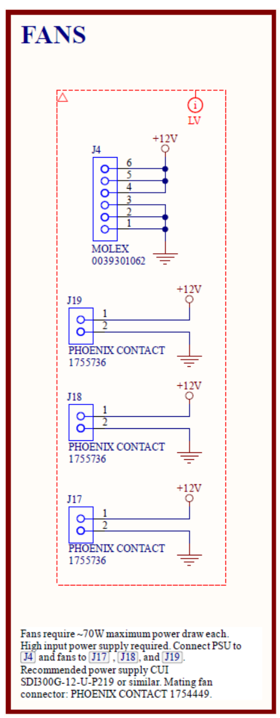

Figure 46: Heat sink fan power connections

5.2 Experimental Validation

5.2.1 Setup

The system was configured with a 129 µH, 600 A three-phase inductor developed by CTM Magnetics®. The load inductor was attached in a wye-connected configuration. The neutral of the wye-connected load was attached to the mid-point of the series-stack capacitors on the power stage of the PCB, as shown in the high-level schematic shown in Figure 47. The design was powered with a Magna Power® TSD1000-30/208+LXI power supply unit (PSU) with a rated output of up to 1000 V and 30 kW. The experimental setup is shown in Figure 48. The output currents, phase voltages, and gate voltages were measured using a Tektronix MSO58B oscilloscope with a rated bandwidth of 1 GHz. These measurements were performed with isolated high-bandwidth probes which are summarized in Table 11. The efficiency measurements were performed with a Hioki® PW6001 power analyzer.

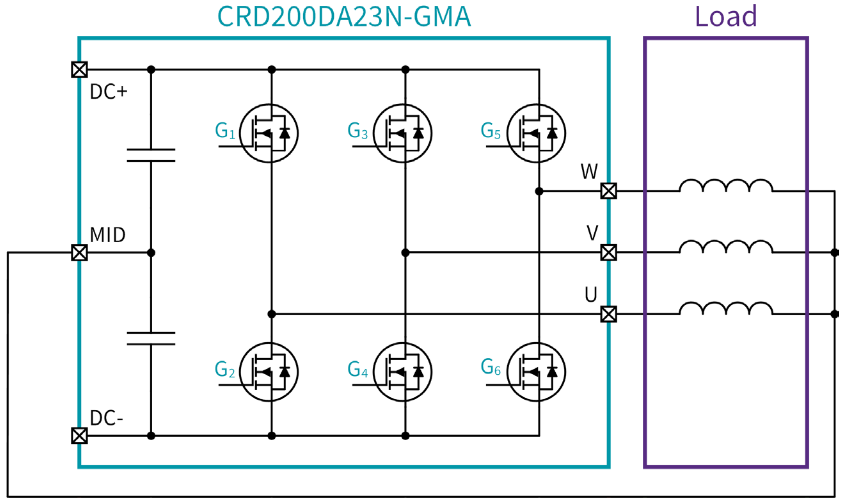

Figure 47: Wye-connected load attached to capacitor mid-point

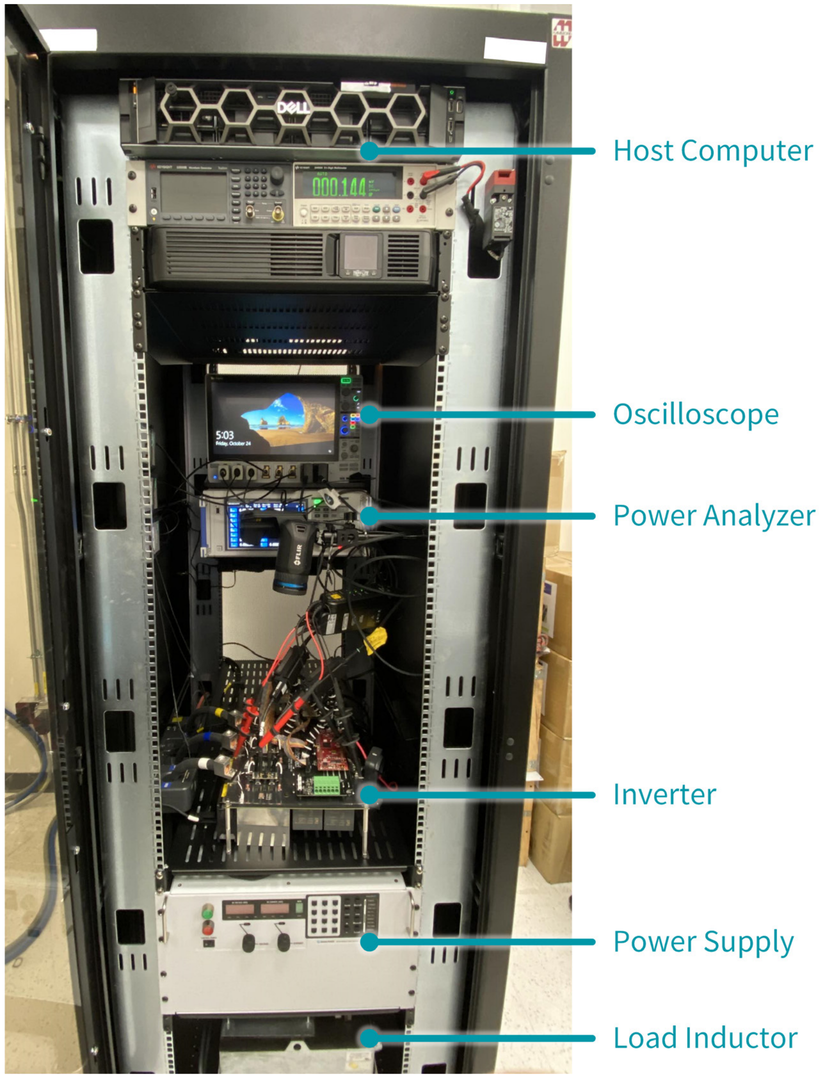

Figure 48: Experimental setup

Table 11: Experimental setup oscilloscope probes

Measurement	Probe	Description
I_U, I_V, I_W	PEM® CWT UM/3/B/1/160	600 A, 30 MHz, Rogowski Coil
V_U, V_V, V_W	Tektronix THDP0200	1.5 kV, 200 MHz, Differential Probe
$V_{GS,W,LS}$, $V_{GS,W,HS}$	Tektronix IsoVu™ TIVH05	50X Tip, 1 GHz, Optically Isolated Probe

5.2.2 Results

The system was evaluated at several operating conditions to validate the system performance. Parameters such as the switching frequency (f_{sw}), deadtime (t_{dead}), and modulation index (mf) were evaluated at a range of values. An example waveform is shown below in Figure 49, demonstrating the system operation over the duration of several fundamental periods at the full load current of 167 A_{rms}. Here the inverter is operating at a bus voltage of 1000 V, a switching frequency of 20 kHz, with 400 ns of deadtime, as summarized in Table 12.

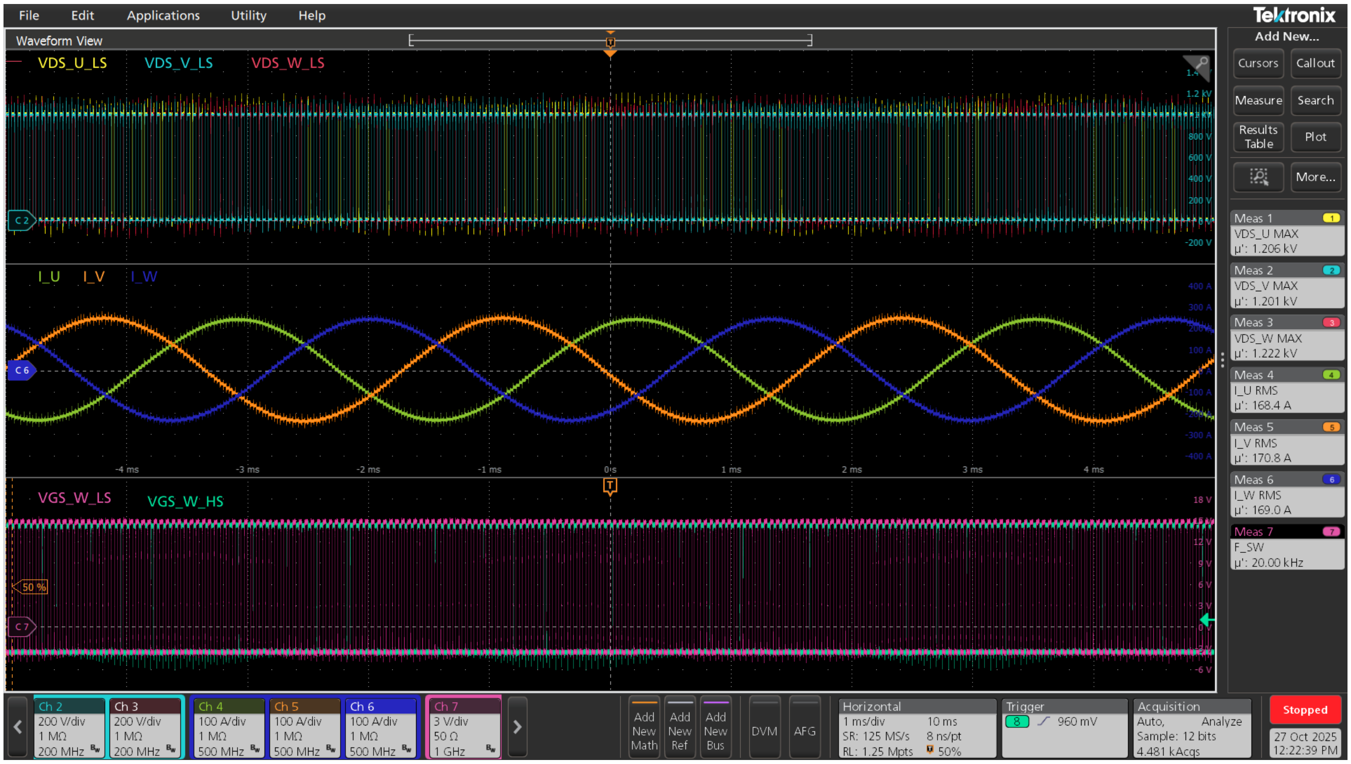

Figure 49: Oscilloscope measurements at 1 kV and 167 A

Table 12: Experimental operating conditions

Parameter	Symbol	Value
Bus Voltage	V_{BUS}	1000 V
Switching Frequency	f_{SW}	20 kHz
Deadtime	t_{dead}	400 ns
Fundamental Frequency	f_{fund}	300 Hz
Gate Resistance	$R_{G(EXT)}$	0 Ω

Additional measurements were performed for shorter time durations to validate other system performance parameters, such as voltage overshoot. An efficiency sweep at the operating conditions shown in Table 12 across a range of output powers is presented in Figure 50. To validate the long-term performance of the evaluation board, the inverter was operated for over 30 minutes under the same test conditions: I_{load} = 167 Arms, V_{bus} = 1000 V, f_{sw} = 20 kHz, t_{dead} = 400 ns, and $T_{ambient}$ = 25 °C. The thermal image in Figure 51 was taken at the end of the allotted time, demonstrating adequate thermal performance of the power modules. The temperature scale is in degree Celsius, and at that time, the thermistor temperature was reading 43 °C. Before shipment, each inverter kit is burned in at 1500 V and 30 A to confirm system operation.

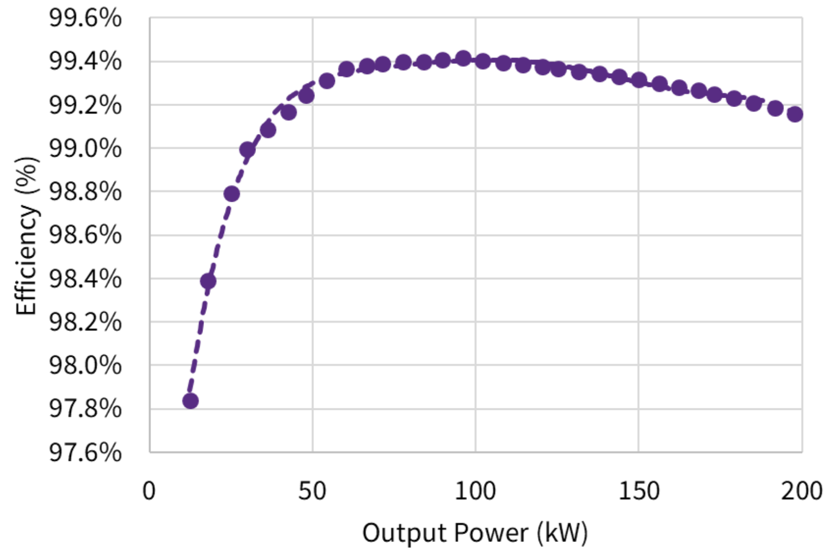

Figure 50: Efficiency vs output power experimental results

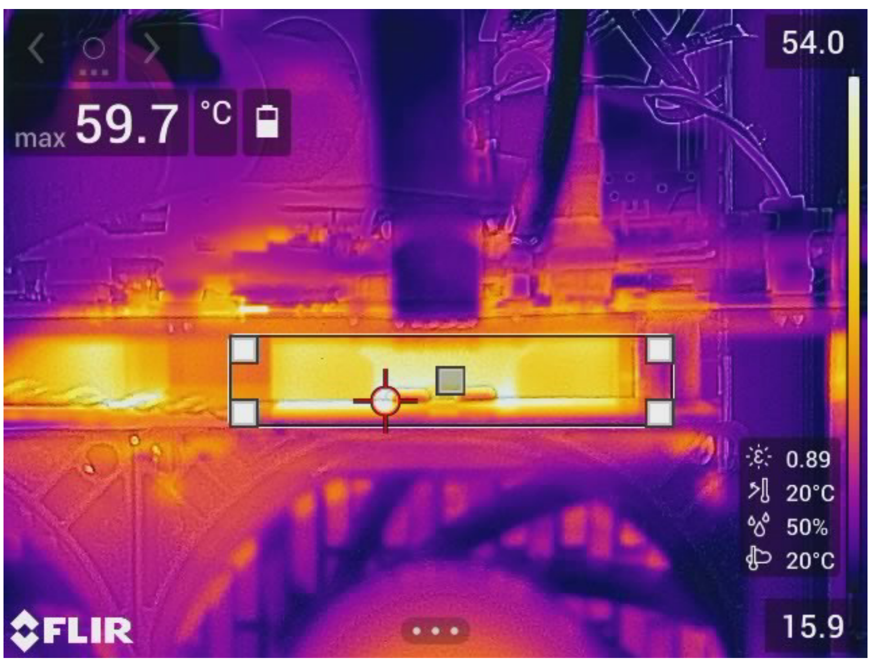

Figure 51: Phase W module temperature at 1 kV and 167 A

5.3 Simulation

A Plexim® PLECS® simulation of the hardware is included as a download with the design files. The top-level of the simulation is shown in Figure 52, and the various subsystems are explained in the following sections. The simulation values are populated using the initialization script found by navigating to **Simulation → Simulation parameters… → Initialization**. The simulation can be employed by interested users as a replacement for purchasing the hardware, as a tool to evaluate whether to purchase the hardware, and/or as a tool for making custom modifications to the controller. This simulation requires an active license of PLECS in order to run the simulation (PLECS Standalone 4.8.3 or newer is recommended). Licenses for PLECS can be purchased at https://www.plexim.com/products/plecs. More information about how to use PLECS can be found in the help guides on the PLECS website and in the program documentation. For users not familiar with PLECS, tutorials covering basic usage of the software are available at https://www.plexim.com/support/tutorials.

As with the actual hardware, the power stage of the inverter uses the Wolfspeed CAB5R0A23GM4T half-bridge baseplate-less module. The power module model is included in the simulation zip folder, so the simulation can be run by simply unzipping the download folder and navigating to **Simulation → Start**.

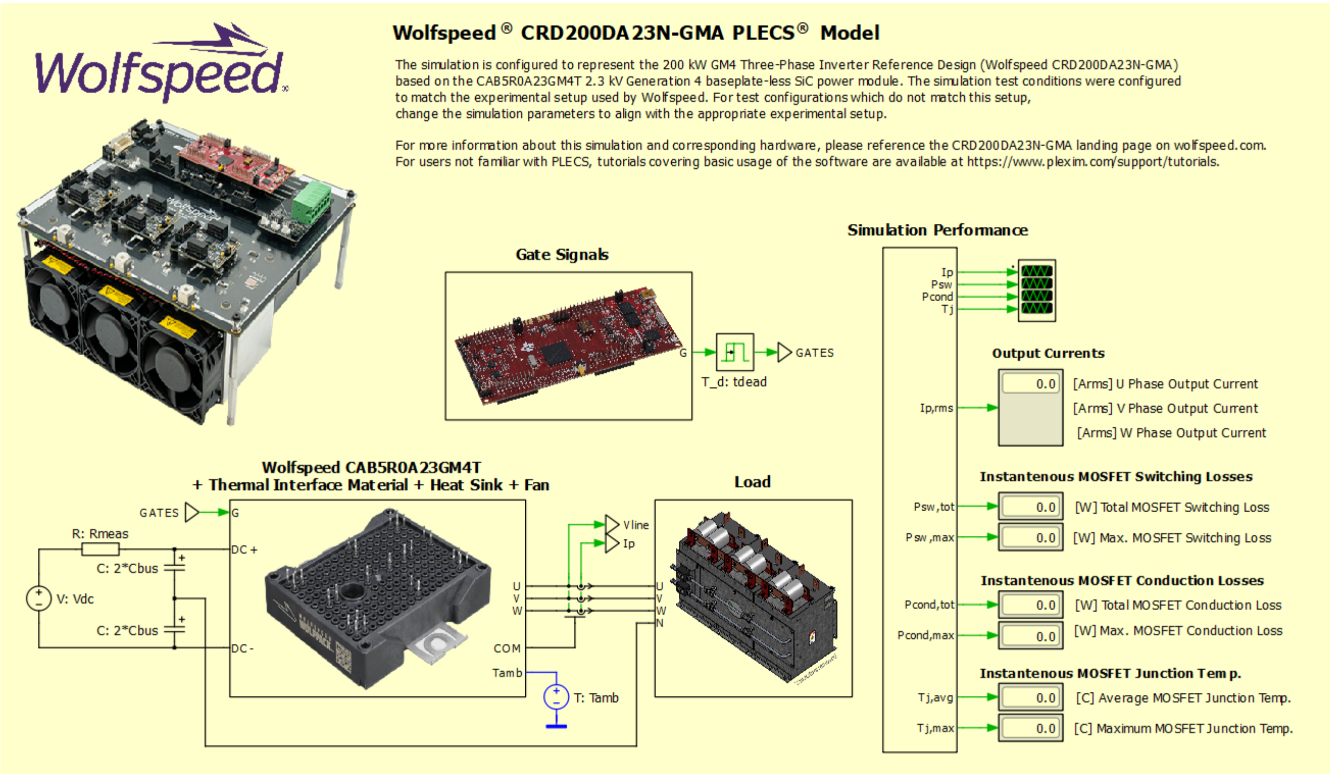

Figure 52: CRD200DA23N-GMA simulation

5.3.1 Power Stage

The power stage subsystem includes the power module MOSFET models and the corresponding thermal networks to the ambient temperature. As described in Section 5.1 of this document, the thermal impedance of the heatsink in this system was directly measured and a 4th order Cauer network was fit to the data. When paired with the PLECS model of the Wolfspeed CAB5R0A23GM4T, this produces an accurate thermal model of the entire system. This pairing is shown in the simulation power stage subsystem shown in Figure 53.

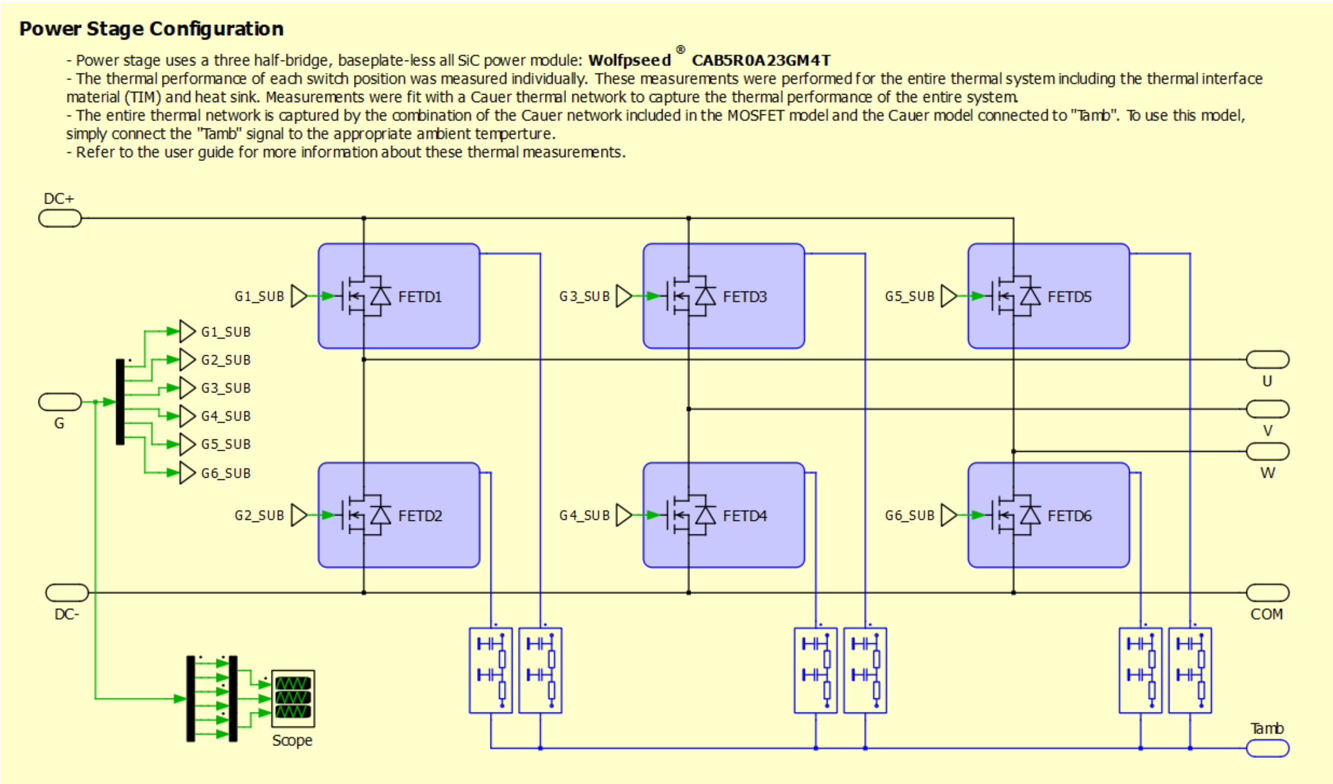

Figure 53: Simulation power stage

5.3.2 Controller

The simulation parameters are configured to match the experimental testbed used to validate the hardware discussed in Section 5.2. To match that configuration, the simulation uses SPWM modulation for generating the gate signals and is operated in an open-loop configuration. The SPWM modulation controller used to generate gate signals is shown in Figure 54.

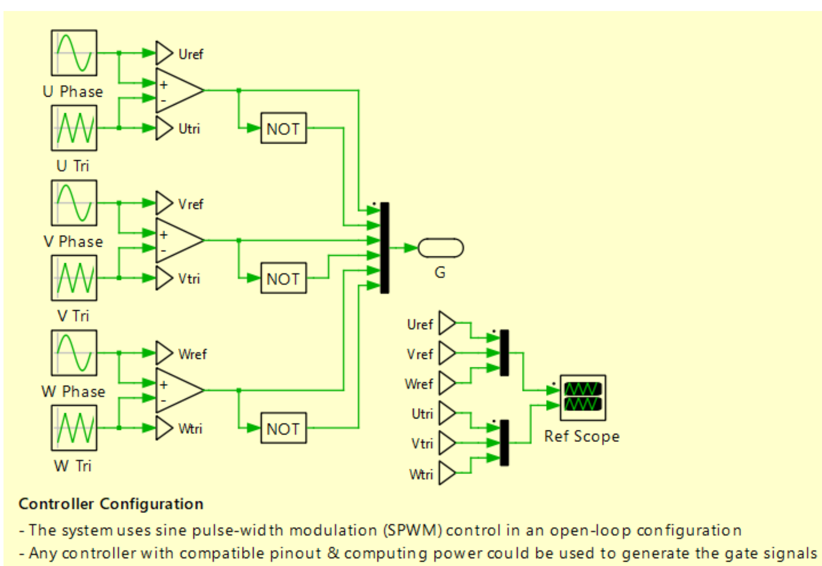

Figure 54: Simulation SPWM controller

5.3.3 Load

The load in the simulation uses the parameters of a 129 µH three-phase inductor configured in a wye-connected setup. This matches the experimental setup discussed in Section 5.2.1. The simulation is a series RL load using the nominal inductance (129 µH) and DC resistance (4 mΩ) values from the inductor datasheet. The load subsystem is shown in Figure 55.

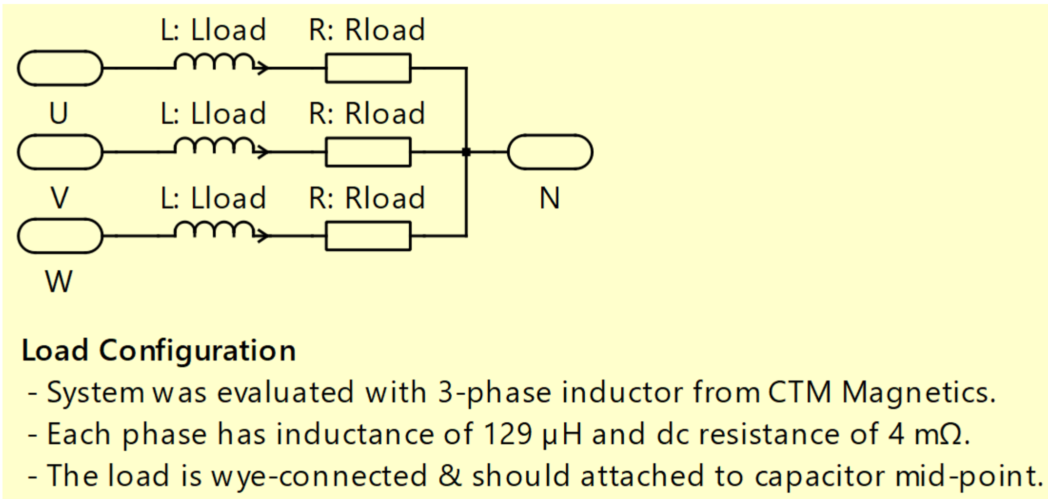

Figure 55: Simulation load

5.3.4 Performance Monitor

The simulation includes a subsystem to monitor the primary performance characteristics of the model (output currents, switching losses, conduction losses, and junction temperature). This subsystem is shown in Figure 56.

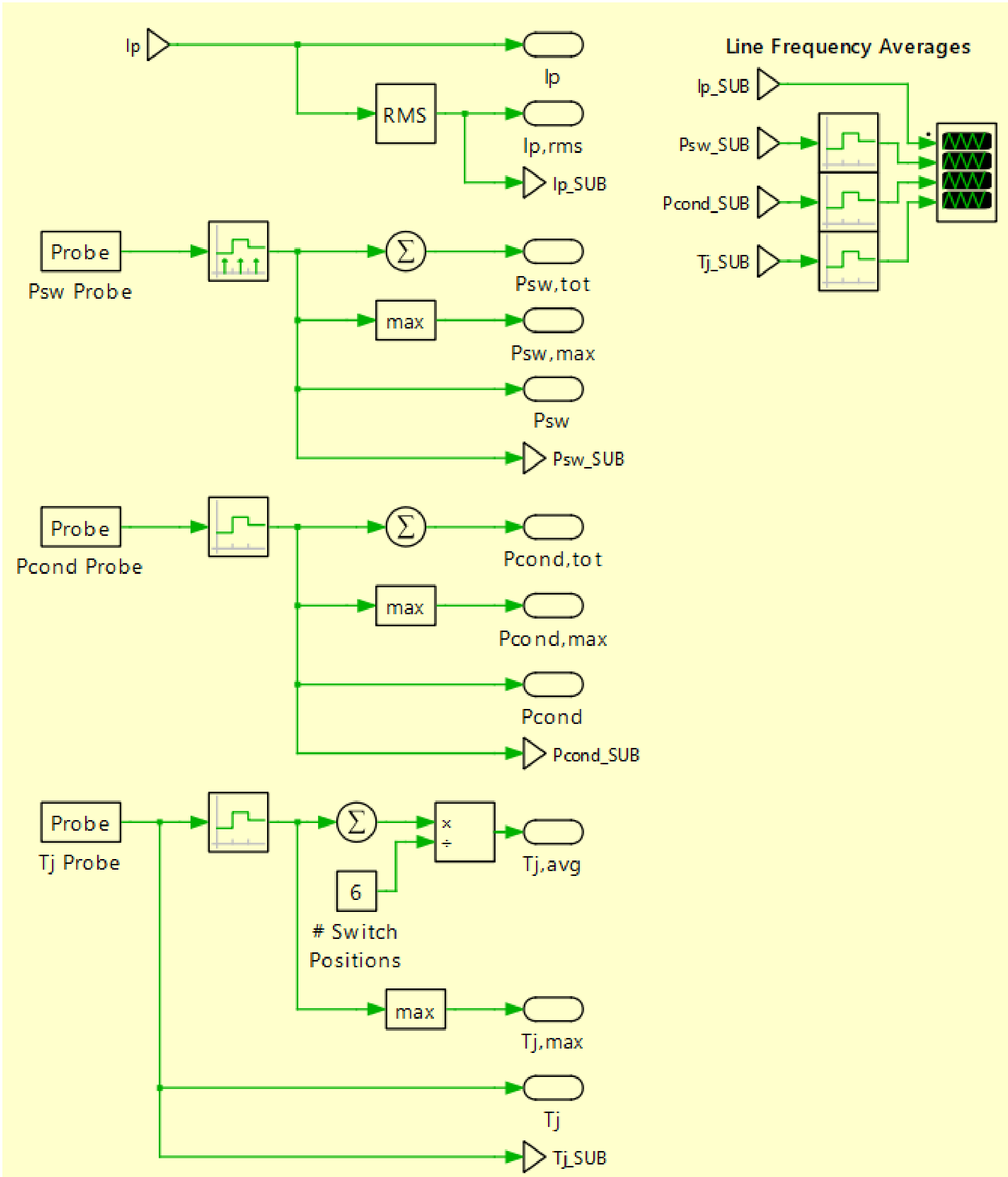

Figure 56: Simulation performance monitor

6. Dimensions

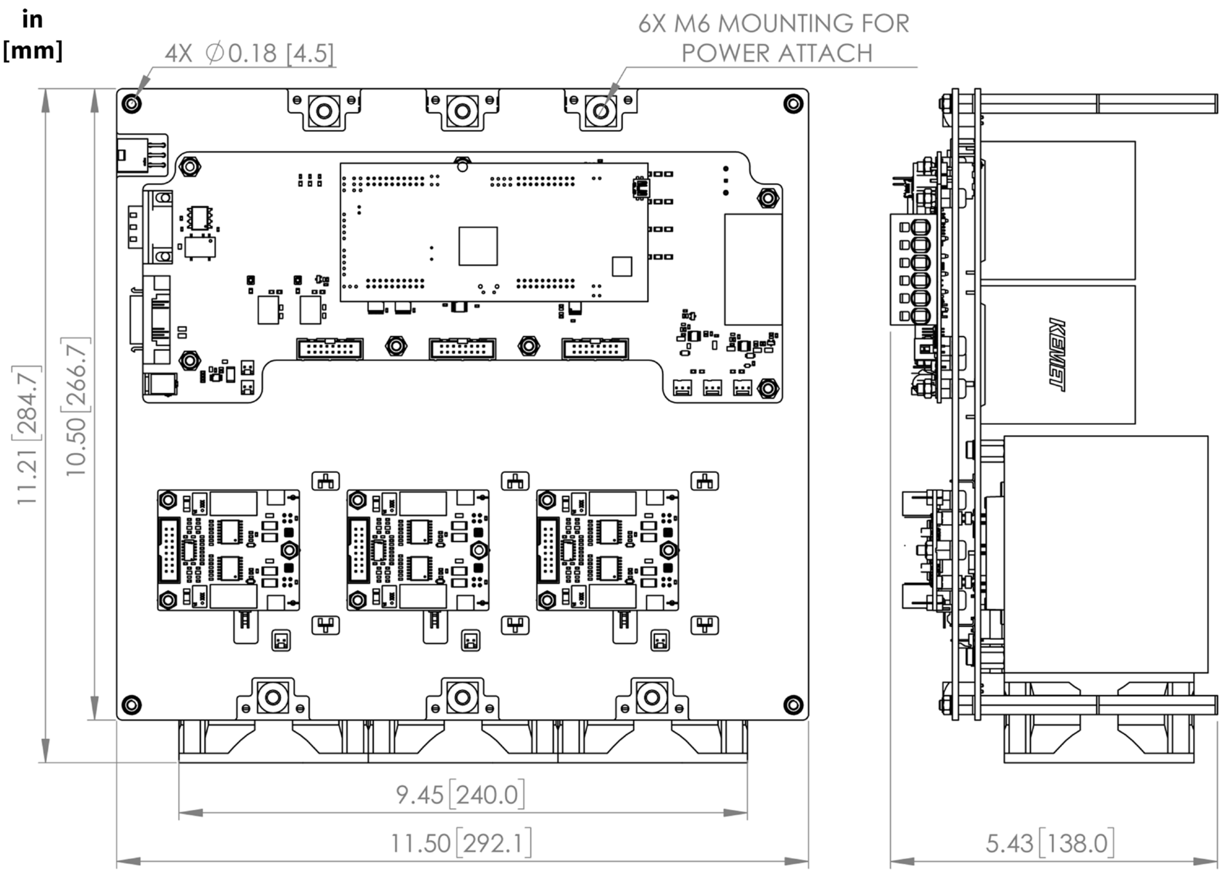

Figure 57: Dimensions of the CRD200DA23N-GMA inverter

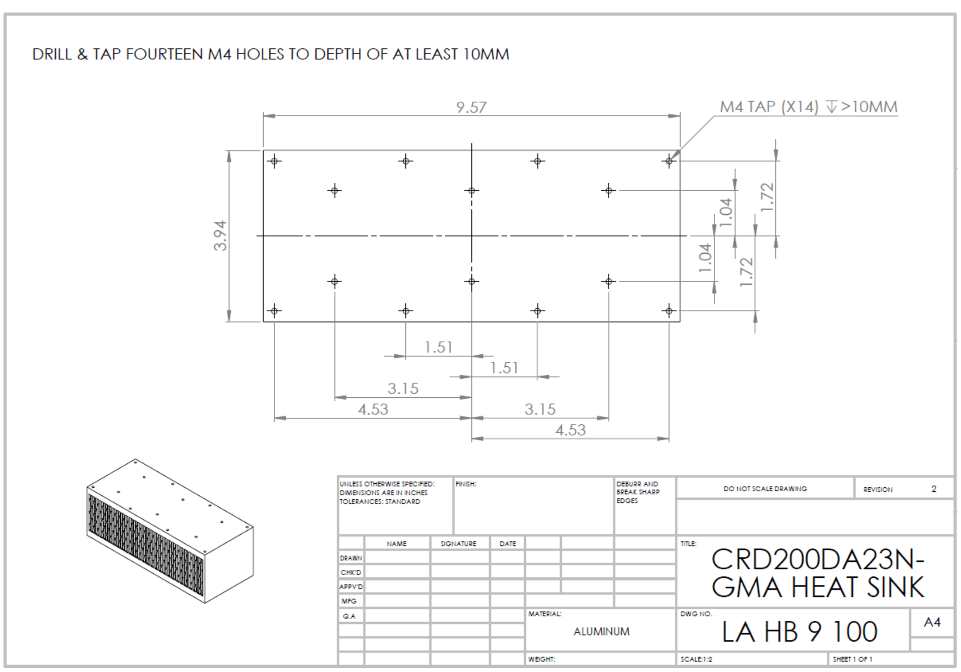

Figure 58: Custom drill and tap modifications to the heat sink

7. Supporting Links and Tools

The following links provide additional information about the 2.3 kV GM WolfPACK power module portfolio and design tools for using the devices. Please navigate to the landing page for this design for additional links and support.

- 2.3 kV GM Module Product Family
- KIT-CRD-CIL23N-GMA: Dynamic Characterization Evaluation Tool Optimized for the Wolfspeed 2300 V WolfPACK™ GM Half Bridge Module Platform
- SpeedVal™: Modular Evaluation Platform
- SpeedFit 2.0 Design Simulator™
- Technical Support Forumhttps://www.wolfspeed.com/cgd12hb00d/

Revision History

Date	Revision	Changes
November 2025	1	Initial Release
February 2026	2	Updated figures to V1.1 hardware. Added heat sink mechanical drawing. Updated simulation to MOSFET + diode models.

IMPORTANT NOTES

PURPOSES AND USE

Wolfspeed, Inc. (on behalf of itself and its affiliates, "Wolfspeed") reserves the right in its sole discretion to make corrections, enhancements, improvements, or other changes to the board or to discontinue the board.

THE BOARD DESCRIBED IS AN ENGINEERING TOOL INTENDED SOLELY FOR LABORATORY USE BY HIGHLY QUALIFIED AND EXPERIENCED ELECTRICAL ENGINEERS TO EVALUATE THE PERFORMANCE OF WOLFSPEED POWER SWITCHING DEVICES. THE BOARD SHOULD NOT BE USED AS ALL OR PART OF A FINISHED PRODUCT. THIS BOARD IS NOT SUITABLE FOR SALE TO OR USE BY CONSUMERS AND CAN BE HIGHLY DANGEROUS IF NOT USED PROPERLY. THIS BOARD IS NOT DESIGNED OR INTENDED TO BE INCORPORATED INTO ANY OTHER PRODUCT FOR RESALE. THE USER SHOULD CAREFULLY REVIEW THE DOCUMENT TO WHICH THESE NOTIFICATIONS ARE ATTACHED AND OTHER WRITTEN USER DOCUMENTATION THAT MAY BE PROVIDED BY WOLFSPEED (TOGETHER, THE "DOCUMENTATION") PRIOR TO USE. USE OF THIS BOARD IS AT THE USER'S SOLE RISK.

OPERATION OF BOARD

It is important to operate the board within Wolfspeed's recommendations and environmental considerations as described in the Documentation. Exceeding specified ratings (such as input and output voltage, current, power, or environmental ranges) may cause property damage. If you have questions about these ratings, please contact Wolfspeed prior to connecting interface electronics (including input power and intended loads). Any loads applied outside of a specified output range may result in adverse consequences, including unintended or inaccurate evaluations or possible permanent damage to the board or its interfaced electronics. Please consult the Documentation prior to connecting any load to the board. If you have any questions about load specifications for the board, please contact Wolfspeed at forum.wolfspeed.com for assistance (and please rely only on forum responses from responders identified as Wolfspeed employees).

Users should ensure that appropriate safety procedures are followed when working with the board as serious injury, including death by electrocution or serious injury by electrical shock or electrical burns can occur if you do not follow proper safety precautions. It is not necessary in proper operation for the user to touch the board while it is energized. When devices are being attached to the board for testing, the board must be disconnected from the electrical source and any bulk capacitors must be fully discharged. When the board is connected to an electrical source and for a short time thereafter until board components are fully discharged, some board components will be electrically charged and/or have temperatures greater than 50˚ Celsius. These components may include bulk capacitors, connectors, linear regulators, switching transistors, heatsinks, resistors and SiC diodes that can be identified using a board schematic. Users should contact Wolfspeed for assistance if a board schematic is not included in the Documentation or if users have questions about a board's components. When operating the board, users should be aware that these components will be hot and could electrocute or electrically shock the user. As with all electronic evaluation tools, only qualified personnel knowledgeable in handling electronic performance evaluation, measurement, and diagnostic tools should use the board.

USER RESPONSIBILITY FOR SAFE HANDLING AND COMPLIANCE WITH LAWS

Users should read the Documentation and, specifically, the various hazard descriptions and warnings contained in the Documentation, prior to handling the board. The Documentation contains important safety information about voltages and temperatures.

Users assume all responsibility and liability for the proper and safe handling of the board. Users are responsible for complying with all safety laws, rules, and regulations related to the use of the board. Users are responsible for (1) establishing protections and safeguards to ensure that a user's use of the board will not result in any property damage, injury, or death, even if the board should fail to perform as described, intended, or expected, and (2) ensuring the safety of any activities to be conducted by the user or the user's employees, affiliates, contractors, representatives, agents, or designees in the use of the board. User questions regarding the safe usage of the board should be directed to Wolfspeed at forum.wolfspeed.com (but please rely only on forum responses from responders identified as Wolfspeed employees).

In addition, users are responsible for:

● compliance with all international, national, state, and local laws, rules, and regulations that apply to the handling or use of the board by a user or the user's employees, affiliates, contractors, representatives, agents, or designees.

● taking necessary measures, at the user's expense, to correct radio interference if operation of the board causes interference with radio communications. The board may generate, use, and/or radiate radio frequency energy, but it has not been tested for compliance within the limits of computing devices pursuant to Federal Communications Commission or Industry Canada rules, which are designed to provide protection against radio frequency interference.

● compliance with applicable regulatory or safety compliance or certification standards that may normally be associated with other products, such as those established by EU Directive 2011/65/EU of the European Parliament and of the Council on 8 June 2011 about the Restriction of Use of Hazardous Substances (or the RoHS 2 Directive) and EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (or WEEE). The board is not a finished end product and therefore may not meet such standards. Users are also responsible for properly disposing of a board's components and materials.

NO WARRANTY

THE BOARD IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, INCLUDING BUT NOT LIMITED TO ANY WARRANTY OF NON-INFRINGEMENT, MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE, WHETHER EXPRESS OR IMPLIED. THERE IS NO REPRESENTATION THAT OPERATION OF THIS BOARD WILL BE UNINTERRUPTED OR ERROR FREE.

LIMITATION OF LIABILITY

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