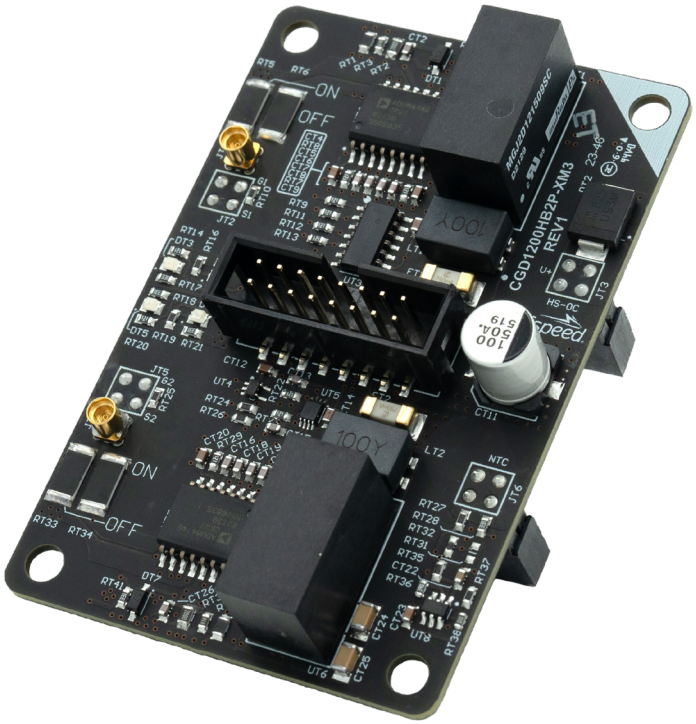
User Guide PRD-09491

CGD1200HB2P-XM3 Gate Driver User Guide



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1. Introduction

The CGD1200HB2P-XM3 gate driver, shown in Figure 1, is a dual channel isolated gate driver optimized for Wolfspeed's high-performance XM half-bridge power modules with the **inline gate pin configuration**. The gate driver is designed for high-frequency operation and can drive high-performance silicon carbide (SiC) power modules. It features separate 2 W isolated power supplies and Analog Devices® ADuM4146 gate drivers for independently operating the high- and low-side switch positions of a SiC power module. It is designed to attach directly to an XM power module and includes input voltage protection, differential inputs for increased noise immunity, soft shutdown, undervoltage lockout, and overcurrent protection. The CGD1200HB2P-XM3 design is intended to be an upgrade to the CGD12HBXMP gate driver by adding integrated gate measurement connections, improving the temperature feedback signaling, improving the overcurrent protection, and decreasing the soft-shutdown resistance for faster turn-off during faults. This user guide provides an overview of the gate driver functions and parameters including connector pinouts and operating guidance.

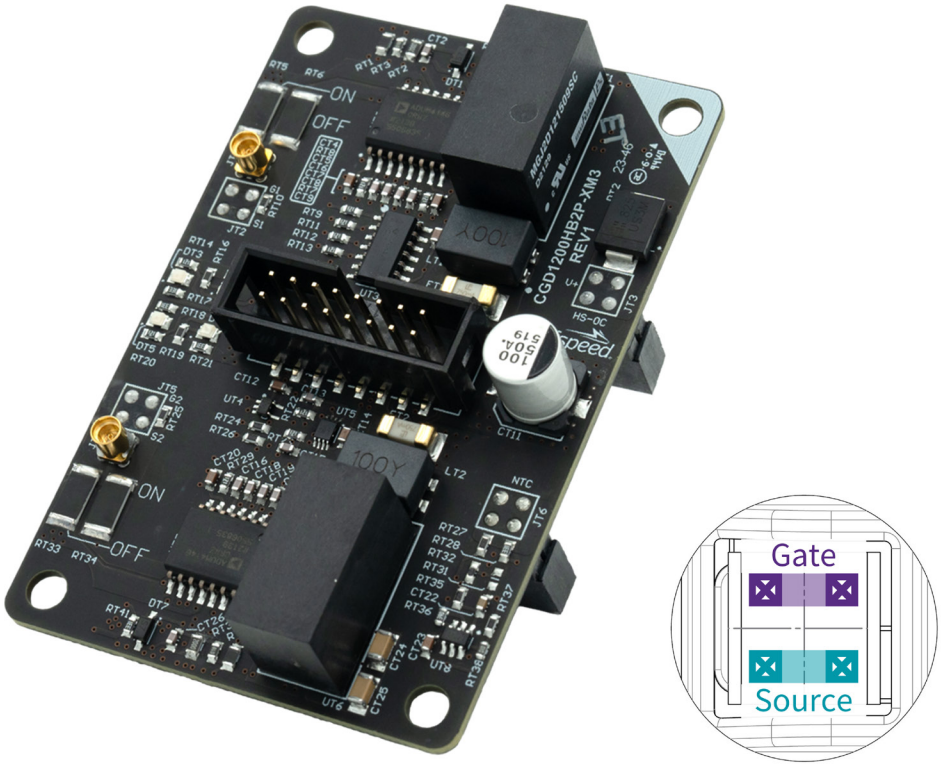

Figure 1: CGD1200HB2P-XM3 gate driver

2. Design Features

The CGD1200HB2P-XM3 gate driver is designed to operate at DC bus voltages up to 1500 V and includes system benefits such as onboard overcurrent, shoot-through protection, and reverse polarity protection. The maximum operating parameters of this gate driver design are shown in Table 1 and the full list of electrical parameters are shown in Table 2. Renderings of the board assembly from various views are shown in Figure 2.

2.1 Maximum Operating Parameters

Table 1: Maximum operating parameters (verified by design)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DC}	-0.5 to 13.2	V
Logic Level Input	V_I	-0.5 to 5.5	
Output Peak Current (T_A = 25 °C)	I_O	±10	A
Output Power Per Channel (T_A = 25 °C)	P_{DRIVE}	2	W
Maximum Switching Frequency (MOSFET Dependent, See Section 4.8)	f_{SW}	80	kHz
Ambient Operating Temperature	T_{OP}	-40 to 85	°C
Storage Temperature	T_{STG}	-40 to 85	

2.2 Assembly

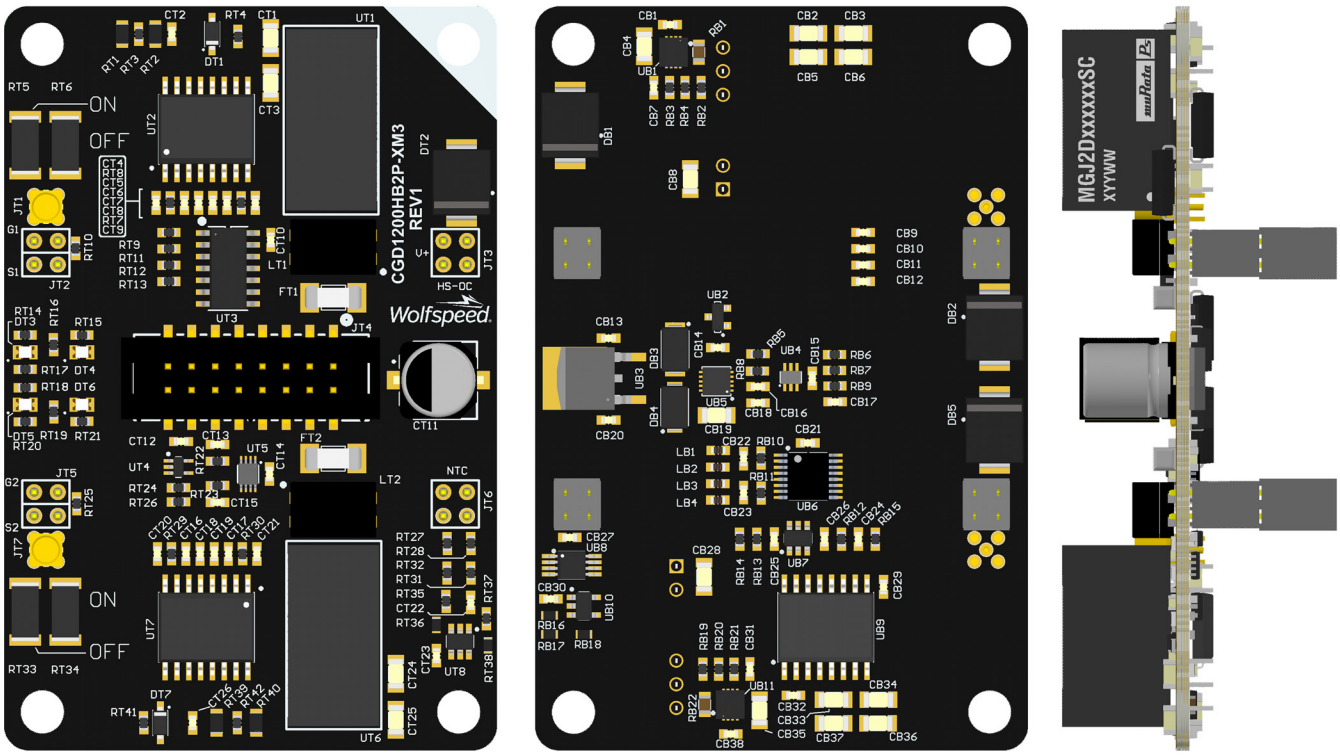

Figure 2: CGD1200HB2P-XM3 rendering views

2.3 Electrical Characteristics

Table 2: Electrical characteristics (T = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V_{DC}	10.8	12	13.2	V	
Secondary Under Voltage Lockout	V_{UVLO}		11.5	12		
Secondary UVLO Hysteresis	V_{HYS}		0.06			
Over Voltage Clamping	V_{OVLO}	18	20	22		
High Level Logic Input Voltage	V_{IH}	3.5		5.5		Single-Ended Inputs
Low Level Logic Input Voltage	V_{IL}	0		1.5		
Diff Input Common Mode Range	V_{IDCM}		± 2.5	± 7		Differential Inputs
Positive-going input threshold voltage, differential input	V_{IT+}			0.2		$V_{ID} = V_{POS-LINE} – V_{NEG-LINE}$
Negative-going input threshold voltage, differential input	V_{IT-}	-0.2				
Differential Output Magnitude	V_{OD}	2	3.7			R_L = 100 Ω
High level Output Voltage	$V_{GATE,HIGH}$		+15			
Low level Output Voltage	$V_{GATE,LOW}$		-4			
Working Isolation Voltage	V_{IOWM}		1500			V_{RMS}
Isolation Capacitance	C_{ISO}		4.9		pF	Per Channel
Common Mode Transient Immunity	CMTI	100			kV/µs	V_{CM} = 1500 V
Output Resistance[1]	$R_{G(IC)-ON}$		0.48	0.98	Ω	Gate Driver Buffer Tested at 1 A
	$R_{G(IC)-OFF}$		0.47	0.81		
External Resistance[2]	$R_{G(EXT)-ON}$		1			External SMD Resistor 2512 (6432 Metric)
	$R_{G(EXT)-OFF}$		1			
Output Rise Time	t_{ON}		223		ns	$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF From 10% to 90%
Output Fall Time	t_{OFF}		208			
Propagation Delay (Turn-Off)	t_{PHL}		120			$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 0 nF From 50% to 50%
Propagation Delay (Turn-On)	t_{PLH}		125			
Over-current Blanking Time	t_{BLANK}		600			$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF
Over-current Propagation Delay to FAULT Signal Low	$t_{PD-FAULT}$		1.3		µs	Does Not Include Blanking
Soft-Shutdown Time	t_{SS}		1.3			$R_{G(EXT)}$ = 1 Ω, C_{LOAD} = 47 nF
Soft-Shutdown Resistance[3]	R_{SS}		5		Ω	Tested at 25 mA
Miller Clamp Resistance	R_{MC}		1.1	2.75		Tested at 100 mA
Miller Clamp Voltage Threshold	V_{MC}	1.75	2	2.25	V	Reference to Source

[1] Output resistance of gate driver integrated circuit (IC).

[2] Additional output resistance is added with surface mount device (SMD) resistors. Separate resistors allowing independent tuning.

[3] Soft-shutdown network will safely turn off the gate if an over-current event is detected.

2.4 Block Diagram

A block diagram of the full gate driver is shown in Figure 3. Both channels (high- and low-side) include a dedicated isolated DC/DC converter and gate driver integrated circuit (IC) for independent modulation of the respective channel. The gate driver communicates with a controller via differential signaling for both input and feedback signals. The gate driver combines all onboard fault signals (i.e. overcurrent and power faults for both channels) into a single global fault signal which is transmitted to the controller to indicate the board status. The board includes an overcurrent detection circuit, independent turn-on and turn-off resistors, Miller clamp, and thermistor feedback. Some notable interface features on the board are indicated in Figure 4.

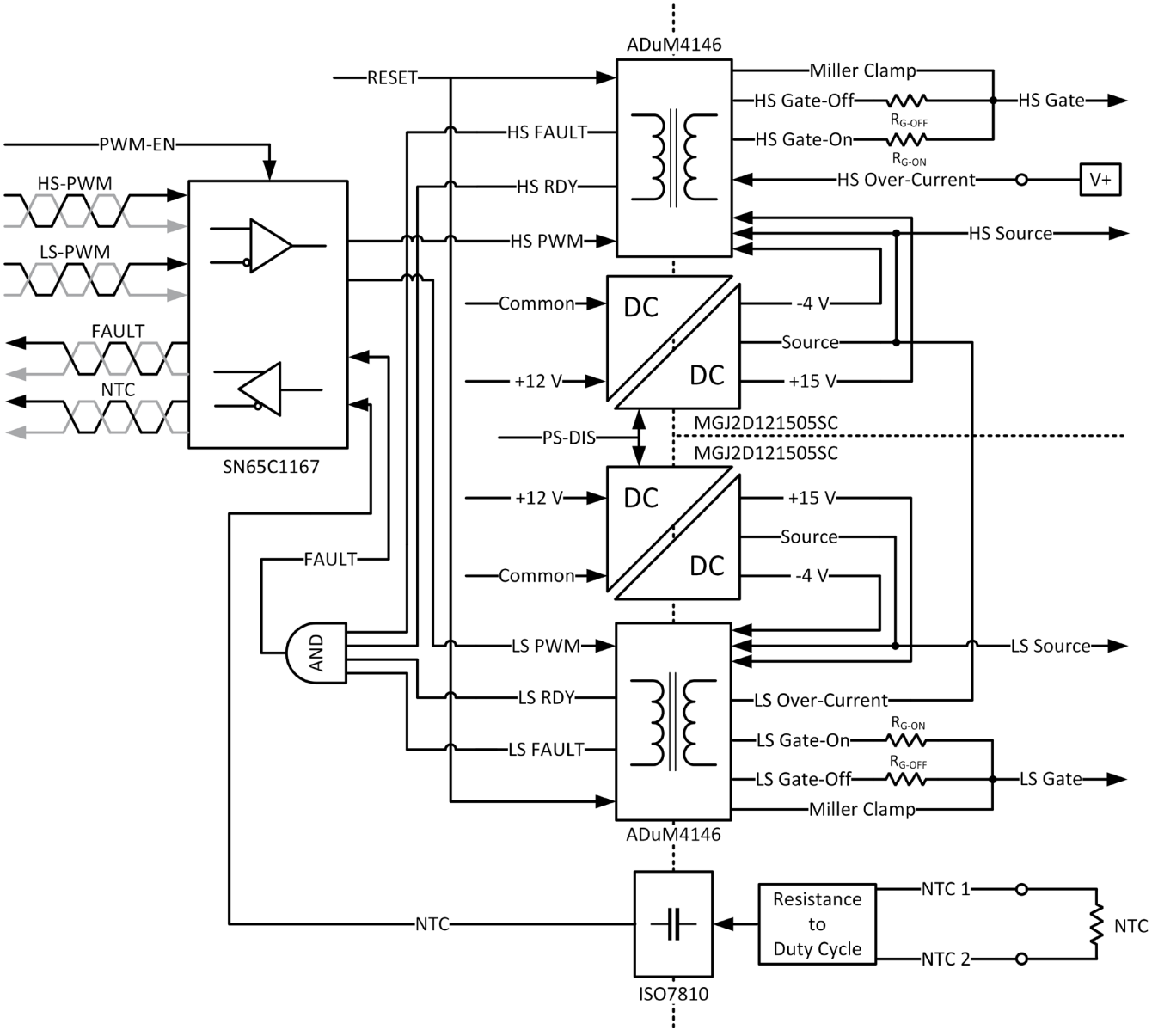

Figure 3: Block diagram of CGD1200HB2P-XM3 gate driver

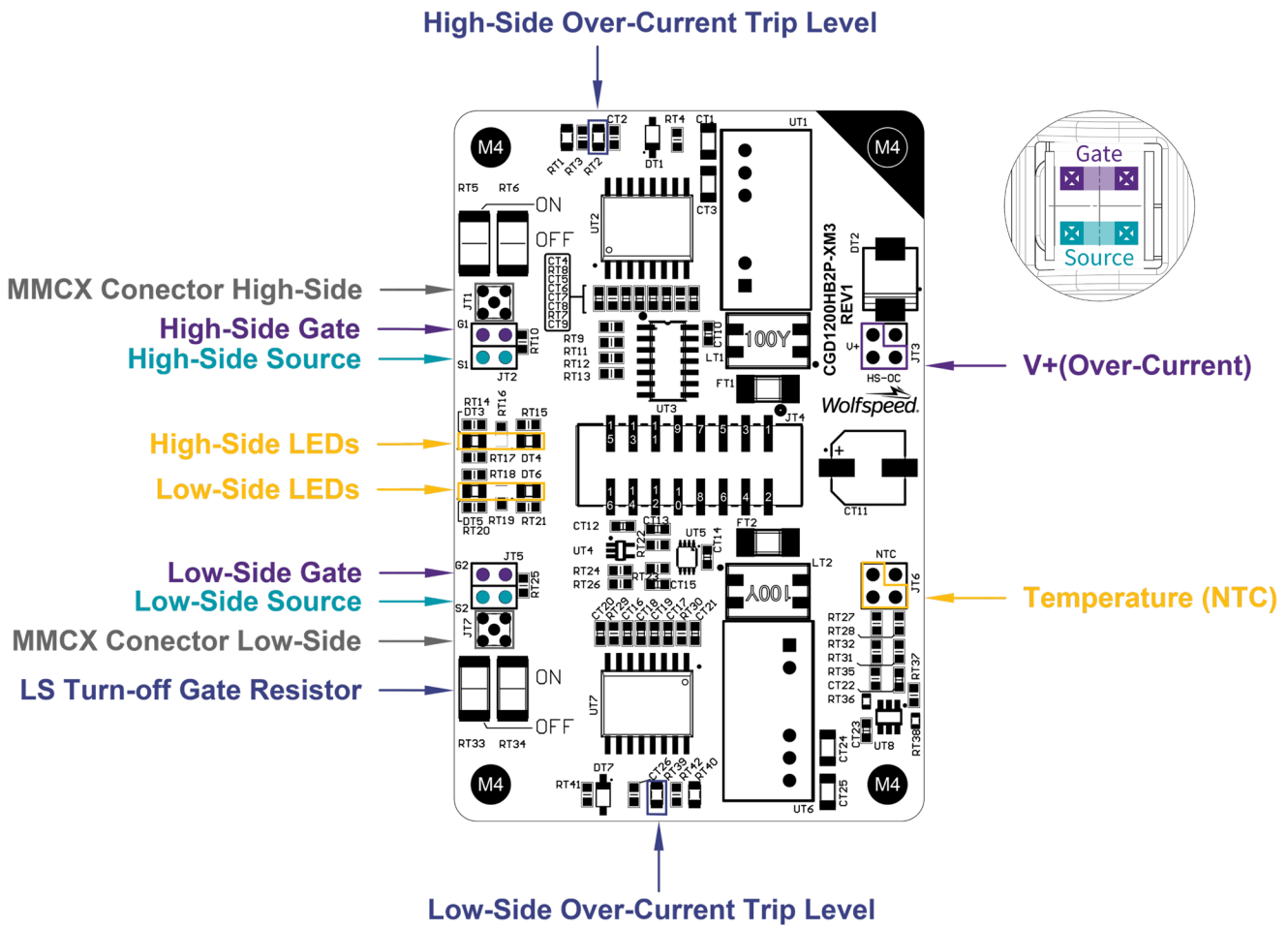

Figure 4: Interface of CGD1200HB2P-XM3 gate driver

3. Inputs/Outputs

The CGD1200HB2P-XM3 gate driver includes multiple connectors for interfacing with the power module and control signals and to perform measurements. This section details the pinout and functionality of each of these connectors. An overview of the purpose of each connector is shown in Table 3 along with the corresponding document section to find additional information.

Table 3: Summary of input/output connectors

Ref. Des.	Side	Description	Section
JT1	Top	High-side V_{GS} measurement	3.5
JT2	Bottom	High-side output	3.2
JT3	Bottom	V+ measurement	3.4
JT4	Top	Input signals	3.1
JT5	Bottom	Low-side output	3.2
JT6	Bottom	Thermistor feedback	3.3
JT7	Top	Low-side V_{GS} measurement	3.5

3.1 Input Connector

The CGD1200HB2P-XM3 gate driver is intended to operate with differential signaling for improved noise immunity compared to single-ended signaling (see Section 4.2). All the control and feedback signals with this gate driver are digital and interface through a single input connector (reference designator *JT4*). This connector orientation and the corresponding pin locations are shown in Figure 5. *JT4* uses part number SBH11-NBPC-D08-SM-BK manufactured by Sullins Connector Solutions and the suggested mating parts are listed in Table 4.

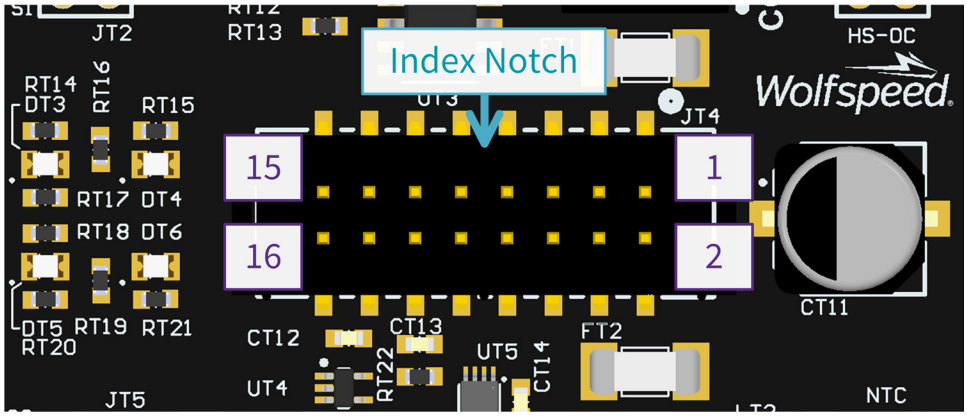

Figure 5: JT4 input connector orientation and pin locations

Table 4: Input connector suggested mating parts

Component	Manufacturer	Part Number	Description
Mating IDC Connector	Sullins Connector Solutions	SBH11-NBPC-D08-SM-BK	16 Position Rectangular Header Connector IDC Gold 28 AWG
Straight Ribbon Cable[1]	3M	HF365/16SF	Flat Ribbon Cable Gray 16 Conductors 0.050" (1.27mm) Flat Cable
Twisted Ribbon Cable[1]	3M	1700/16 100SF	Flat Ribbon Cable Multiple 16 (8 Pair Twisted) Conductors 0.050" (1.27mm)
Mating Vertical (PCB Mount)	Sullins Connector Solutions	SFH11-PBPC-D08-ST-BK	16 Position Header Connector 0.100" (2.54mm) Through Hole Gold
Mating Right-Angle (PCB Mount)	Sullins Connector Solutions	SFH11-PBPC-D08-RA-BK	16 Position Header Connector 0.100" (2.54mm) Through Hole, Right Angle Gold

[1] When using ribbon cable for long connections, it is recommended to use twisted-pair ribbon cable for improved noise immunity.

3.1.1 Pinout

Table 5: Pinout of JT4 input connector

Pin	Name	Description
1	VDC	Power supply input pin (+12 V Nominal Input).
2	Common	Common.
3	HS-PWM-P*	Positive line of 5 V differential high-side PWM signal pair. Terminated into 120 Ω.
4	HS-PWM-N*	Negative line of 5 V differential high-side PWM signal pair. Terminated into 120 Ω.
5	LS-PWM-P*	Positive line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω.
6	LS-PWM-N*	Negative line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω.
7	$\overline{\text{FAULT-P}}$*	Positive line of 5 V differential fault condition signal pair. Drive strength 20 mA. A low state on FAULT indicates when a desaturation fault has occurred. The presence of a fault precludes the gate drive output from going high.
8	$\overline{\text{FAULT-N}}$*	Negative line of 5 V differential fault condition signal pair. Drive strength 20 mA.
9	THERM-P*	Positive line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA. Temperature measurement is encoded via duty cycle.
10	THERM-N*	Negative line of 5 V temperature dependent resistor output signal pair. Drive strength 20 mA. Temperature measurement is encoded via duty cycle.
11	$\overline{\text{PS-DIS}}$	Pull down to disable power supply. Pull up or leave floating to enable. Gate and source are connected with 10 kΩ when disabled.
12	Common	Common.
13	PWM-EN	Pull down to disable PWM input logic. Pull up or leave floating to enable. Gate driver output will be held low through turn-off gate resistor if power supplies are enabled.
14	Common	Common.
15	Reset	When a fault exists, bring this pin high for >500 ns to clear the fault.
16	Common	Common.

* Inputs 3-10 are differential pairs.

3.1.2 Signal Descriptions

PWM Signals: High-side and low-side pulse-width modulation (PWM) signals are RS-422 compatible differential inputs. The termination impedance of the differential receiver is 120 Ω. Overlap protection is provided to prevent both the high-side and low-side gates from turning on simultaneously. The overlap protection should not be used as a dead time generator.

$\overline{\text{FAULT}}$ Signal: The fault signal is a RS-422 compatible differential output with a maximum drive strength of 20 mA. A high signal (positive line > negative line) means there are no fault conditions for either gate driver channel. This signal will be low if an overcurrent fault or undervoltage-lockout (UVLO) fault condition is detected on either channel. The onboard light-emitting diodes (LEDs) will indicate the fault condition. See Sections 3.6 and 4.4 for more details.

THERM Signal: THERM output is a differential signal that returns the resistance of the temperature sensor integrated into XM modules. It is a duty cycle signal that encodes the resistance of the temperature sensor.

The approximate temperature of the module can be determined from this resistance. See the Section 4.7 for further details.

$\overline{PS\text{-}DIS}$: The PS-DIS signal disables the output of the isolated DC/DC converters for the two channels. It is a single-ended input that must be pulled low to turn off the power supplies. With the power supplies disabled the gate will be held low with a 10 kΩ resistor. This signal can be used for startup sequencing.

PWM-EN: This is a single-ended input that enables the PWM inputs for both channels. When this signal is pulled down the differential receivers for both channels are disabled, and the gates will both be pulled low through $R_{G(EXT)\text{-}OFF}$. All protection circuitry and power supplies will continue to operate including FAULT and THERM outputs.

RESET: This is a single-ended input that can be used to clear overcurrent faults on the gate driver. To clear an overcurrent fault, this signal must be commanded high for at least 500 ns. While the signal remains high, the outputs of the gate driver remain disabled. On the gate driver board, this input is held low with a 10 kΩ resistor. This signal resets both channels of the gate driver.

3.2 Output Connectors

The output connectors on the CGD1200HB2P-XM3 gate driver are four pin headers designed to attach directly to the XM power modules with inline gate pins. An example connection is shown in Figure 6. The power bussing connects directly to the power terminals of the module. **The CGD1200HB2P-XM3 gate driver should not be used on XM power modules with crossed gate pins** (see PRD-07128). The high-side and low-side output connectors are isolated from each other and do not share a source connection. The gate and source connections for both channels, *JT2* and *JT5*, are shown in Figure 7.

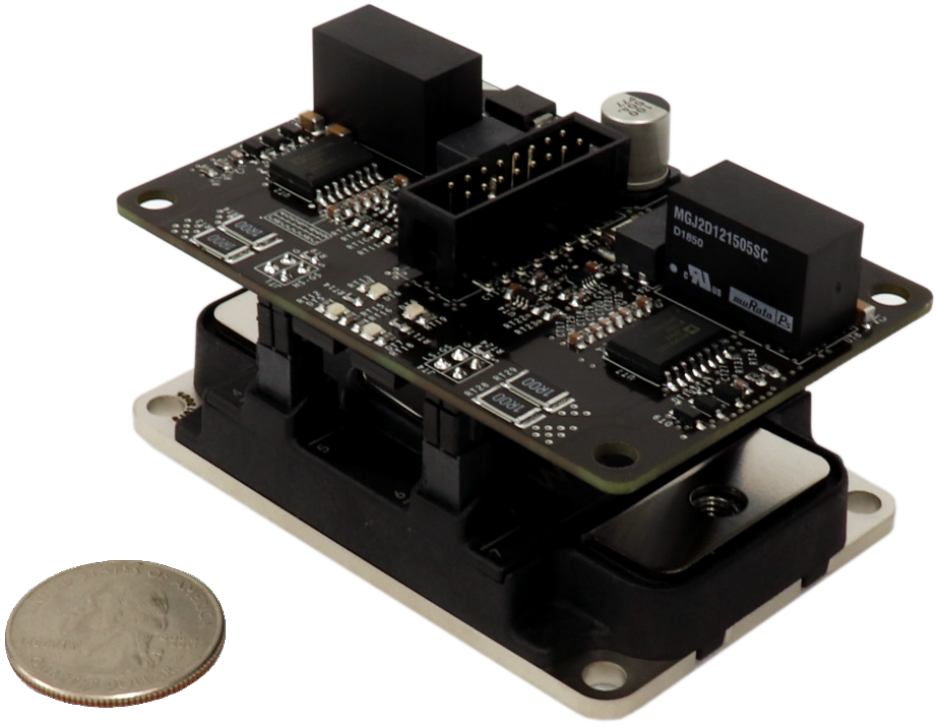

Figure 6: Example gate driver attached to XM power module

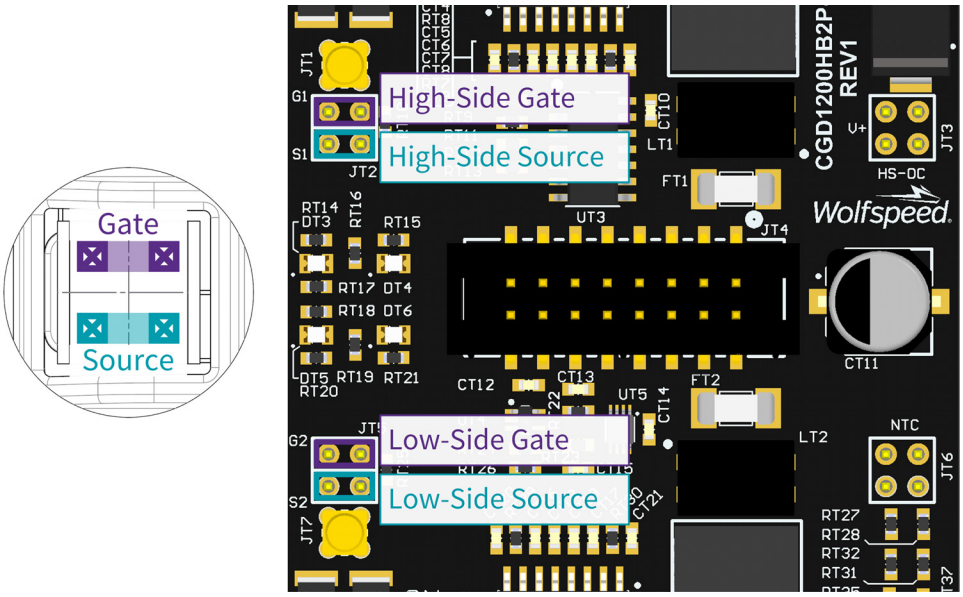

Figure 7: JT2 and JT5 output connectors orientations and pin locations

3.3 Thermistor Connector

The XM power modules include an integrated negative temperature coefficient (NTC) thermistor for monitoring the baseplate temperature of the module (see PRD-08376). The CGD1200HB2P-XM3 gate driver includes circuitry to directly measure this thermistor and encode the resistance as a duty cycle to the controller. The thermistor connector, *JT6*, attaches directly to the XM module and is shown in Figure 8. Two pins of the connector are attached to one side of the thermistor (shown as "-" in the figure) and one pin is attached to the other side of the thermistor (shown as "+" in the figure). See Section 4.7 for more information about the thermistor circuit and corresponding duty cycle encoding.

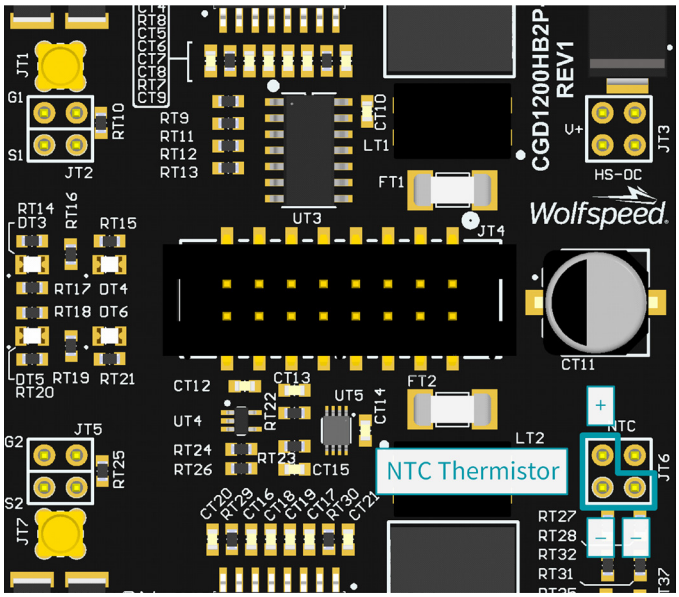

Figure 8: JT6 thermistor connector orientation and pin locations

3.4 V+ Connector

The desaturation circuit employed on this design for overcurrent protection (see Section 4.4.3) requires accurate feedback of the MOSFET drain terminals to identify when the module is conducting elevated current. For overcurrent protection of the low-side switch position, the desaturation circuit can directly measure the high-side source terminal on the gate driver to determine the drain voltage of the low-side position. For overcurrent protection of the high-side switch position, the XM power module family provides access to the high-side drain terminal through a dedicated connector. The CGD1200HB2P-XM3 gate driver includes a connector, *JT3*, to access the high-side drain terminal for overcurrent protection. This connector, shown in Figure 9, engages with the XM module the same as the output connectors and thermistor connector. All the pins of the connector are attached to the high-side drain terminal.

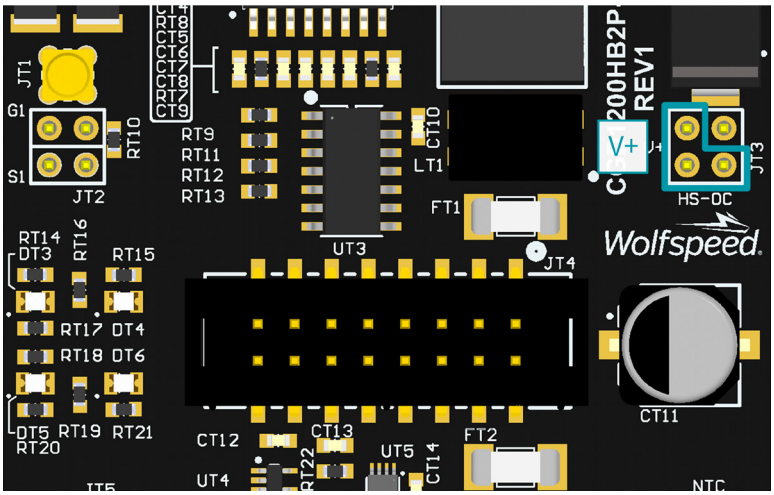

Figure 9: JT3 V+ connector orientation and pin locations

This connector cannot be left floating as the overcurrent fault will trip immediately when the high-side gate is actuated. If bench-top testing of the gate driver is required, it is acceptable to short this connector to the high-side source to prevent the overcurrent fault from tripping.

3.5 Gate-to-Source Voltage Measurement Connectors

A high-fidelity gate-to-source voltage measurement (V_{GS}) is critical for many applications such as device characterization, system commissioning, and troubleshooting. The CGD1200HB2P-XM3 gate driver includes integrated micro-miniature coaxial (MMCX) connectors for measuring the V_{GS} outputs of the gate driver. The pinouts and locations for the measurement connectors are shown in Figure 10. A variety of probes can interface directly with these standard MMCX connectors. Wolfspeed recommends performing these measurements with an optically isolated probe such as the Tektronix® IsoVu™ series of probes to ensure high common-mode rejection during measurements. This is especially critical for the high-side V_{GS} measurement which is referenced to a varying voltage node. If this gate driver board is attached to the device under test through an interface board (i.e. the board is not directly attached to the power module), it is recommended to measure the gate-to-source voltage on the interface board rather than on this gate driver to ensure a high-fidelity measurement.

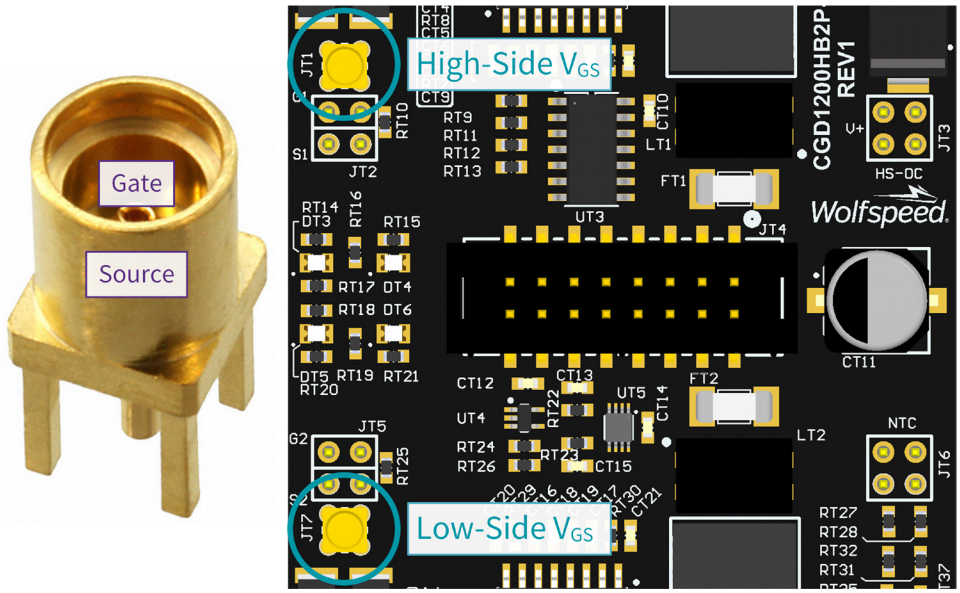

Figure 10: JT1 and JT7 measurement connectors orientations and pin locations

3.6 Status Indicators

The CGD1200HB2P-XM3 gate driver includes four LEDs, shown in Figure 11, to indicate the state of the board. The functionality of these LEDs is summarized in Table 6. In normal operation, the green READY LEDs (*DT3* and *DT5*) will be illuminated, indicating that the gate driver board is functioning as expected. When the system faults due to an overcurrent event, the channel(s) where the fault occurred will illuminate the corresponding red FAULT LED (*DT4* and/or *DT6*). When the gate driver has an UVLO or thermal shutdown (TSD) event, the READY LED of the relevant channel(s) will be extinguished. The status of the gate driver board depending on the LED states is summarized in Table 7.

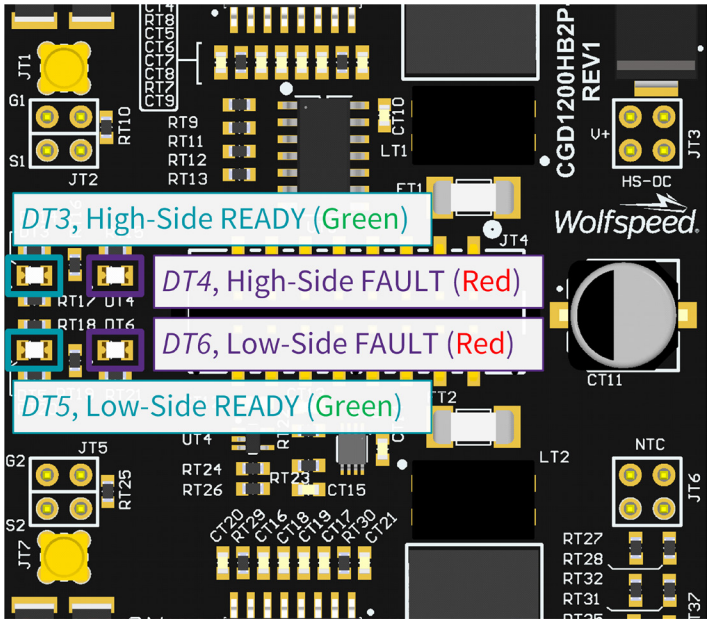

Figure 11: Status LEDs: locations and purposes

Table 6: Status LED descriptions

LED	Color	Description
DT3	Green	High-Side READY
DT4	Red	High-Side FAULT
DT5	Green	Low-Side READY
DT6	Red	Low-Side FAULT

Table 7: Status LED states

READY LED (*DT3* | *DT5*)	FAULT LED (*DT4* | *DT6*)	Description
1	0	Normal operation. No issues.
0	X	Bad power rail(s) or thermal shutdown. Check input power quality, fuses, component failure, and output short-circuit.
X	1	Overcurrent fault. Clear fault condition and reset gate driver.

1 = LED On | 0 = LED Off | X = Irrelevant

4. Features

The CGD1200HB2P-XM3 gate driver includes several design features intended to enable it to efficiently and reliably drive high-performance SiC MOSFETs at high frequencies. These features – which enable higher efficiency, noise immunity, flexibility, and protection – are detailed in this section.

4.1 Independent Gate Resistors

The design includes separate external turn-on and turn-off resistors for both channels of the gate driver. The different resistors allow for independent tuning of the turn-on and turn-off switching dynamics. This can be useful for optimizing switching losses while staying within the safe operating bounds. By default, the CGD1200HB2P-XM3 gate driver includes 1 Ω gate resistors for turn-off and turn-on for both channels, though the resistors can be easily changed to adjust the switching dynamics. The default resistors used are Vishay Dale CRCW25121R00FKEGHP resistors in a surface-mount 2512 (6432 metric) footprint. In an effort to maximize performance, it is recommended to use pulse-rated resistors when replacing/changing the gate resistors. The locations of the gate resistors are shown in Figure 12, and the purpose of each resistor is summarized in Table 8. See PRD-09301 for more information about independent gate resistor tuning.

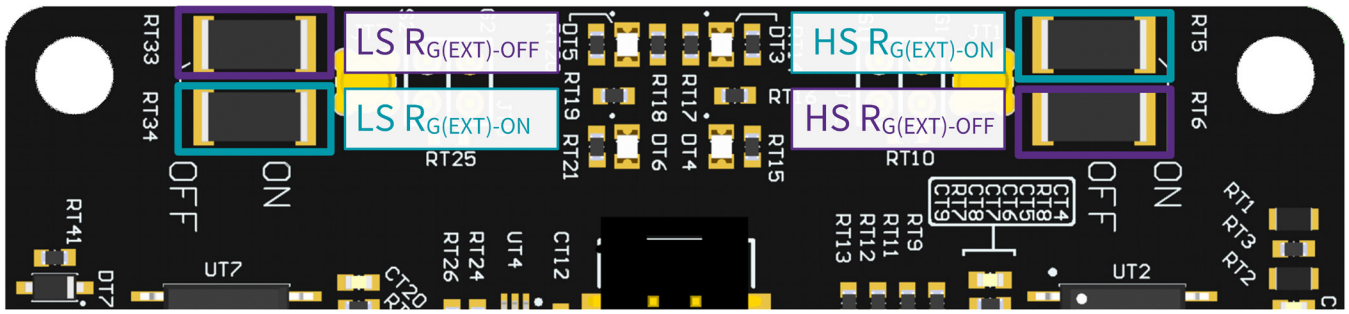

Figure 12: External turn-on and turn-off gate resistor locations

Table 8: External gate resistors descriptions

Ref. Des.	Default	Description
RT5	1 Ω	High-Side External Turn-On Resistor
RT6	1 Ω	High-Side External Turn-Off Resistor
RT33	1 Ω	Low-Side External Turn-Off Resistor
RT34	1 Ω	Low-Side External Turn-On Resistor

4.2 Differential Signaling

Signal integrity is critical when controlling power devices with a gate driver. A gate driver that is susceptible to the powerful interference generated by power devices can induce a shoot-through condition in the module. The extremely fast turn-on and turn-off times during the switching events in a SiC power system can create electromagnetic interference (EMI) that can easily couple onto the gate control signals. For this reason, differential signaling was adopted instead of standard, single-ended connections between the gate driver and control board. More information about differential signaling compared to single-ended connections is provided in PRD-09301.

Differential signaling significantly reduces the impact of radiated noise from the switching events of a power module. A single-ended signal can be converted to a differential signal by transmitting both the original signal and its complement in two closely coupled wires. At the receiver, the two signals are compared in order to reconstruct the original signal. Figure 13 illustrates this principle with an example of induced noise forced onto the cable somewhere between the transmitter and receiver. The noise affects both the original signal and the complement by the same magnitude assuming that the cables are consistently coupled. Thus, when the receiver compares the two signals, the difference is unaffected by the noise induced on the line and the intended original signal is created.

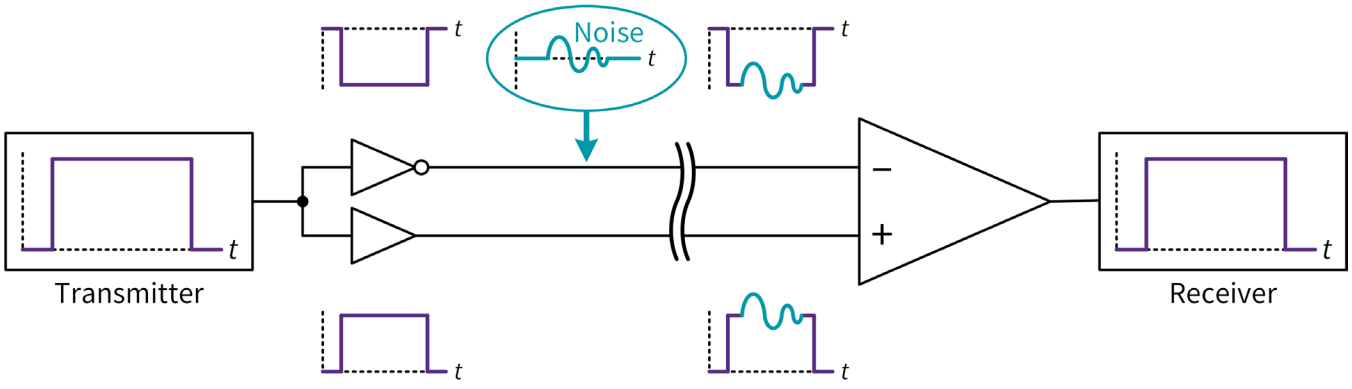

Figure 13: Noise immunity improvement provided by differential signaling

The CGD1200HB2P-XM3 gate driver requires differential communication for proper performance. This can be achieved through differential transceivers included directly on a control board or using a single-ended to differential transceiver board. Wolfspeed provides the CGD12HB00D 2-channel differential transceiver companion tool for adding differential signaling to projects. For a reference design which adds differential

transceivers to the control board, see the control board design from the CRD300DA12E-XM3 inverter. The differential circuit implemented on the CGD1200HB2P-XM3 gate driver board is shown in Figure 14.

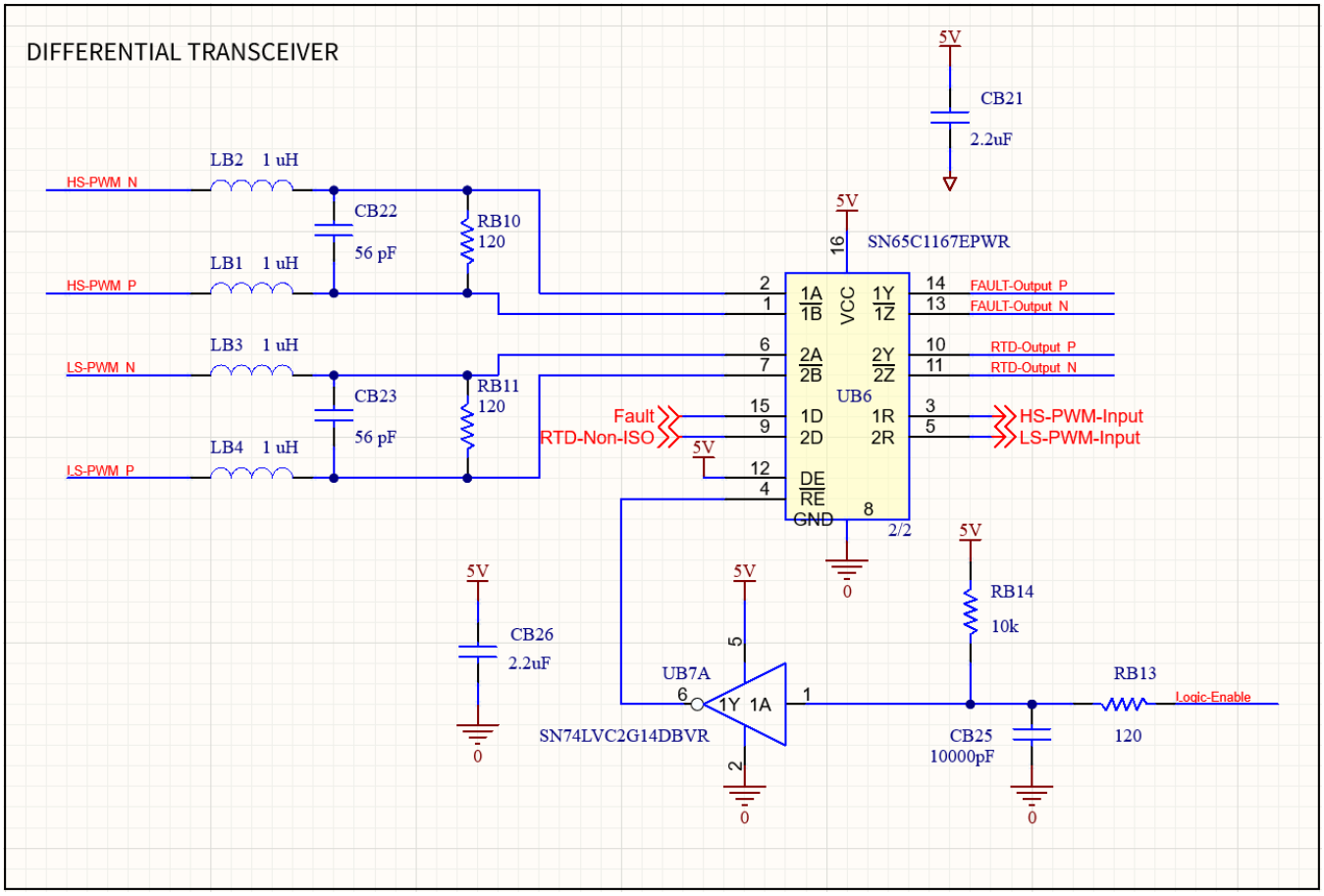

Figure 14: Differential signaling circuit

4.3 Adjustable Output Voltages

By default, the gate driver outputs a high voltage of +15 V and a low voltage of -4 V. The default onboard isolated power supply directly generates +15 V and -5 V rails (Figure 15), and an onboard linear regulator is employed to reduce the output-low voltage from -5 V to -4 V (Figure 16). These voltages can be manipulated to characterize and/or operate the SiC power module under different bias conditions.

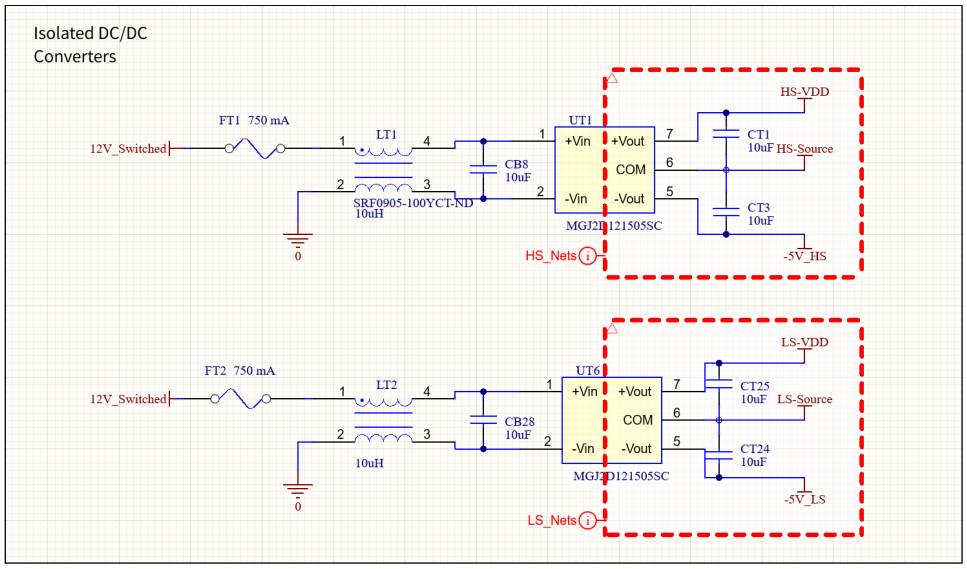

Figure 15: Isolated power supply circuits

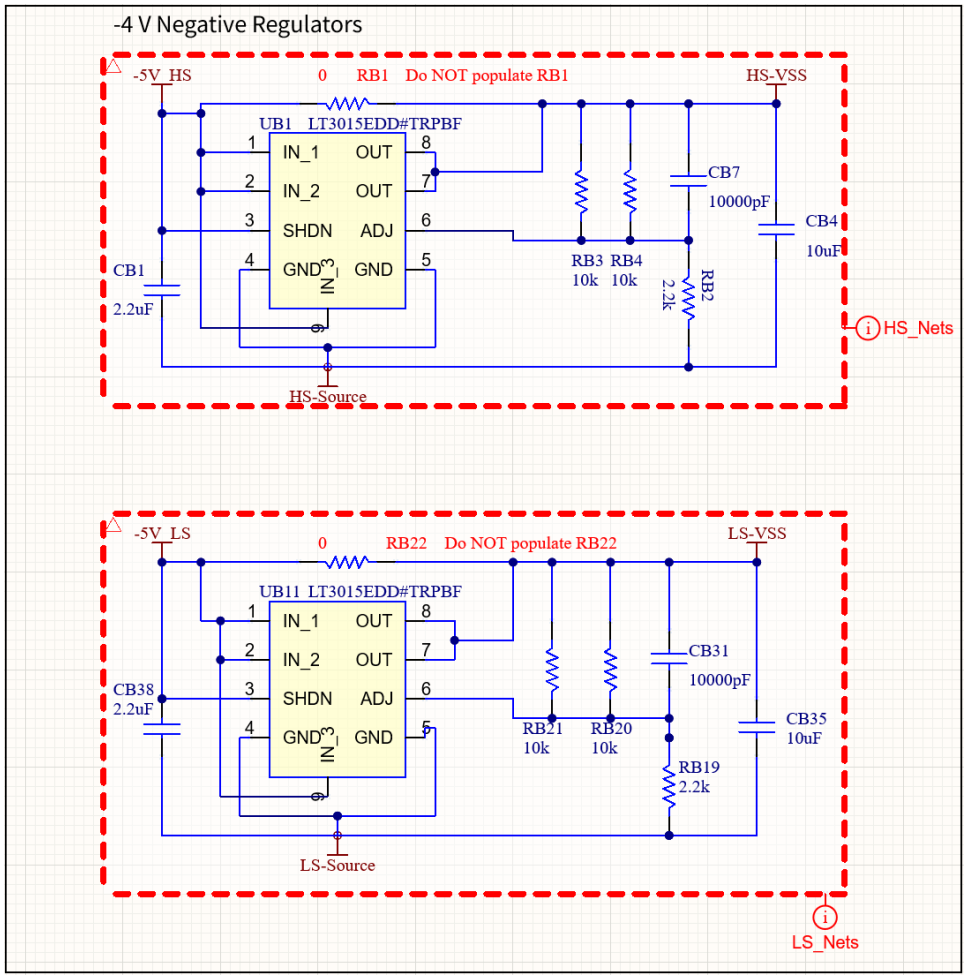

Figure 16: Negative linear regulator circuits to generate -4 V turn-off voltage

To change the turn-off voltage, change the feedback resistor network on the linear regulator to adjust the voltage using the equation below. The output voltage of the linear regulator can be adjusted between -1.22 V and (V_{IN} + 0.3 V). The linear regulator can also be bypassed by removing the linear regulator and populating the unpopulated 0 Ω resistors on the board (*RB1* and *RB22*).

$$V_{OUT} = -1.22\ V\left(1 + \frac{R_2}{R_1}\right) + \left(I_{ADJ}\right)(R_2)$$

where

R_1: bias resistor attached to the common rail [Ω]
R_2: bias resistor attached the output voltage rail [Ω]
I_{ADJ}: bias current (30 nA at 25 °C, see component datasheet for more information) [A]

The calculation for the default circuit configuration of -4 V is shown below for reference.

$$-1.22\ V\left(1 + \frac{5\ k\Omega}{2.2\ k\Omega}\right) + (30\ nA)(5\ k\Omega) = -4\ V$$

To adjust the output-high voltage (or as an alternative method to change the output-low voltage), simply swap the isolated power supply on the board. The isolated power supply used on the board uses an industry-standard 5-pin 7-SIP footprint, so many manufacturers have solutions with different output voltages. Note that the power supply is critical to maintaining high isolation on the gate driver board. If changing the isolated power supply, ensure that it has suitable isolation ratings for the intended application.

The power modules are not intended to be operated continuously in the linear region, so the user should ensure that the selected voltages are within the safe operating area of the device. Also, the overcurrent protection circuit trip point is biased from the output-high voltage rail (see Section 4.4.4), so modifying this voltage can influence the trip point of the overcurrent protection circuit. Furthermore, the digital isolator used for the thermistor feedback circuit (see Section 4.7) is powered from the gate driver output-low voltage rail. Configuring the output-low voltage rail too low could lose operation of the thermistor feedback circuit. Careful scrutiny should be employed if the power rails are being modified.

4.4 Faults / Protections

The CGD1200HB2P-XM3 gate driver is protected from input +12 V power quality issues, isolated power supply issues, signal overlap, and overcurrent events in the power module. This section discusses these faults in more detail and how to adjust them. Table 9 provides a logic table summary indicating the state of the gate driver outputs depending on the various input signals and/or fault statuses.

Table 9: Output logic table depending on inputs and faults

PWM	PWM-EN	PS-DIS	RESET	Overcurrent/ UVLO	FAULT	Output
H	H or Z	H or Z	L	No	H	H
L	H or Z	H or Z	L	No	H	L
X	L	H or Z	L	No	H	L
X	X	L	X	No	L	Z
X	H or Z	H or Z	L	Yes	L	L

H = High | L = Low | X = Irrelevant | Z = High Impedance

4.4.1 Input Voltage Protection

The CGD1200HB2P-XM3 gate driver includes overvoltage, inrush current, and reverse voltage protection on the +12 V power input (pin 1) of the input connector, *JT4*. The inrush current protection is implemented through a power management circuit, shown in Figure 17, which can be enabled/disabled through the *PS-DIS* signal to remotely handle start-up sequencing. The implemented overvoltage and reverse voltage protection circuit is shown in Figure 18. The Zener diode protects from input voltage spikes greater than 20 V (nominal) and the P-channel MOSFET protects from the positive and negative polarities being reversed. Incorrect connections should be avoided when using the CGD1200HB2P-XM3 gate driver, although these circuit elements are included to protect the system if it is incorrectly wired.

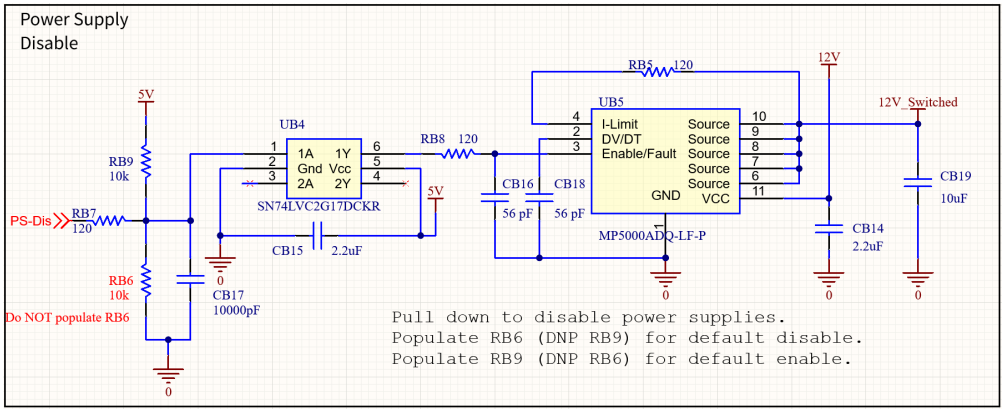

Figure 17: Input overcurrent protection and power disable circuit

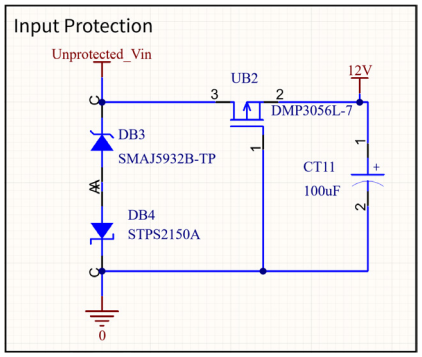

Figure 18: Input overvoltage and reverse voltage protection circuit

4.4.2 Undervoltage Lockout

The Analog Devices ADuM4146C gate driver IC used on this design features integrated UVLO. The UVLO circuit detects when the output rails of the isolated DC/DC converter fall below safe operating conditions for the gate driver. A UVLO fault indicates that the potential between the split output voltage rails has fallen below the UVLO active level. The gate for the channel where the fault occurred will be pulled low through $R_{G(EXT)-OFF}$ for the duration of the fault regardless of the PWM input signal. The fault will automatically clear once the potential has risen above the UVLO inactive level. There is hysteresis for this fault to ensure safe operating conditions. The UVLO faults for both channels are combined along with the overcurrent fault in the FAULT output signal. When there is no UVLO fault present, a green LED indicates a power good state. The LED, *DT3*, indicates a high-side power good status, and *DT5* indicates a low-side power good status.

4.4.3 Overcurrent Fault

An overcurrent (OC) fault is an indication of an overcurrent event in the SiC power module. The overcurrent protection circuit, shown in Figure 19 for the low-side and in Figure 20 for the high-side, measures the drain-to-source voltage (V_{DS}), and the fault will indicate if this voltage has risen above a level corresponding to the safe current limit. When a fault has occurred, the corresponding gate driver channel will be disabled, and the gate will be pulled down through a soft-shutdown resistance, R_{SS}. The drain-source limit can be configured through onboard resistors. The overcurrent fault is latched upon detection and must be cleared by the user with a high pulse of at least 500 ns on the *RESET* signal. The various timing and voltage trip levels presented in Table 2 and Section 4.4.4 are defined notionally in the timing diagram shown in Figure 21.

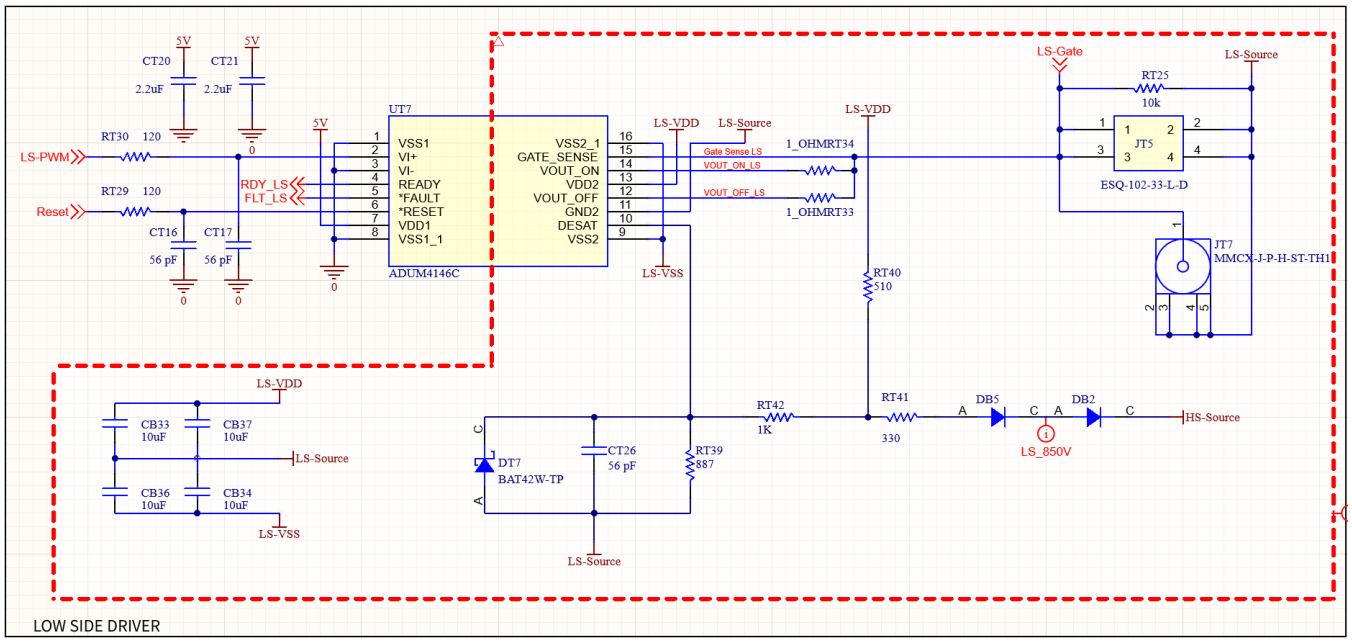

Figure 19: Low-side gate driver circuit with overcurrent protection

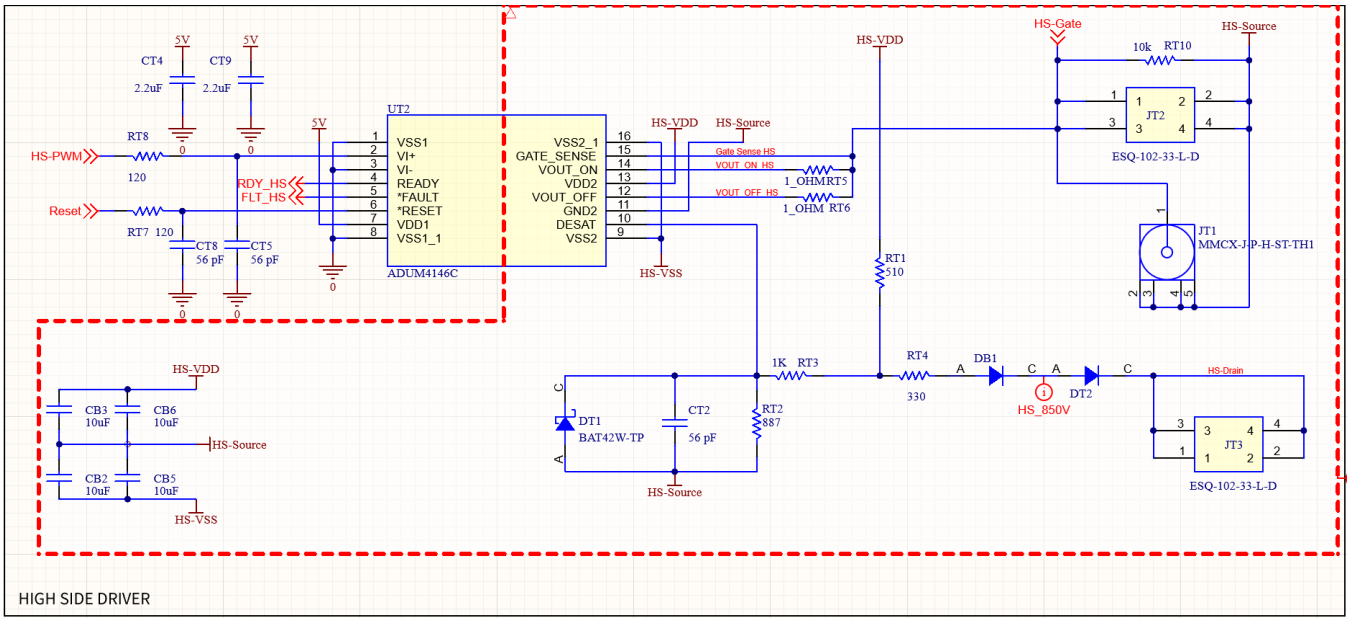

Figure 20: High-side gate driver circuit with overcurrent protection

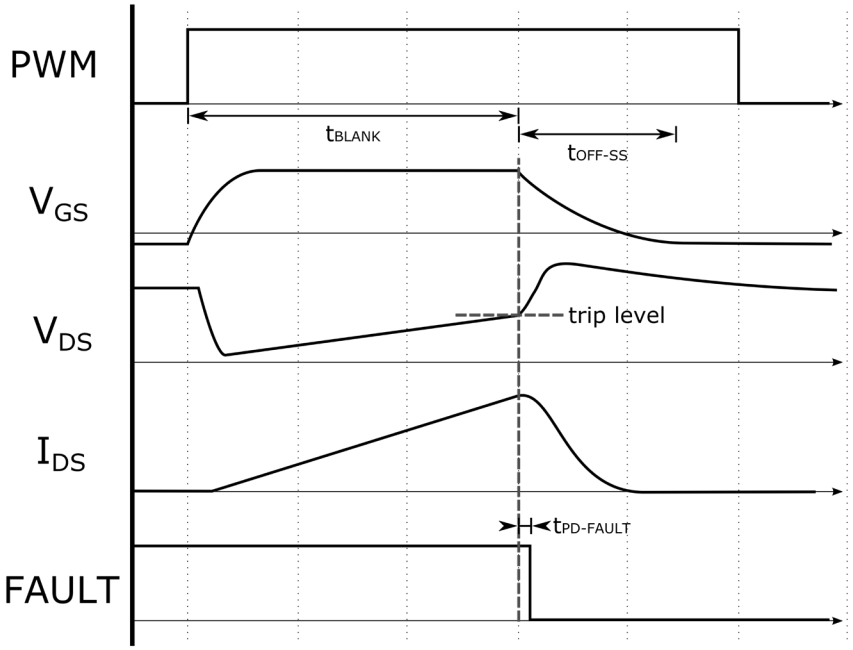

Figure 21: Overcurrent fault timing diagram

4.4.4 Overcurrent Trip Level

The OC fault detection circuit, shown in Figure 19 and Figure 20, measures the on-state V_{DS} across each switch position and triggers a fault condition if the voltage rises above the predefined set level. The circuit is simplified into the notional diagram shown in Figure 22. Referring to this figure, the intermediary voltages V_2 and V_X and the trip resistor, R_X, can be calculated using the following equations:

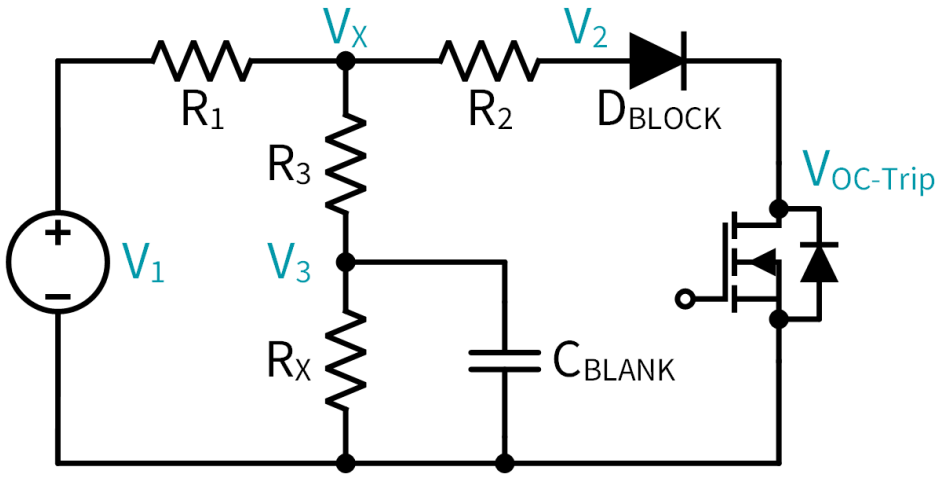

Figure 22: Notional overcurrent fault circuit

$$V_2 = V_{OC-Trip} + N_D \cdot V_F \;\; ; \;\; V_x = \frac{R_2\, R_3\, V_1 + R_1\, R_3\, V_2 + R_1\, R_2\, V_3}{R_1\, R_2 + R_1\, R_3 + R_2\, R_3} \;\; ; \;\; R_X = \frac{V_3 \cdot R_3}{V_X - V_3}$$

where

V_2: intermediate voltage shown in Figure 22 [V]
$V_{OC-Trip}$: target overcurrent trip voltage [V]
N_D: number of series high-voltage blocking diodes
V_F: forward voltage of the high-voltage blocking diode(s) [V]
V_X: intermediate voltage shown in Figure 22 [V]
V_1: source voltage (output-high gate driver voltage) [V]
V_3: internal comparator trip voltage of the gate driver IC [V]
R_1, R_2, R_3: circuit resistor values [Ω]
R_X: resistor value required to trip at the appropriate overcurrent value [Ω].

To select an appropriate overcurrent trip level, refer to the I_D vs. V_{DS} output characteristic curves in the applicable module datasheet. As an example, the pulse-current rating of Wolfspeed's CAB450M12XM3 is 900 A; therefore, an overcurrent trip point of 1000 A at 25 °C is selected. On the I_D vs. V_{DS} curve, the drain-to-source voltage at the 1000 A operating condition is approximately 2.9 V. Hence, the over-current trip voltage, $V_{OC-Trip}$, should be approximately 2.9 V. Using this value and with the values from the schematic (shown below), the necessary trip resistor, R_X, can be calculated, as shown below.

$V_{OC-Trip}$: 2.9 V (from the datasheet I_D vs V_{DS} plot of the example module)
N_D: 2 (from gate driver schematic)
V_F: 0.5 (from high-voltage diode datasheet)
V_1: 15 V (from gate driver schematic)
V_3: 3.5 V (from the Analog Device ADuM4146C datasheet)
R_1: 510 Ω; R_2: 330 Ω; R_3: 1 kΩ (from gate driver schematic)

$$V_2 = 2.9\,V + 2 * \; 0.5\,V \rightarrow \boldsymbol{V_2 = 3.9\,V}$$

$$V_x = \frac{330\ \Omega * 1000\ \Omega * 15\ V + 510\ \Omega * 1000\ \Omega * 3.9\ V + 510\ \Omega * 330\ \Omega * 3.5V}{510\ \Omega * 330\ \Omega + 510\ \Omega * 1000\ \Omega + 330\ \Omega * 1000\ \Omega} \rightarrow \boldsymbol{V_x = 7.466\ V}$$

$$R_x = \frac{3.5\ V * 1000\ \Omega}{7.466\ V - 3.5\ V} = \frac{3500}{3.966} \rightarrow \mathbf{R_x = 883\ \Omega}$$

By default, the CGD1200HB2P-XM3 gate driver is configured with a 2.9 V overcurrent trip voltage, and therefore an 883 Ω resistor (approximately). To change the trip value, follow the calculation procedures discussed above. As discussed in Section 3.4, the high-side overcurrent connector, *JT3*, cannot be left floating as the overcurrent fault will trip immediately when the high-side gate is actuated. If bench-top testing of the gate driver is required, it is acceptable to short this connector to the high-side source to prevent the overcurrent fault from tripping. The same phenomenon exists for the low-side, and it is acceptable to short the high-side source (low-side drain) to the low-side source for bench-top testing.

4.4.5 Miller Clamp

When a switch position is in the off state, high *dV/dt* in other switch positions can cause current flow through the Miller capacitance of a MOSFET and ultimately induce noise into the gate. To prevent false turn-on of the device, it is important that the gate driver has a low-impedance to the turn-off voltage when the device is off to ensure the gate of the MOSFET is held low. The Analog Devices ADuM4146 gate driver IC employed on this design features an integrated Miller clamp circuit. When the gate voltage drops below a 2 V internal reference, the Miller clamp latch is engaged, which is a low-impedance connection to the output-low voltage rail. In this configuration, the external turn-off resistor still controls the turn-off dynamics, and the gate driver has a low-impedance connection to dissipate Miller charge even when a high-valued turn-off resistor is employed.

4.4.6 Interlock Protection

In a half-bridge circuit, commanding both channels on simultaneously short-circuits the bus and can cause extreme currents. While the overcurrent protection circuit discussed in 4.4.3 can prevent catastrophic damage this gate driver also includes circuitry intended to prevent both channels from being commanded on simultaneously. This interlock protection, also commonly referred to as shoot-through or anti-overlap protection, applies an XOR logic gate to the two input signals, preventing either output from going high if both signals are commanded on simultaneously, as shown in Table 10. This can help with noise rejection if noise causes one of the commanded signals to flip and it can help prevent issues from a faulty controller. Notably, this protection should not be relied upon for generating dead time. The implemented interlock protection circuit is shown in Figure 23.

Table 10: Interlock protection logic table

HS PWM	LS PWM	$V_{GS,HS}$	$V_{GS,LS}$
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

H = High | L = Low

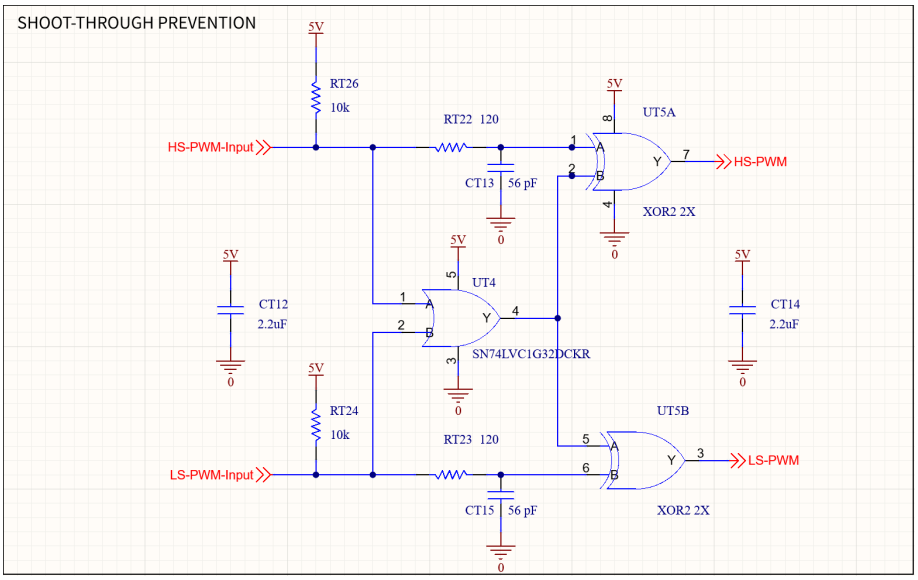

Figure 23: Interlock prevention circuit

4.5 Soft Shutdown

When an overcurrent fault occurs, hard turn-off of the device (i.e. turning the device off normally) can induce large voltage overshoots due to the enormous *di/dt* event. To ensure the device voltage does not exceed safe operating area, the Analog Devices ADuM4146 includes an integrated soft shutdown feature. When the overcurrent fault is detected, a secondary N-channel MOSFET is used to shutdown the device. The second MOSFET has a resistance approximately 35 times more resistive than the normal turn-off MOSFET. Using this approach turns the power device off in a controlled manner to reduce the chance of an overvoltage spike.

4.6 Timing Definitions

Table 2 provides various timing parameters to indicate the propagation delays of the gate driver. These timing parameters are shown visually in Figure 24 for the gate signals.

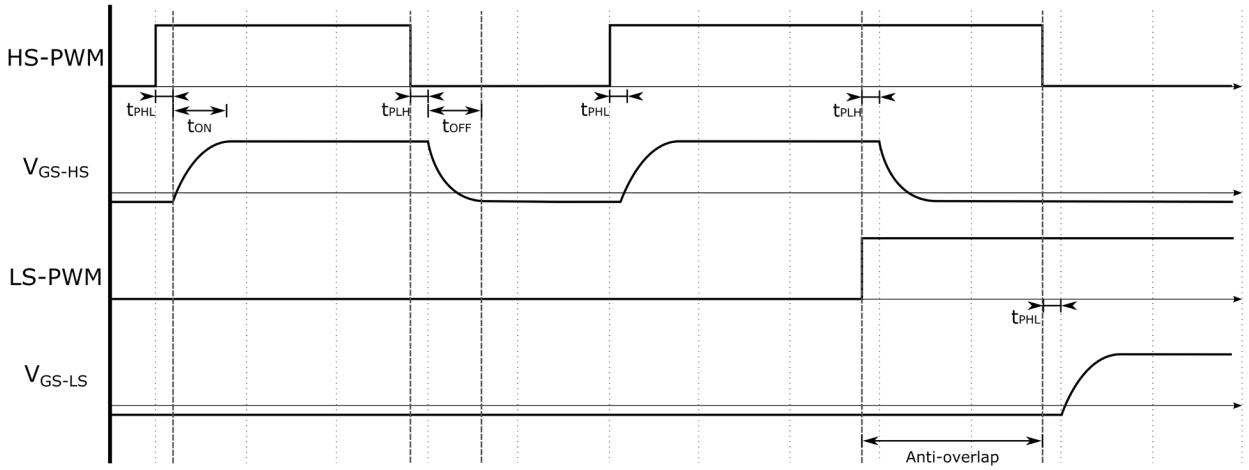

Figure 24: Gate timing diagram

4.7 Thermistor Feedback

The resistance measurement of the XM3 power module's NTC thermistor is available on the input connector (*JT4*) of the gate driver as a differential pair on pins 9 and 10 (see Section 3.1). The thermistor resistance is converted to a PWM signal with varying duty cycle using the circuit shown in Figure 25. The NTC thermistor measurement circuit is attached to the low-side gate drive channel, and a digital isolator is used to transmit the duty cycle-encoded signal back to the primary side of the driver. For this reason, the NTC signal does not need any additional isolation and can be included in the same ribbon cable as the rest of the gate driver's signals.

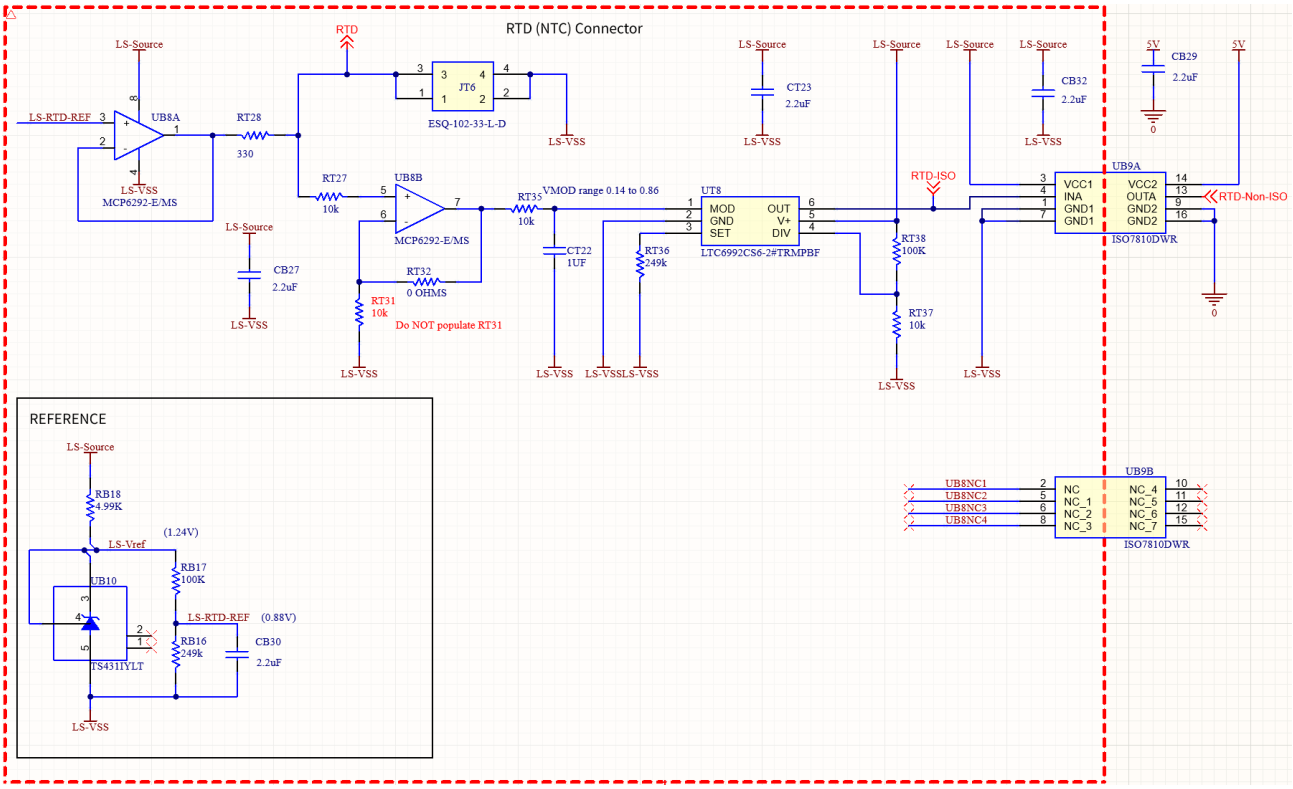

Figure 25: Thermistor resistance to duty cycle conversion circuit

The temperature to duty cycle relationship of the thermistor is shown in Figure 26 and the corresponding numerical values are shown in Table 11. The duty cycle-encoded signal is transmitted at 50 kHz. On the controller side, the duty cycle-encoded signal can be interpreted by directly measuring the duty cycle using edge detection or the signal can be converted to an analog signal with a simple resistor-capacitor (RC) circuit. If using the analog approach, the RC circuit should have a long enough time constant to maintain a stable signal and then it can be measured with an analog-to-digital converter (ADC). The temperature reported by the thermistor differs largely from the junction temperature of the SiC MOSFETs and should not be used as an accurate junction temperature measurement (see PRD-08376).

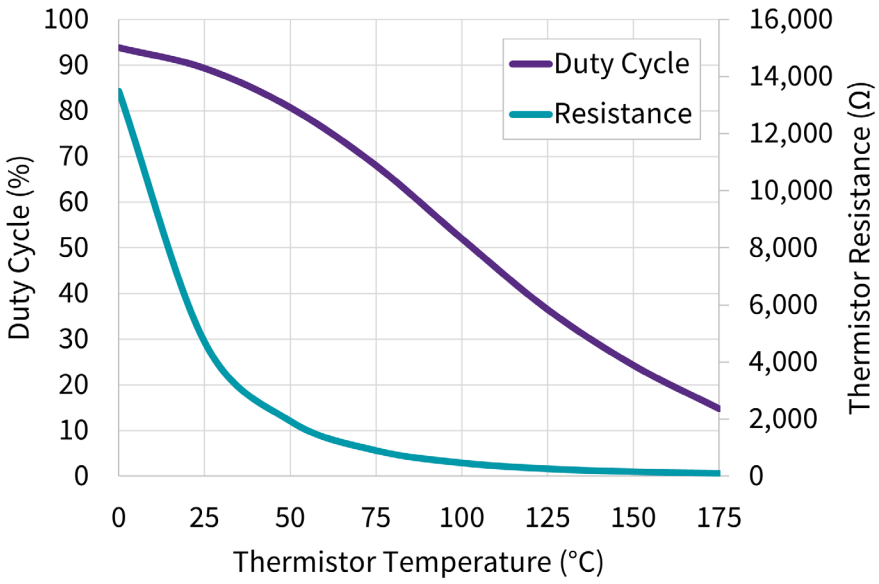

Figure 26: Relationship between thermistor temperature, thermistor resistance, and output duty cycle

Table 11: Gate driver thermistor characteristics

Thermistor Temperature (°C)	Thermistor Resistance (Ω)	Output Duty Cycle (%)
0	13,491	93.8
25	4,700	89.3
50	1,928	80.7
75	898	68.0
100	464	52.0
125	260	36.5
150	156	24.3
175	99	14.8

4.8 Power Estimates

The gate driver power required to drive a switch position at a target switching frequency is calculated using the equation below. The gate charge is dependent on the datasheets of the module being driven. Once the required gate driver power is calculated, the required input power can be calculated from the efficiency curves on the datasheet of the applicable power supply. This calculation is for one channel of the gate driver.

$$P_{SW} = Q_G \cdot f_{SW} \cdot \Delta V_{PS}$$

where

P_{SW}: per channel gate driver power [W]
Q_G: total gate charge [C]
f_{SW}: switching frequency [Hz]
ΔV_{PS}: difference in isolated power supply voltage rails ($V_{PS,HIGH} - V_{PS,LOW}$) [V]

This calculation can be manipulated to determine the maximum switching frequency possible with a gate driver and power module combination (with some margin). An example calculation for the CAB450M12XM3 power module and CGD1200HB2P-XM3 gate driver is demonstrated below.

P_{SW}: 2 W (rated output power of the isolated power supplies on the gate driver)
Q_G: 1300 nC (provided in CAB450M12XM3 datasheet)
$V_{PS,HIGH}$: 15 V (default positive output voltage of the isolated power supply)
$V_{PS,LOW}$: -4 V (default negative output voltage of the isolated power supply)
ΔV_{PS}: 19 V ($V_{PS,HIGH} - V_{PS,LOW}$)

$$f_{SW} \leq \frac{2\ W}{1300\ nC \cdot 19\ V} \rightarrow f_{sw} \leq 80\ kHz$$

5. Dimensions

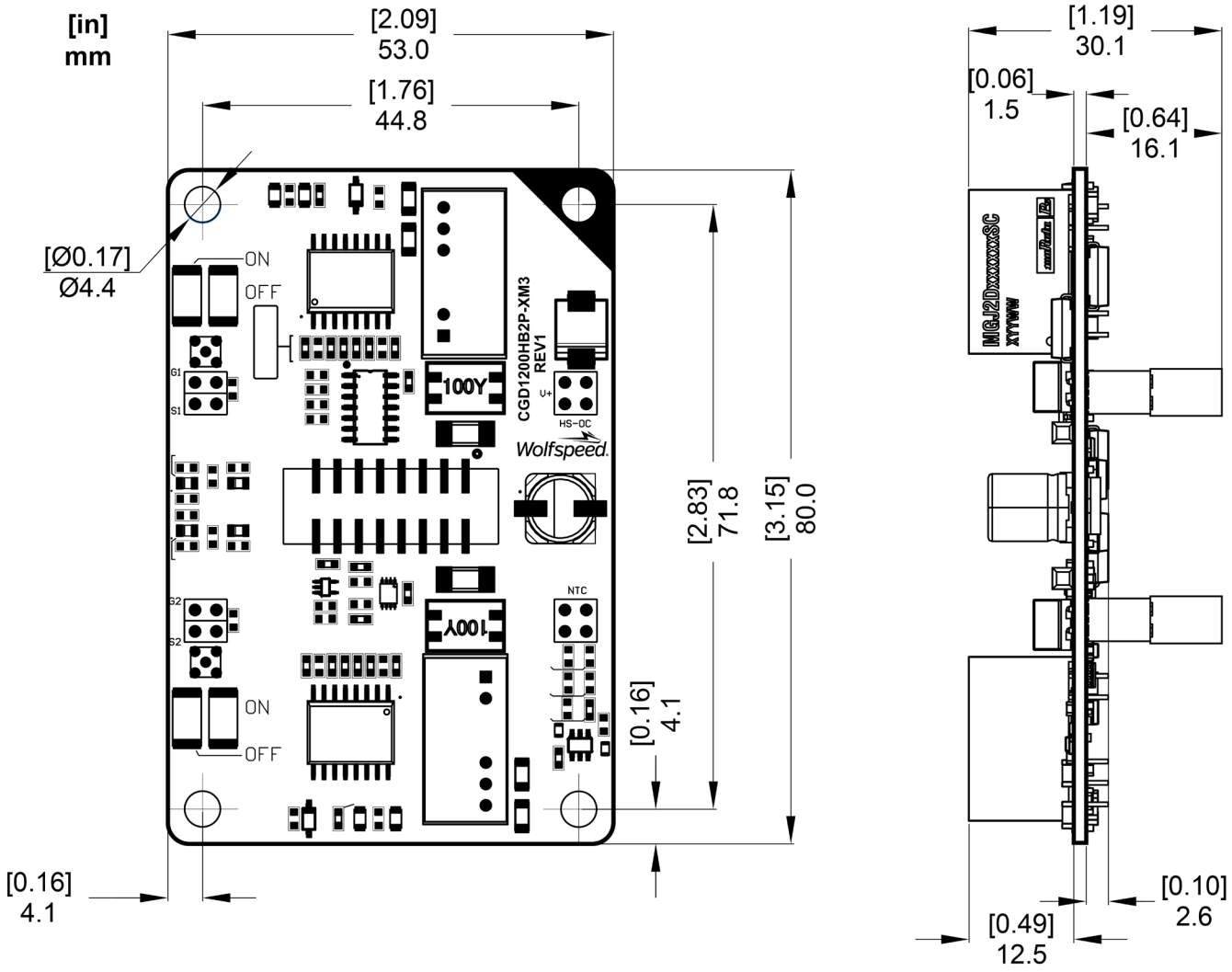

Figure 27: Dimensions of the CGD1200HB2P-XM3 gate driver

6. Supporting Links and Tools

The following links provide additional information about gate drivers, XM power modules, and design tools for using power modules. Please navigate to the landing page for this design for additional links and support.

6.1 Evaluation Tools and Support

- XM Module Product Family
- KIT-CRD-CIL17N-XM: Dynamic Performance Evaluation Board for the XM Modules
- KIT-CRD-CIL12N-XM3: Evaluation Tool for the XM3 Module Platform
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum
- All Wolfspeed Gate Drivers

6.2 Dual Channel Gate Driver Board

- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

6.3 Application Notes

- PRD-07128: XM Module Signal Pinout Clarification Guide
- PRD-09301: Gate Driver Design for SiC Power Modules
- PRD-04814: Design Options for Wolfspeed Silicon Carbide MOSFET Gate Bias Power Supplies

Revision History

Date	Revision	Changes
September 2025	1	Initial Release

IMPORTANT NOTES

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