

 $650V~15m\Omega~VGS~Optimized~Silicon~Carbide~Power~MOSFET~N-Channel~Enhancement~Mode$

Features

- Industry compatible drive voltage +15V..18V
- Industry standard Top Side Cooled (TSC) package
- · High power dissipation capability
- · Optimized package with separate driver source pin
- High-speed switching with low capacitances
- Soft body diode to minimize voltage overshoots
- Halogen free, RoHS compliant

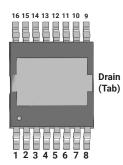
Benefits

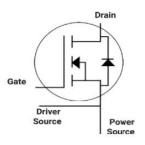
- Compatible with industry standard gate drivers
- Increase power density
- Reduce cooling requirements
- · Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Increase system switching frequency

Applications

- EV Chargers
- Solar/ESS
- Motor Control
- Industrial Power Supplies
- High Voltage DC/DC Converters

Package









Orderable Part Number	Package	Marking		
C4MV015065T-TR	TOLT (TSC)	C4MV015065T		

Key Parameters

Parameter	Symbol	Min.	Тур.	Max	Unit	Conditions	Note
Drain - Source Voltage	V _{DS}			650		T _c = 25°C	
Maximum Gate - Source Voltage	V _{GS}	-10		+23	V		Refer to PRD-04814
	I _D		150		A	V _{GS} = 18 V, T _C = 25 °C, T _J ≤175 °C	Fig 19 Note 1
DC Continuous Drain Current			111			V _{GS} = 18 V, T _C = 100 °C, T _J ≤175 °C	
Pulsed Drain Current	I _{DM}			390		t_{Pmax} limited by T_{jmax} $V_{GS} = 18V, T_{C} = 25 ^{\circ}C$	Fig 22
Power Dissipation	P _D		714		W	$T_c = 25 ^{\circ} ^{\circ} C, T_J = 175 ^{\circ} ^{\circ} C$	Fig 20
Operating Junction and Storage Temperature	T _J , T _{stg}	-55		175			
Solder Temperature	T _L			260	°C	According to JEDEC J-STD-020	

Note (1): Verified by Design

Electrical Characteristics (T_c = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650				V _{GS} = 0 V, I _D = 100 μA	
V	0 . T	1.8	2.6	3.8	V	V _{DS} = V _{GS} , I _D = 15.32 mA	Fig. 11
$V_{GS(th)}$	Gate Threshold Voltage		2.2			$V_{DS} = V_{GS}$, $I_D = 15.32$ mA, $T_J = 175$ °C	
I _{DSS}	Zero Gate Voltage Drain Current		1	50	μΑ	V _{DS} = 650 V, V _{GS} = 0 V	
I _{GSS}	Gate-Source Leakage Current		10	250	nA	V _{GS} = 18 V, V _{DS} = 0 V	
V	Recommended Turn On Gate-Source Voltage		+15+18				Refer to
$V_{GS (op)}$	Recommended Turn Off Gate-Source Voltage		-50		V		PRD- 09634
			15	21		V _{GS} = 18 V, I _D = 55.72 A	Fig. 4,
$R_{\text{DS(on)}}$	Drain-Source On-State Resistance		27		mΩ	V _{GS} = 18 V, I _D = 55.72 A, T _J = 175°C	5, 6
			18			V _{GS} = 15 V, I _D = 55.72 A	
a			42		S	V _{DS} = 20 V, I _{DS} = 55.72 A	Fig. 7
G fs	Transconductance		39		3	V _{DS} = 20 V, I _{DS} = 55.72 A, T _J = 175°C	
C _{iss}	Input Capacitance		4488		_		
C_{oss}	Output Capacitance		277		pF	$V_{GS} = 0 \text{ V, } V_{DS} = 0 \text{V to } 400 \text{ V}$ $f = 100 \text{ kHz}$ $V_{AC} = 25 \text{ mV}$	Fig. 17, 18
C_{rss}	Reverse Transfer Capacitance		24				
E _{oss}	C _{oss} Stored Energy		28		μJ		Fig. 16
C _{o(er)}	Effective Output Capacitance (Energy Related)		362				
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		517		pF	$V_{GS} = 0 \text{ V, } V_{DS} = 0 400 \text{V}$	Note: 3
Eon	Turn-On Switching Energy (Diode FWD)		110			V_{DS} = 400 V, V_{GS} = -4 V/18 V, I_{D} = 55.72 A,	
E _{OFF}	Turn-Off Switching Energy (Diode FWD)		66		μJ	$R_{G(ext)} = 2.5 \Omega$, L= 59 μ H, $T_J = 175$ °C FWD = Internal Body Diode	
t _{d(on)}	Turn-On Delay Time		16			,	
t _r	Rise Time		7		1	$V_{DD} = 400 \text{ V}, V_{GS} = -4 \text{ V}/18 \text{ V}$ $I_D = 55.72 \text{ A}, R_{G(ext)} = 2.5 \Omega,$	
t _{d(off)}	Turn-Off Delay Time		41		ns	Timing relative to V _{DS}	
t _f	Fall Time		10]	Inductive load	
R _{G(int)}	Internal Gate Resistance		1.5		Ω	f = 1 MHz	
Q_{gs}	Gate to Source Charge		46			V _{DS} = 400 V, V _{GS} = -4 V/18 V	
Q_{gd}	Gate to Drain Charge		48		nC	$V_{DS} = 400 \text{ V}, V_{GS} = -4 \text{ V}/18 \text{ V}$ $I_{D} = 55.72 \text{ A}$	Fig. 12
Qg	Total Gate Charge		178			Per IEC60747-8-4 pg 21	

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 400V $C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 400V

3

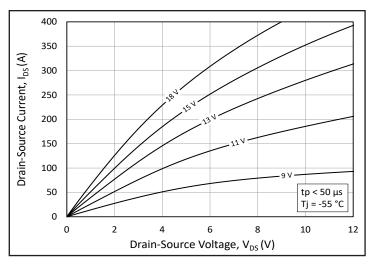
Reverse Diode Characteristics ($T_c = 25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Тур.	Max.	Unit	Test Conditions	Note
.,	Diode Forward Voltage	4.9		V	$V_{GS} = -4 \text{ V, } I_{SD} = 27.9 \text{ A, } T_{J} = 25 \text{ °C}$	Fig. 8.
$V_{ ext{SD}}$		4.4			$V_{GS} = -4 \text{ V, } I_{SD} = 27.9 \text{ A, } T_{J} = 175 ^{\circ}\text{C}$	Fig. 8, 9, 10
Is	Continuous Diode Forward Current		100		$V_{GS} = -4 \text{ V, } T_{C} = 25^{\circ}\text{C}$	
I _{SM}	Diode pulse Current		390	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t _{rr}	Reverse Recovery time	14		ns		
Q _{rr}	Reverse Recovery Charge	934		nC	$V_{GS} = -4 \text{ V, } I_{SD} = 55.72 \text{ A, } V_{R} = 400 \text{ V}$ dif/dt = 11638 A/µs, $T_{J} = 175 ^{\circ}\text{C}$	
I _{rrm}	Peak Reverse Recovery Current	106		А		
t _{rr}	Reverse Recovery time	48		ns		
Q _{rr}	Reverse Recovery Charge	327		nC	V _{GS} = -4 V, I _{SD} = 55.72 A, V _R = 400 V dif/dt = 2115 A/µs, T _r = 175 °C	
I	Peak Reverse Recovery Current	23		Α Διιγαί Στιονίγρο, τη το σ		

Thermal Characteristics

Symbol	Parameter	Тур.	Unit	Test Conditions	Note
R _{eJC}	Thermal Resistance from Junction to Case	0.21	°C/W		Fig. 21

Typical Performance



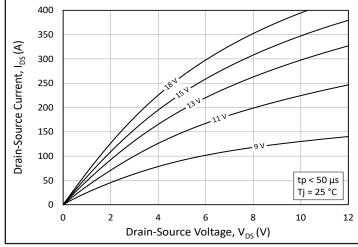
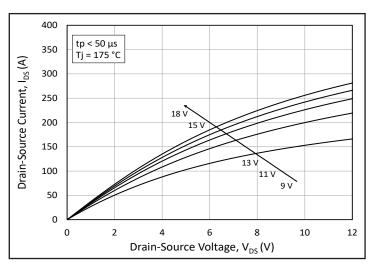


Figure 1. Output Characteristics T_J = -55 °C





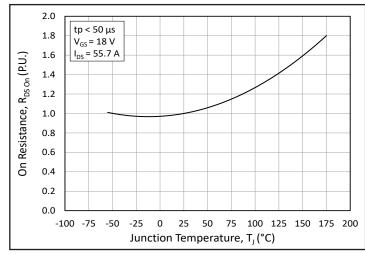
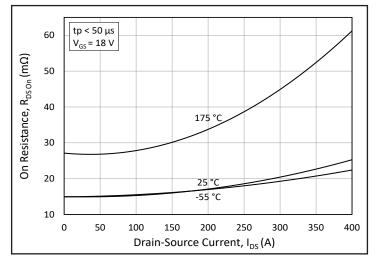


Figure 3. Output Characteristics T_J = 175 °C

Figure 4. Normalized On-Resistance vs. Temperature



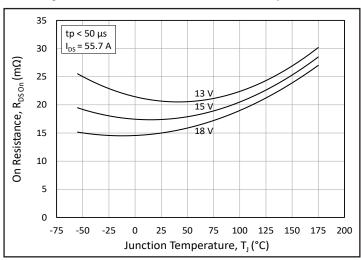


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

Typical Performance

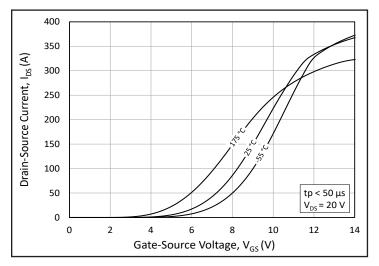


Figure 7. Transfer Characteristic for Various Junction Temperatures

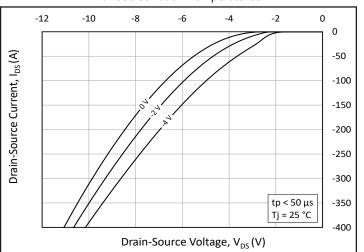


Figure 9. Body Diode Characteristic at 25 °C

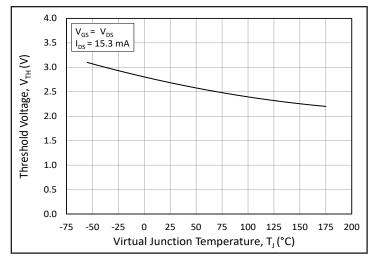


Figure 11. Threshold Voltage vs. Temperature

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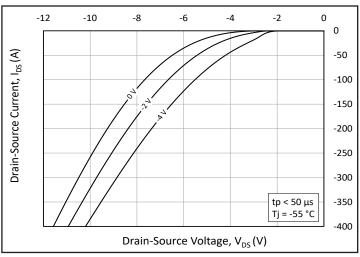


Figure 8. Body Diode Characteristic at -55 °C

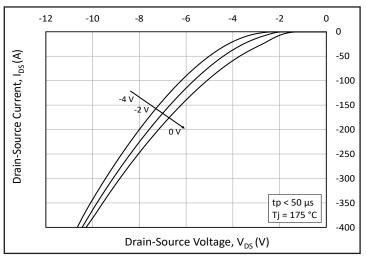


Figure 10. Body Diode Characteristic at 175 °C

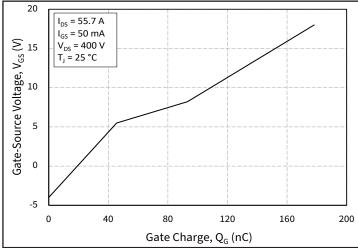


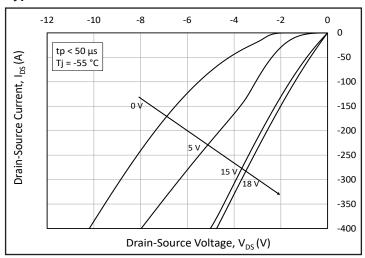
Figure 12. Gate Charge Characteristics

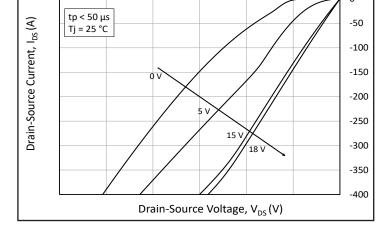
-12

-10

-8

Typical Performance





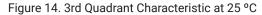
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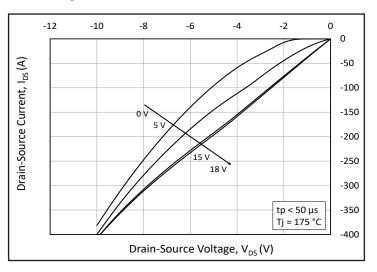
-4

-2

0

Figure 13. 3rd Quadrant Characteristic at -55 °C





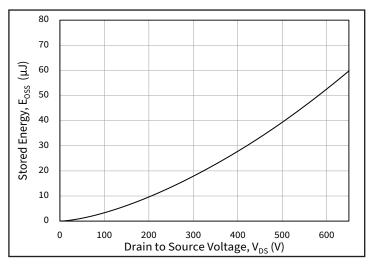
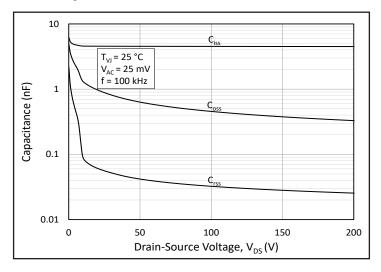


Figure 15. 3rd Quadrant Characteristic at 175 °C

Figure 16. Output Capacitor Stored Energy



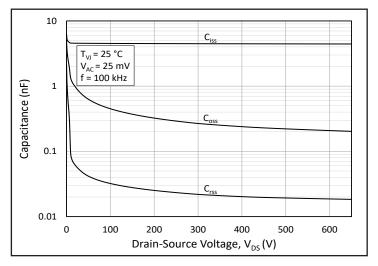


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

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Typical Performance

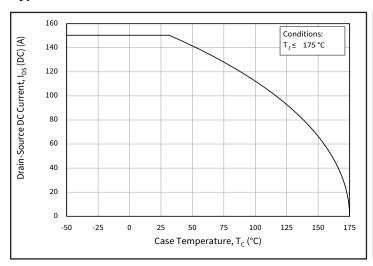


Figure 19. Continuous Drain Current Derating vs.

Case Temperature

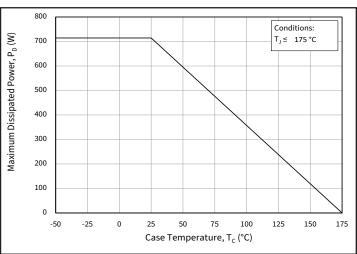


Figure 20. Maximum Power Dissipation Derating vs.

Case Temperature

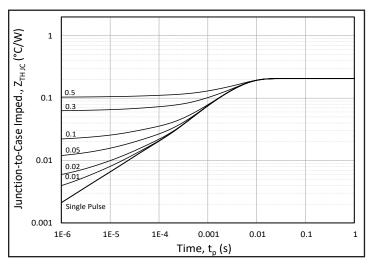


Figure 21. Transient Thermal Impedance (Junction - Case)

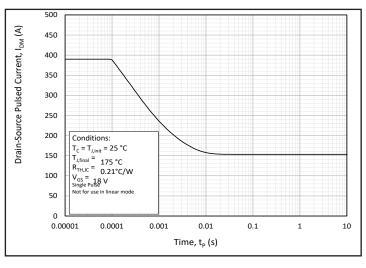


Figure 22. Safe Operating Area

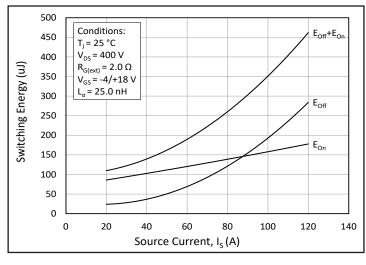


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 400V)

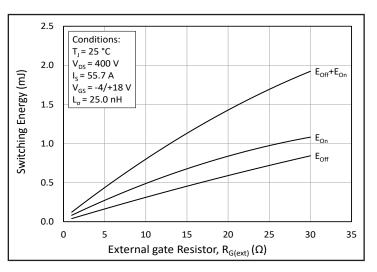


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

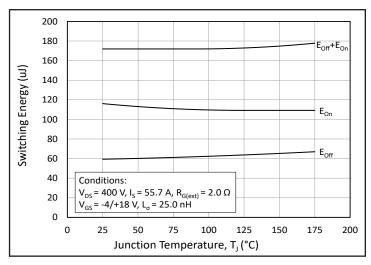


Figure 25. Clamped Inductive Switching Energy vs.
Temperature

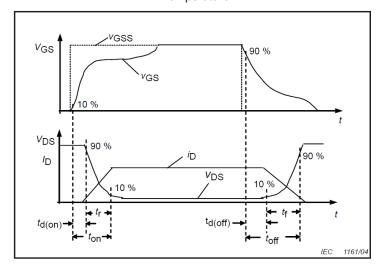


Figure 27. Switching Times Definition

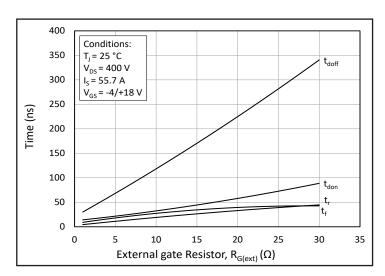


Figure 26. Switching Times vs. $R_{G(ext)}$

Test Circuit Schematic

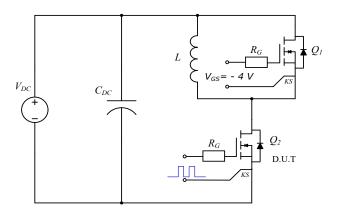
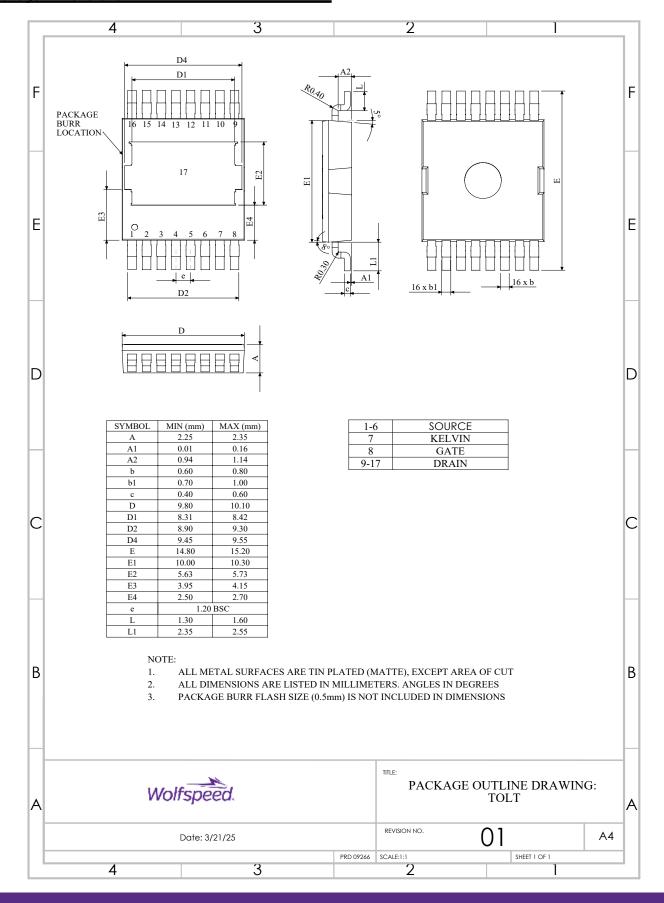


Figure 28. Clamped Inductive Switching Waveform Test Circuit

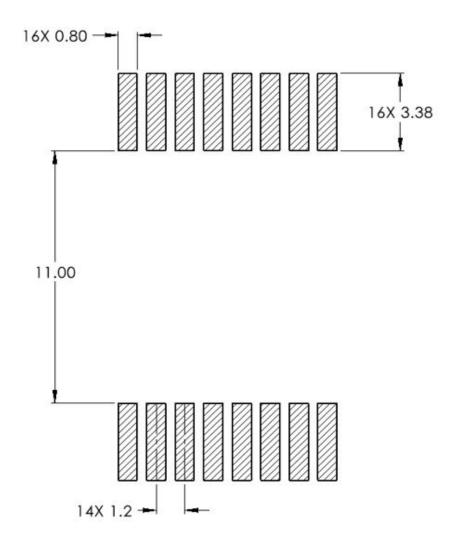
Package Dimensions



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Recommended Solder Pad Lavout

All dimensions in mm



Revision history

Document Version	Date of release	Descriptiion of changes
1	November 2025	Initial release

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4600 Silicon Drive Durham, NC 27703 USA Tel: +1.919.313.5300 www.wolfspeed.com/power

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