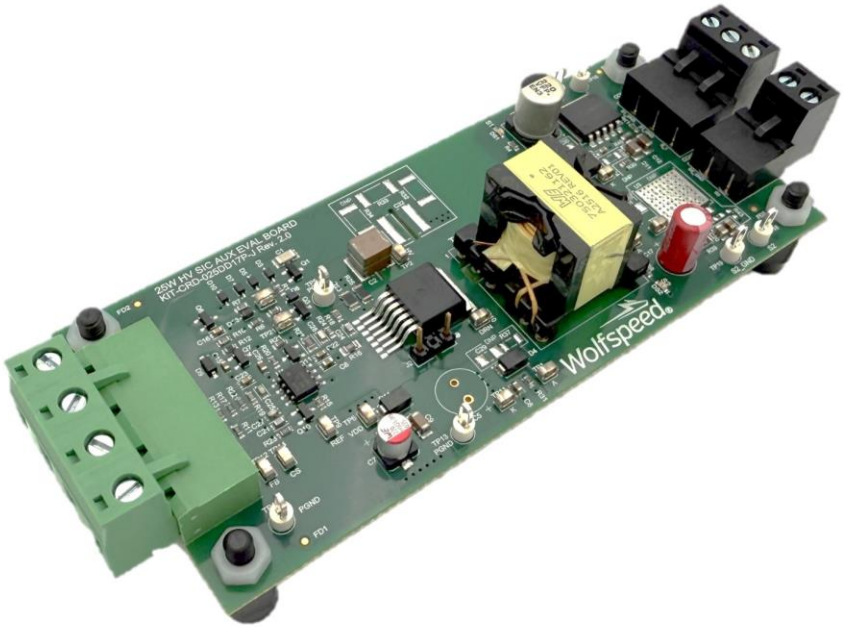
User Guide PRD-09375

KIT-CRD-025DD17P-J: 25W Auxiliary Power Flyback Evaluation Platform User Guide



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KIT-CRD-025DD17P-J: 25W Auxiliary Power Flyback Evaluation Platform User Guide

The KIT-CRD-025DD17P-J evaluation platform demonstrates the use of 1700V silicon carbide (SiC) MOSFETs in a single-switch flyback configuration and provides a flexible design that can be used to evaluate and optimize the performance of the flyback converter, SiC MOSFET, and transformer. The C3M00900170x MOSFET family utilized in this design has a wide operating gate-source voltage (Vgs) range of 12-18V, making it an easy and low-cost drop-in compatible with existing Si or SiC single-switch designs. This primary-side-regulated converter (with an auxiliary winding) eliminates the need for an opto-coupler and provides a space- and cost-optimized solution for industrial applications like solar inverters, electric vehicle charging, motor drive and HVAC applications, etc. This user guide provides an overview of KIT-CRD-025DD17P-J including key system specifications, schematics, hardware setup, and test results.

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This document is prepared as a user guide to install and operate Wolfspeed evaluation hardware.

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- Death
- Serious injury
- Electrocution
- Electrical shock
- Electrical burns
- Severe heat burns

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- 电击
- 电灼伤
- 严重的热烧伤

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1. Introduction

The KIT-CRD-025DD17P-J platform offers a flexible and efficient solution for engineers aiming to evaluate and optimize flyback converters, SiC MOSFETs, transformers, and related components. It operates from 60VDC-1000VDC input voltage, accommodating a broad spectrum of high-voltage applications like solar inverters, electric vehicle charging, motor drives, heat pumps and air conditioning, and other energy storage systems. It has a typical regulated output of around 15V up to 25W. It also provides the user with an option to add and utilize a second secondary output.

The single-switch flyback topology shown in Figure 1 and utilized in this KIT is a primary-side-regulated converter that eliminates the need for an opto-coupler and provides a space- and cost-optimized solution. This KIT is flexible, providing the user with ample test points, an option to add and second secondary isolated output, footprints to test different clamp circuit options like the RCD or the ZD clamp, and footprints for optimizing snubber components.

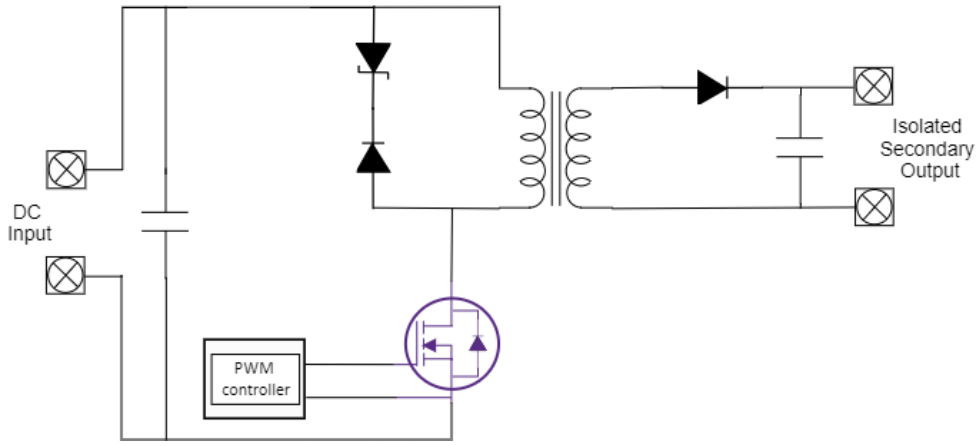

Figure 1: Single-Switch Flyback Topology

2. Description

2.1 Key Electrical Specifications

Parameter	Test Condition	Min.	Typ.	Max.	Unit
Input Voltage		60	-	1000	V
Output Voltage	No load, Vin= 1000V	-	15.1	-	V
	50% load, Vin= 1000V	-	15	-	V
	100% load, Vin= 1000V	-	14.7	-	V
Maximum Output Current	60V<Vin<100V	-	1.2*	-	A
	100V<Vin<300V	-	1.5*	-	

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	300<Vin<1000V	-	1.67*	-	A
Maximum Output Power	300<Vin<1000V	-	-	25*	W
Load Regulation		-2	-	+1	%
Switching Frequency	V_{in} = 800V, I_{out} = 1.67A	-	42.5	-	kHz
Peak Efficiency	Vin= 400V, I_{out} = 1.67A		81.5		%
Full-Load Efficiency	Vin= 1000V, I_{out} = 1.67A		75.4		%
*Output power is limited by the thermals of the system. The KIT is tested at an ambient temperature of 25^{0}C. Consider appropriate derating if KIT operated at higher ambient temperatures.					

2.2 Board and Connectors Overview

Figure 2 shows the board dimensions. The board stand-offs and external input and output female connectors are not included as a part of the dimensions.

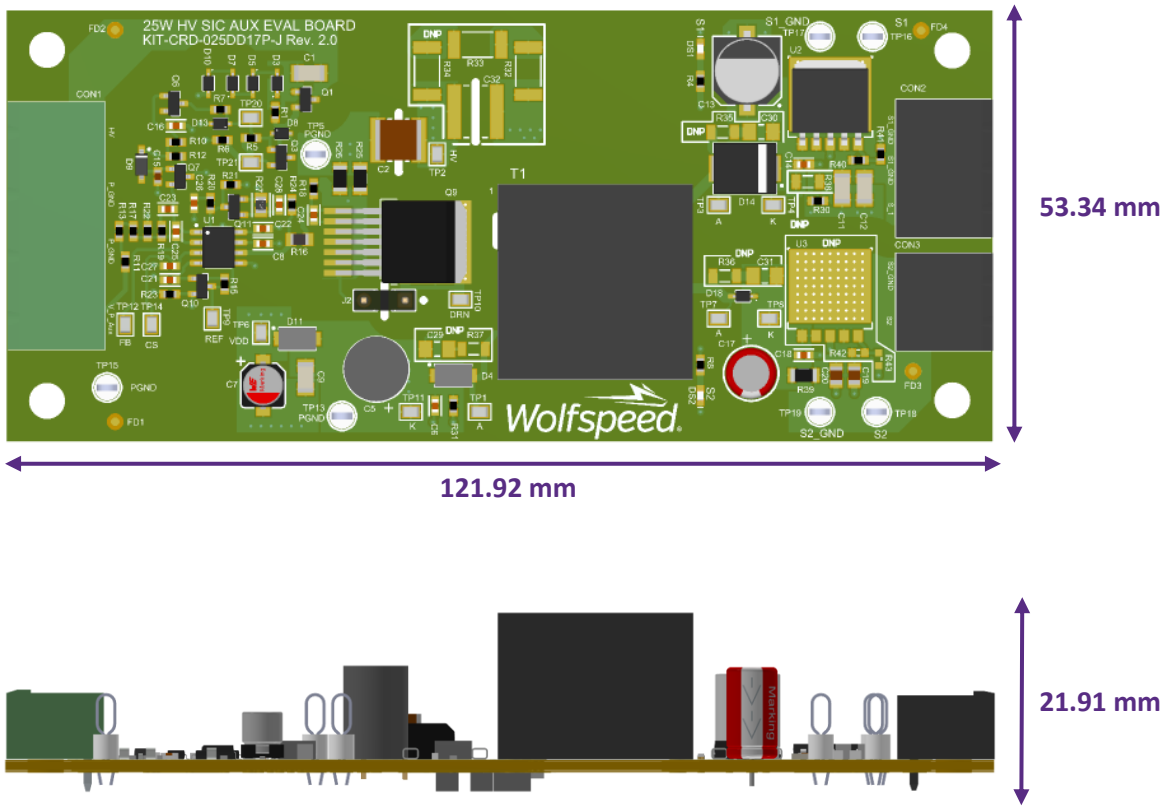

Figure 2: KIT-CRD-025DD17P-J Product Dimensions: Top view (top) and Front View (bottom)

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Table 1 and figure 3 overview the main components of the KIT.

Item	Description
1	Input High-Voltage and Primary Auxiliary Voltage Connector
2	High-Voltage Start-up for VDD
3	PWM Controller and Control Circuit
4	Primary SiC Switch- C3M0900170J
5	Flyback Transformer
6	Main Secondary (1) Output Stage
7	Secondary 1 Voltage Connector
8	Optional Secondary (2) Output Stage
9	Optional Secondary 2 Voltage Connector

Table 1: KIT-CRD-025DD17P-J Board Overview Description

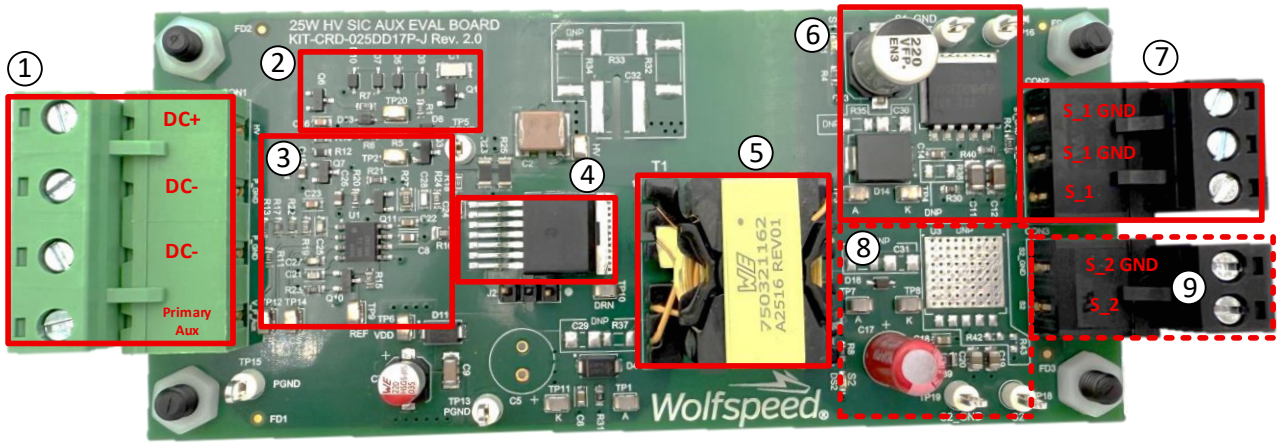

Figure 3: KIT-CRD-025DD17P-J Board Overview

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3. Schematic Diagram

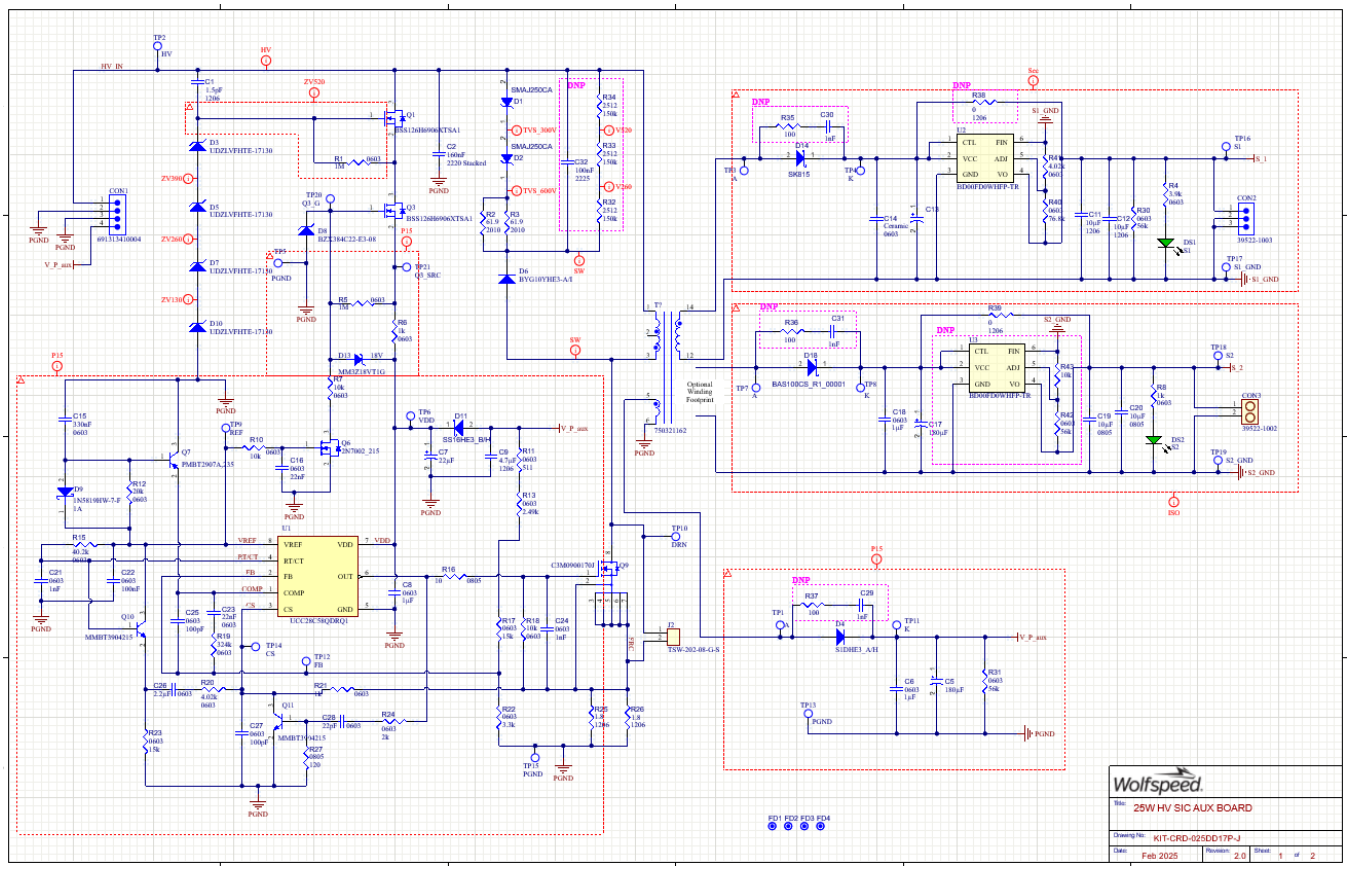

Figure 4: KIT-CRD-025DD17P-J Schematic Diagram

4. Hardware Set-up & Testing

4.1 Hardware Equipment

DC Input Source: The input source must be an adjustable DC source whose output can be adjusted up to the maximum bus voltage desired for testing. It must be capable of supplying at least 2A of current that is needed for start-up.

DC Load: A programmable electronic load or a resistor bank may be used. Both should be capable of supporting at least 20V with 0 to 2A of output current.

Power Meter: A power analyzer from Yokogawa Test and Measurement Corporation (P/N: WT 5000) or any other equivalent power analyzer can be used. The current and voltage measurement range can be set to “Auto”, so it chooses the correct resolution for measuring the low voltage and current output.

Oscilloscope: A 4-channel 500 MHz or greater oscilloscope with HV probes for the input and at least 1 differential voltage probe for the output voltage is recommended.

Thermal Camera: Optional, but useful to monitor the temperature of the KIT.

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4.2 Connection Diagram

CON1 is the input high voltage male connector on the board and CON2 is the low voltage male connector for the main secondary output. KIT-CRD-025DD17P-J comes with the compatible female connectors- H11 and H10 for CON1 and CON2 respectively for a quick connection. These connectors can be used to connect to the input high-voltage supply and output load as shown in figure 5.

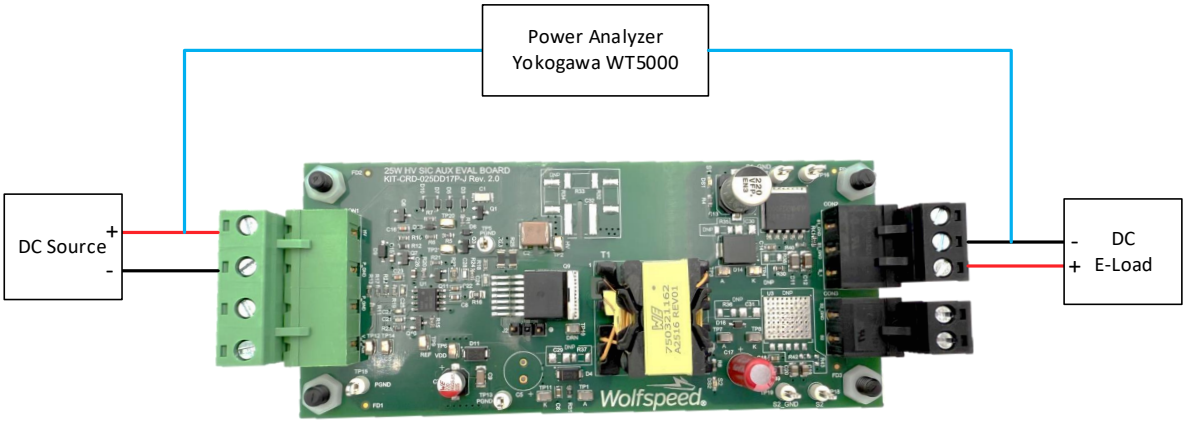

Figure 5: Connection Diagram for testing KIT-CRD-025DD17P-J

4.3 Test Points

Table 2 gives an overview of the test points on KIT-CRD-025DD17P-J.

Designator	Description	Designator	Description
J2	Primary MOSFET Q9 Drain-Source Voltage	**TP10**	DRN- Q9 MOSFET Drain (Switch Node)
TP1	Transformer Auxiliary Winding Output	**TP11**	S2 rectifier output (Optional)
TP2	HV- Input Voltage	**TP12**	FB- Inverting input to the error amplifier
TP3	Transformer S1 Winding Output	**TP14**	CS- Current Sense Pin
TP4	S1 rectifier output	**TP16**	S1- S1 Output Voltage
TP5, TP13, TP15	PGND- Primary Ground	**TP17**	S1_GND- Isolated Ground for S1
TP6	VDD- PWM Controller Bias Supply	**TP18**	S2- S2 Output Voltage (Optional)
TP7	Transformer S2 Winding Output (Optional)	**TP19**	S2_GND- Isolated Ground for S2

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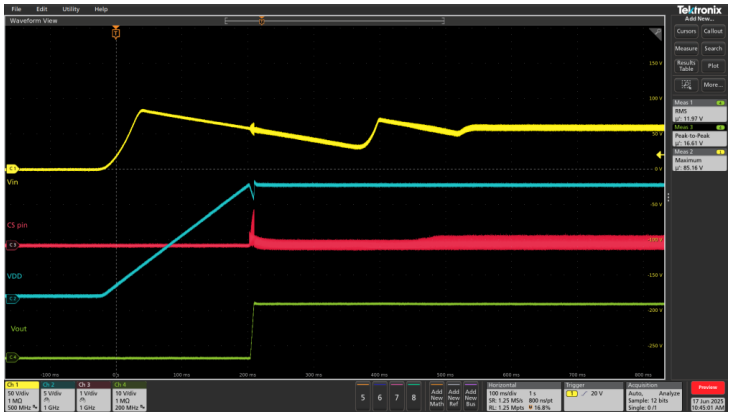
TP8	S2 rectifier output	**TP20**	Start-up MOSFET Q3 gate
TP9	VREF- Controller Reference Output	**TP21**	Start-up MOSFET Q3 source

Table 2: KIT-CRD-025DD17P-J Test Point Description

4.4 Testing the Unit

The steps below for powering on the KIT should be followed in the order in which they are listed:

- Connect the KIT as shown in figure 5. If not using a power analyzer, use digital multimeters with appropriate rating to connect to TP2 (+) and TP5 (-) for input voltage measurement and TP16 (+) and TP17(-) for isolated output voltage measurement.
- Connect a high-voltage probe to measure the input voltage and low-voltage probes to measure the VDD voltage and CS pin voltage.
- Connect a differential probe between S1 and S1_GND to measure the output voltage.
- Set the oscilloscope to single trigger on Vin rising at 30V. Set the time scale to 100ms/div.
- Set the load to 0.1A current.
- Turn-on the input voltage supply at 60V with a 2A current limit for inrush current. The scope should trigger, and the user can observe the waveform that should be like figure 6.



- *Figure 6: Start-up waveform at V_{in}=60V and I_{out} = 0.1A*

- The user can verify some test-point voltages at this time:
  - S1 (V_{out}) ≈ 15.1 V
  - VDD ≈ 16.2 V
  - VREF ≈ 5V
  - FB ≈ 2.5V
- The output current can now be increased to 1.2A. The V_{out} will decrease to approximately 14.95V.
- The above steps can be repeated at 300V input voltage with a 1.5A load current. The V_{out} will approximately be 14.88V.

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- If the above steps go smoothly, the user can proceed to test the KIT at various test conditions listed in the following sections and compare the waveforms to the typical waveforms listed in Section 5.5.

5. Test Results

5.1 Load Regulation

Figure 7 shows the load regulation for KIT-CRD-025DD17P-J at different input voltages. The overall regulation stays within +1% to -2% of 15V output voltage across all load conditions.

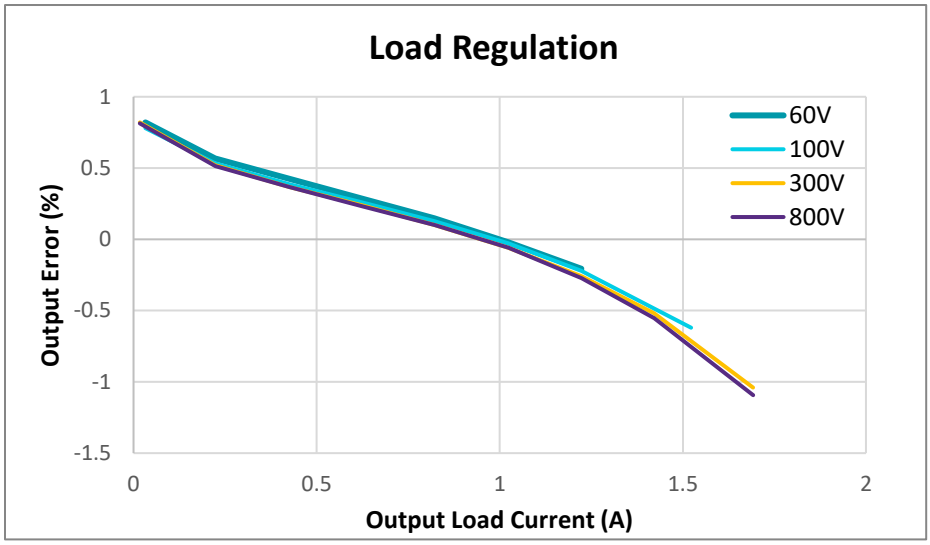

Figure 7: Load Regulation at different Input Voltages

5.2 Line Regulation

Figure 8 shows the line regulation for KIT-CRD-025DD17P-J at different output currents. The overall regulation stays within +1% to -2% of 15V output voltage across the input voltage range.

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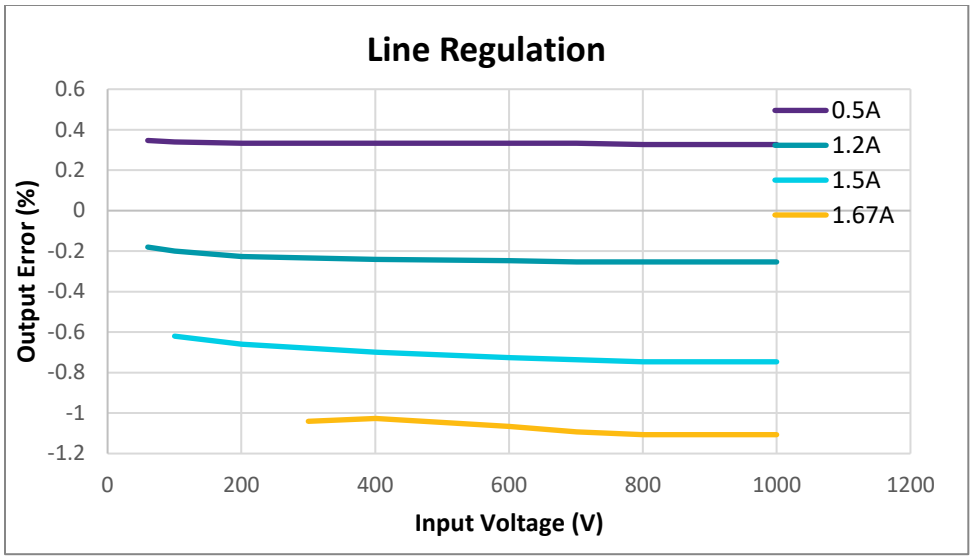

Figure 8: Line Regulation at different Output Currents

5.3 Efficiency

Figure 9 shows the efficiency curves of KIT-CRD-025DD17P-J for different input voltages. The peak efficiency of the design is greater than 80% at 300V input voltage.

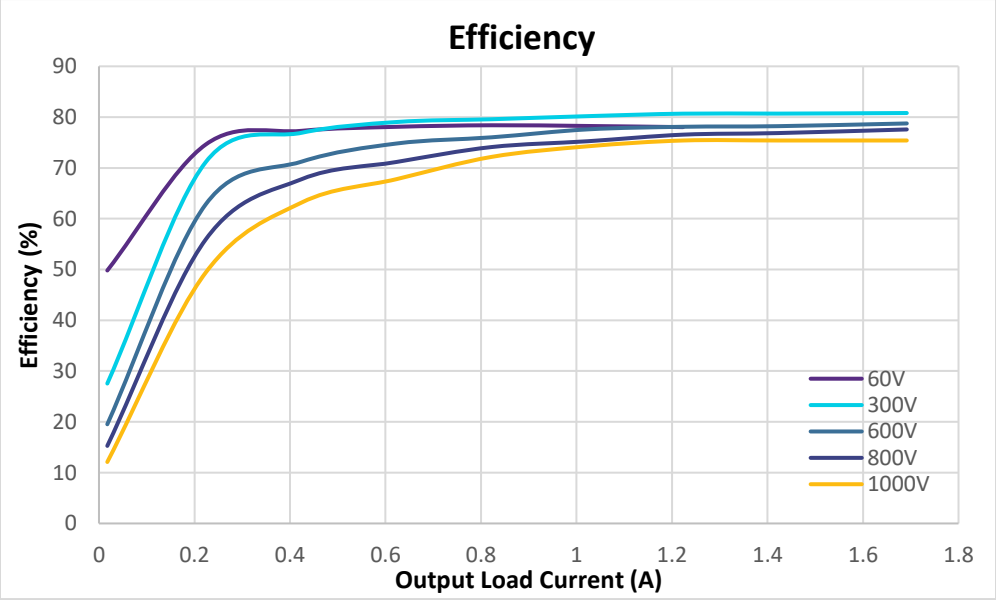

Figure 9: Efficiency vs Output Load Current at Different Input Voltages

5.4 Thermal Performance

KIT-CRD-025DD17P-J was placed in a protective enclosure for this test. This enclosure does not provide any forced air cooling. The thermal measurements were taken using a thermal camera. Figure 10 shows the thermal

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image of KIT-CRD-025DD17P-J at 60V input voltage and 1.2A output current. The temperatures of the primary SiC MOSFET, transformer, and the output stage can be noted from this image. The temperature of the output rectifier is the bottleneck for maximum output power achieved.

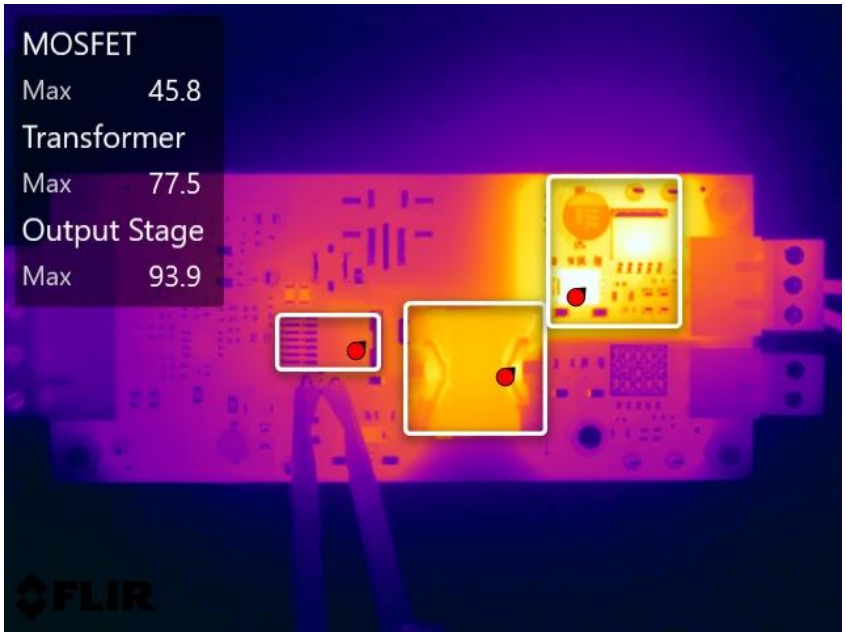

Figure 10: Thermal Image at Steady-Stage V_{in}=60V, I_{out}= 1.2A

Figure 11 shows the worst-case thermals for KIT-CRD-025DD17P-J at 1000V input voltage and 1.67A output current. The temperature of the output rectifier rises to about a 120^{0}C and the transformer is at 95^{0}C.

Figure 11: Thermal Image at Steady-Stage V_{in}=1000V, I_{out}= 1.67A

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Figure 12 shows the temperature plot for the primary SiC MOSFET, transformer, and output rectifier with respect to the output current.

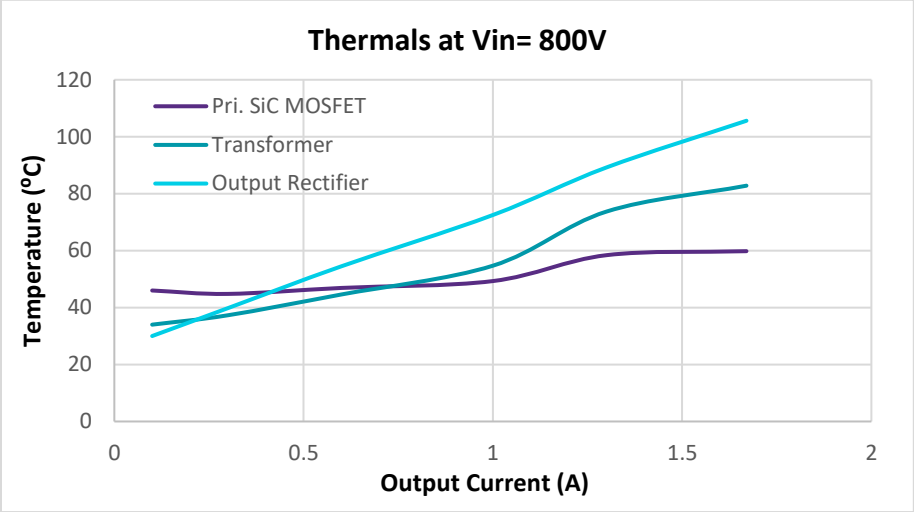
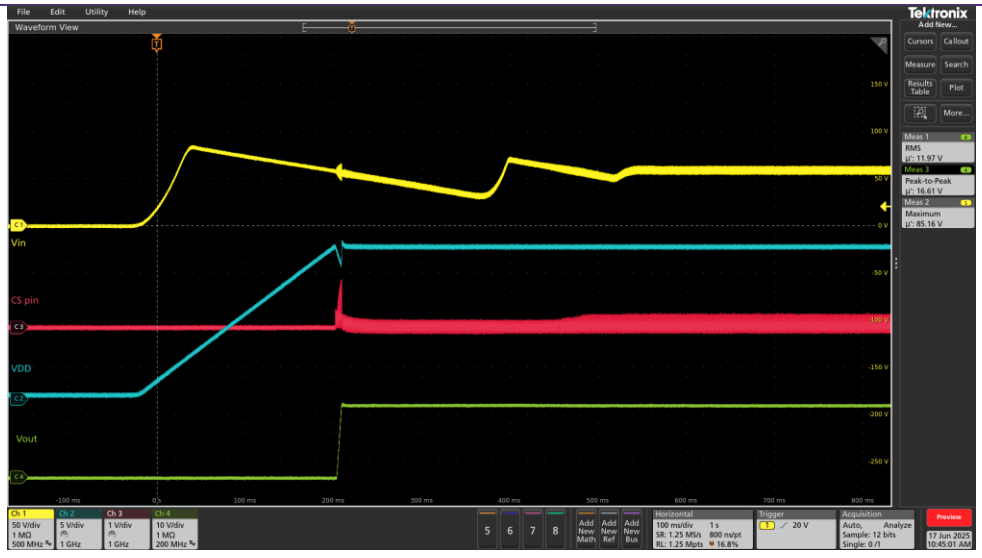


Figure 12: Component Temperature vs Output Current at V_{in} = 800V

Note: The ambient temperature for all testing is 25°C. If the user wishes to operate at higher ambient temperatures, the output power should be derated accordingly.

5.5 Typical Waveforms

Description	Waveform
Start-up Waveforms	
V_{in}= 60V, I_{out}= 0.1A CH1- Input Voltage CH2- VDD CH3- CS pin CH4- Vout	

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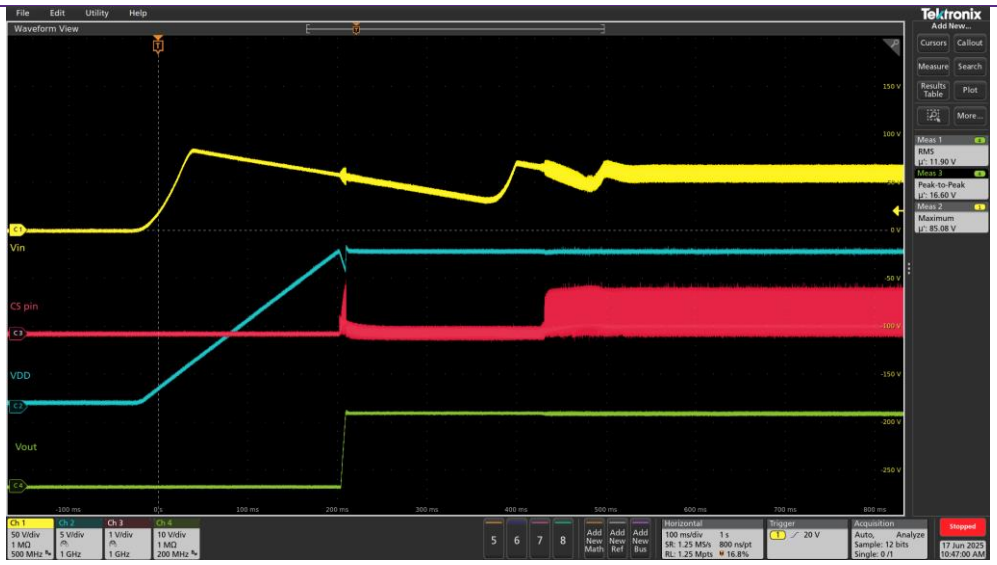
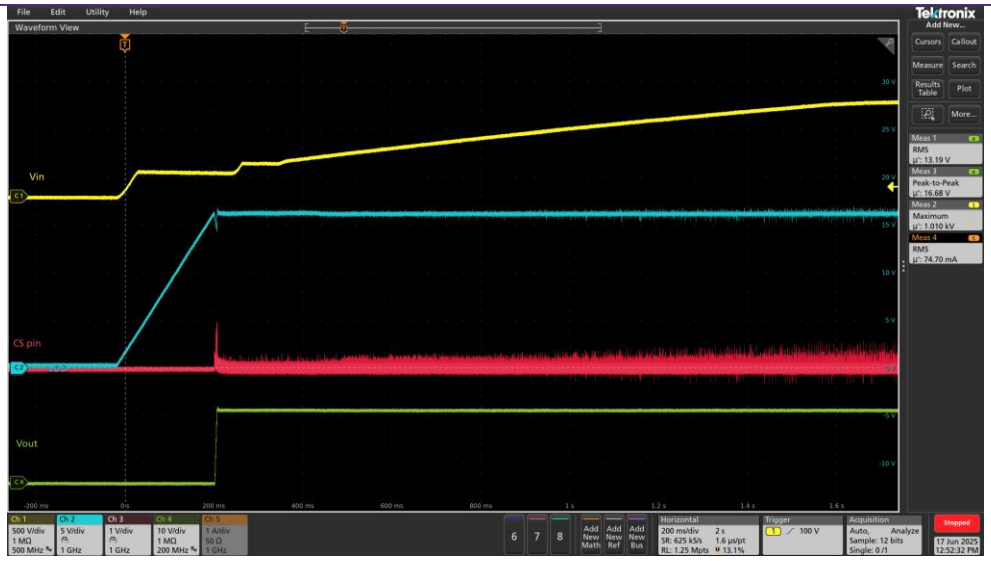
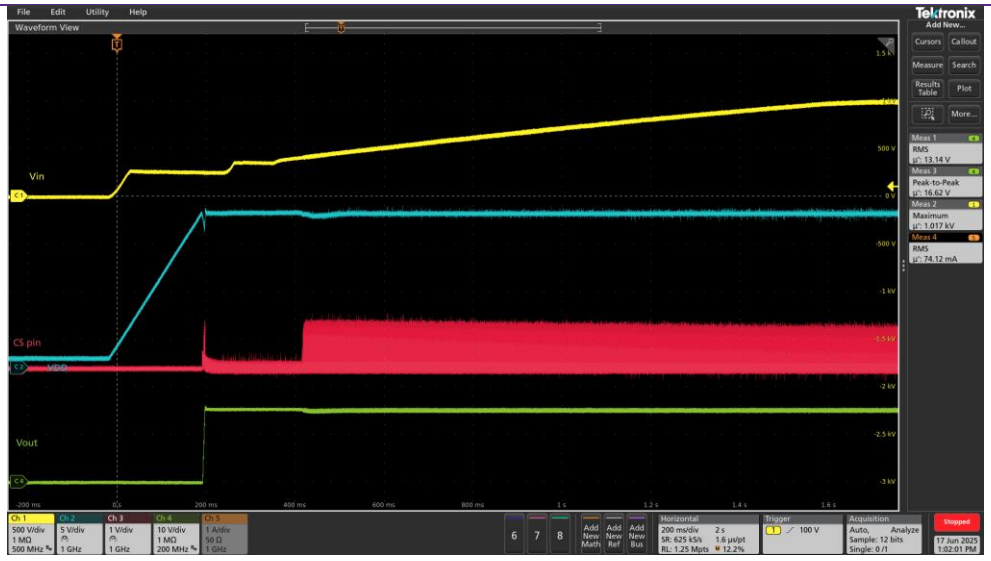
V_{in}= 60V, I_{out}= 1.2A CH1- Input Voltage CH2- VDD CH3- CS pin CH4- Vout	
V_{in}= 1000V, I_{out}= 0.2A CH1- Input Voltage CH2- VDD CH3- CS pin CH4- Vout	
V_{in}= 1000V, I_{out}= 1.67 A CH1- Input Voltage CH2- VDD CH3- CS pin CH4- Vout	

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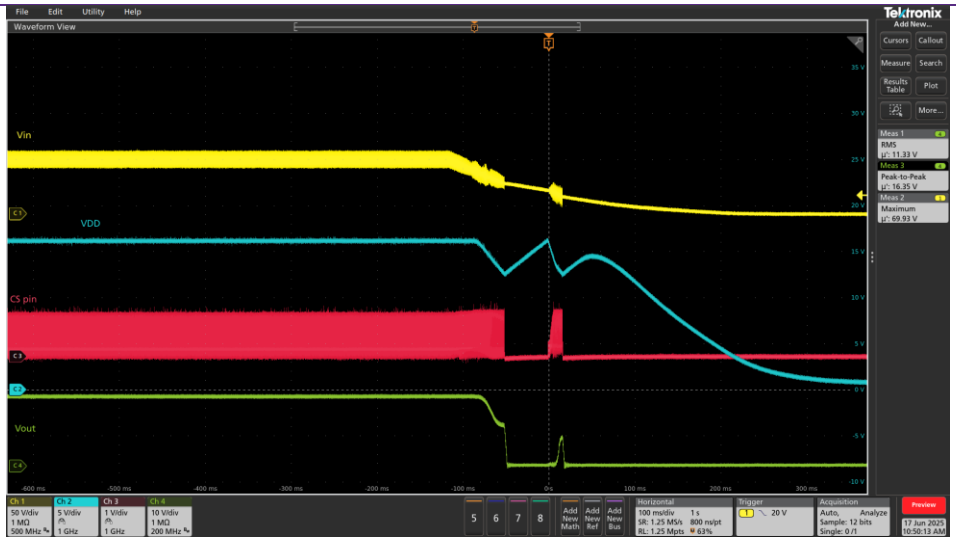
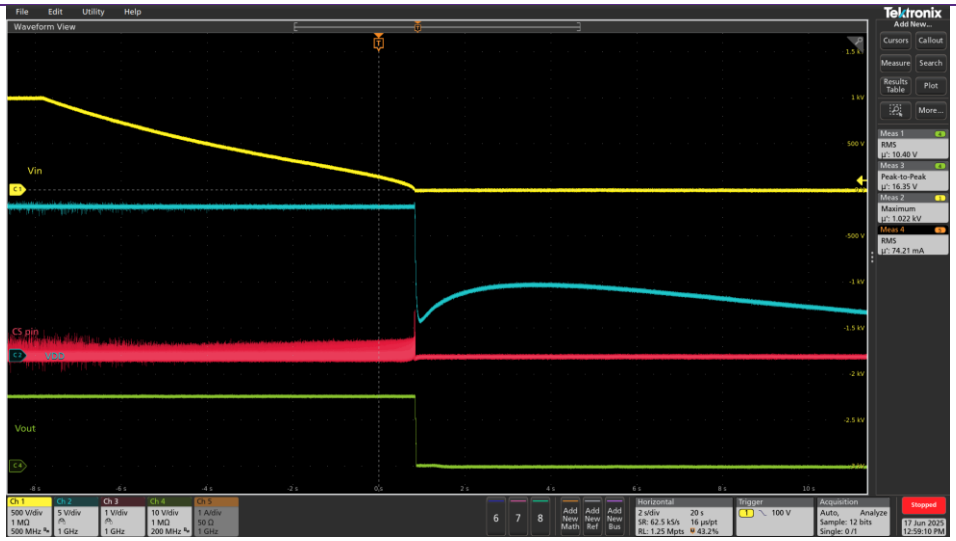
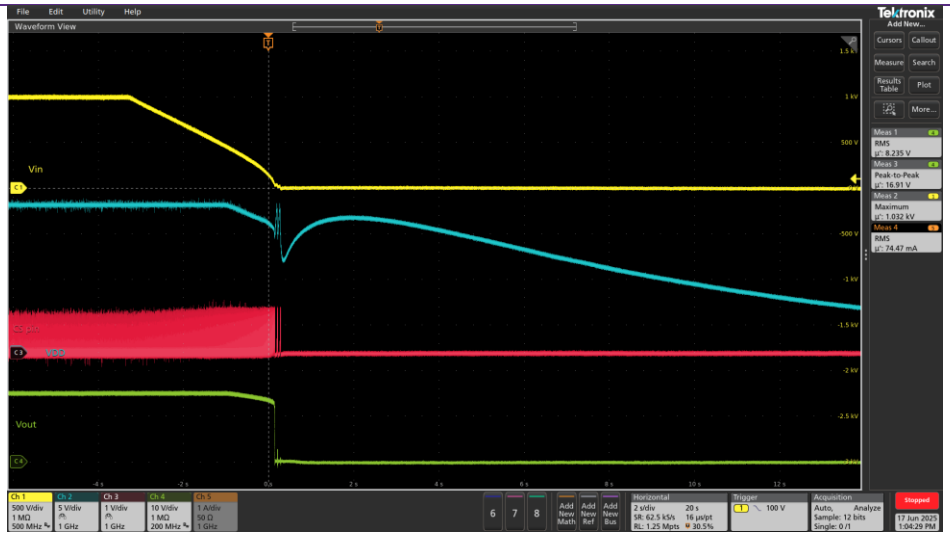
Shut-down Waveforms	
V_{in}= 60V, I_{out}= 1.2A CH1- Input Voltage CH2- VDD CH3- CS pin CH4- Vout	
V_{in}= 1000V, I_{out}= 0.2A CH1- Input Voltage CH2- VDD CH3- CS pin CH4- Vout	
V_{in}= 1000V, I_{out}= 1.67A CH1- Input Voltage CH2- VDD CH3- CS pin CH4- Vout	

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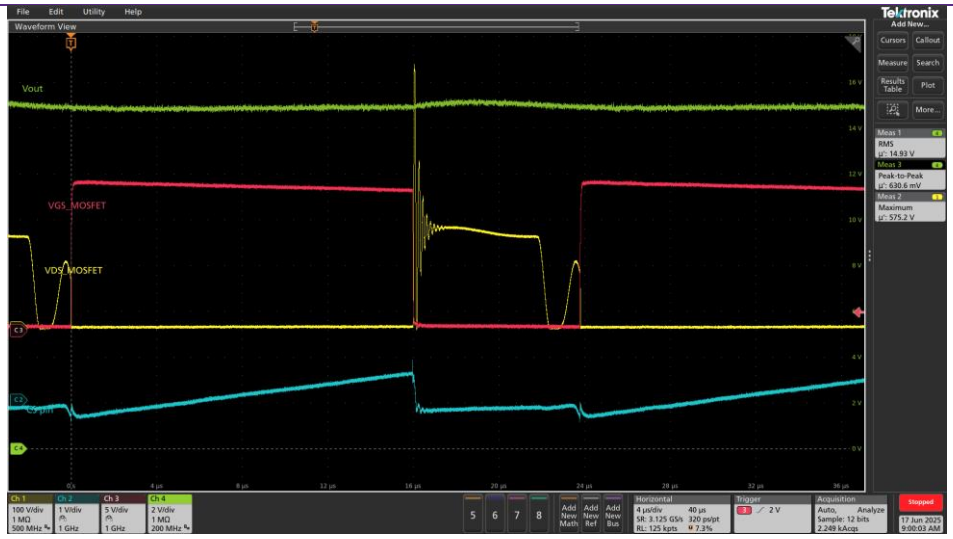
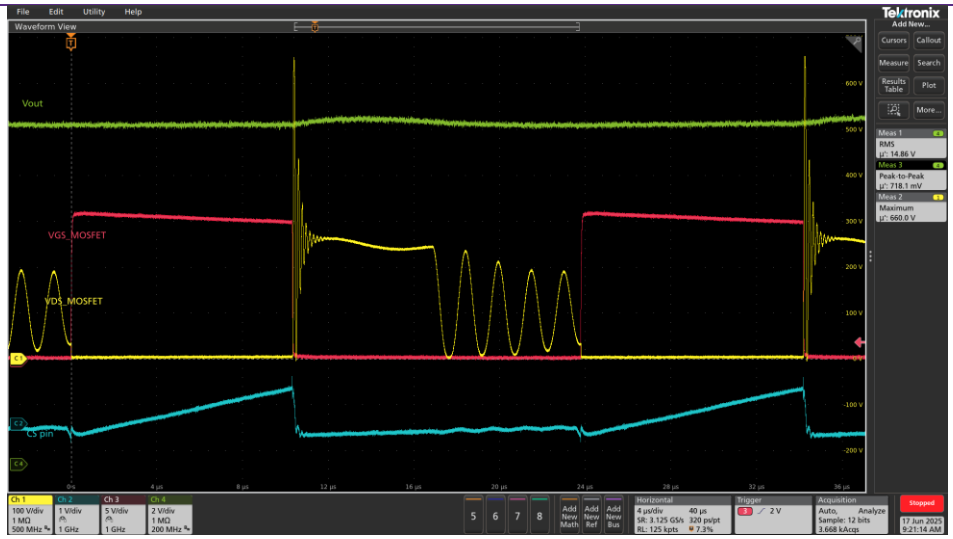
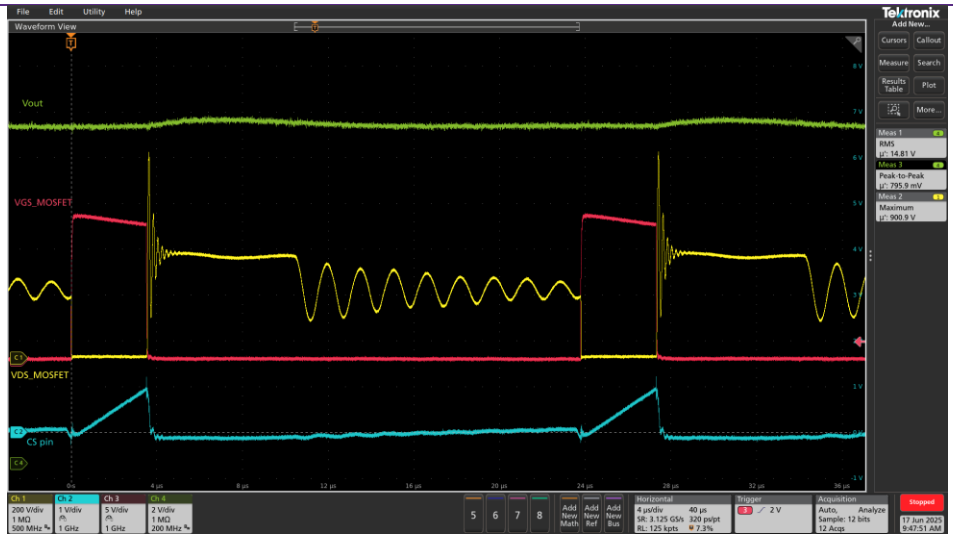
Steady-State Waveforms	
V_{in}= 60V, I_{out}= 1.2A CH1- MOSFET drain-source voltage (SW node) CH2- CS pin CH3- MOSFET gate-source voltage CH4- Vout	
V_{in}= 100V, I_{out}= 1.5A CH1- MOSFET drain-source voltage (SW node) CH2- CS pin CH3- MOSFET gate-source voltage CH4- Vout	
V_{in}= 300V, I_{out}= 1.67A CH1- MOSFET drain-source voltage (SW node) CH2- CS pin CH3- MOSFET gate-source voltage CH4- Vout	

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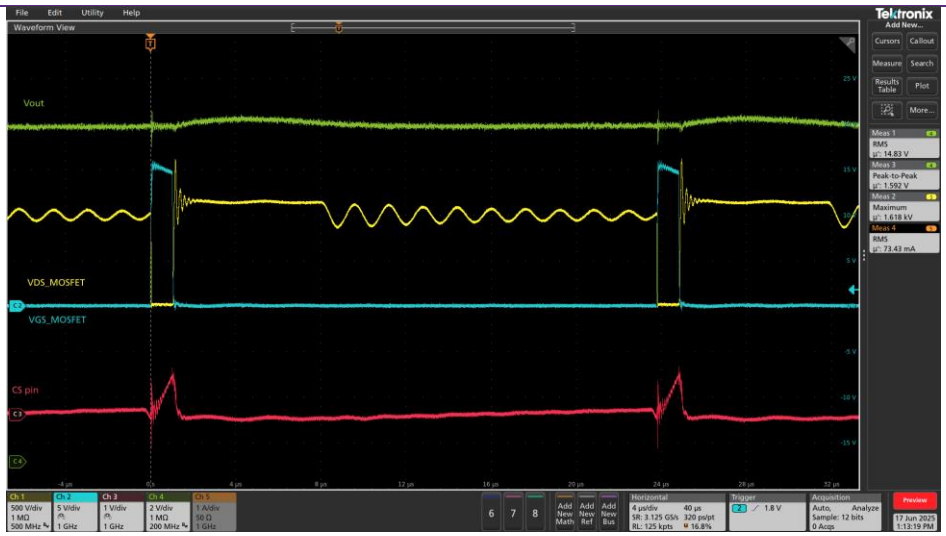
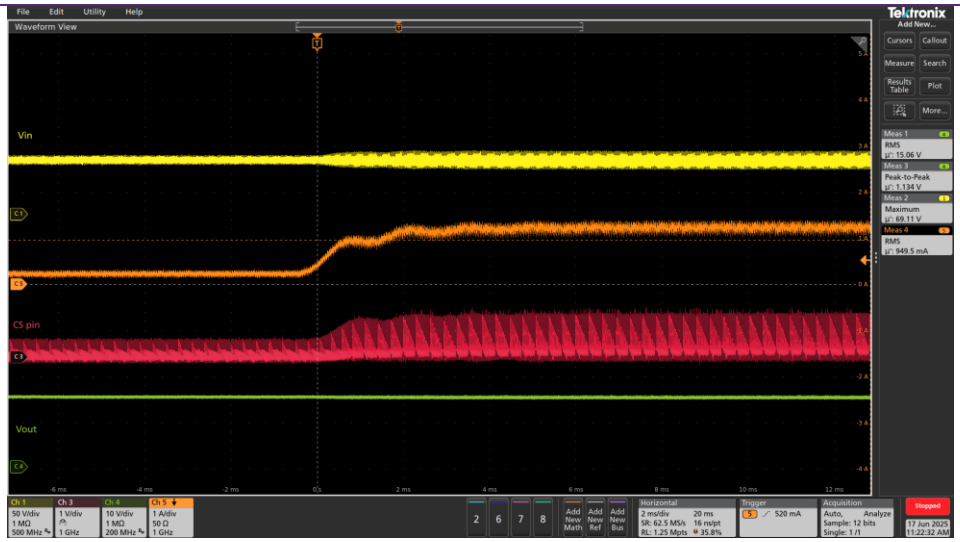
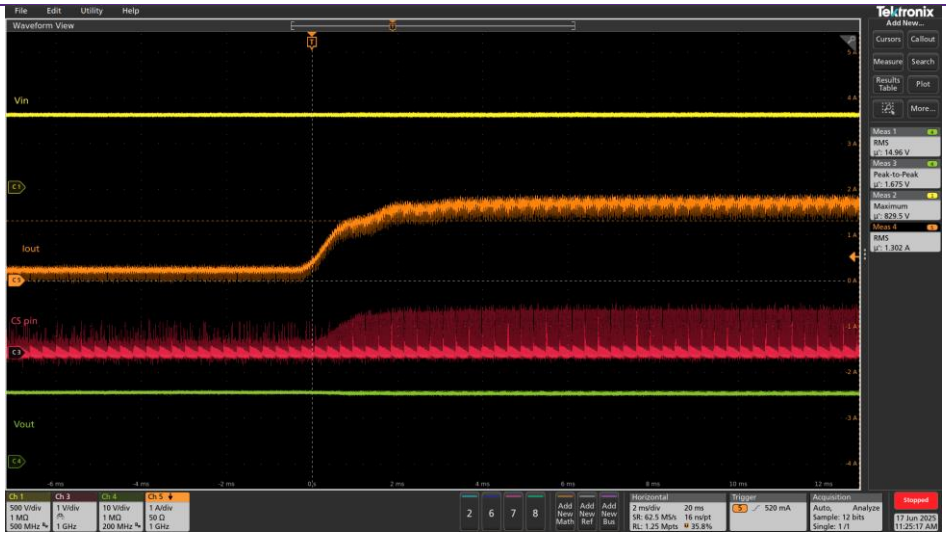
V_{in}= 1000V, I_{out}= 1.67A CH1- MOSFET drain-source voltage (SW node) CH2- CS pin CH3- MOSFET gate-source voltage CH4- Vout	

Transient Waveforms

V_{in}= 60V, I_{out}= 0.2 to 1.2A CH1- Input Voltage CH3- CS pin CH4- Vout CH5- Output Current	
V_{in}= 800V, I_{out}= 0.2 to 1.67A CH1- Input Voltage CH3- CS pin CH4- Vout CH5- Output Current	

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Revision History

Date	Revision	Changes
July 2025	1	Initial Release

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