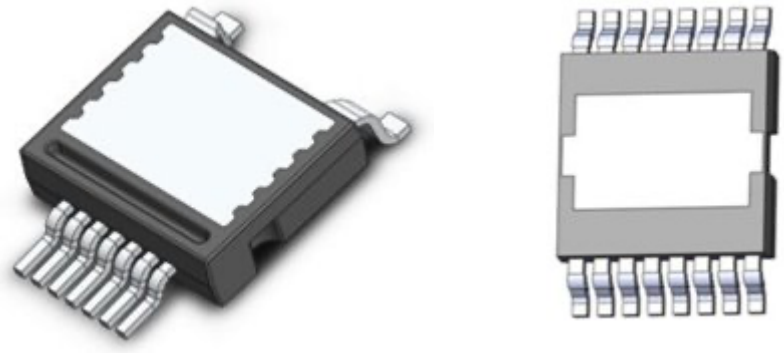
Application Note **PRD-08182**

Designing with Wolfspeed Top Side Cooled Packages



Introduction

The trend of current power electronics systems is towards high efficiency and high power-density designs. Silicon Carbide (SiC) has a unique combination of critical electric field and electron velocity, enabling low on-state resistance at the device level. Compared to its Silicon-based counterpart, SiC MOSFETs have a smaller capacitance and much better recovery on the body diode, resulting in low switching losses. The low on-state resistance and low switching losses provided by Silicon Carbide enables higher power density and higher switching frequencies in a wide variety of power electronics applications. These high-power-density systems impose new challenges towards the thermal management of SiC power devices to optimize device and system level performance.

Traditional through-hole packages such as the TO-247 provide a good thermal performance but are difficult to assemble in an automated environment. Surface mount packages such as the TO-263-7L are easy to assemble with automated assembly equipment but bring on challenges in thermal management. Wolfspeed's top side cooling packages enable high power density and high efficiency by leveraging the advantage of the through-hole package on thermal performance, while also having the advantage of a surface mount package for assembly.

This application note introduces the benefits of top side cooled (TSC) SiC packages along with Wolfspeed's current top side cooling product portfolio. Assembly and thermal measurement of discrete power devices in these packages is also detailed. This application note aims to help users to make their own thermal-mechanical design decisions when using Wolfspeed discrete top side cooled SiC power devices.

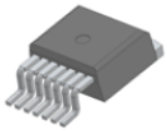
Contents

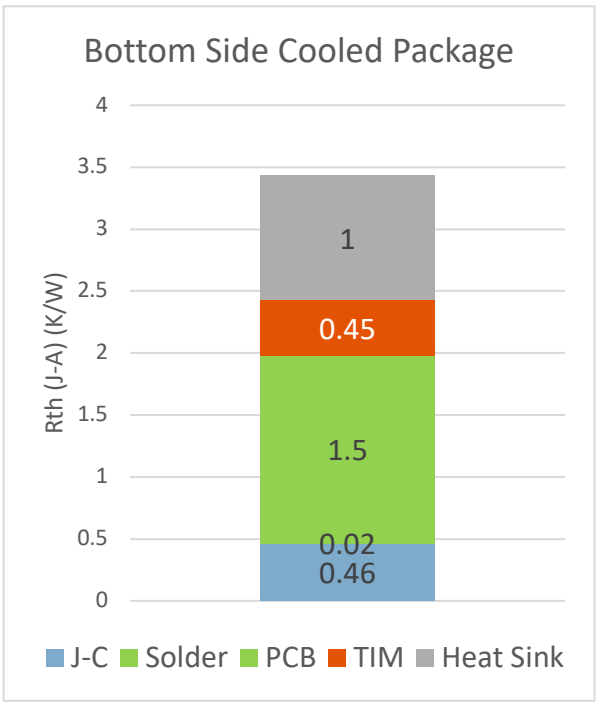
1. Advantages of Top Side Cooling

1.1 Benefits of Top Side Cooling

Most standard surface mount discrete power packages in use today remove heat through the bottom side of the package into the solder joint and PCB board to a shared heat sink where it is then dissipated into the ambient environment. These packages, also known as bottom side cooled (BSC) packages, have been the traditional design of surface mount power packages in recent years along with through hole power packages. With the ever-growing demand for higher power density, cooling of these devices and systems becomes more and more challenging. As more devices with higher power dissipations are added to the same PCB, keeping the overall system cool becomes a difficult task, which then limits system performance. Looking at the thermal resistance (R_θ) network of a system containing BSC packages, one can see that the PCB contributes the highest thermal resistance to the overall system and therefore is a good candidate to attempt to remove from the thermal path to increase system thermal performance. Top side cooling packages do just that, dissipating the heat through the top side of the package instead of the bottom side, which removes the PCB from the thermal path and creates an improved overall system thermal impedance, R_θ. A comparison of the thermal resistance network of BSC and TSC packages with a 1200V 40mO MOSFET device can be seen in

Figure 1 below.





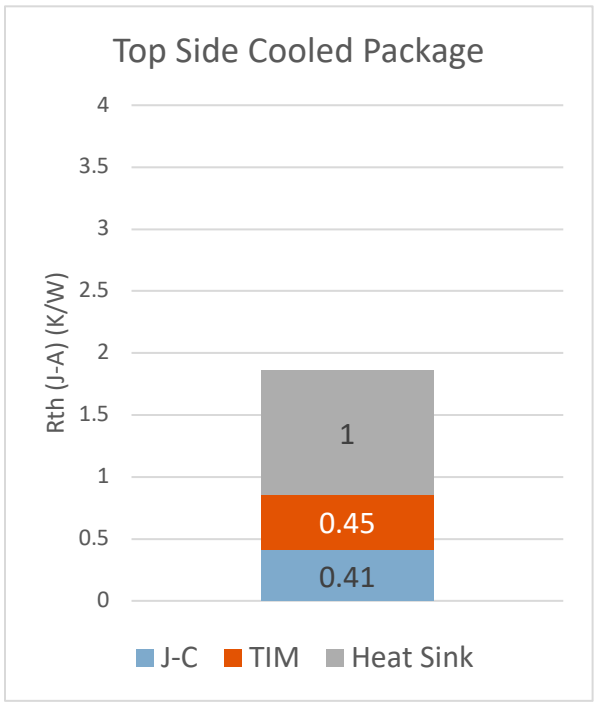


Figure 1: BSC vs. TSC System R_θ Network

Removing the heat through the top side of the package instead of the bottom side provides additional benefits as well, such as higher system power density, improved system size, and higher thermal cycling reliability which will all be detailed further in the following sections.

In addition to the thermal benefits of a TSC package, the PCB layout can be improved. With BSC devices, the area under the drain pad, and sometimes beyond, are filled with thermal vias to conduct heat through the PCB. These vias prevent any other signals or power planes from routing through the area. With TSC devices, it is possible to include other power pours through the region of the board under the device, minimizing power loop inductances. It also provides more flexibility for placing components on the opposite side of the PCB from the device since that surface is no longer needed for the heatsink interface.

1.2 Top Side Cooling Methodology

Top side cooled packages are mounted to the PCB using the same standard SMT process as bottom side cooled packages. To dissipate the heat out of the top of the package instead of the bottom, the lead frame inside the package is flipped 180 degrees such that the die sits upside down in the upper portion of the package, allowing direct heat flow to the top surface. An exposed metal drain pad on the top surface of the package helps to dissipate the generated heat to the heatsink and then eventually to the system surroundings. A thermal interface material (TIM) is required between the package and the heatsink to create a good thermal interface that promotes continuous heat flow and acts as an electrical insulator.

Figure 2 shows a schematic of the general thermal path for a TSC package mounted to a PCB and heatsink.

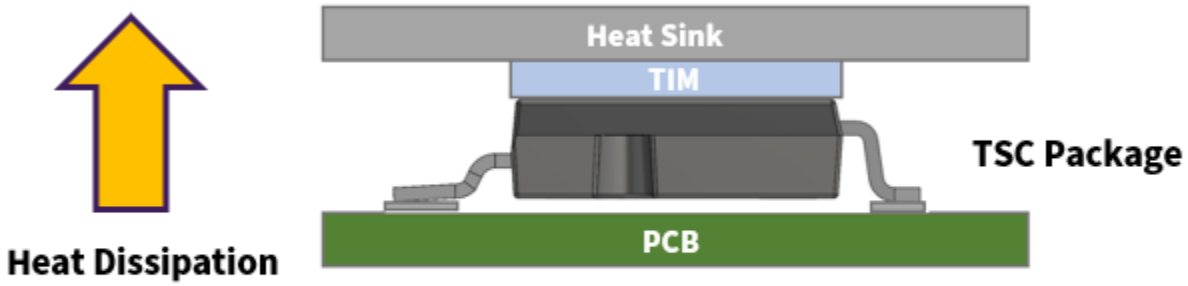


Figure 2: Top Side Cooled Package Concept

As previously mentioned, this creates a significantly improved thermal path that no longer includes the PCB or the solder joints and at the same time opens up the bottom side of the PCB, which can be used for other system components to potentially increase the system power density and reduce overall system size.

While the concept of top side cooling is similar to bottom side cooled devices, assembling TSC packages requires special consideration and design techniques at a system level. System stack up tolerances, planarity of devices, and correct application of TIMs are some of the assembly challenges that if approached correctly, allow the TSC benefits such as increased power density and decreased system R_{θ} to be realized. These system level assembly techniques will be addressed along with the pros and cons of various assembly approaches later in this application note.

2. Wolfspeed TSC Package Offerings

Wolfspeed has two packages featuring top side cooling, the TOLT package and the U2, renderings of both packages can be seen below in Figure 3 :

TOLT **U2**

Figure 3: Wolfspeed Family of Top Side Cooling Packages

The Wolfspeed TOLT package is an industry standard low-profile (2.35mm height), small footprint, top side cooled package which can be compared to the bottom side cooled Wolfspeed TOLL package from an application standpoint. In addition to the advanced thermal benefits of this package, the Wolfspeed TOLT

package also provides enhanced thermal cycling capabilities compared to the TOLL package thanks to the presence of gull-wing leads, further cementing its value proposition. TOLT helps to optimize the system level cost with its ease of assembly and small form factor, allowing for high performing, power dense systems. The TOLT package mainly targets indoor applications such as servers, datacenters, telecom, industrial power supplies, and portable charging industries to name a few.

The Wolfspeed U2 is a medium profile (3.6mm height), top side cooled package which can be compared to the bottom side cooled D2PAK from an application standpoint. The U2 package shares an industry standard footprint with other similar packages available in the market. Significant thermal improvement compared to the standard D2PAK allows for numerous application opportunities in both the indoor and outdoor space to improve overall system power density and performance. Some example applications for the U2 package include ESS, solar, fast charging, industrial power sources, and motor drives.

3. Assembly of Top Side Cooled Packages

This section of the application note will detail some of the popular mounting options that can be used to mount top side cooled packages to a shared heatsink, along with system design considerations that must be addressed with each of the options. Multiple thermal interface materials will be examined, and each option's tolerance analysis, thermal performance, and system level performance will be addressed. This section is provided as a general design guideline only and should be used as a reference along with other power electronics mounting best practices for each specific end application.

3.1 Thermal Interface Materials (TIM)

To enable the benefits of top side cooling, a proper TIM must be used to ensure the heat is dissipated away from the package efficiently while also maintaining electrical isolation between the cold plate and the top metal drain tab of the package. There are three main thermal interface material options that are popular when using a top side cooled package: Aluminum Nitride (AlN) Substrate, silicone gap pad, and Liquid Gap filler. Each of these thermal interface materials were studied from an assembly and system level perspective to help provide a detailed analysis of each mounting option along with the benefits and challenges that come with them. Assembly methods and TIMs for top side cooled devices are not limited to just the three methods listed here, rather these are just popular options that were used for this study. However, they generally fall into one of the 3 categories analyzed here: hard ceramic, flexible and compressible sheet, and liquid or epoxy. There are many more TIM options in the market today and TIM selection should be based off the details of the end application as well as manufacturing capabilities and cost. Each of the three different mounting options mentioned will be detailed, followed by comparisons of all options on tolerance stack up, thermal performance, and system level performance to provide an in-depth guide on how to use each material in a top side cooled environment.

3.1.1 Aluminum Nitride Substrate

Ceramic substrates, such as AlN are an electrically insulating, high thermally conductive material that is a simple option to use between a top side cooled device and the shared heatsink. Thanks to its material

properties, AlN substrates provide the highest thermal conductivity of the TIMs studied, while also keeping the system design simple by providing excellent electrical isolation. During system level testing, a 1mm thick AlN substrate was used to ensure proper electrical isolation while also maintaining excellent R_θ performance. A schematic of this mounting option can be seen below:

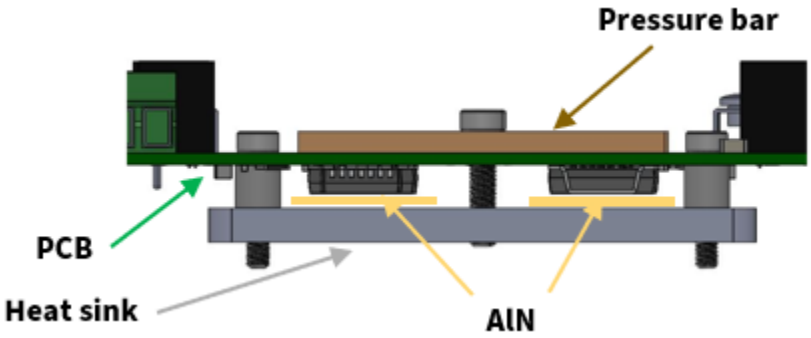


Figure 4: AlN TSC Mounting Setup

Although it has great thermal properties, the rigid AlN substrate does not conform well to potential rough surfaces therefore standard thermal grease was used on both sides of the substrate to overcome any thermal contact resistance that may have been present. The rigidity of the substrate also prevents any conforming to potential uneven package heights that may be created during assembly so careful consideration must be taken during assembly of the TSC devices to keep them as planar as possible if using a shared heatsink.

If proper placement protocol of packages is followed and devices are kept planar, assembly of this method is quite simple, easily allowing for automated or semi-automated assembly to increase manufacturing throughput. The heatsink is attached to the PCB using screws (with an attached pressure bar) on either side of the packages to apply equal pressure, with the AlN substrates sandwiched in between as shown in Figure 4.

3.1.2 Silicone Gap Pad

Silicone gap pads are thermally conductive, fiberglass reinforced, soft pad material and may come with an adhesive or natural tack on both sides that provide electrical isolation between the package and heatsink. The pad used in this testing is Bergquist TSP 1800ST, which has a nominal thickness of 0.203mm and will compress to fill any microscopic irregularities in the surfaces of the two interfaces to aid in thermal performance. To enable peak thermal conductivity over their operating life, constant pressure must be applied to the silicone pad to help it conform to each interface. This is done by attaching the heatsink to the PCB using screws on either side of the packages keeping the silicone pad constantly pressed against the devices with even pressure. Excess pressure can potentially tear or damage the pad so calibrated tools are recommended to ensure equal pressure is applied to all screws. Recommended pressure and torque ratings for Wolfspeed TSC packages will be covered later in this application note. Thermal performance versus pressure applied can be found in each specific silicone pads technical datasheet, which should be studied prior to use. A schematic of this mounting option can be seen below:

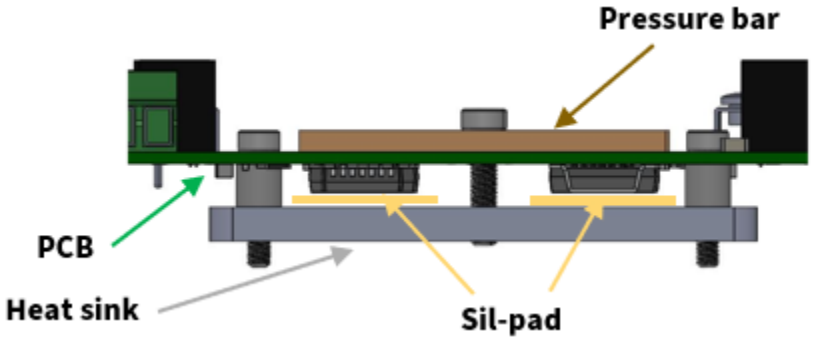


Figure 5: Silicone Pad TSC Mounting Setup

Assembly of this method is also quite simple and is very similar to using an AlN substrate. The silicone pad is cut to size and applied to the heatsink where the top of the devices will make contact, making sure it extends past all edges of the device slightly to prevent any electrical shortage between the drain tab and heatsink. If the devices are close together, the silicone pad can be cut in a way that it is shared among numerous devices to allow for faster assembly. The assembler must make sure that the pad chosen has a dielectric breakdown voltage high enough for their specific operating voltage.

3.1.3 Liquid Gap filler

The third TIM that was studied for top side cooling packages was a liquid gap filler material (Bergquist TGF 4500CVO) which was used in two slightly different mounting setups. Liquid gap fillers provide excellent thermal and mechanical performance while inducing minimal stress on the package during assembly, helping to improve performance and reliability across assemblies. They also enable easy dispensing and therefore are well suited for high-volume manufacturing environments. Because they are liquid when applied, gap filler materials conform to highly intricate surfaces, filling in gaps and rough surfaces, helping to improve the thermal resistance. These materials are cured in place to become semi-solid before use in any applications. Each liquid gap filler material has a specific breakdown voltage and must be applied in a thick enough layer to provide enough electrical insulation between the package and the heatsink depending on the working voltage of the system. In this specific case, for a 1200V MOSFET, the thickness of gap filler material used was around 1.5mm for a 1200V MOSFET TSC device. A schematic of this mounting option can be seen below:

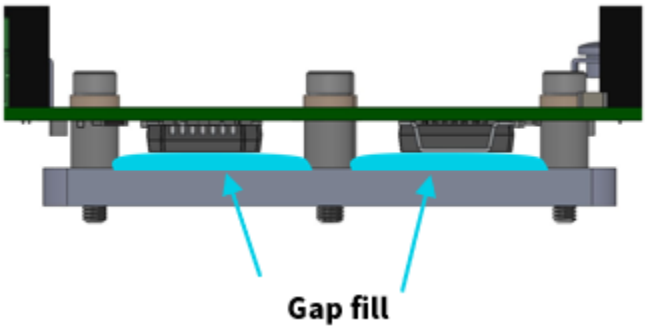


Figure 6: Liquid Gap Filler TSC Mounting Setup

When assembling using this method, careful consideration must be taken when dispensing the gap filler. Reduction of any air gaps is critical to maintain the thermal performance of the system, while enough volume must be dispensed to ensure electrical isolation. To aid in this, it is recommended that a spacer is used between the heatsink and the PCB to maintain equal thickness of gap filler material across multiple devices. Any extra gap filler material that leaks out around the package will not cause any thermal performance changes in the devices but instead ensures that enough material was dispensed.

3.1.4 Liquid Gap filler with Silicone Pad

A hybrid approach was also studied where the thickness of the gap filler was reduced, and a silicone pad was added at the interface to the heatsink. The reasoning for this was the pad can guarantee electrical isolation, and the thickness of the gap filler can be minimized to just what is required to account for tolerance variations. This hybrid option was tested to attempt to find a middle ground between the two while utilizing the best properties of each TIM. The downside to this mounting option is the addition of the second TIM adds to the complexity of the assembly operation and may not be suitable for high-volume manufacturing. Additionally, the silicone pad is not able to be compressed as much due to the addition of the gap filler layer, resulting in diminished thermal performance.

3.2 Tolerance Analysis

To further investigate the four popular mounting options described in the previous sections and their differences, they must also be examined from a tolerance analysis perspective to gain a better understanding of the potential impact on system level performance across numerous devices.

The first step in being able to understand the overall system stack-up is understanding the TSC package design, how it is attached to the PCB, and how this may differ from other types of surface mount packages. The Wolfspeed U2 and TOLT package offerings have two different lead designs which impact the assembly of the packages and the overall system tolerance. The U2 is designed with a positive standoff lead, which means that when the leads of the package are attached to the PCB, there is a small gap between the package body and the PCB. This gap is minuscule and cannot be seen by the naked eye but provides numerous benefits and is therefore a critical part of the package design. Figure 7 below shows an example of a side-view of a positive standoff package.

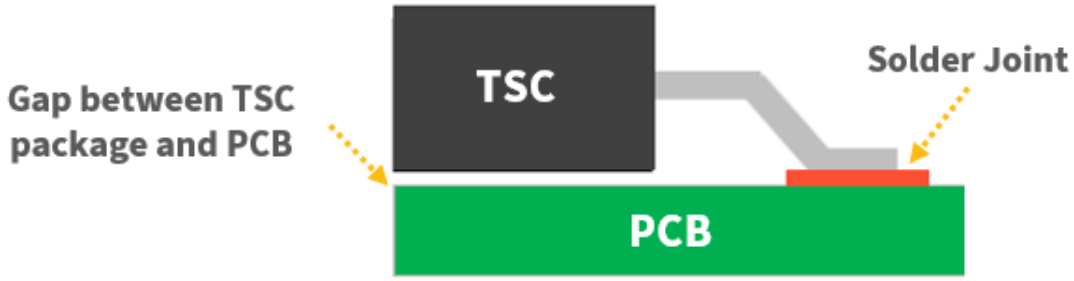


Figure 7: Example of Positive Standoff Design

Most leaded standard surface mount packages (not limited to power packages) use some sort of positive standoff design which enables the use of standard solder paste stencil height, requires no extra board cleaning before reflow soldering, and can be attached to the PCB with SMD glue to enable double side PCB component soldering. The main downside to using a positive standoff design in a TSC package is that there is elevated solder joint stress due to the clamping force it sees between the heatsink and the PCB. System level testing shows that this added stress on the solder joints does not impact the reliability of Wolfspeed's U2 since the package body and leads are designed specifically to incorporate this added stress and disperse it in a way that prevents damage from occurring. However, with the positive standoff design, the tolerance of the lead height must be factored into the overall package height tolerance when considering the spacing from the PCB to the heatsink.

The Wolfspeed TOLT package is designed with a negative standoff lead, meaning that the package body sits flush on the PCB, below the bottom of the package lead. Figure 8 below shows an example of a side-view of a negative standoff package.

Figure 8: Example of Negative Standoff Design

With the negative standoff design, the tolerance of the package lead is taken out of consideration and now only the package body contributes to the overall height tolerance. This is a benefit in TSC devices to help reduce height variation from package to package, allowing for a thinner and more uniform TIM layer. The negative standoff design also minimizes the mechanical stress on the solder joints from the clamping force between the heatsink and PCB and allows the EMC portion of the package body to take on this stress. Due to the fact that

the leads do not sit directly on the PCB, the assembly process must be designed in such a way to ensure the solder paste layer is thick enough to reliably fill the gap between the lead and the PCB and provide proper wetting of the joint. In some cases, this can mean that a non-standard solder paste stencil must be used, and extra solder paste may need to be placed under these packages compared to other non-power components on the same PCB.

Both the U2 positive standoff and TOLT negative standoff provide certain benefits to TSC power packages but the assembler and designer must be aware of which standoff design is present on their chosen package and take the necessary steps to ensure proper use in their system.

Once the package design is understood, the TIM chosen must be examined to determine its impact on the overall system tolerance. When using a silicone pad as a TIM, the main design choice (along with R_{θ} value of the pad) is the thickness of the pad. The thickness and compressibility of the gap pad must account for any variation from device to device of any packages that are sharing the same heat sink. The variations from device to device include any solder joint related tolerances, the overall package tolerance, as well as the heatsink flatness.

These tolerances all must be incorporated into the pad choice and the thickness of the pad must be enough to overcome a worst-case scenario of any worst-case combination of these tolerances. As mentioned in the TIM section of this Application Note, the silicone pad used in this system level testing was 0.203mm thick, which provided enough thickness to overcome any tolerance differences. A tolerance analysis should be performed in each design to aid in the selection of an appropriate TIM.

Similar system level tolerances also need to be understood when using liquid gap filler as a TIM material in a TSC package system to provide optimal performance. Each type of gap filler material has its own material properties such as thermal impedance and electrical breakdown voltage which must be understood prior to system design. Along with the system tolerances described for the silicone pad, when using a gap filler material, the operating voltage must also be considered, and the thickness of gap filler needs to be substantial enough to allow electrical isolation between the drain metal and the heatsink. That minimum thickness of the gap filler is determined by its isolation characteristics, and the system requirements for isolation voltage. While having additional gap filler over this minimum calculated thickness helps ensure electrical isolation, it also will have a negative impact of the thermal resistance of the TIM interface potentially causing reduced device performance. In order to ensure the minimum thickness is maintained in all tolerance scenarios, standoffs between the PCB and heatsink should be used to maintain the minimum desired thickness of gap filler across all devices on a shared heatsink. The standoff height should be designed so that it provides the minimum thickness of gap filler across all devices including any tolerance differences from package to package.

These system level tolerances along with package and TIM selection are crucial to the successful design of an optimized system using TSC packages. Understanding the materials used and requirements of each system design will allow for proper application of these packages and ensure long term reliability of the devices and overall system.

3.3 System Level Considerations

As mentioned previously, there are system level assembly considerations when using TSC packages to ensure optimal performance of the devices. These challenges mainly apply to applications where multiple TSC devices are sharing a heatsink. The key to utilizing the significant device level thermal performance benefits of TSC packages is to prevent system level assembly from causing issues that increase the thermal resistance from the case to heatsink and therefore potentially impacting device performance. When multiple devices are sharing the same heatsink, planarity of the devices mounted to the PCB is critical. Figures 9 and 10 show two examples of design and assembly issues affecting the planarity of TSC packages:

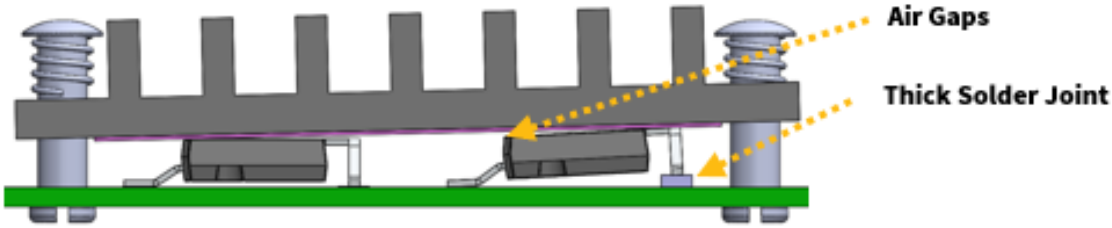


Figure 9: Thick Solder Joint

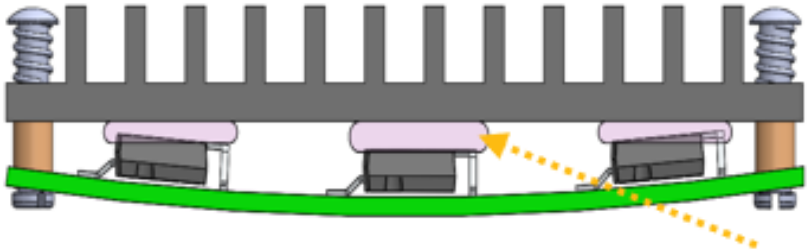


Figure 10: PCB Board Warping

Figure 9 shows a case where one of the TSC packages has a thick solder joint on just the drain side of the device, which causes the whole package to have a tilt. This tilt can occur depending on the relative amount of copper and thermal reliefs on the PCB on the two sides of the component. Since the device on the left has nominal solder joints on both sides and no tilt, the heatsink only contacts the high point of the tilted device and creates an air gap. Since air is a bad thermal conductor, this causes the system R_{θ} of the tilted device to be much higher, creating a hotter Tj and reduced device performance and long-term reliability. To prevent this issue from occurring, solder pad thermal reliefs, solder paste application, and including stencil design and thickness, must be carefully considered and the ability to replicate this process is crucial. Consideration must be taken as well to the application of the chosen TIM so that the thickness is the same throughout all devices sharing a heatsink.

Another assembly level challenge that must be considered is potential warping of the PCB board as shown in Figure 10. This can be caused by improper or insufficient PCB to heatsink attachment. The PCB can also become warped during the soldering process due to imbalanced copper pours, heavy components, or large unsupported distances. To help prevent this, use as many screws or springs distributed throughout the design as possible to help create equal pressure across the PCB, and ensure the PCB design soldering process yield a board with minimal warpage. A thicker PCB or more rigid PCB material can also be considered to help distribute the force evenly. These assembly level considerations help ensure optimal performance of the TSC devices and the system to allow the benefits of TSC devices to truly standout.

4. Test Board Design

To test the Wolfspeed TSC packages at a system level and provide real-world feedback, a test board was designed to run multiple system level tests. Thermal measurements were taken before and after stress tests to compare the performance of each of the different TIM solutions. This test PCB holds 6 Wolfspeed U2 packages oriented to create three independent legs of half-bridge configuration. Each leg has DC link connections at the top and the bottom of the leg. Each device is connected to a DC/DC power converter to provide gate bias of +15 V to the gate pin of the device. All the devices are connected directly to the 15V output of the DC/DC and are therefore gated on once auxiliary power (+12 V) is supplied to the board. Each of the three legs have +DC and -DC link screw terminal connectors. Each leg has a 4-pin connector to measure the V_{DS} voltage for each device. The test PCB is designed such that only the top-side cooled MOSFETs are placed on the bottom side of the board, all other components are placed on the top side of the board. Figure 11 shows a schematic of the connections realized on the board.

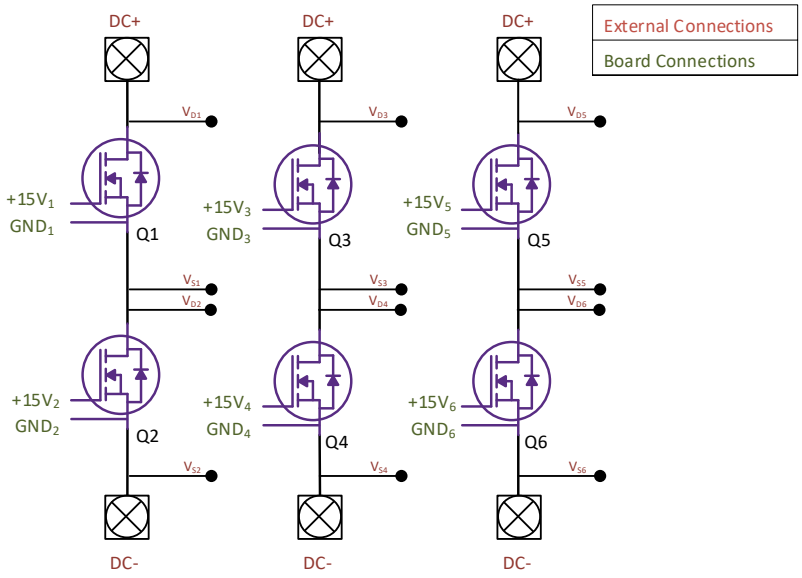


Figure 11: Test Board Electrical Connections Schematic

The desired TIM mounting option was applied to the devices/heatsink and the heatsink was attached to the PCB using screws (and pressure bars depending on the TIM chosen) through the 9 mounting holes that matched threaded holes in the heatsink. To aid in thermal testing and transportation, 8 plastic threaded standoffs were attached around the edge of the PCB assembly to lift it off the bench top. Multiple angles of images showing this test vehicle can be seen below:

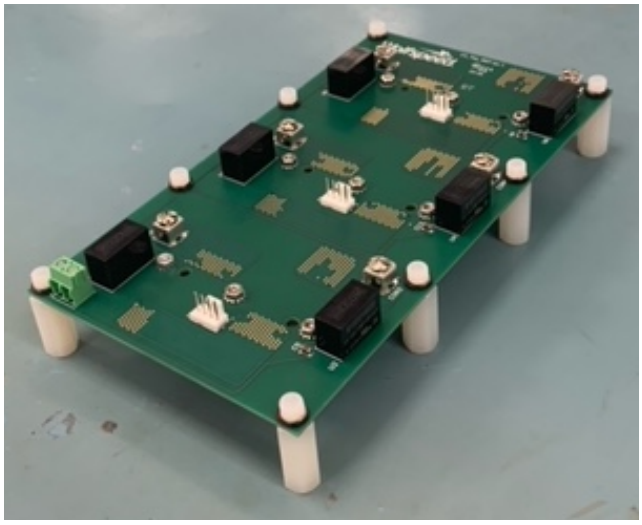


Figure 12 Test Board Isometric View

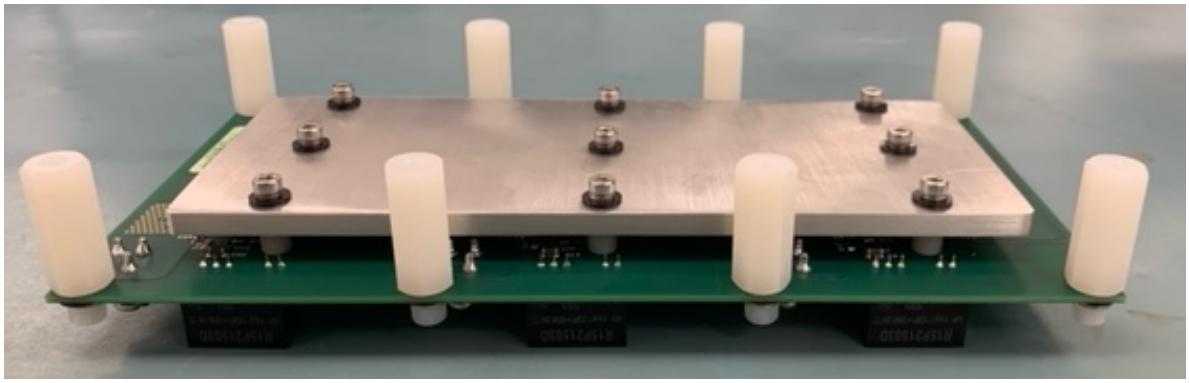


Figure 13 Test Board Bottom View

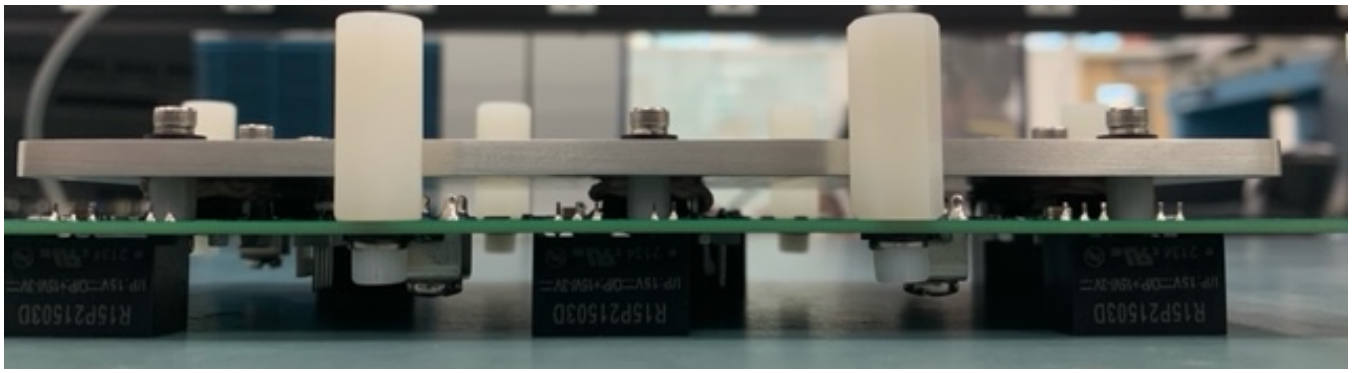


Figure 14 Test Board Side View

This test board assembly allowed the multiple TIMs and mounting options to be studied from a mechanical robustness, electrical functionality, and thermal performance perspective to help provide real-world results that can be used to help determine the best design options for certain applications environments. The details of the specific tests performed and the results for each TIM and mounting option will be covered in the next section.

5. System Testing

To further study the differences of top side cooled devices and their various mounting options, system level testing was performed on the test boards described in the previous section. Standard power electronics system level testing such as temperature cycling, moisture/humidity, and mechanical vibration were performed on numerous boards using all four mounting options previously described. The goal of this testing was to determine if there is any effect on the performance of the devices after the system and TIM was put through rigorous conditions, potentially degrading it.

The temperature cycling performed on the test boards was defined by IPC9701 condition TC3 which states -40°C to 125°C for 1000 cycles with a 10-minute dwell. Temperature cycle testing is designed to detect failure modes caused by CTE (coefficient of thermal expansion) mismatch between devices, TIMs, and PCBs. Most of the time, these failures will occur in the solder joint area of the board so pre and post testing inspection of the solder joints following IPC-A-610 guidelines was performed on all tested boards. Temperature cycling can also help discover internal package defects that may be present in the epoxy mold compound, or any issues with internal wire bonds. This testing was performed in a single chamber industrial oven. Electrical testing to confirm the functionality of the devices along with determining the system R_{θ} value was performed before and after temperature cycling testing to determine the effects that the testing had on the devices and the system.

The mechanical vibration testing performed followed ISO 19453-3 (2018) guidelines which defines testing requirements for electronic equipment on road vehicles. ISO 19453-3 (2018) Section 4.1.2.4 Test IV references random vibration testing of 8 hours per axis (X, Y, and Z) at breakpoint values of 10Hz, 400Hz, and 1000Hz. Mechanical vibration testing is used to test the durability of fragile materials, such as the AlN TIM, to ensure there is no damage that will cause reduced system performance. To ensure that no damage occurred during this testing, high potential (hi-pot) testing was performed between the heatsink and the positive and negative

bus terminals on the PCB as shown in Figure 15. A 4.5kV DC hi-pot voltage was applied for 10 seconds to check isolation.

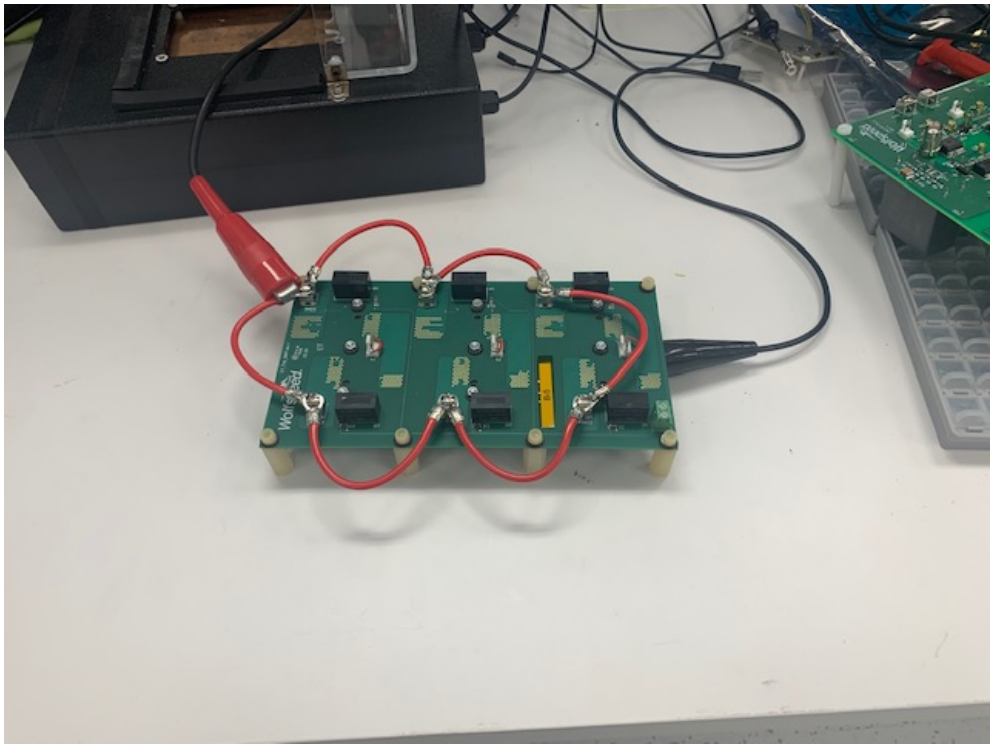


Figure 15: Hi-Pot Testing Setup

More specific system level tests were also performed on the test boards based on which mounting method was used and what the most likely mode of failure would be for that specific TIM. In addition, excess pressure testing was performed on these devices to test the durability of the lead design influencing the positive standoff of the U2 to ensure reliability under extreme conditions that may be seen in the field. This section will be broken down by each of the four mounting methods studied, detailing what system level tests were performed, how many boards were tested, along with thermal and mechanical results and observations.

5.1 AlN Substrate

Using an AlN substrate as a TIM in a TSC system is relatively straight-forward from an assembly perspective so the focus for this method's testing was how the AlN performs under the various environmental conditions. The main concern of this mounting method is any sort of damage occurring to the AlN. If any environmental condition causes the AlN to crack or break, the electrical isolation between the heatsink and the package will be compromised, potentially causing failure of that device in the system. With that in mind, the list of tests performed on the test boards using this mounting option can be seen in Table 1.

Table 1: System Tests for AlN Mounting

Item	Test	Description	Conditions	# Parts Tested
1	Mechanical Vibration	Mechanical vibration testing of full assembly	ISO 19453-3	1 Board (6 TSC Packages)
2	Temperature Cycle	Temperature cycling on board	IPC-9701 TC3, -40C to 125C, 1000 cycles, 10 min dwell	3 Boards (18 TSC Packages)

Each test listed in Table 1 was performed with a unique assembly, meaning boards did not go through multiple tests and the stress was not cumulative.

The first test in Table 1, mechanical vibration, did not result in any breaking or cracking of any of the 6 AlN substrates being used as a TIM material in this setup. Hi-Pot testing was passed successfully at the designated conditions before and after the mechanical vibration testing which proved that the TIM maintained electrical isolation between the package and the heatsink. As the fragility of the AlN is one of its biggest downsides as a TIM interface in this setup, this test was able to prove the ability of this TIM to be a practical option when using TSC packages.

Temperature cycling to IPC-9701 was performed on 3 test boards using AlN as the TIM and no damage or shifting of the substrates was observed. Visual inspection of all solder joints of the 18 TSC packages was performed pre and post temperature cycling and no issues were observed. To properly gauge what effect the temperature cycling had on the TSC packages, system thermal resistances were calculated on all the packages before and after the testing. Since measuring the heatsink surface temperature or package case temperature can provide inaccurate results due to uneven heat flow, this was done by using measured device electrical characteristics to determine each package's junction to heatsink thermal impedance, $R_{\theta JH}$ and then take the average value of the 6 packages per board to determine a board $R_{\theta JH}$. Step 1 of this process was to measure the $R_{DS(on)}$ of the devices on the test board at a specified current level, which in this testing it was done at a current of 12A with $15V_{GS}$ being applied to the devices. Using the $R_{DS(on)}$ vs. T_J chart from the TSC package datasheet, a T_J for each package was estimated at the specified current level and measured $R_{DS(on)}$. The junction to ambient thermal impedance, $R_{\theta JA}$ was then found by subtracting the ambient temperature during testing from the calculated T_J and dividing it by the power dissipation from each device. To accurately compare just the TIM performance, the known internal junction to case thermal impedance, $R_{\theta JC}$ and the calculated heatsink to ambient thermal impedance, $R_{\theta HA}$ were subtracted from the total $R_{\theta JA}$, resulting in the TIM thermal impedance, $R_{\theta CH}$. This allows direct thermal performance comparison between the multiple TIM and mounting setups. The results of this testing for the 3 boards built using AlN as a TIM that went through temperature cycling can be seen in Table 2 below:

Table 2: AlN System R_θ Testing Results

Board	Calculated TIM $R_{\theta CH}$ (C/W)	TIM $R_{\theta CH}$ (Pre-Temp Cycle (C/W))	TIM $R_{\theta CH}$ (Post-Temp Cycle (C/W))
#1	~0.4	0.42	0.44
#2		0.51	0.54
#3		0.27	0.30

As shown in the table, the actual testing results match up extremely well to the calculated TIM $R_{\theta CH}$ results. The AlN substrate theoretically had the best thermal performance out of the TIMs studied here and the thermal testing confirmed the low thermal impedance of this material. The slight variation from board to board on R_{θ} can be partially contributed to the fact that the T_j of the device was estimated from a chart and that depending on the board, it took more time for some devices to reach steady state than others. Comparing the TIM $R_{\theta CH}$ values before and after the temperature cycle testing, it can be seen that no damage was caused by this applied thermal stress and there was no significant reduction of TIM performance. This testing demonstrates that the AlN substrate is a viable option as a TIM for TSC packages.

5.2 Silicone Pad

The system using the silicone pad was subjected to the same system level tests that were performed on the AlN assemblies; mechanical vibration and thermal cycling. While the silicone pad does not have the same cracking concern as the AlN substrate, its ability to handle temperature cycling and mechanical vibration was studied to ensure it has the robustness to hold up in environmental conditions it may see in the field.

Mechanical vibration testing of test boards using silicone pads as the TIM showed some interesting results when it came to overall package design. When using competitor TSC packages, which have a sharp corner on the top drain pad, rips and tears occurred in the pad which eliminates the electrical isolation between the package and the heatsink and results in a failure of that device. When using Wolfspeed TSC packages which do not have this sharp topside drain edge, no ripping of the silicone pad occurs, and all devices passed mechanical vibration testing. This is a critical find because without electrical isolation, TSC packages cannot function as intended and will result in reduced system performance or even complete system failure in the field.

Wolfspeed Part **Competitor Part**

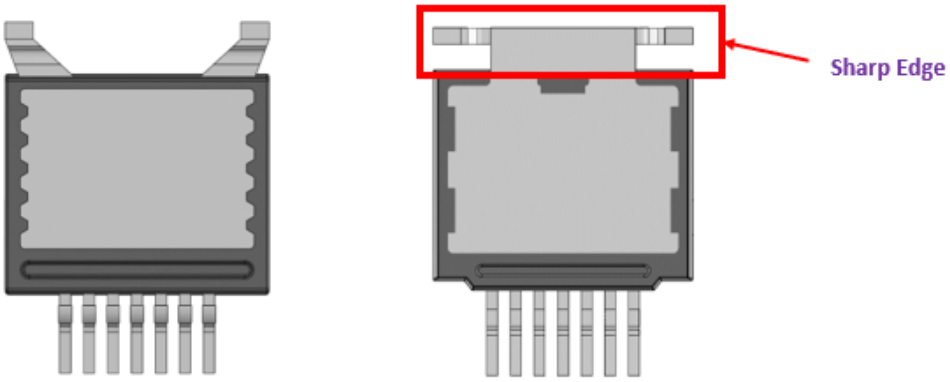


Figure 16: Wolfspeed vs. Competitor Package

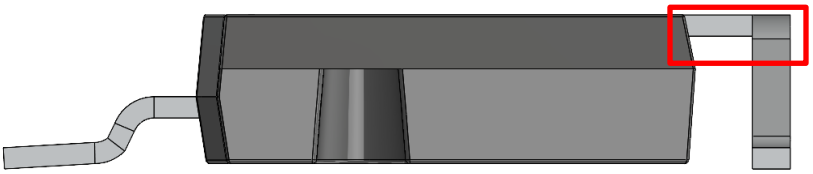


Figure 17 Competitor Part Drain Tab Design

The temperature cycling performed on these test boards, following the same conditions as the AlN mounting method, did not show any signs of damage to the pad or any of the solder joints of the devices. The TIM $R_{\theta CH}$ measurement results are shown in Table 3.

Table 3 Silicone Pad System $R_{\theta CH}$ Results

Board	Calculated TIM $R_{\theta CH}$ (C/W)	TIM $R_{\theta CH}$ (Pre-Temp Cycle (C/W))	TIM $R_{\theta CH}$ (Post-Temp Cycle (C/W))
#1	~0.9	0.85	0.87
#2		0.72	0.71
#3		1.04	1.04

The results of the thermal testing of the silicone pad mounting option also show very good comparison to the calculated TIM $R_{\theta CH}$ value and consistent performance is seen between the pre and post temperature cycling values. As expected, the $R_{\theta CH}$ is slightly higher than the AlN but also shows the durability to be able to handle multiple environmental conditions. Additionally, the assembly using a silicone pad is simplified since there is no need for applying thermal grease. The compressibility of the silicone pad can help accommodate height and coplanarity differences between packages unlike the AlN method. The results of the system level testing of the silicone pad also shows that it is a viable TIM and mounting option for TSC packages.

5.3 Liquid Gap filler with Silicone Pad

As detailed in section 3.1.3, liquid gap filler has different potential failure modes as compared to using an AlN substrate or a silicone pad and therefore to get a complete understanding of using this TIM in a TSC system,

some additional system level tests were added to this test plan. Table 4 shows the test plan that was used for system testing for both assembly methods using gap filler as a TIM material:

Table 4 System Tests for Gap filler Mounting

Item	Test	Description	Conditions	# Parts Tested
1	Mechanical Vibration	Mechanical vibration testing of full assembly	ISO 19453-3	1 Board (6 TSC Packages)
2	Temperature Cycle	Temperature cycling on board	IPC-9701 TC3, -40C to 125C, 1000 cycles, 10 min dwell	3 Boards (18 TSC Packages)
3	Moisture/Humidity	Expose boards to high moisture/humidity conditions	JESD22-A101 85C, 85%RH 1000 Hours	3 Boards (18 TSC Packages)
4	Low Temp Storage	Expose boards to low temp storage conditions	JESD22-A119 1000 Hours at -40C	3 Boards (18 TSC Packages)
5	High Temp Storage	Expose boards to high temp storage conditions	JESD22-A103 1000 Hours at 125C	3 Boards (18 TSC Packages)

The addition of the moisture/humidity, low temperature storage, and high temperature storage account for the potential delamination of the gap filler material to occur. Various application and curing conditions can have effects on the performance of liquid gap filler and its ability to handle certain environmental conditions. Any delamination of the gap filler material can lead to reduced or complete loss of electrical isolation performance which can compromise device and system performance. Any air gaps that may arise as a result of these environmental conditions can cause serious degradation in thermal performance of the interface. The additional tests are rather simple in theory, but they help to show the robustness of this material if it is applied and used properly. The mechanical vibration and temperature cycling of these test boards both followed the same conditions used for the AlN and silicone pad assembly methods.

None of the system tests using gap filler with a silicone pad resulted in failures of the TIM. There was no delamination found, which was confirmed by hi-pot testing before and after all the system level tests along with visual inspection. The thermal resistance was measured pre and post temperature cycle testing and the results can be seen in Table 5.

Table 5: Gap filler with Silicone Pad System R_{θ} Results

Board	Calculated TIM $R_{\theta CH}$ (C/W)	TIM $R_{\theta CH}$ (Pre-Tests Avg (C/W)	TIM $R_{\theta CH}$ (Post-Tests Avg (C/W))
#1	~1.2	2.68	2.41
#2		2.88	2.67
#3		3.05	2.70

Contrary to the other TIM and mounting methods presented thus far, the liquid gap filler with a silicone pad option showed TIM $R_{\theta CH}$ results that did not match up with calculated values. The TIM in this case performed much worse than expected. The reasoning behind this is believed to be the added thermal interface of the gap filler with the silicone pad. Contact resistances can be detrimental in a thermal network, causing reduced thermal performance due to the presence of micro airgaps and a non-fluid medium for the heat to flow. Another contributing factor is that the silicone pad relies on pressure to achieve its thermal conductivity properties. With the liquid gap filler in the joint, very little pressure is applied to the pad, resulting in higher interface resistance at the heatsink surface. Simulated environments usually use best case scenarios and do not account for real-life assembling of these two TIMs together. Looking closer at the post-tests TIM R_{θ}, a reduction can be seen as compared to the pre-test's TIM R_{θ}. This is caused by continued curing of the gap filler material as the tests are being performed. There are multiple curing schedules that can be used for most gap filler materials, ranging from days at room temperature to just a couple of hours at an elevated temperature in an oven. The tests boards used here were cured at room temperature, so when exposed to slightly elevated temperatures, some minor continuation of curing most likely occurred, improving the performance of the TIM over time.

System level testing of the liquid gap filler with a silicone pad mounting method showed that it can handle most environmental conditions it may see in the field, but if low system thermal resistances are required, it may not be the best option to use for TSC packages.

5.4 Liquid Gap Filler

The last TIM and mounting method tested at a system level was the thick liquid gap filler method, which is the exact same as the previous method described without the additional silicone pad. This mounting method was put through the same testing procedure as the gap filler with silicone pad to again predominantly look for any delamination and reduced thermal performance post system testing.

Results of this system testing provided showed no failures in the thermal interface. There was no delamination found, which was confirmed by hi-pot testing before and after all the system level tests along with visual inspection. Thermal resistance was evaluated using the same testing procedure was performed as the other mounting methods, and the results can be seen in Table 6.

Table 6: Gap filler System R_{θ} Results

Board	Simulated TIM $R_{\theta CH}$ (C/W)	TIM $R_{\theta CH}$ (Pre-Tests Avg (C/W))	TIM $R_{\theta CH}$ (Post-Tests Avg (C/W))
#1	~2	1.48	1.09
#2		1.33	1.26
#3		2.06	1.93

The TIM $R_{\theta CH}$ results shown in Table 6 further cement the conclusion about the added contact resistance caused by the addition of a silicone pad in the previous mounting method described, since the thermal results here are much better matched to the simulated values that were expected. Once again there was a slight improvement of $R_{\theta CH}$ performance post system testing due to further curing of the gap filler material. This mounting method

performed better than expected in terms of thermal performance and durability and is another viable option that can be used with TSC packages.

Looking at the thermal testing results of all four TIM and mounting methods described, each is a viable option that can be used for top side cooled packages. The AlN and silicone pad have higher thermal performance but have less ability to make up for device and assembly tolerance. Both mounting methods using the liquid gap filler material have moderate to lower thermal performance but exert less stress on the PCB and pins and can account for assembly and package tolerances very well. The main decision of which TIM and mounting method should be used should come down to the thermal performance required, the manufacturing options, the end system application, and the environmental conditions it will be exposed to. The thermal results and system level testing observations presented in this application note can serve as a guide when designing top side cooled devices into a system.

5.5 Excess Mounting Pressure Testing

As discussed in Section 3 of this application note, the U2's positive standoff creates many benefits for improved assembly but also can create concern about the reliability of the leads under the clamping force that occurs on top side cooled devices between the heatsink and the PCB. To ensure that this clamping force in most applications will not cause any damage or reduced reliability to the package, excess pressure testing was performed on the U2 as part of the overall top side cooling system testing discussed in the previous section.

Two tests were run as part of the excess force testing to attempt to cover most potential applications of this package. These two tests included applying two different forces on the packages and then running them through either temperature cycling (-55C to 150C) or high temperature storage (175C for 500hrs) and then comparing parameters from before and after the testing. The test setup included the parts mounted between two flat, aluminum bars that had M3 screw holes on either side of all the packages to apply the force. The screws were tightened with a torque of 1Nm, which converts to around 660N of force, using a calibrated torque wrench. Twenty samples of the U2 under these conditions were subjected to the temperature cycling conditions and nine samples were subjected to the high temperature storage conditions. Once the testing was completed, the parts were then electrically measured for VDSON, IDSS, IGSS, and VTH along with other electrical parameters and compared to the measured values prior to the testing to ensure that no damage had occurred to the device. No significant changes in any electrical parameter were found after the force and temperature testing was applied to these packages. Additionally, the height of the packages was also measured pre and post testing to attempt to observe any non-elastic characteristics of the EMC or any damage to the package leads. No significant changes in package height were observed which is critical to help maintain co-planarity between devices that may be sharing the same heatsink. This testing was then repeated, except this time the screws were tightened with a torque of 1.5Nm, which converts to around 1000N of force. Even under these conditions, no change in electrical performance or package height were found.

The conclusion from this testing was that there are no concerns with the positive standoff design of the U2 causing any damage or reliability issues while mounted to a heatsink. The mounting contact between the package and the heatsink should evenly distribute the forces across the package body, avoiding any concentrated loads. Conservatively, the maximum screw torque applied to clamp the packages between the

PCB and heatsink should be between 1-1.5Nm. In general, the applied force should be centrally located, avoiding higher forces near the edge of the package body to endure safe and reliable use of the package.

6. Conclusions

Top side cooled power packages provide improved system thermal performance and allow for higher power density and innovative system designs to be realized. Multiple examples of how to use these packages in real-world systems with some of the various popular TIM and mounting options were detailed to help aid in design choices. Following the design recommendations provided in this Application Note, along with standard best practice manufacturing methods of power electronics, Wolfspeed's top side cooling portfolio packages can be used to their fullest potential safely and correctly, to provide the best SiC power device performance in the market today.

7. Revision history

Date	Version	Description
October 2023	1	Initial App Note Release
August 2025	2	