

Mitigating Package Induced Failures

This application note examines the primary components of power modules, identifies common failure mechanisms, and discusses limitations in current packaging techniques. SiC MOSFETs enhance power system performance by offering higher breakdown voltages, faster switching, and improved thermal management. As power semiconductors continue to improve, there is an expectation that packaging technology will keep pace. To prevent an industry performance bottleneck, advancements in packaging methods must align with the capabilities of these power devices.

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1. Introduction

Power module packaging plays a key role in power electronics design by bridging the power device to its application. Modern power devices are constructed out of wide band gap materials such as silicon carbide (SiC) to provide higher breakdown voltage, faster and more efficient switching and improved thermal management within the same die area. Thus, to avoid an industry bottleneck, packaging methods must improve in tandem with power devices to meet the improved performance characteristics they offer. This application note will discuss the main components of two popular types of module-builds (shown in Figure 1), failures and common failure mechanisms of power module packages, common packaging limitations and methods to identify package level failures.

2. Packaging Components

A standard power module package consists of many different components layered together. Six of the main components will be discussed in further detail in the subsections of this chapter, starting from the bottommost component and continuing to the topmost component, which is the order in which the module is assembled.

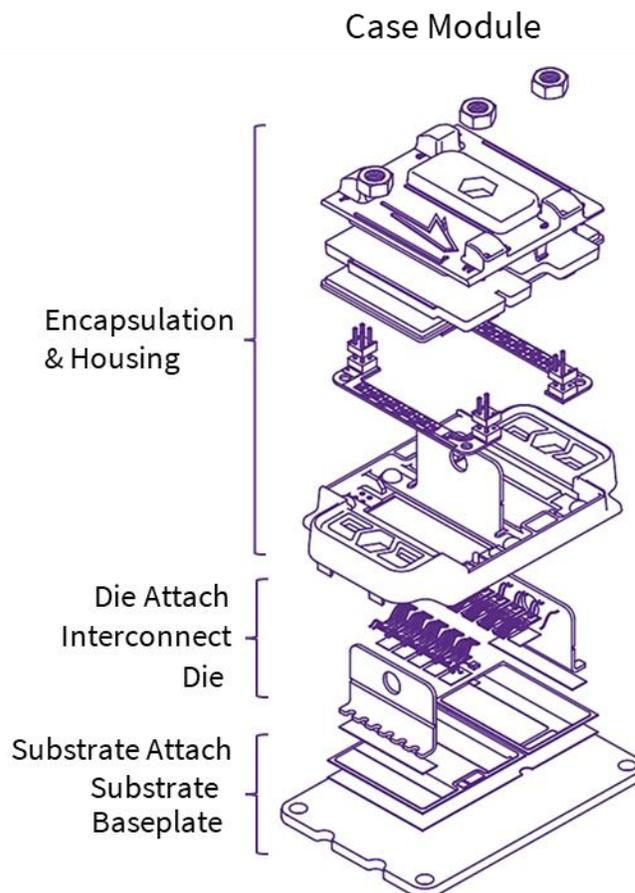


Figure 1: Exploded 3D view of a case module (left) and lead frame module (right).

2.1 Base Plate

Base plates are typically only found in case modules. This component is made of a thermally conductive material allowing heat to be removed from the package. Copper (Cu) is the most common material used followed by Aluminum Silicon Carbide (AlSiC). Cracking or chipping reduces the base plate's mechanical stability, thermally conduction capability, and the capacity to isolate the module from foreign materials. Failures that involve the base plate are typically found during optical and CSAM inspection electrical isolation testing of the power module and are often caused by mechanical damage.

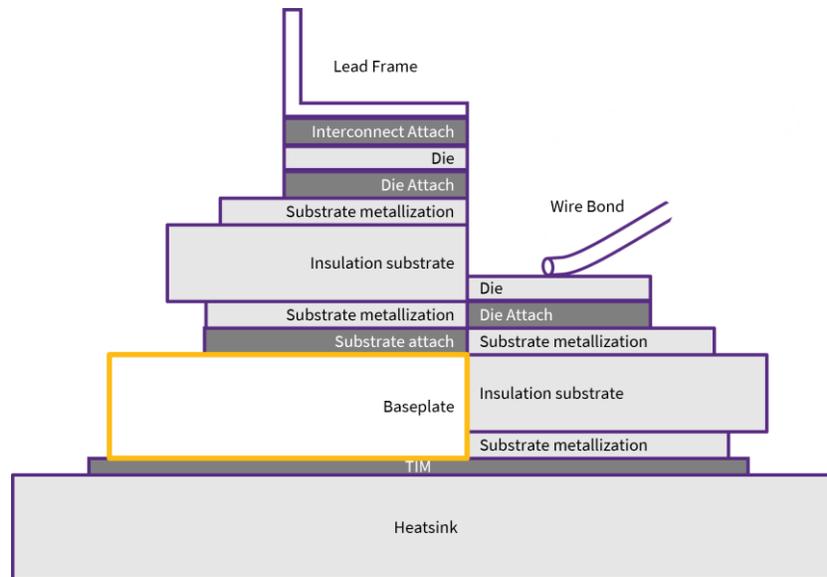


Figure 2: Power module stack up (Baseplate)

2.2 Substrate

The substrate plays several key roles in power module design. It typically consists of several stacked layers of metals and ceramics. It functions as an electrical interconnection between various devices, provides voltage isolation, acts as a heat transfer path, and gives mechanical support to other components within the module. The most common processes for substrates include Direct Bonded Copper (DBC), Direct Bonded Aluminum (DBA), and Active Metal Brazing (AMB), all of which consists of a ceramic layer sandwiched between two metal layers. Insulated metal base plate (IMB) is another popular process that combines the base plate and substrate into a more compact design. There are tradeoffs between the different processes; for example, DBA will perform better in thermal cycling than DBC but will have a worse thermal performance [1]. IMB can offer a cheaper substrate option and performs well through thermal cycling. Knowing a system's power and thermal requirements can help identify the necessary materials and attach method needed for effective power module design.

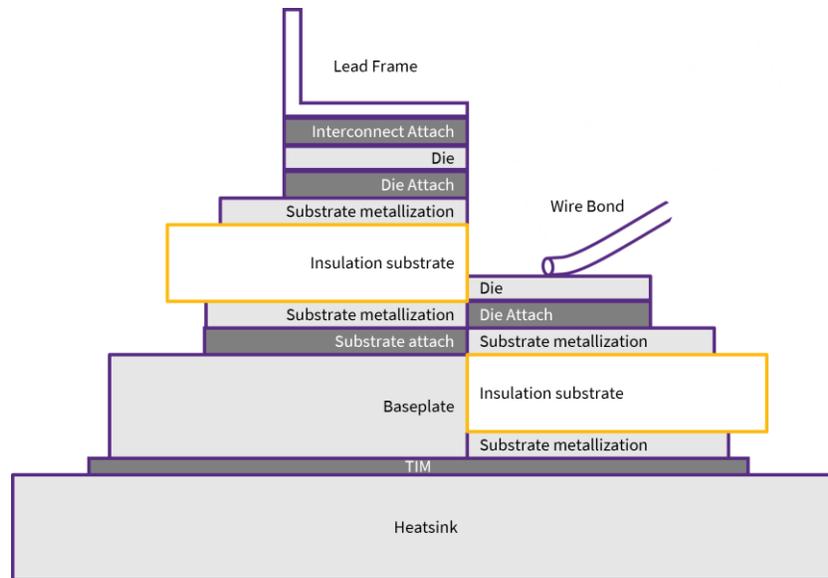


Figure 3: Power module stack up (Substrate)

	DBC	DAB	IMS
Conductor	Cu	Al	Cu
Insulator	Al_2O_3 , AlN, Si_3N_4	Al_2O_3 , AlN	Epoxy
Manufacturing Process	DCB, AMB	DAB	Lamination

Table 1: Summary table of substrate stack options and their manufacturing process

2.3 Die to Substrate Attach: Solder / Sinter

Various attach methods are utilized by power module manufacturers to connect the power device to the substrate. The substrate attach material must provide electrical, thermal and mechanical support between the die and substrate. These techniques can be used for base plate-substrate attach (thermal interface material may also be used), die-drain attach, die-source attach, and connection of other components on to the substrate like lead attachments.

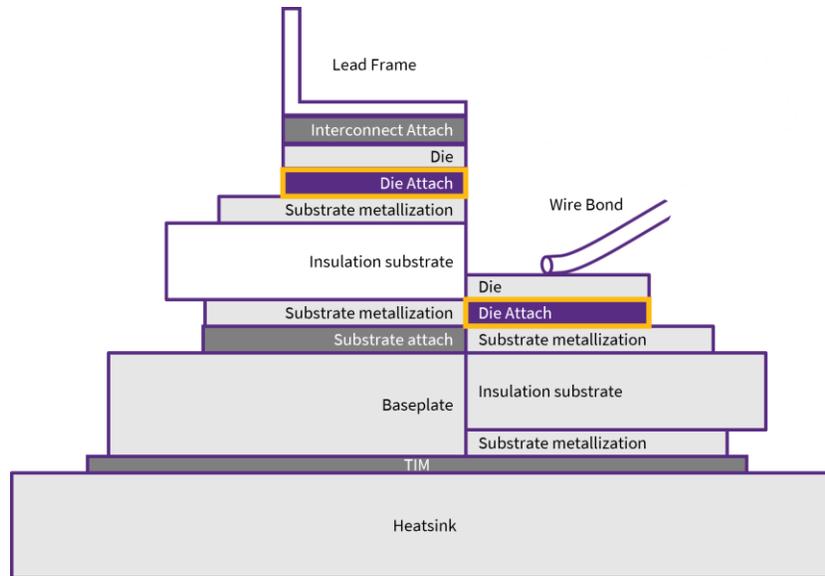


Figure 4: Power module stack up (Die Attach)

Solder

Solder is one of the oldest and most common attach methods. Solder alloys fuse two metal surfaces together using a molten filler metal, which melts and solidifies at a particular temperature, forming a strong metallurgical bond between the components. Most solder alloys are based on combinations of two or more base elements. The melting points of the alloys are generally much lower than the pure metal component it is fusing with. Flux is added to improve the quality of the solder bond by removing oxide films that form on the surface of metals being soldered.

Sinter

Silver and Copper are popular materials used for sintering because of their strong mechanical properties. Sintering is a process in which a metal powder is heated and compressed, diffusing and densifying into a solid. Sinter does not go through a phase change and creates a robust joint that does not melt until temperatures reach $>700^{\circ}\text{C}$. It also performs better than solder in mechanical testing by shielding the components from physical pressure and shocks through a solid mechanical bond. It is critical that the sinter paste is deposited correctly for the best performance.

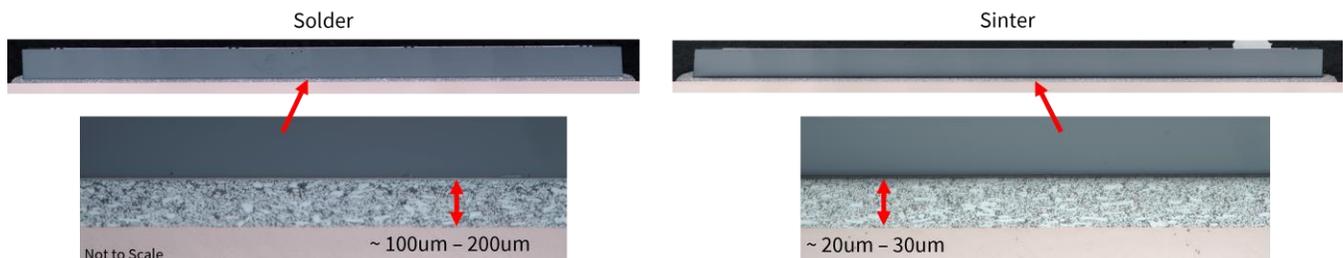


Figure 5: Wolfspeed die soldered (left) and sintered (right) to a substrate w/ their recommended thickness ranges

Wolfspeed recommends targeting a final bond line thickness of $\sim 100\text{-}200\ \mu\text{m}$ for soldered attach and $\sim 20\text{-}30\ \mu\text{m}$ for sintered attach. A tradeoff exists between thermal and reliability performance and substrate attach

thickness. A thin layer of attach material will have better thermal performance but worse reliability. As the layer thickens, reliability improves, but thermal performance degrades. If the layer becomes too thick, however, the reliability performance tapers off and eventually regresses. More information on these two attach methods can be found in Wolfspeed’s attach method app notes [2] [3] [4].

2.4 Devices / Die

The next layer is the semiconductor power device or die that is being packaged. These devices can be made from many different semiconductors such as Si, SiC, GaN, etc. and can vary from IGBTs, BJTs, MOSFETs, Diodes, etc. When selecting a power die product for power module design electrical parameters such as $R_{DS(on)}$ and switching losses, and mechanical characteristics such as the die metallization materials and die size must be considered to obtain optimal performance.

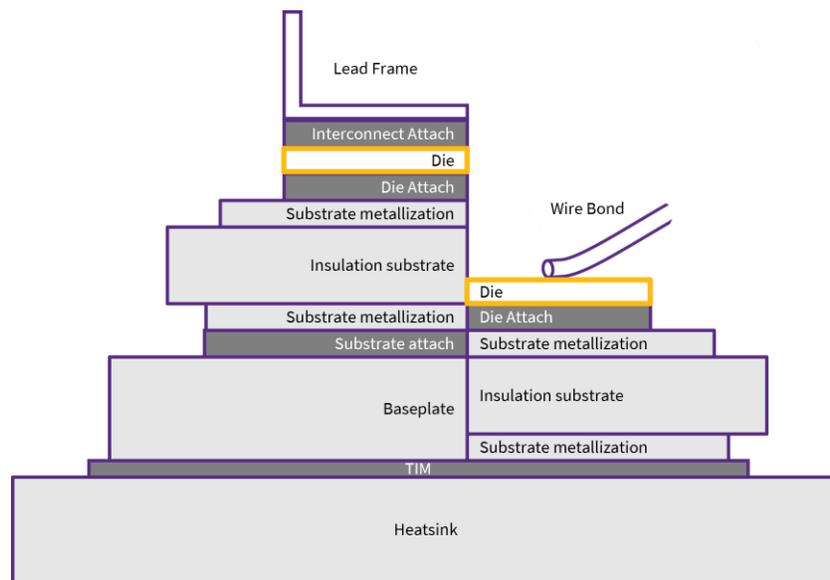


Figure 6: Power Module stack up (Die/Devices)

2.5 Interconnects: Wire Bonds / Leads / Clips

Interconnects electrically connect the top surface metal pads on the die to other components in the module or the substrate. Multiple interconnect technologies are available including wire bonding, ribbon bonding, tape automated bonding, flip chip bonding, clip bonding, and more. Each has its own set of advantages and disadvantages in terms of cost, manufacturability, electrical and mechanical properties, and reliability. The two types of interconnects are signal connections and power connections. The signal connection is designed to carry relatively low currents and is used to modulate the device between an “on” and “off” state. Power connections are designed to carry high currents used to transfer power through the device. For more information on wire bonding, reference the Wolfspeed wire bonding app note [5].

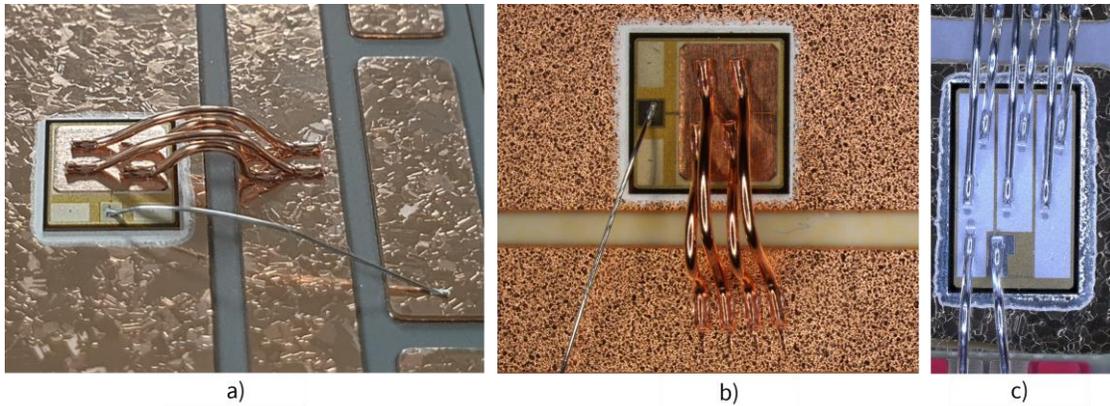


Figure 7: (a) Wolfspeed die sintered to a substrate stack of Cu and AlN and interconnected with Cu power wire bonds. (b) A die sintered to a substrate stack with Cu and Al₂O₃, and interconnected with Cu power wire bonds. (c) A die soldered to a substrate stack with Cu and AlN and interconnected with Al power wire bonds.

Wire Bonds

Although historically Aluminum (Al) wire bonds are a cheap and well-studied top-side interconnect option, they can limit the performance of the module. A single wire bond can significantly add to the overall package parasitics, and aluminum's material properties limit the ampacity of a system due to the inability to dissipate heat. They have large footprints and are considered one of the weakest components for reliability. Wire bonds also make it very challenging to incorporate double-sided cooling techniques, which are often crucial for optimal thermal performance. Other materials can replace aluminum (such as copper) and offer improved thermal reliability performance but will not mitigate inherent issues with wire bonds such as high parasitics and mechanical reliability concerns.

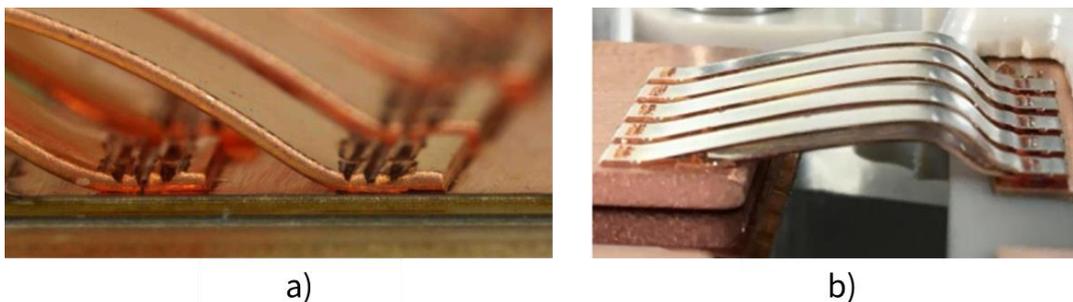


Figure 8: (a) Copper ribbon bond from Heraeus using ultrasonic Cu bonding and (b) Aluminum ribbon bonding using laser bonding [6].

Lead Frame & Ribbon Bonding

Lead frames and ribbon structures are alternative interconnect options. They help reduce path parasitics and improve thermomechanical reliability. These options offer a large cross-section with which to bond, thus improving current capacity and potentially allowing for top-side cooling. Copper is typically material of choice, which requires alternative metallization options for SiC die due to reliability issues with copper such as sinking.

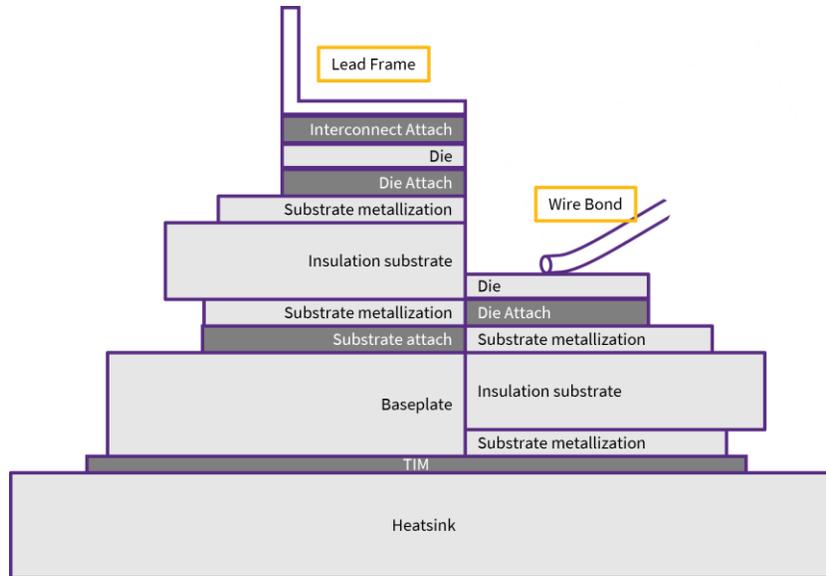


Figure 9: Power module stack up (Interconnects)

2.6 Encapsulation & Housing

The housing and encapsulant help protect the module's components from the environment. Encapsulation also improves the voltage rating of the device by preventing arcing between different electrodes. Encapsulants can consist of silicone gels, epoxies, or molding compounds. Casings are generally made from plastic and provide components with protection from environmental pollution, mechanical support and electrical insulation. Casings also provide signal and power contact locations.

3. Failures & Common Failure Mechanisms

Failures are categorized by severity of damage to device operation. The three main categories include loss of form, loss of function and loss of operation. Loss-of-form failures include cosmetic or surface level defects such as scratches or cracks. Loss-of-function failures occur when a product no longer electrically performs within a range specified by the data sheet. Loss-of-operation occurs when a product completely fails and is rendered unusable.

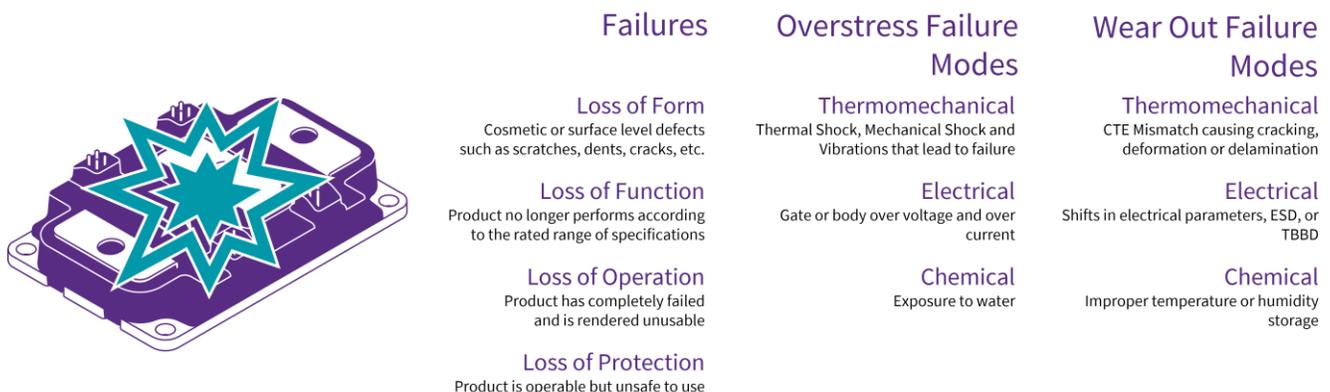


Figure 10: Example of Failure Categories and Failure Modes

3.1 Chip-level Failures

Failures at the die level are considered chip-level failures and often lead to loss of function or loss of operation. These failures could be due to manufacturing defects, natural wear on the part, operation of the part outside of technical parameters, or many other individual or combined reasons.

3.2 Package Level Failures

Package level failures are failures in the packaging materials surrounding a power device. This includes power and signal electrical and thermal connections, and all isolation materials external to the power device. Failures at the package level can cause damage to other parts of the device, especially in high energy electrical failures, which can complicate failure and root-cause analysis. For instance, thermal runaway events caused by degraded solders can lead to damage to the underlying substrate as well as damage to the surrounding isolation material, the power device, and the interconnects attached to the power device. This high-energy electrical damage is internally described under a blanket term known as “Electrically-Induced Physical Damage” (EIPD). EIPD often makes it difficult to precisely determine the root cause of the failure event. An example of EIPD can be seen in Figure 12 below.

The burn mark not only visually obscures the area that requires inspection, but the burned chemicals can make it difficult to use chemical analysis techniques. The mechanical damage can destroy the evidence that would point to the root cause.

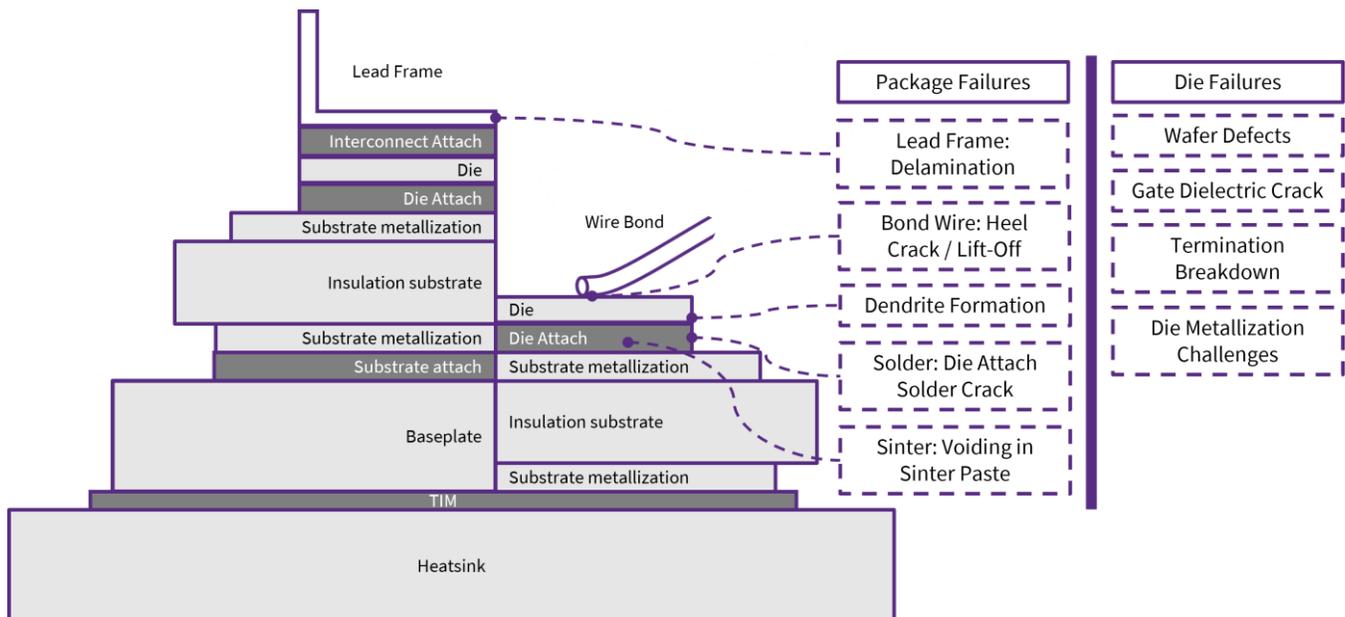


Figure 11: Differentiation between package level and chip level failures. Abbreviated stack up of power module with general location of package failures specified.

3.3 Package Level Failure Mechanisms

The two main types of failure mechanisms observed are overstress and wear-out mechanisms. Failure mechanisms lead to failure modes, generally categorized by thermomechanical, electrical, or chemical failures.

Overstress mechanisms

Overstress mechanisms are caused by a single extreme event exceeding the specification of the device or module, such as dropping or spilling of the device. Overstress mechanisms exacerbate package level failures. Thermal runaway is the leading failure mode, most often caused by thermal or mechanical shock induced damage to the module.

Thermomechanical Failure Modes

Thermomechanical failures are failures due to the thermal and mechanical variations or shocks faced by a module during operation. Dropping and excessive shaking are examples of thermomechanical overstress mechanisms that can lead to failure. Environmental testing such as electrostatic discharge testing, thermal shock testing (TST), mechanical shock testing, and vibration testing must be performed to meet industry standards.

Electrical Failure Modes

Electrical overstress mechanisms include gate overvoltage or overcurrent and drain-source overvoltage or overcurrent. Exceeding electrical specifications of the devices can lead to arcing inside the module and degradation of certain materials. When excessive drain-source voltage is applied, the power device can begin to avalanche and potentially lead to its destruction. Excessive gate voltage can cause immediate or accelerated gate oxide degradation leading to time-dependent dielectric breakdown (TDDB) type failure of the device.

Chemical Failure Modes

Temperature, humidity, stress, and voltage can induce chemical reactions leading to different failure mechanisms within the different materials of the package. Breakdown of encapsulation material and unwanted phase transitions of various materials during operation are results of excessive or improper chemical overstress.

Wear-out mechanisms

Wear-out mechanisms are defined as gradual repeated application of low-stress test conditions on a power module over extended periods of time. Reliability testing is performed at the die level to understand die-level failure modes. Similar test methodologies are performed at the package level to better understand package level wear-out mechanisms such as thermomechanical creep and fatigue, electromigration, metal ion migration, corrosion, and degradation of interconnections and insulation layers.

Thermomechanical Failures

Thermomechanical failures are the most common failures observed due to mismatches in the coefficient of thermal expansion (CTE) inherently present between adjacent layers in the module. Common examples are fractures and cracking, deformation, delamination, and creep across and within different components of the module. These failures normally occur at the interface of two or more materials.

Electrical Failures

Most failures in the device first show up in the form of an electrical failure and may need to be probed further to find the root cause. Common electrical failures include shifts in static electrical characteristics, electrostatic discharge, hillock formation, and junction spiking.

Chemical Failures

Temperature, humidity, stress, and voltage induce chemical reactions leading to different failure mechanisms within the different materials of the package. Common examples are dendrite formation, corrosion, and intermetallic diffusion.

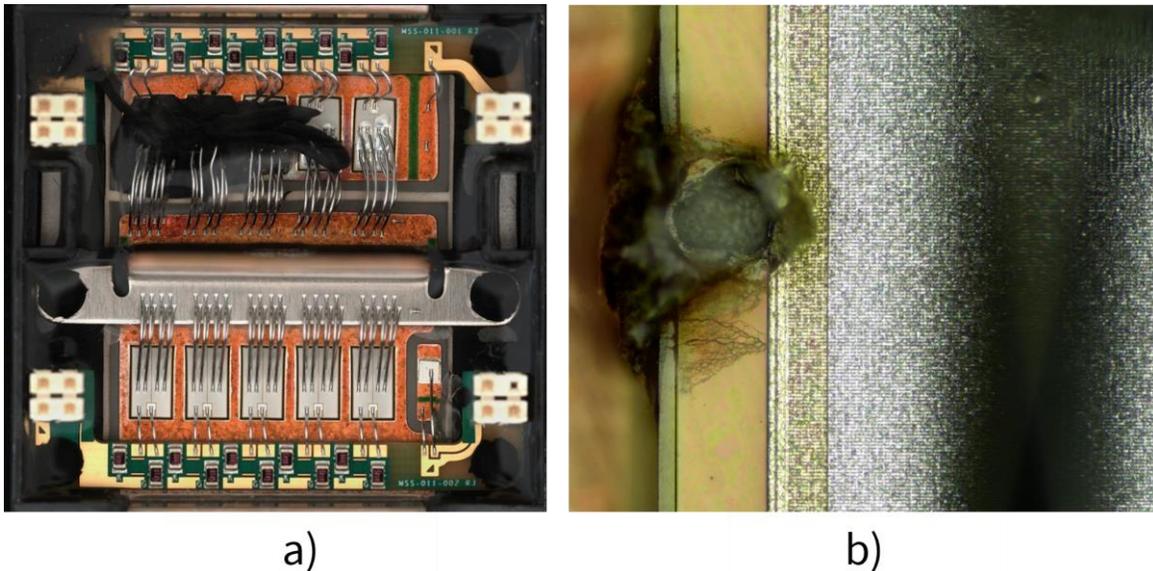


Figure 12: (a) EIPD with a large burn mark that covers the source location and obscures details that would help with root cause analysis. (b) Image of dendrite formation that led to a short between drain and source along the edge termination of the die.

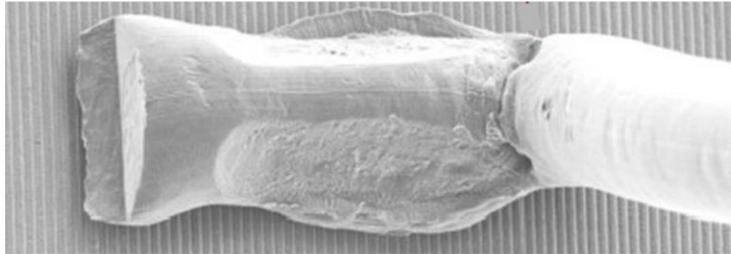
4. Package Limitations

Packaging technology for SiC power devices has not kept pace with developments made to SiC die. Major limitations exist in materials and processing methods that limit the maximum potential of SiC devices in power applications. Interconnects contribute parasitic inductance and non-negligible parasitic resistance into the overall power loop and create various reliability issues [7]. Thermomechanical design strategies and cooling techniques currently available limit device ratings to 175°C - 200°C [1]. Process temperatures for interconnects, encapsulation, die-level metallization stacks, and package level components also limit high-temperature operation [7]. Moving forward, the power industry is pushing to increase the current density-per-unit die area and requires the same high thermal performance of the module [8].

4.1 Limitations of Wire Bonds

Wire bonds are a major limitation to the performance of a module. Wire bonds significantly add to the overall package parasitics, have large footprints, and are one of the weakest components for reliability, with bond-wire heel cracking and lift-off being popular failure methods (shown in Figure 13). Aluminum, the most common wire bond material, limits the ampacity of a system due to the lack of ability to dissipate heat. Copper wire-bonding (shown in Figure 7), though it comes with associated challenges, is an encouraging alternative, with improved thermal/electrical conductivity, high yield strength, improved reliability, and operation at high temperatures. Key process improvements are necessary for the continued adoption of wire bonds at elevated temperatures. Other techniques like the use of copper clips, copper pins, press packs, and double-sided cooling are alternative

interconnect methods with various advantages such as lower parasitics and improved switching performance, heat transfer, and reliability [9].



a)



b)

Figure 13: Wire bond failure due to (a) heel damage and (b) lift off.

4.2 Limitations of Die Attach Methods

Die-attach methods, like soldering, have low melting points and are subject to extreme mechanical stress due to the CTE mismatch with wide-bandgap materials. Newer techniques like sintering have provided improvements, however, reliability failures modes like creep, fatigue, and electrochemical migration persist.

4.3 Limitations of Encapsulation

Encapsulation is another limiting factor in packaging. Encapsulation can either be soft encapsulants like silicon gels and elastomers or hard encapsulants like epoxies. Soft encapsulants have a large CTE mismatch from other components in the module limiting their use at hot temperatures. Epoxies see a similar CTE mismatch and are prone to thermal degradation at elevated temperatures due to their low glass transition temperature [10].

5. How to Identify Package Induced Failures

One challenge for module manufacturers is the ability to pass reliability testing, which requires a large investment of material and time to qualify a product. Performing reliability testing prior to product release helps identify processes that may cause early life-time failures.

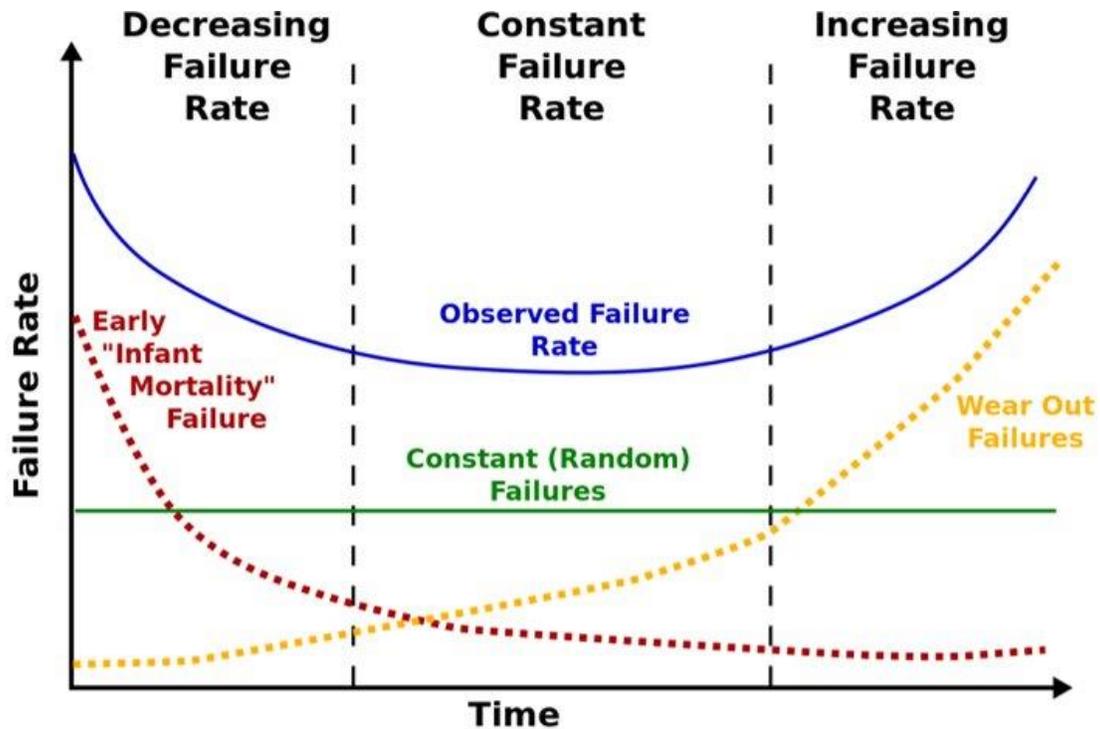


Figure 14: The Bathtub Curve

One method used to depict the failure rate of an entire population of products over time is to reference the bathtub curve shown in Figure 14. The observed failure rate of the population of a product is separated into three regions or curves. The early failure curve (dashed red) has a high probability of early-life failures and has a decreasing failure rate over time. Early failures can occur due to poor yield, manufacturing defects, or design errors and most overstress mechanisms will fail in this region. The constant failure curve (solid green) represents failures that randomly occur at a low or normal rate. The causes of these failures include using the product outside of its datasheet specifications or mishandling the product. The final curve represents wear-out failures (dashed yellow) that occur at the end of the life of the device caused by general fatigue, wear-out mechanisms discussed above, and gradual deterioration. Combining these curves creates a bathtub shape that represents the observed failure rate of a product.

Defects in package assembly methods are inevitable in large-scale production environments. Tool quality can degrade over time and can produce products that fall out of specifications. These products are screened out to avoid early lifetime failure. Common screening methods include visual inspection and end-of-line (EOL) testing. Visual inspection during and after assembly and during accelerated life testing can help identify the root cause of a failure. Typically, EOL testing applies pass/fail criteria based on tolerances set around datasheet specifications. These specifications are often static characteristics but can include reliability and destructive testing specifications. Power module manufacturers can refer to AQG-324 for a list of module-level reliability tests [11]. Failure mechanisms can be identified through reliability, EOL, and destructive testing methods. Overstress mechanisms are commonly identified through EOL and destructive testing such as surge and short-circuit testing. Wear-out mechanisms are often identified through reliability testing.

6. Guide To Determine Failure Mechanism

Often, the root cause of failure is challenging to identify. Many different systematic approaches have been developed to help identify, correct, and eliminate future failures from occurring such as 8D, FMEA, and 5 Whys. It is recommended that these methodologies are utilized before sharing information with Wolfspeed to better understand the cause of failure.

	Pros	Cons
8D	Structured Framework Team Collaboration Focuses on prevention	Complexity Too much focus on symptoms
5 Whys	Simple and Effective Iterative Process	Limited Depth Subjective nature Not always applicable
FMEA	Early Detection of Risk Process Improvement	Complexity Limited Scope

Table 2: Pros and Cons of various corrective methodologies

Information that would be helpful to include after a failure occurs includes any completed FA reports, test type, setup and test parameters, pre- and post-failure DC characteristics, and any waveforms captured before, during, and after the failure.

7. Conclusion

Packaging techniques can often result in a bottleneck, limiting the capability and performance of power modules. Moving forward, the power industry is pushing for devices with lower specific on-state resistance, which will increase the current density of the power die and force the power module to be able to manage the additional heat dissipation. To address this issue, new packaging techniques are being developed and optimized, some of which have been discussed at a high level here. Additionally, there are various types of failures and failure modes that define the limitations of the package. Performing screening, EOL testing, and reliability testing can help to avoid field failures and identify process improvements.

Revision History

Date	Revision	Changes	Authors
May 2025	1	Initial Release	Nicolas Lozada; Sharan Sharma; Josh Pennington

References

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