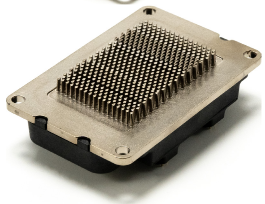
CAB525F12XM3

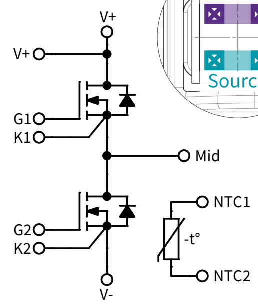
V_{DS}	1200 V
I_{DS}	525 A_{RMS}

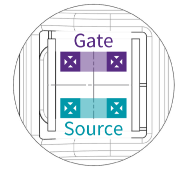
1200 V, 2.6 mΩ, Silicon Carbide, Half-Bridge Module

Technical Features

- High Power Density Footprint
- High Junction Temperature (175 °C) Operation
- Low-Inductance (6.7 nH) Design
- Implements Wolfspeed's Third Generation SiC MOSFET Technology
- Silicon Nitride Insulator and Copper Baseplate
- Advanced Direct Cooling Baseplate







Typical Applications

- Motor and Motion Control
- Vehicle Fast Chargers
- Uninterruptable Power Supplies
- Smart-Grid / Grid-Tied Distributed Generation
- Traction Drives
- E-mobility

System Benefits

- Terminal layout allows for direct bus bar connection without bends or bushings enabling a simple, low-iductance design.
- Isolated, integrated temperature sensing enables high-level temperature protection.
- Dedicated high-side Kelvin-drain pin enables direct voltage sensing for gate driver overcurrent protection.

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Drain-Source Voltage	V_{DS}			1200	V	T_F = 25 °C	
Maximum Gate-Source Voltage	$V_{GS\,max}$	-8		+19	V	Transient	Note 1 Fig. 34
Operational Gate-Source Voltage	$V_{GS\,op}$		-4/+15		V	Static	Note 1 Fig. 34
Implementable Current, Inverter Operation	I_{IMP}			525	A_{RMS}	T_F = 60 °C, F_S = 5 kHz	Fig. 22
DC Continuous Drain Current, Flow Rate = 4 LPM	I_D			450	A	V_{GS} = 15 V, T_F = 25 °C, T_{VJ} ≤ 175 °C	Notes 2, 3, 4 Fig. 20
			411		A	V_{GS} = 15 V, T_F = 60 °C, T_{VJ} ≤ 175 °C	
Pulsed Drain Current	I_{DM}		1050		A	t_{Pmax} limited by $T_{VJ\,op}$ V_{GS} = 15 V, T_F = 25 °C	
Power Dissipation	P_D		1034		W	T_F = 25 °C, T_{VJ} ≤ 175 °C	Note 5 Fig. 21
Operational Virtual Junction Temperature	$T_{VJ(op)}$	-40		175	°C		

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance
Note (2): Current limit at T_F = 25 °C imposed by package
Note (3): Current limit T_F = 60 °C calculated by $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)}(T_{J(max)}, I_{D(max)}))}$
Note (4): Verified by design
Note (5): $P_D = (T_{VJ} - T_F) / R_{TH(JF,\,Typ)}$

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MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6	V	V_{DS} = V_{GS}, I_{DS} = 140 mA	
			2.0			V_{DS} = V_{GS}, I_{DS} = 140 mA, T_{VJ} = 175 °C	
Zero Gate Voltage Drain Current	I_{DSS}		5	200	µA	V_{GS} = 0 V, V_{DS} = 1200 V	
Gate-Source Leakage Current	I_{GSS}		50	1300	nA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (MOSFET Only)	$R_{DS(on)}$		2.6	3.4	mΩ	V_{GS} = 15 V, I_D = 450 A	Fig. 2 Fig. 3
			4.7			V_{GS} = 15 V, I_D = 450 A, T_{VJ} = 175 °C	
Transconductance	g_{fs}		348		S	V_{DS} = 20 V, I_D = 450 A	Fig. 4
			333			V_{DS} = 20 V, I_D = 450 A, T_{VJ} = 175 °C	
Turn-On Switching Energy, T_{VJ} = 25 °C, T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{On}		25.4 24.0 24.4		mJ	V_{DD} = 600 V, I_D = 450 A, V_{GS} = -4 V/15 V, $R_{G\text{-}ON(ext)}$ = 4.0 Ω, $R_{G\text{-}OFF(ext)}$ = 0.0 Ω, L_σ = 10.2 nH	Fig. 11 Fig. 13
Turn-Off Switching Energy, T_{VJ} = 25 °C, T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{Off}		7.5 8.1 8.4				
Internal Gate Resistance	$R_{G(int)}$		2.5		Ω	f = 100 kHz	
Input Capacitance	C_{iss}		38		nF	V_{GS} = 0 V, V_{DS} = 800 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		1.5				
Reverse Transfer Capacitance	C_{rss}		35		pF		
Gate to Source Charge	Q_{GS}		385		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V, I_D = 450 A, Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		475				
Total Gate Charge	Q_G		1300				
FET Thermal Resistance, Junction to Fluid	$R_{th\ JF}$		0.145		°C/W	4 LPM per Module; T_F = 60 °C	Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Body Diode Forward Voltage	V_{SD}		4.7		V	V_{GS} = -4 V, I_{SD} = 450 A	Fig. 7
			4.2			V_{GS} = -4 V, I_{SD} = 450 A, T_{VJ} = 175 °C	
Reverse Recovery Time	t_{RR}		78		ns	V_{GS} = -4 V, I_{SD} = 450 A, V_R = 600 V, di/dt = 5.1 A/ns, $R_{G\text{-}ON(ext)}$ = 4.0 Ω, T_{VJ} = 175 °C	
Reverse Recovery Charge	Q_{RR}		7.2		µC		
Peak Reverse Recovery Current	I_{RRM}		169		A		
Reverse Recovery Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{RR}		0.2 0.9 1.1		mJ	V_{DD} = 600 V, I_D = 450 A, V_{GS} = -4 V/15 V, $R_{G\text{-}ON(ext)}$ = 4.0 Ω, L_σ = 10.2 nH	Fig. 14

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Temperature Sensor (NTC) Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resistance at 25 °C	R_{25}		4700		Ω	T_{NTC} = 25 °C
Tolerance of R_{25}				±1	%	
Beta Value for 25°C to 85°C	$B_{25/85}$		3435		K	
Beta Value for 0°C to 100°C	$B_{0/100}$		3399		K	
Tolerance of $B_{25/85}$				±1	%	
Maximum Power Dissipation	P_{25}			50	mW	

Steinhart & Hart Coefficients for NTC Resistance & NTC Temperature Computation (T in K)

$$\ln\left(\frac{R}{R_{25}}\right) = A + \frac{B}{T} + \frac{C}{T^2} + \frac{D}{T^3}$$

A	B	C	D
-1.289E+01	4.245E+03	-8.749E+04	-9.588E+06

$$\frac{1}{T} = A_1 + B_1 \ln\left(\frac{R}{R_{25}}\right) + C_1 \ln^2\left(\frac{R}{R_{25}}\right) + D_1 \ln^3\left(\frac{R}{R_{25}}\right)$$

A_1	B_1	C_1	D_1
3.354E-03	3.001E-04	5.085E-06	2.188E-07

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Package Resistance, M1 (High-Side)	$R_{3\text{-}1}$		0.72		mΩ	T_C = 125°C, Note 6 & 7
Package Resistance, M2 (Low-Side)	$R_{1\text{-}2}$		0.63		mΩ	T_C = 125°C, Note 6 & 7
Stray Inductance	L_{Stray}		6.7		nH	Between terminals 2 & 3, f = 10 MHz
Case Temperature	T_C	-40		125	°C	
Mounting Torque	M_S	2.0	3.0	4.0	N-m	Baseplate, M4 bolts
		2.0	4.0	5.0		Power Terminals, M5 bolts
Weight	W		188		g	
Case Isolation Voltage	V_{isol}	4.0			kV	AC, 50 Hz, 1 minute
Comparative Tracking Index	CTI	600				
Clearance Distance		12.5			mm	From 2 to 3, Note 7
		11.5			mm	From 1 to Baseplate, Note 7
		5.7			mm	From 2 to 5, Note 7
		13.7			mm	From 5 to Baseplate, Note 7
Creepage Distance		14.7			mm	From 2 to 3, Note 7
		14.0			mm	From 1 to Baseplate, Note 7
		14.7			mm	From 2 to 5, Note 7
		14.3			mm	From 5 to Baseplate, Note 7

Note (6): Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance
Note (7): Numbers reference the connections from the Schematics and Pin Out section of this document

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Typical Performance

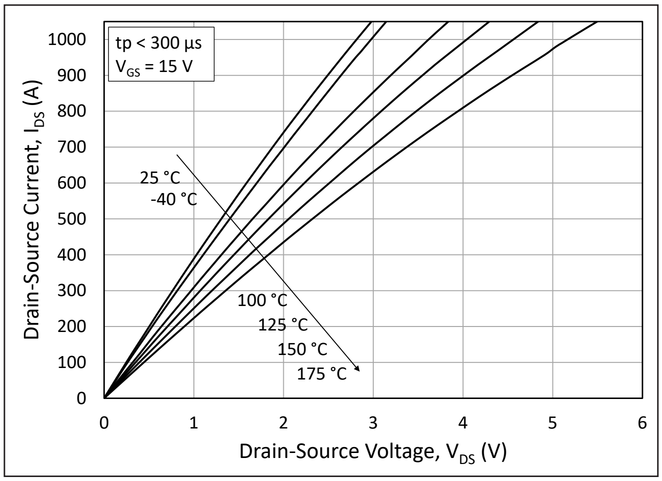

Figure 1. Output Characteristics for Various Junction Temperatures

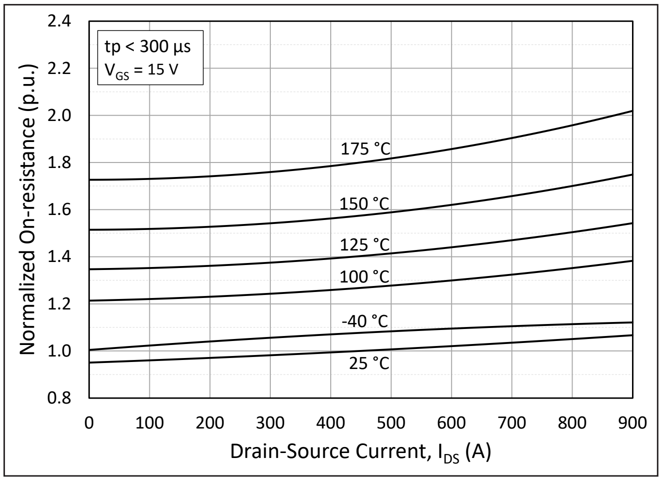

Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

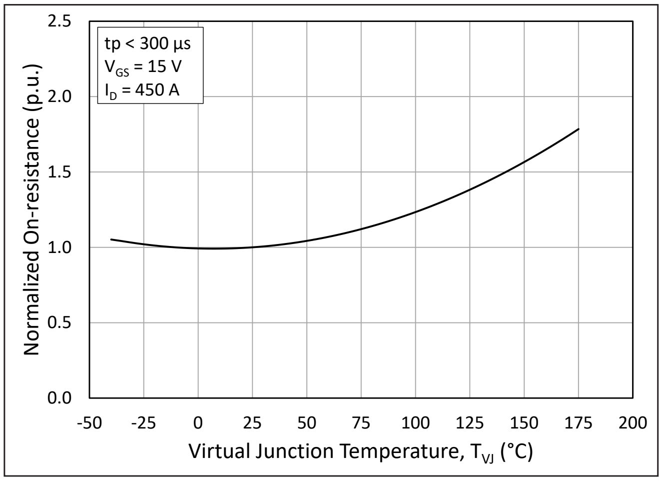

Figure 3. Normalized On-State Resistance vs. Junction Temperature

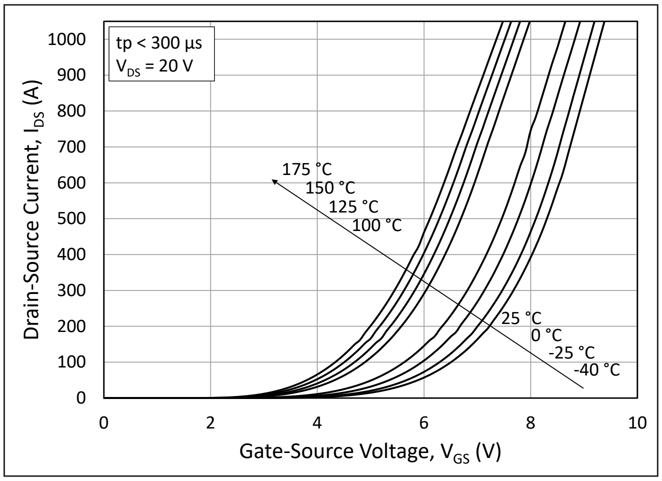

Figure 4. Transfer Characteristic for Various Junction Temperatures

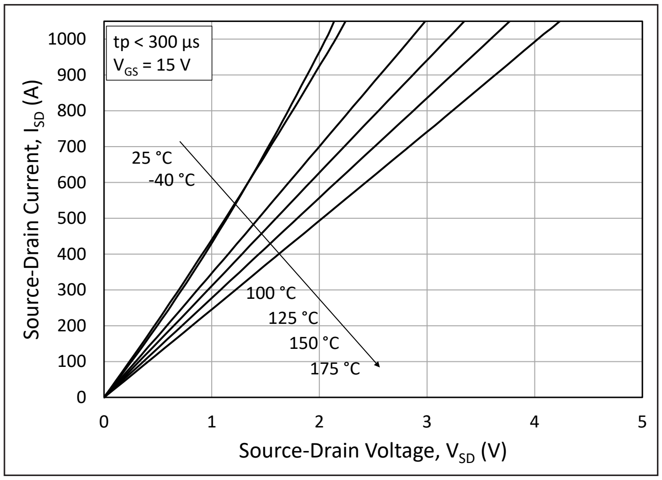

Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

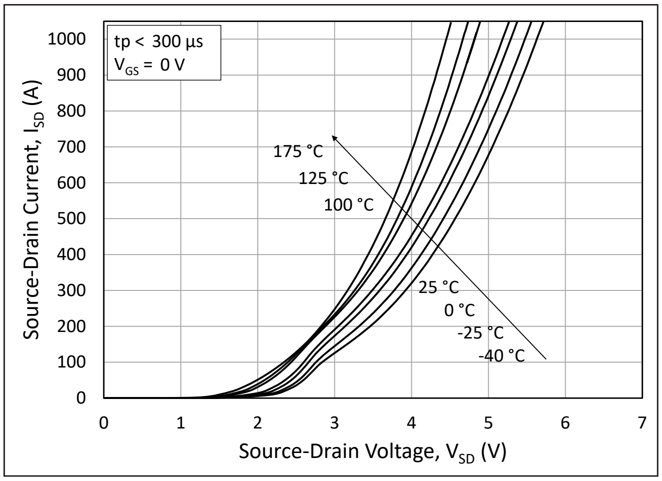

Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Body Diode)

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Typical Performance

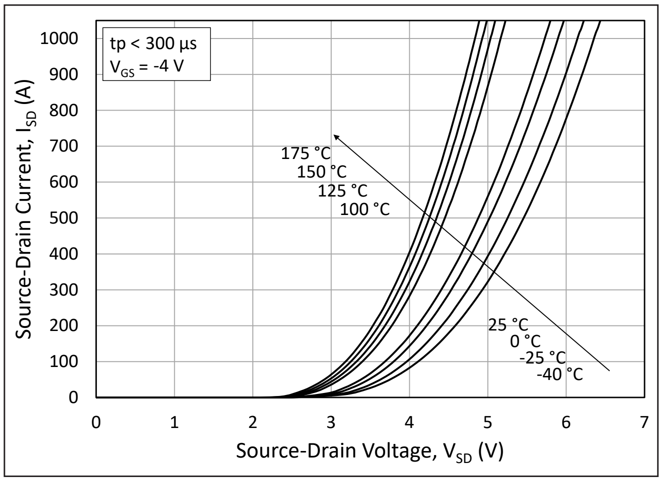

Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = - 4 V (Body Diode)

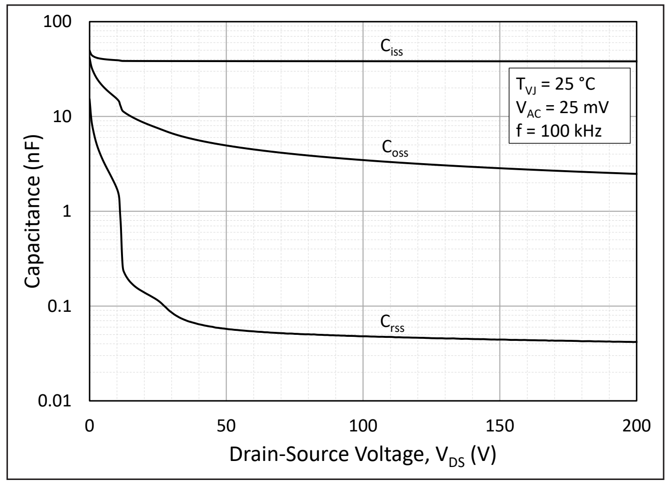

Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

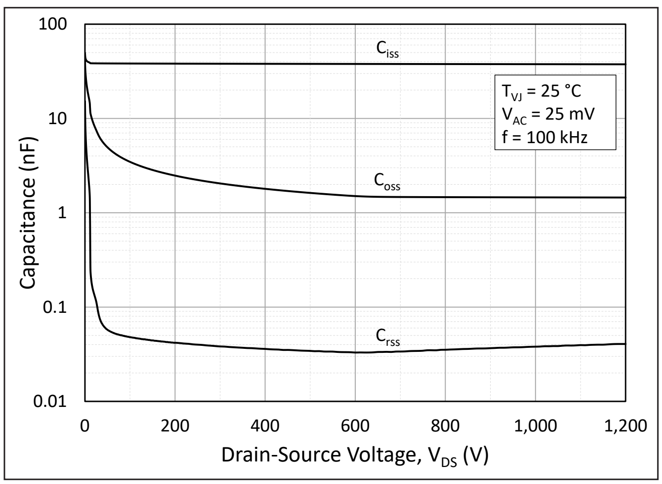

Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

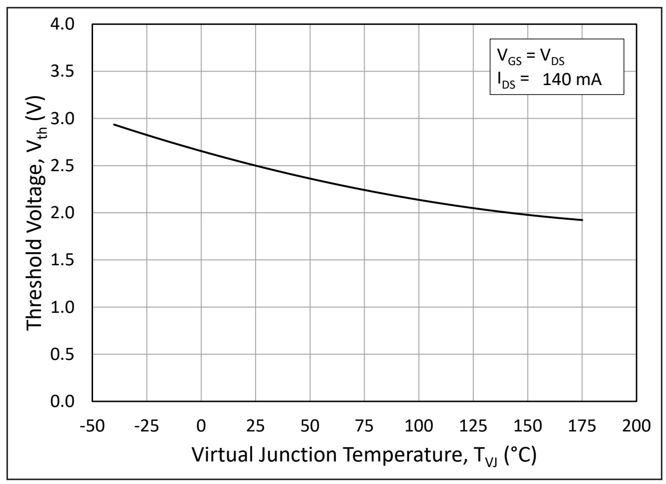

Figure 10. Threshold Voltage vs. Junction Temperature

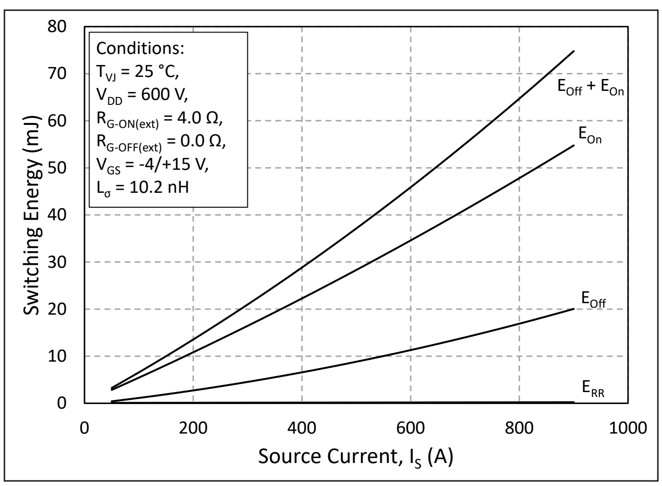

Figure 11. Switching Energy vs. Drain Current (V_{DD} = 600 V)

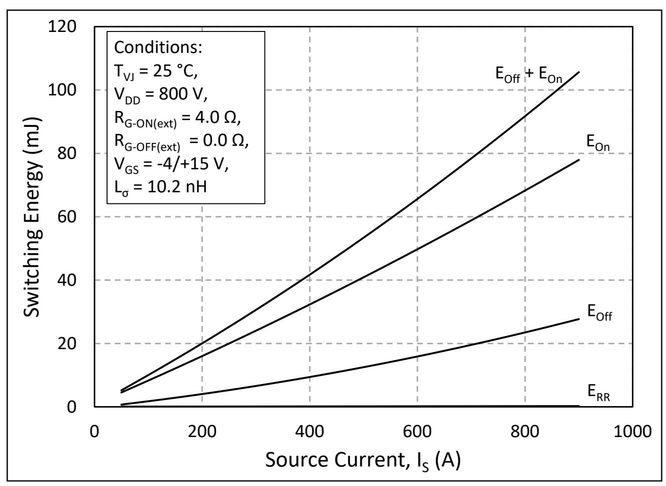

Figure 12. Switching Energy vs. Drain Current (V_{DD} = 800 V)

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Typical Performance

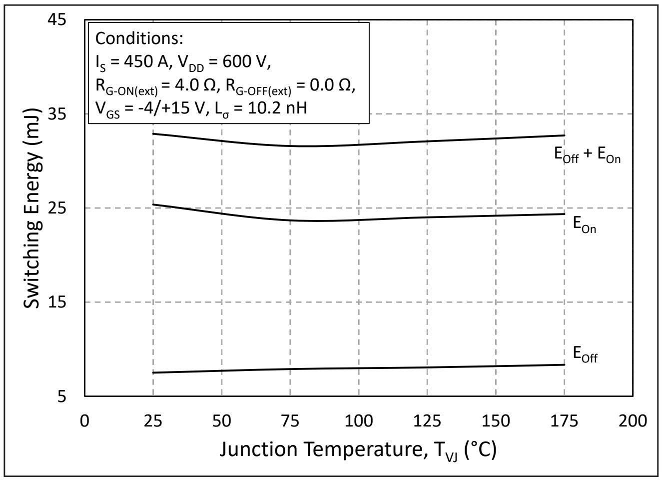

Figure 13. MOSFET Switching Energy vs. Junction Temperature

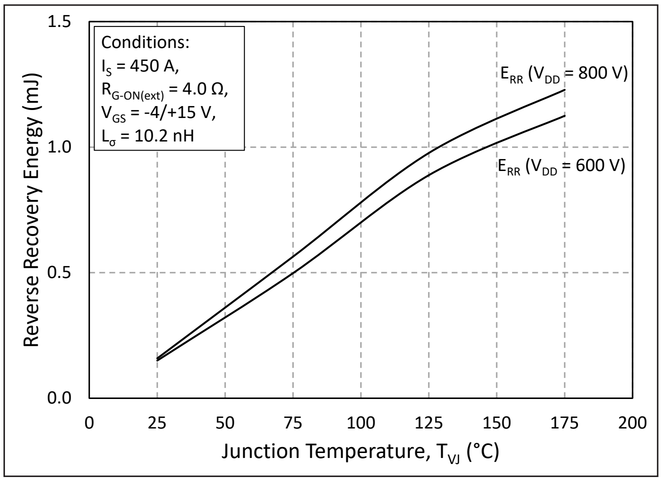

Figure 14. Reverse Recovery Energy vs. Junction Temperature

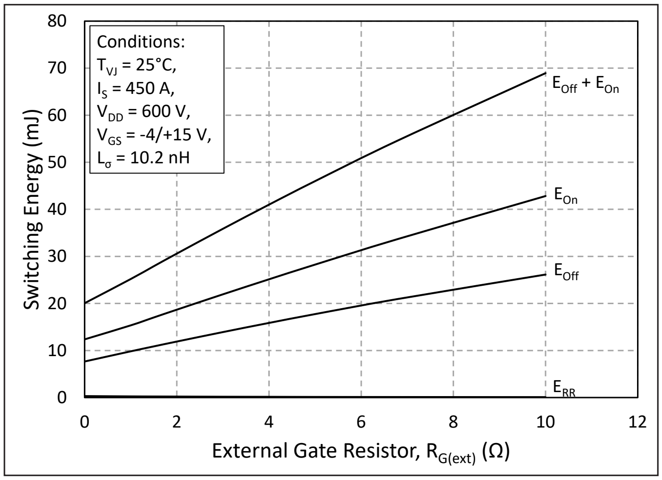

Figure 15. MOSFET Switching Energy vs. External Gate Resistance

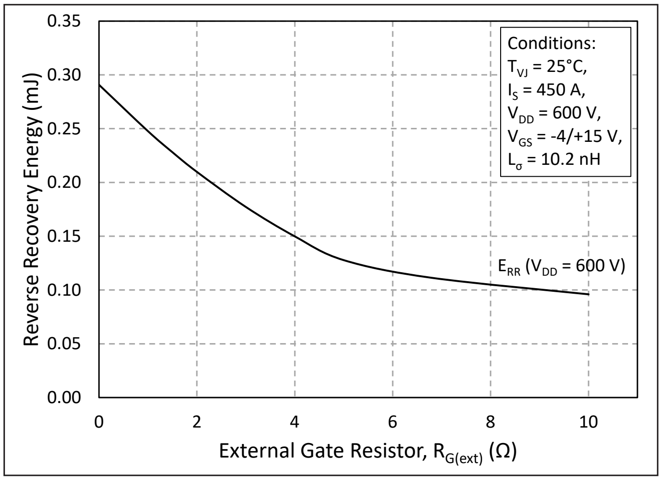

Figure 16. Reverse Recovery Energy vs. External Gate Resistance

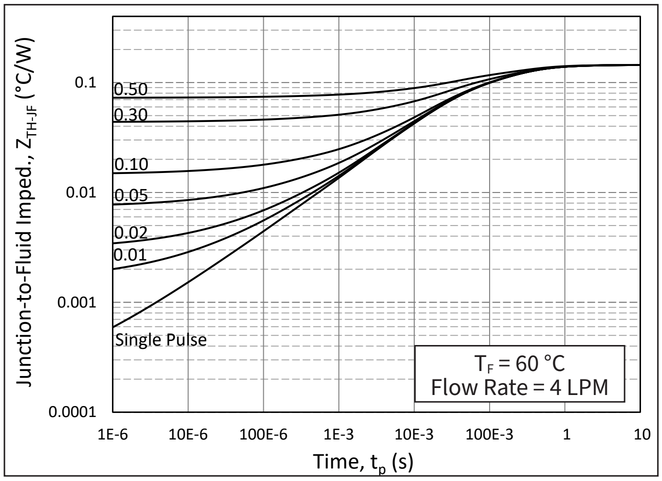

Figure 17. MOSFET Junction to Fluid Transient Thermal Impedance, $Z_{th\ JF}$ (°C/W)

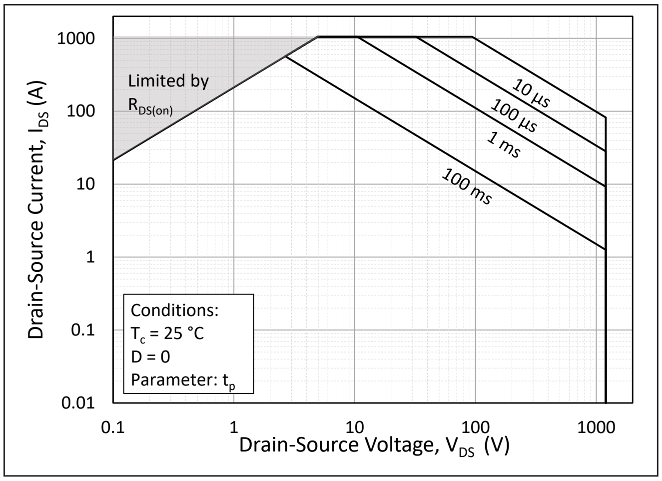

Figure 18. Forward Bias Safe Operating Area (FBSOA)

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Typical Performance

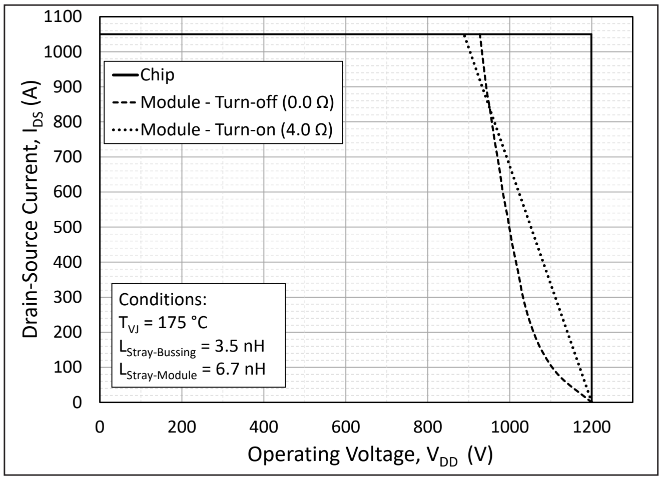

Figure 19. Switching Safe Operating Area

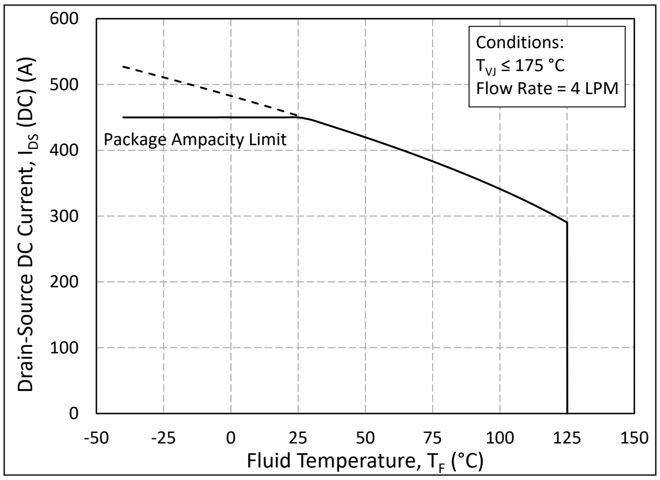

Figure 20. Continuous Drain Current Derating vs. Liquid Temperature

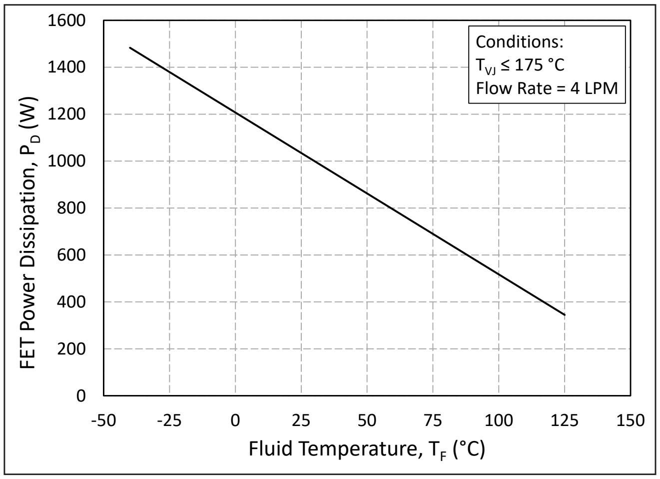

Figure 21. Maximum Power Dissipation Derating vs. Liquid Temperature

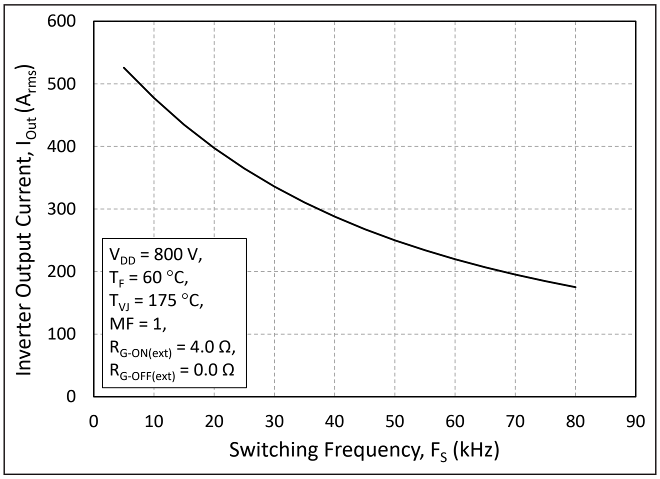

Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

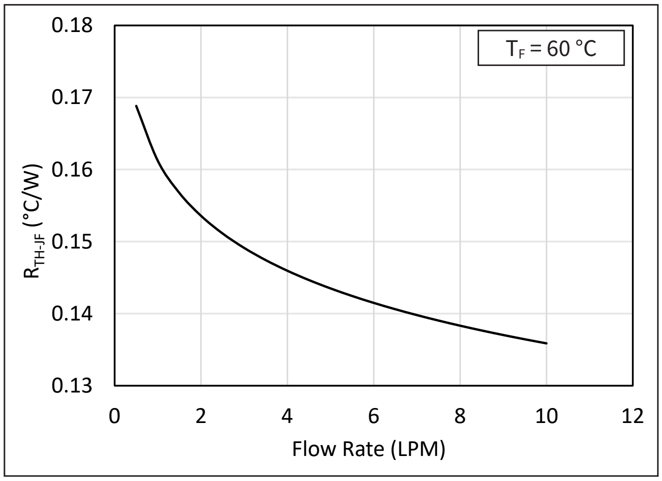

Figure 23. Typical R_{TH-JF} vs Flow Rate

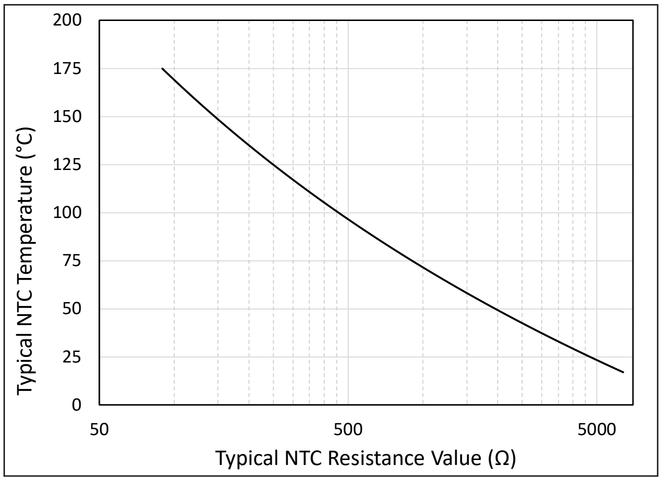

Figure 24. Typical NTC Resistance vs. Temperature

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Timing Characteristics

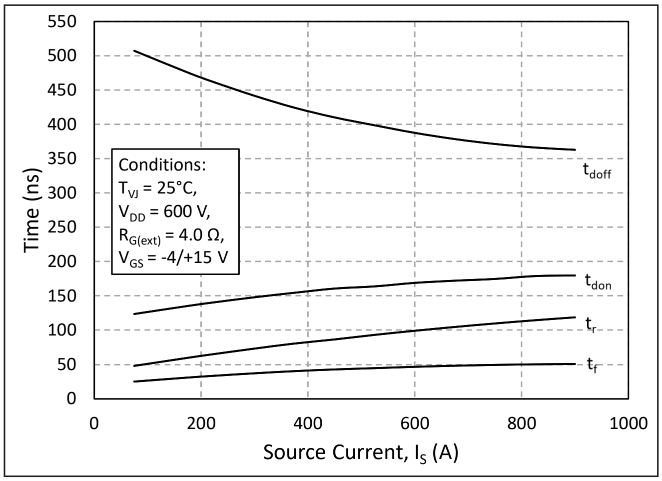

Figure 25. Timing vs. Source Current

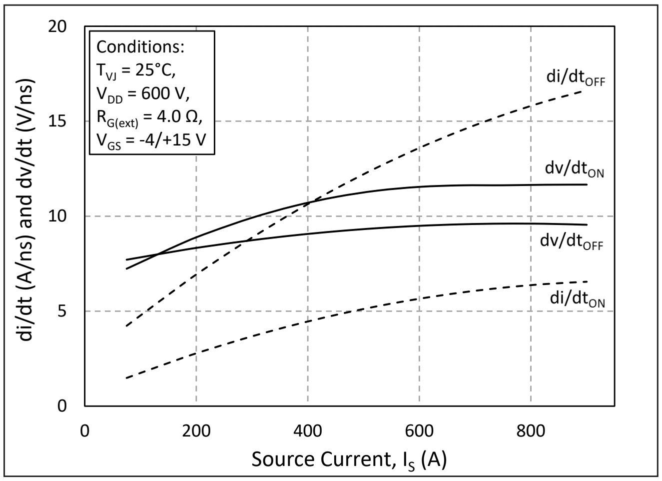

Figure 26. dv/dt and di/dt vs. Source Current

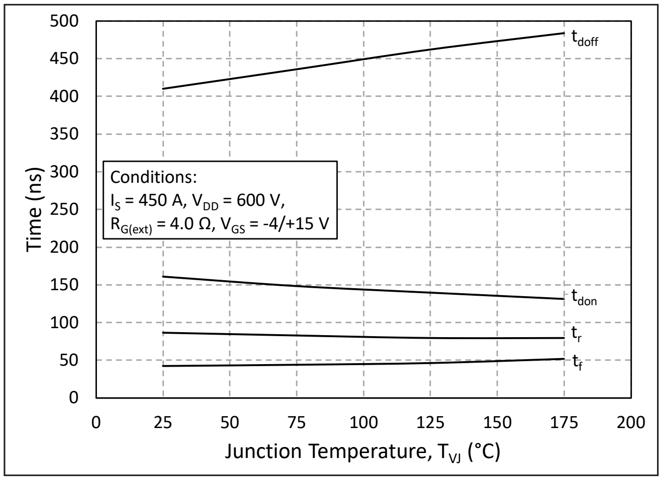

Figure 27. Timing vs. Junction Temperature

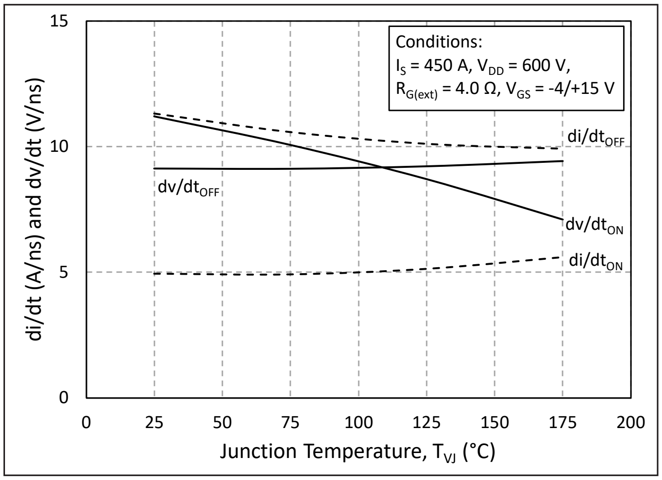

Figure 28. dv/dt and di/dt vs. Junction Temperature

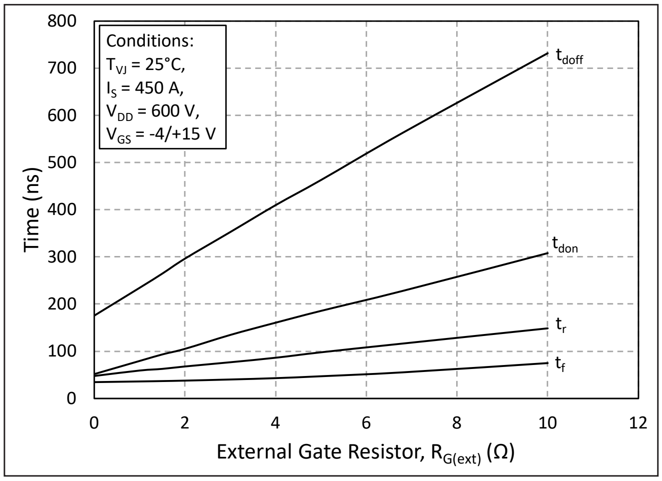

Figure 29. Timing vs. External Gate Resistance

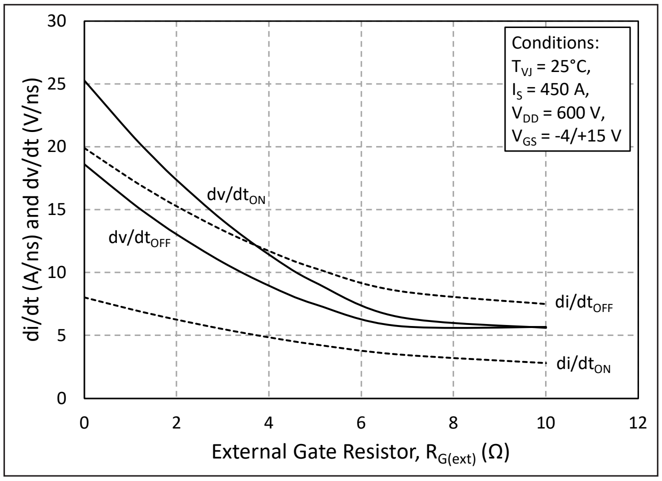

Figure 30. dv/dt and di/dt vs. External Gate Resistance

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Definitions

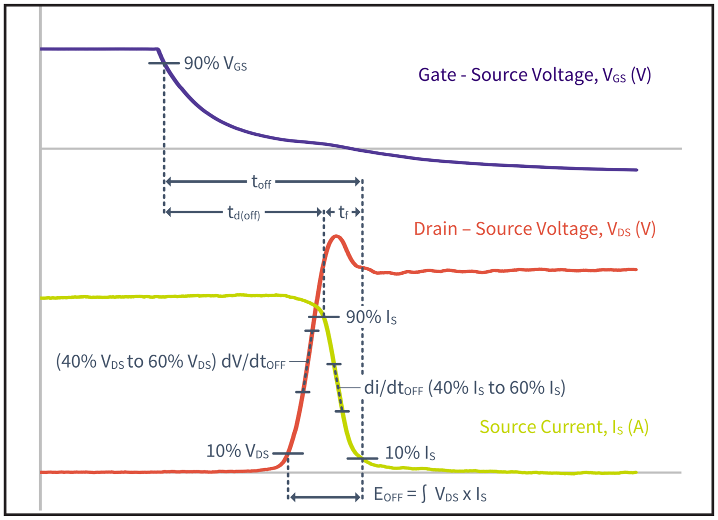

Figure 31. Turn-off Transient Definitions

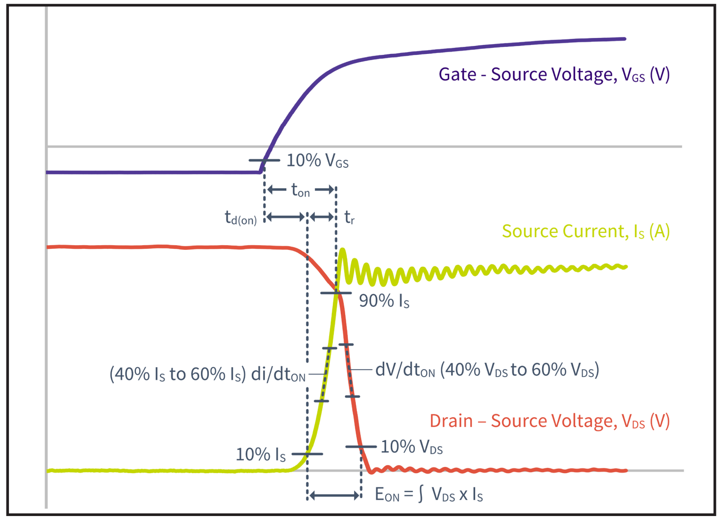

Figure 32. Turn-on Transient Definitions

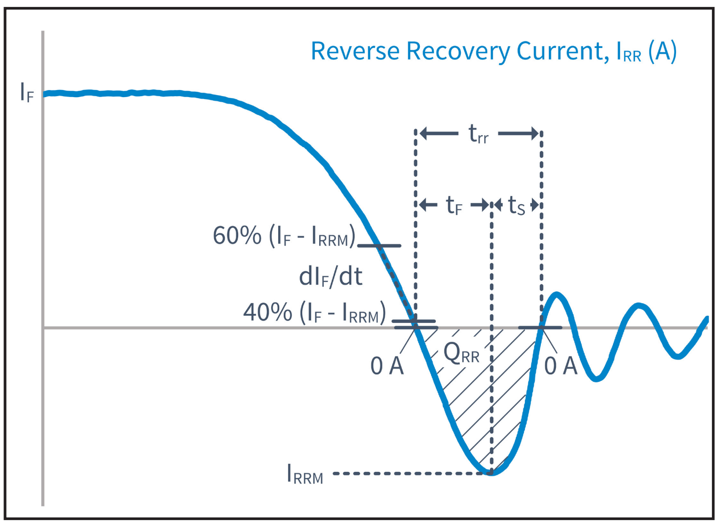

Figure 33. Reverse Recovery Definitions

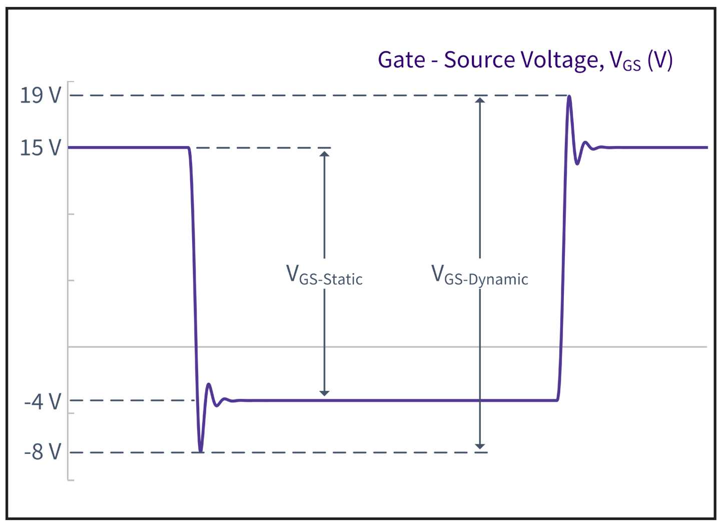

Figure 34. V_{GS} Transient Definitions

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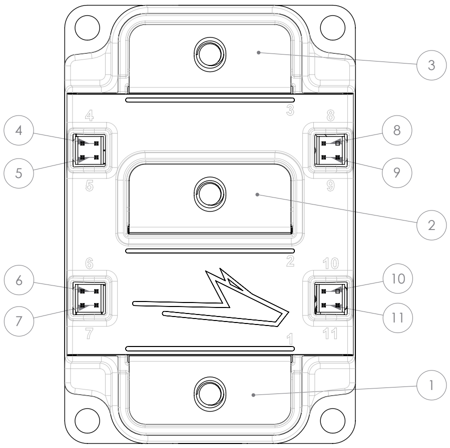
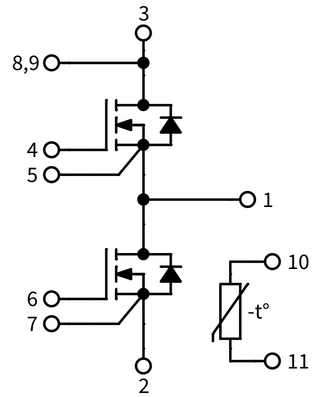
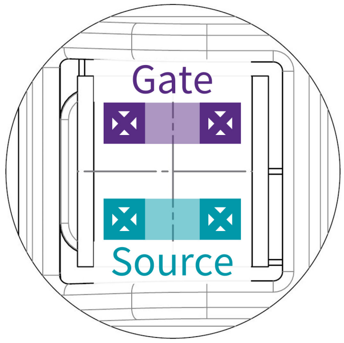
Schematic and Pin Out

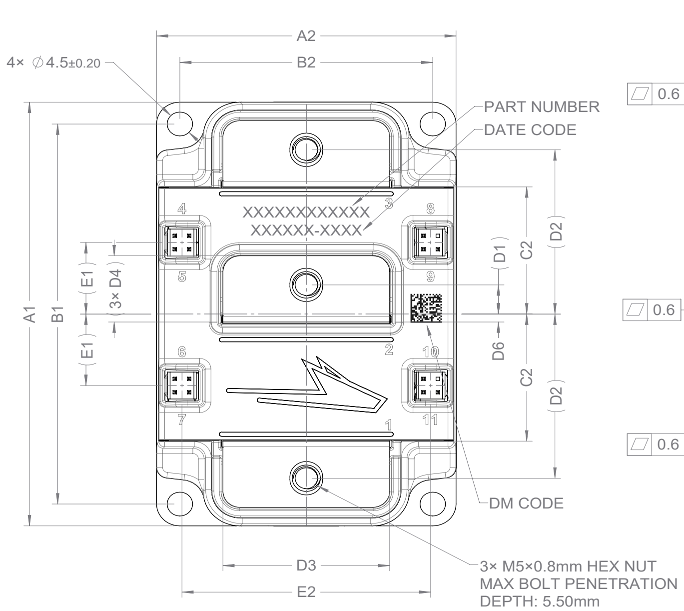


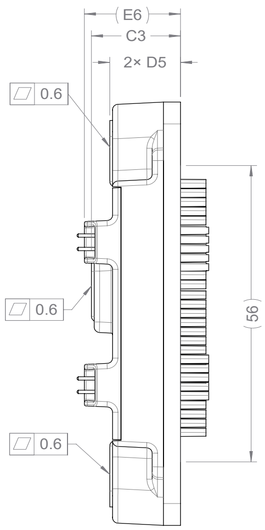


Zoom View of Signal Pinout

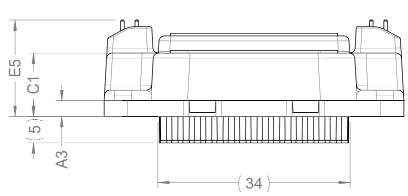


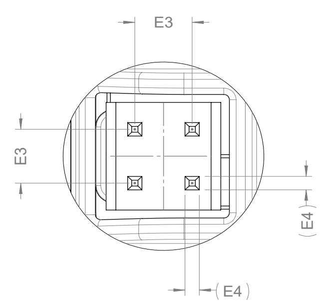
Package Dimension (mm)





DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	80.00	±0.30
A2	53.00	±0.30
A3	3.00	±0.30
B1	71.75	±0.50
B2	44.75	±0.50
C1	12.00	+0.80 -0.30
C2	24.00	±0.90
C3	15.75	+1.52 -0.70
D1	(5.50)	REF.
D2	(31.00)	REF.
D3	29.50	±0.35
D4	(3× 12.50)	REF.
D5	2× 12.50	+1.51 -0.94
D6	1.50	±1.5
E1	(13.50)	REF.
E2	44.00	±0.50
E3	2.54	±0.50
E4	(0.64)	REF.
E5	18.31	+1.07 -1.06
E6	(17.00)	REF.





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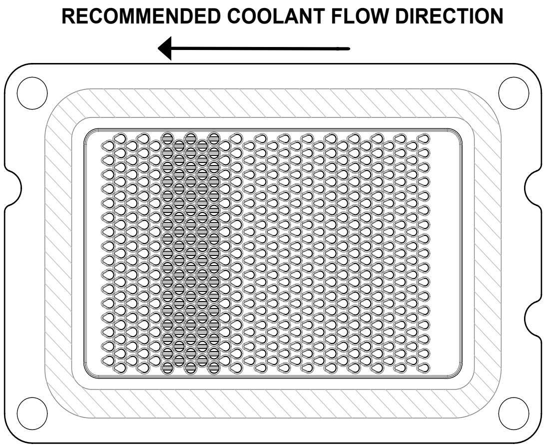
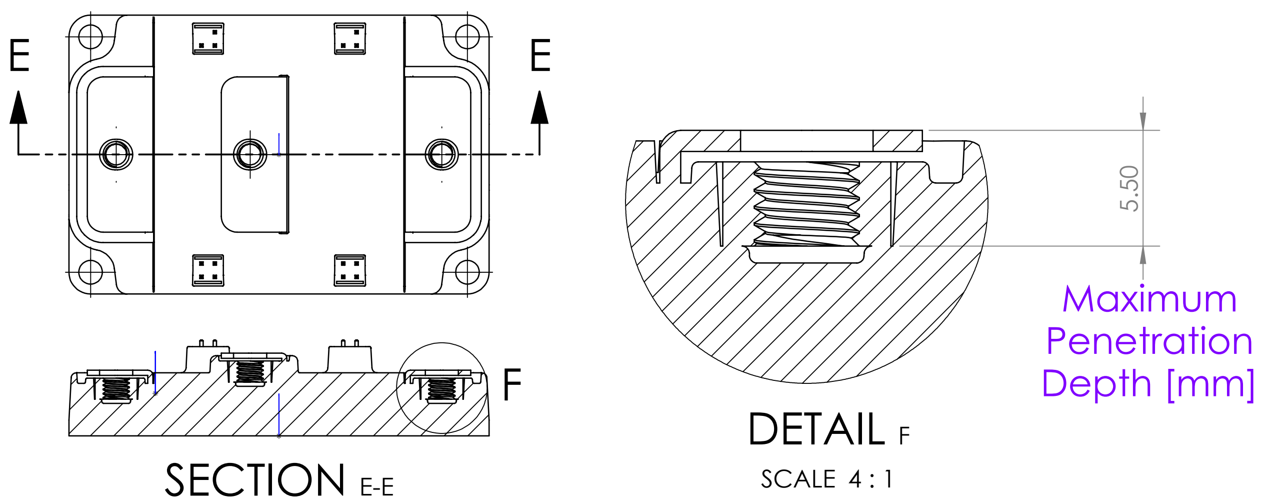
PinFin Flow Direction



Package Dimensions (mm)



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Supporting Links & Tools

Evaluation Tools & Support

- All SiC Module PLECS Models
- All SiC Module LTspice Models
- KIT-CRD-CIL12N-XM3: Dynamic Performance Evaluation Board for the XM3 Module
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum

Dual-Channel Gate Driver Board

- CGD12HBXMP: XM3 Evaluation Gate Driver
- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers
- FRDMGD3160XM3EVM: GD3160 XM3 Half-Bridge Evaluation Kit
- UCC5880QEVM-057 Evaluating Gate Driver for Wolfspeed XM3 Modules
- UCC5880INVERTEREVM Evaluating Board for Wolfspeed XM3 Modules
- Si828x Gate Driver Boards for Wolfspeed XM3 Modules

Application Notes

- XM Module Signal Pinout Clarification Guide
- XM Mounting Guide
- XM3 Thermal Interference Material Guide
- Thermal Characterization Methods and Applications
- PRD-06832: Design Options for Wolfspeed® Silicon Carbide MOSFET Gate Bias Power Supplies

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