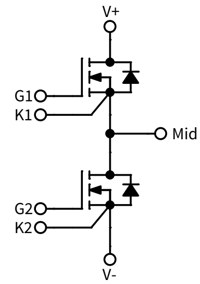
CAB3R5M12DM4

1200 V, 3.5 mΩ, Silicon Carbide, Half-Bridge Module

V_{DS}	**1200 V**
I_{DS}	**300 A**

Technica Features

- Ultra-Low Loss
- High Frequency Operation
- Light Weight AlSiC Baseplate
- Zero Turn-Off Tail Current from MOSFET
- Normally-Off, Fail-Safe Device Operation



Typical Applications

- e-Mobility and Motor Drives
- EV Chargers
- High-Efficiency Converters / Inverters
- Renewable Energy

System Benefits

- Enables Compact, Lightweight Systems
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Voltage	V_{DS}			1200	V		
Gate-Source Voltage, Maximum Value	$V_{GS\,(max)}$	-8		+19		Transient	Fig. 32 Note 1
Gate-Source Voltage, Recommended	$V_{GS\,(op)}$		-4/+15			Static	
DC Continuous Drain Current (T_{VJ} < 175 °C)	I_D		383		A	V_{GS} = 15 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	Notes 2, 3, 5 Fig. 20
			293			V_{GS} = 15 V, T_C = 90 °C, T_{VJ} ≤ 175 °C	
Pulsed Drain Current	I_{DM}		766			t_{Pmax} limited by T_{VJmax} V_{GS} = 15 V, T_C = 25 °C	
Power Dissipation	P_D		980		W	T_C = 25 °C, T_{VJ} ≤ 175 °C	Fig. 21 Note 4
Operational Virtual Junction Temperature	$T_{VJ(op)}$	-40		175	°C		

Note (1): Recommended turn-on gate voltage is 15 V with ±5% regulation tolerance

Note (2): Current limit calculated by $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)}(T_{VJ(max)}, I_{D(max)}))}$

Note (3): Verified by design

Note (4): $P_D = (T_{VJ} - T_C) / R_{TH(JC,typ)}$

Note (5): Please refer to Application Note, PRD-07635, for guidance on PCB ampacity

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MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.7	3.6	V	V_{DS} = V_{GS}, I_D = 81 mA	
			2.2			V_{DS} = V_{GS}, I_D = 81 mA, T_{VJ} = 175 °C	
Zero Gate Voltage Drain Current	I_{DSS}		4	200	μA	V_{GS} = 0 V, V_{DS} = 1200 V	
Gate-Source Leakage Current	I_{GSS}		40	1000	nA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		3.5	4.6	mΩ	V_{GS} = 15 V, I_D = 311 A	Fig. 2 Fig. 3
			6.5			V_{GS} = 15 V, I_D = 311 A, T_{VJ} = 175 °C	
Transconductance	g_{fs}		278		S	V_{DS} = 20 V, I_D = 311 A	Fig. 4
			273			V_{DS} = 20 V, I_D = 311 A, T_{VJ} = 175 °C	
Turn-On Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{On}		3.7 3.7 3.8		mJ	V_{DD} = 600 V, I_D = 300 A, V_{GS} = -4 V/15 V, $R_{G(EXT)}$ = 0 Ω $L_σ$ = 17.4 nH	Fig. 11 Fig. 13
Turn-Off Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{Off}		3.0 3.2 3.3				
Internal Gate Resistance	$R_{G(int)}$		1.6		Ω	f = 100 kHz	
Input Capacitance	C_{iss}		29		nF	V_{GS} = 0 V, V_{DS} = 800 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		0.9				
Reverse Transfer Capacitance	C_{rss}		73		pF		
Gate to Source Charge	Q_{GS}		268		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V, I_D = 311 A, Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		312				
Total Gate Charge	Q_G		1044				
FET Thermal Resistance, Junction to Case	$R_{th\ JC}$		0.153		°C/W		Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
Body Diode Forward Voltage	V_{SD}		6.2		V	V_{GS} = -4 V, I_{SD} = 311 A	Fig. 7
			5.7			V_{GS} = -4 V, I_{SD} = 311 A, T_{VJ} = 175 °C	
DC Source-Drain Current (Body Diode)	I_{BD}		192		A	V_{GS} = -4 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	
			131			V_{GS} = -4 V, T_C = 90 °C, T_{VJ} ≤ 175 °C	
Reverse Recovery Time	t_{RR}		38.3		ns	V_{GS} = -4 V, I_{SD} = 300 A, V_R = 600 V di/dt = 19.3 A/ns, T_{VJ} = 175 °C	Fig. 31
Reverse Recovery Charge	Q_{RR}		6.2		µC		
Peak Reverse Recovery Current	I_{RRM}		269		A		
Reverse Recovery Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{RR}		1.1 1.6 2.6		mJ	V_{DD} = 600 V, I_D = 300 A, V_{GS} = -4 V/15 V, $R_{G(ON)}$ = 0 Ω, L_σ = 17.4 nH	Fig. 14

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Package Resistance, M1 (High-Side)	$R_{3\text{-}1}$		0.41		mΩ	T_C = 125°C, Note 6
Package Resistance, M2 (Low-Side)	$R_{1\text{-}2}$		0.56			T_C = 125°C, Note 6
Stray Inductance	L_{Stray}		10.9		nH	Between DC- and DC+, f = 10 MHz
Case Temperature	T_C	-40		125	°C	
Mounting Torque	M_S		1.1	2.3	N-m	Baseplate, M4 bolts
Weight	W		41		g	
Case Isolation Voltage	V_{isol}	4			kV	AC, 50 Hz, 1 minute
Comparative Tracking Index	CTI	600				
Clearance Distance			4.2		mm	Terminal to Terminal
			13.4			Terminal to Heatsink
Creepage Distance			8.8			Terminal to Terminal
			15.5			Terminal to Heatsink

Note (6): Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance

Typical Performance

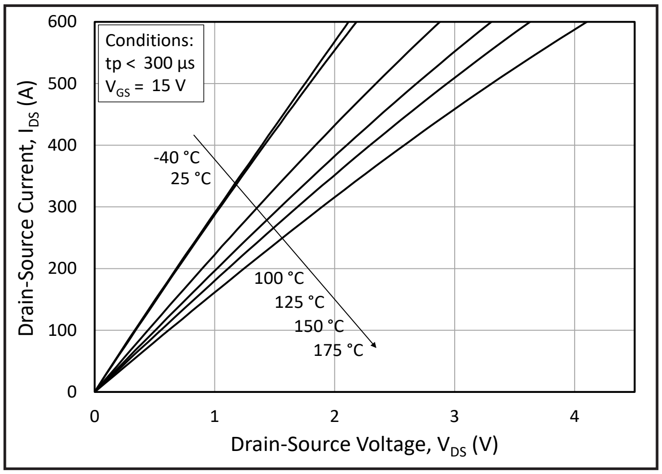


Figure 1. Output Characteristics for Various Junction Temperatures

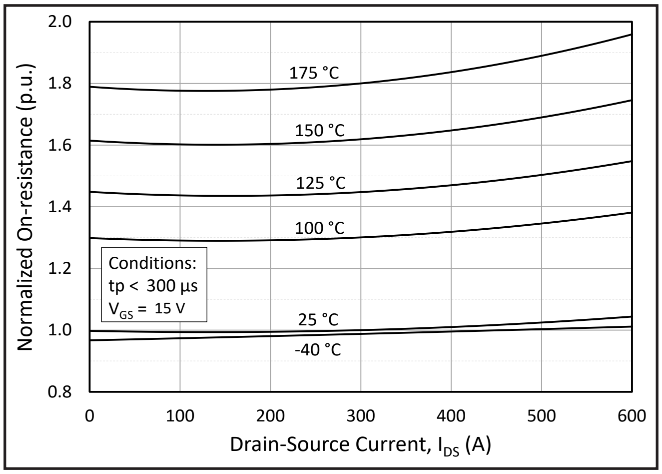


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

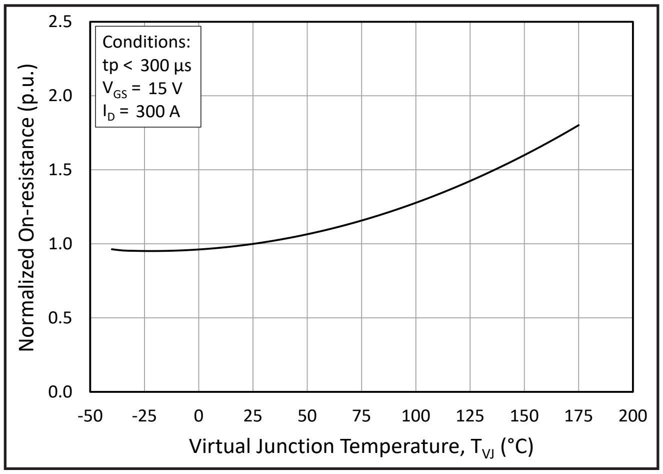


Figure 3. Normalized On-State Resistance vs. Junction Temperature

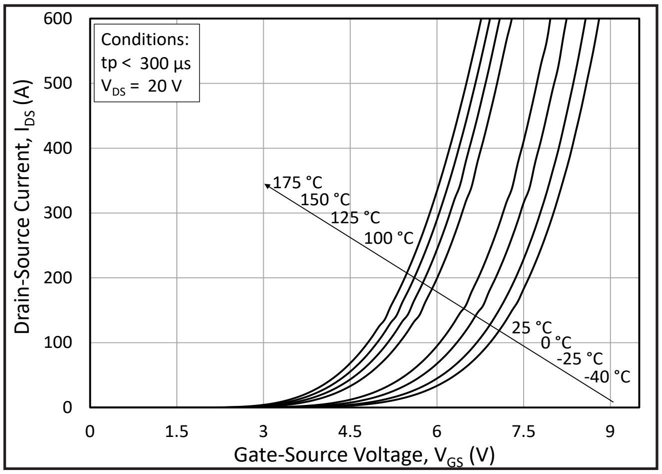


Figure 4. Transfer Characteristic for Various Junction Temperatures

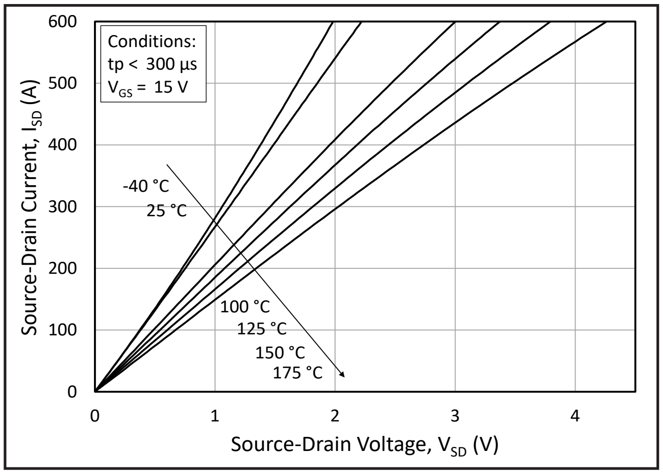


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

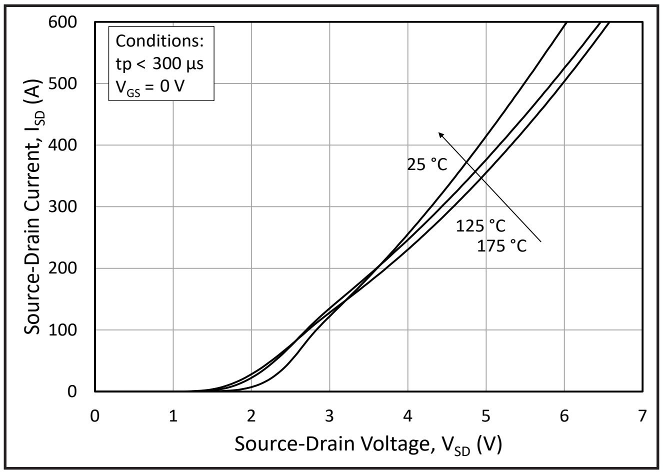


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Body Diode)

Typical Performance

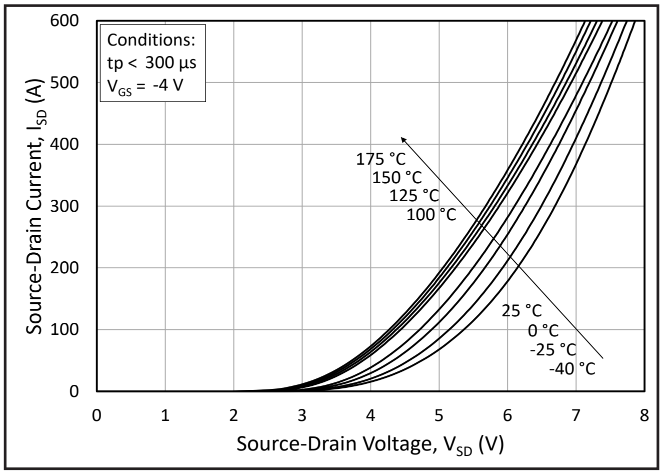


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = - 4 V (Body Diode)

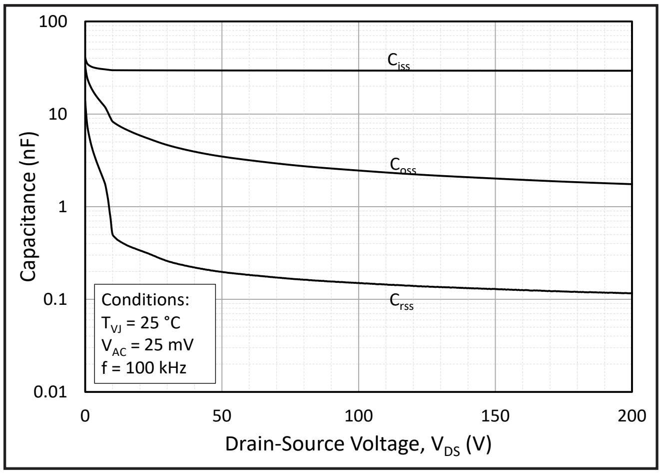


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

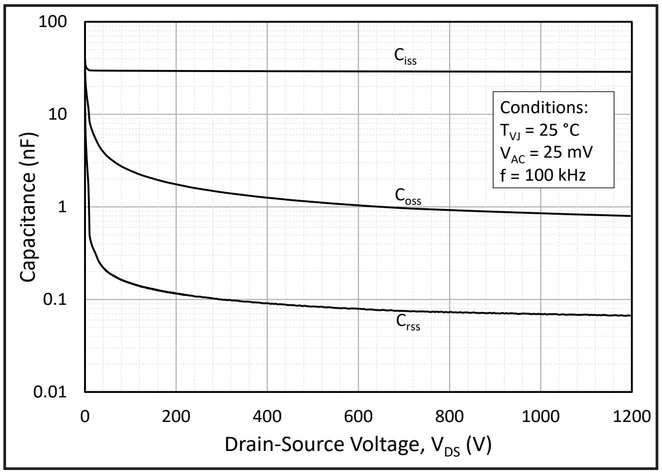


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

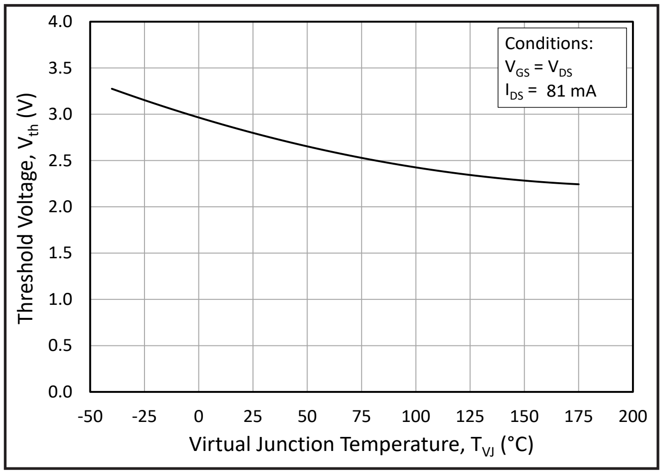


Figure 10. Threshold Voltage vs. Junction Temperature

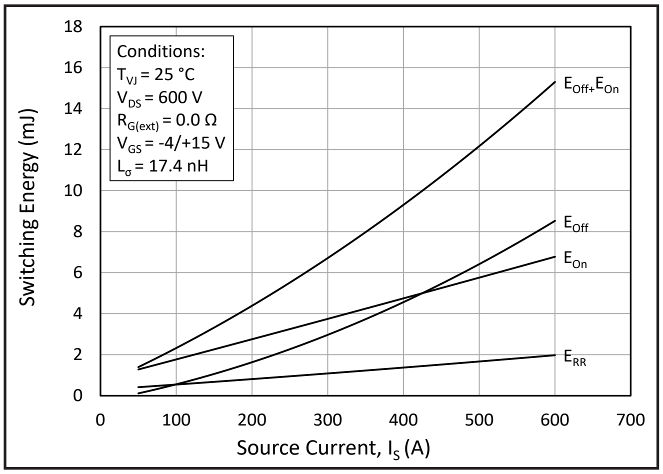


Figure 11. Switching Energy vs. Drain Current (V_{DD} = 600 V)

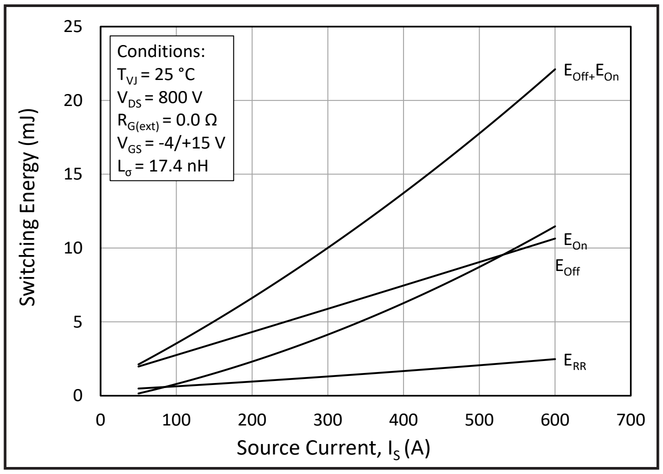


Figure 12. Switching Energy vs. Drain Current (V_{DD} = 800 V)

Typical Performance

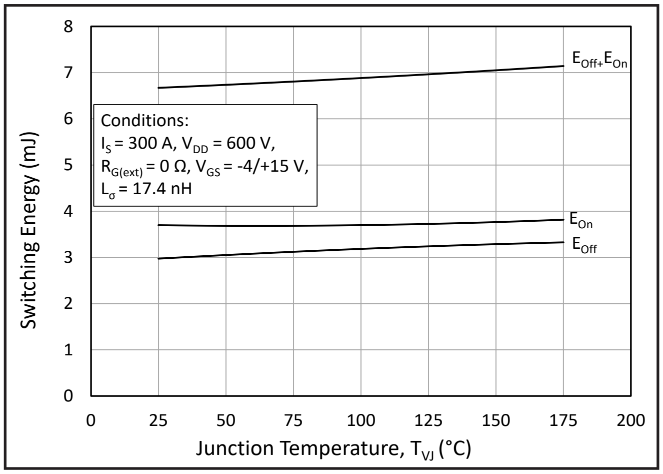


Figure 13. MOSFET Switching Energy vs. Junction Temperature

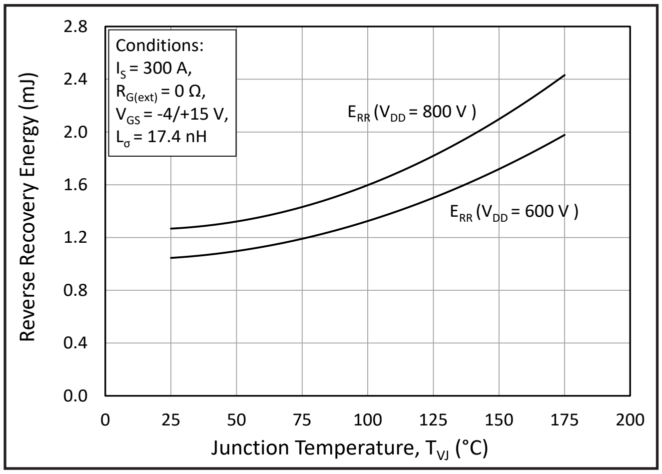


Figure 14. Reverse Recovery Energy vs. Junction Temperature

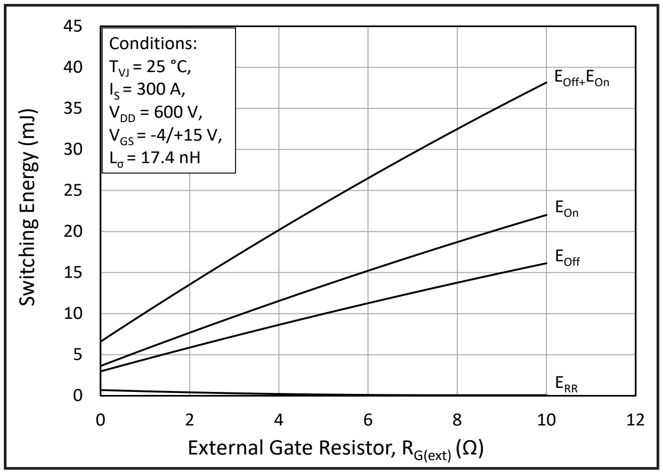


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

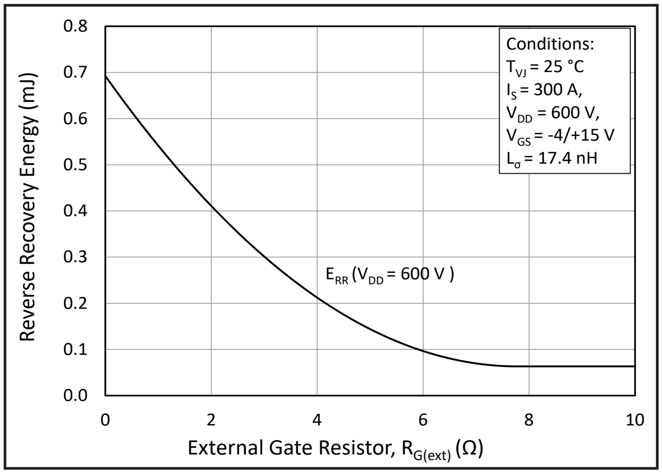


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

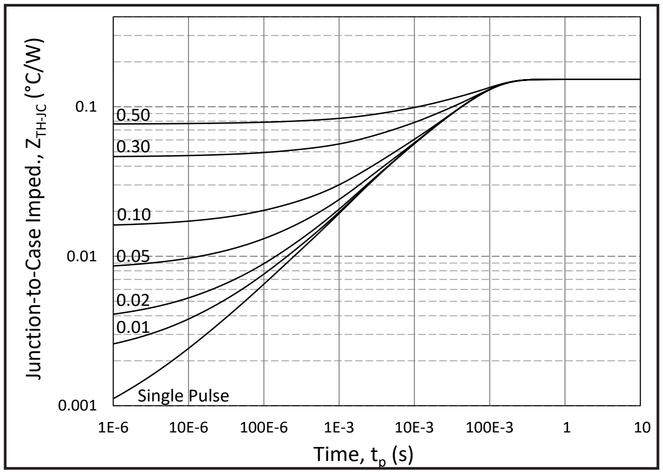


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, $Z_{th\ JC}$ (°C/W)

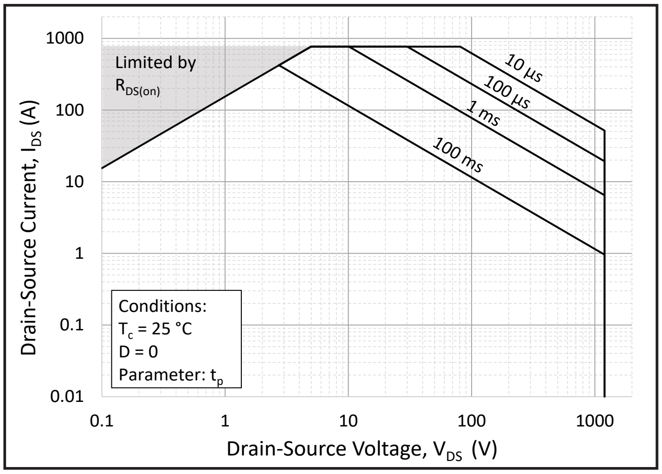


Figure 18. Forward-Bias Safe Operating Area (FBSOA)

Typical Performance

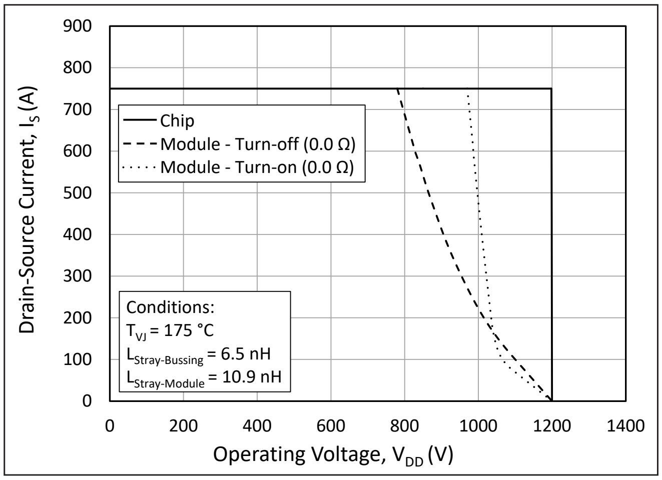


Figure 19. Switching Safe Operating Area

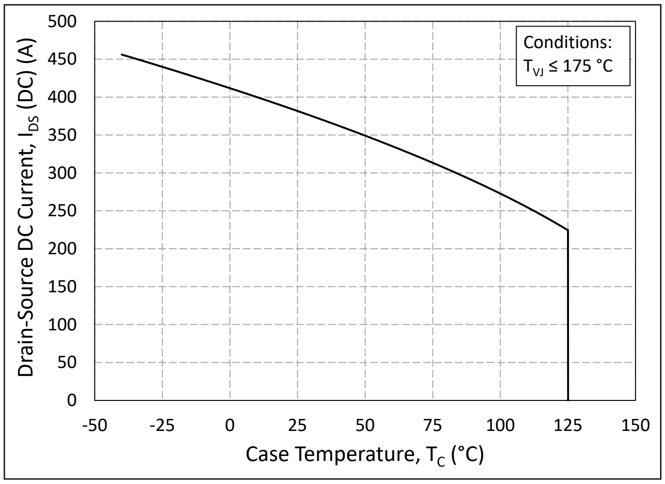


Figure 20. Continuous Drain Current Derating vs. Case Temperature

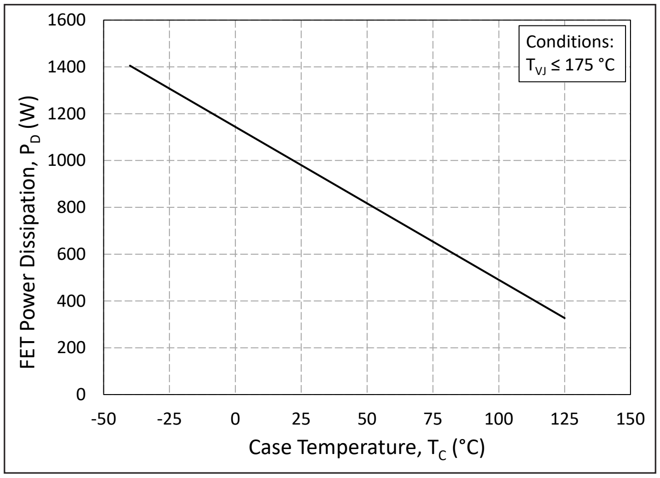


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

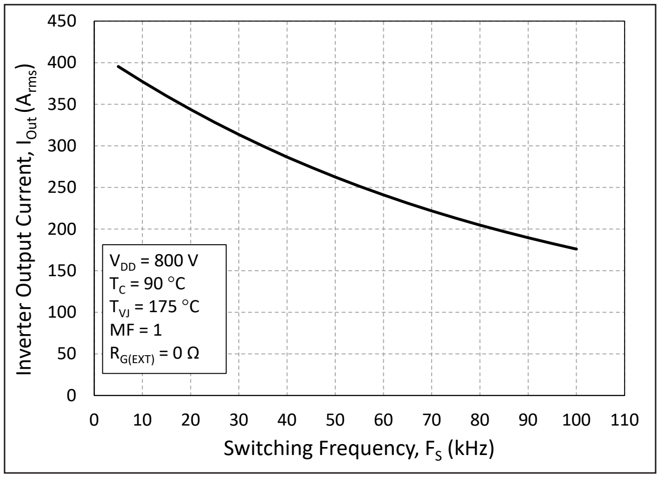


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

Timing Characteristics

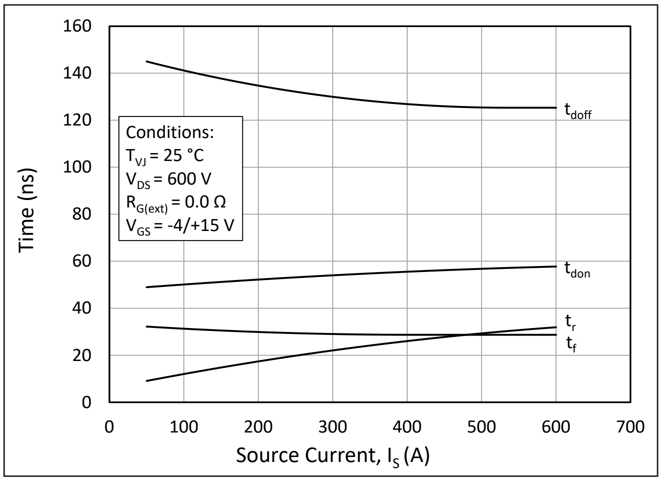


Figure 23. Timing vs. Source Current

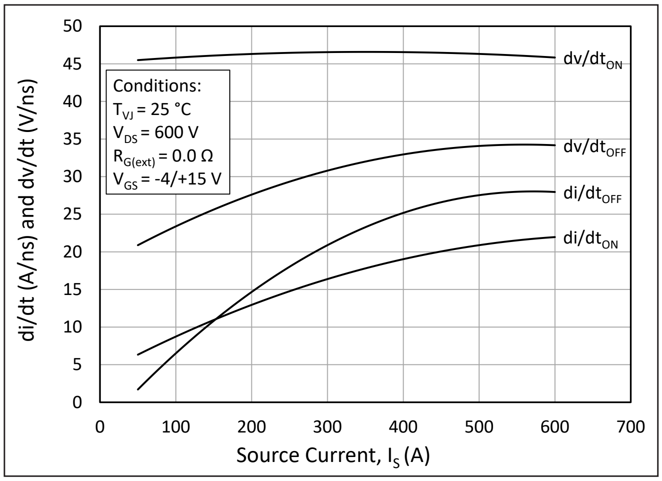


Figure 24. dv/dt and di/dt vs. Source Current

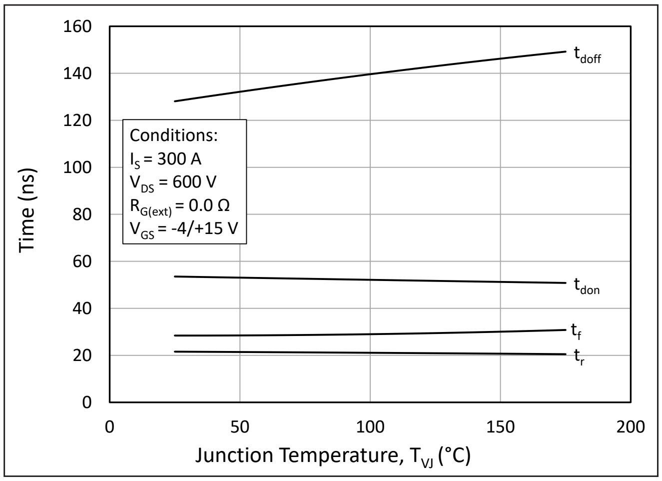


Figure 25. Timing vs. Junction Temperature

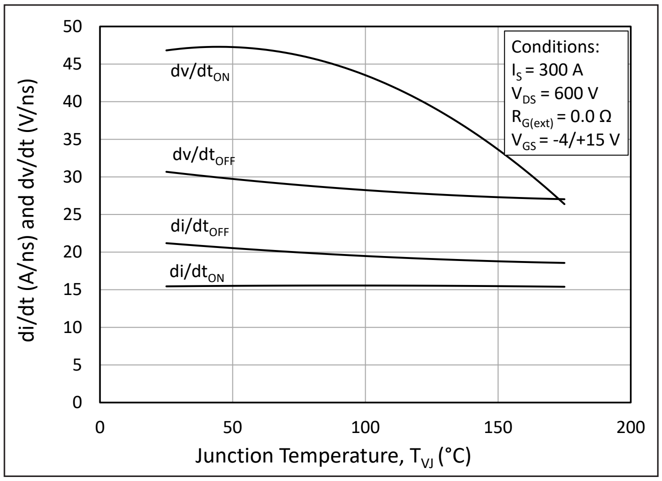


Figure 26. dv/dt and di/dt vs. Junction Temperature

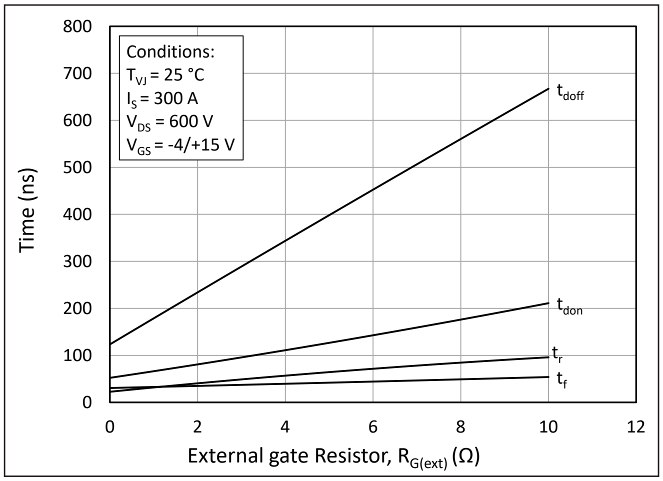


Figure 27. Timing vs. External Gate Resistance

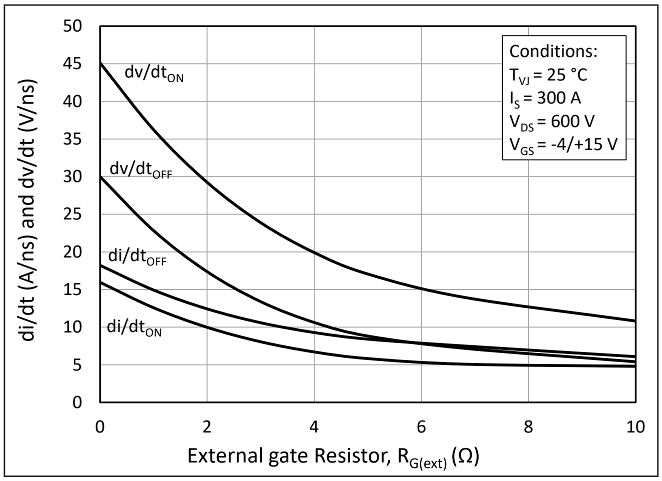


Figure 28. dv/dt and di/dt vs. External Gate Resistance

Definitions

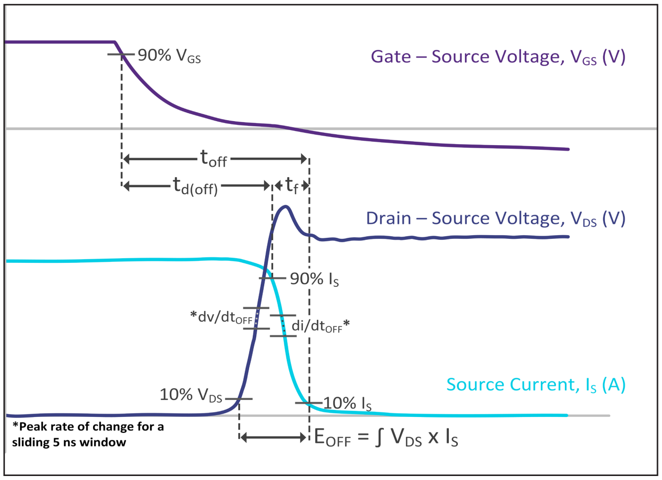


Figure 29. Turn-off Transient Definitions

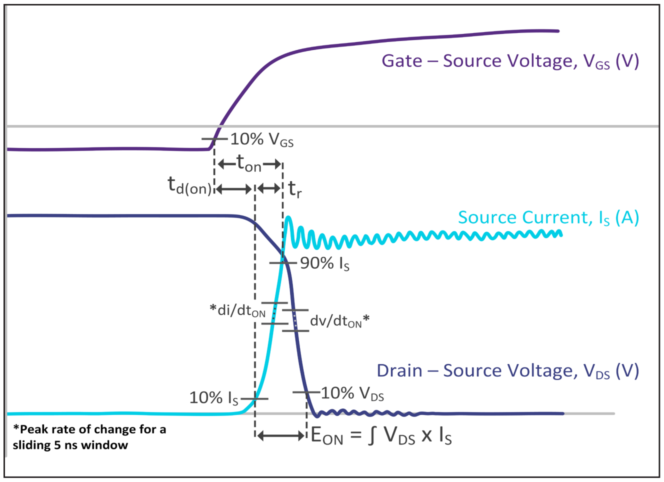


Figure 30. Turn-on Transient Definitions

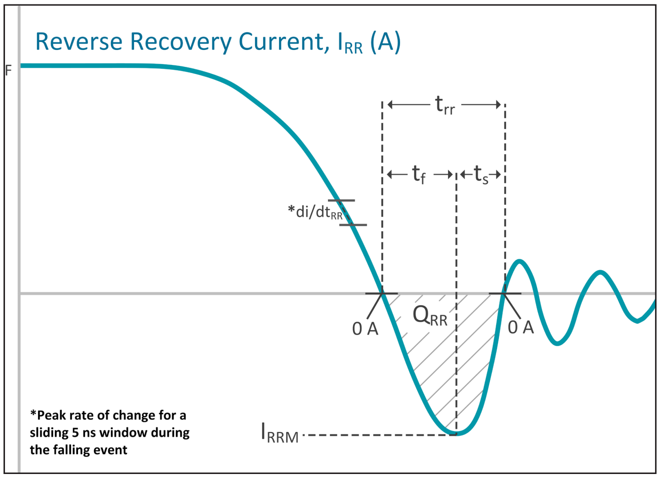


Figure 31. Reverse Recovery Definitions

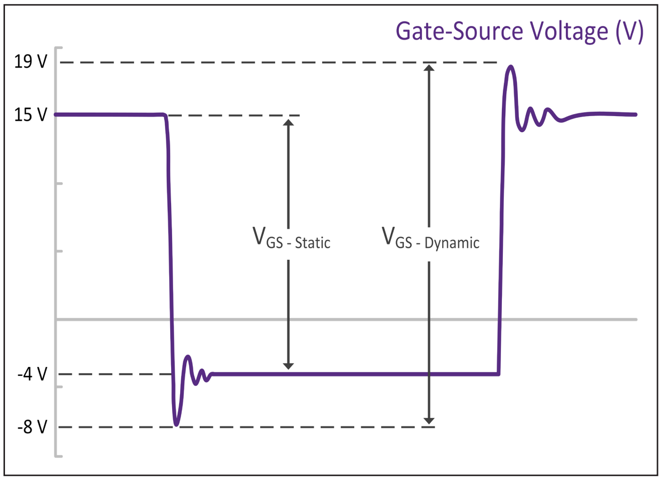
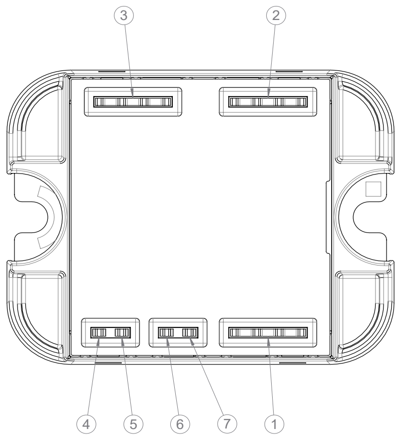
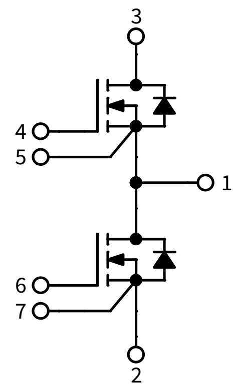


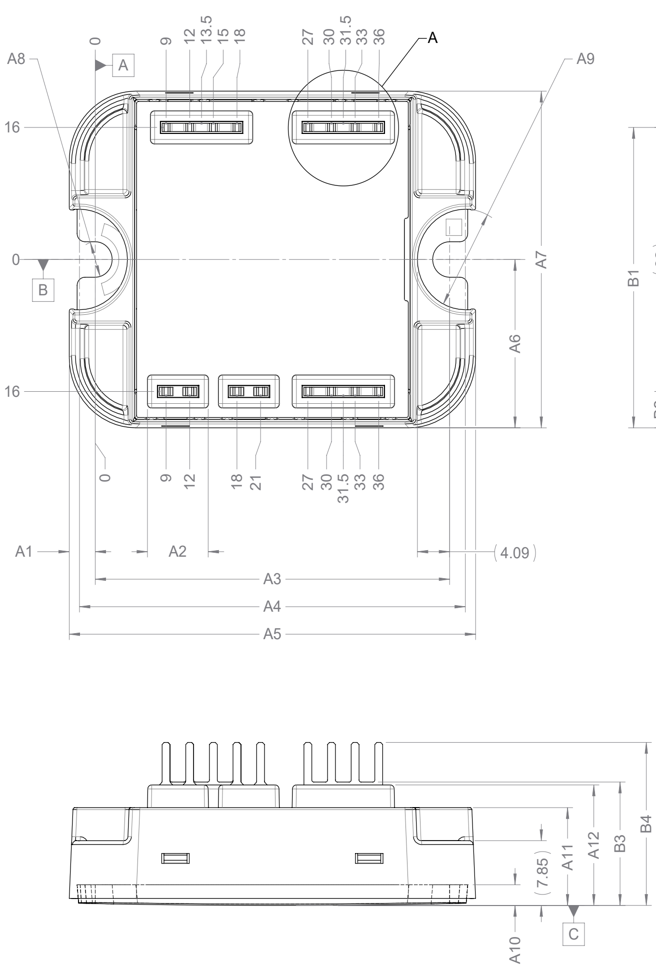
Figure 32. V_{GS} Transient Definitions

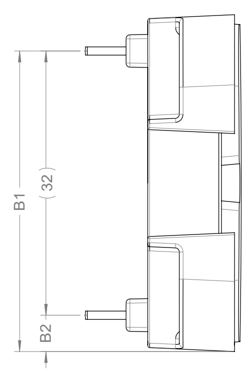
Schematic and Pin Out

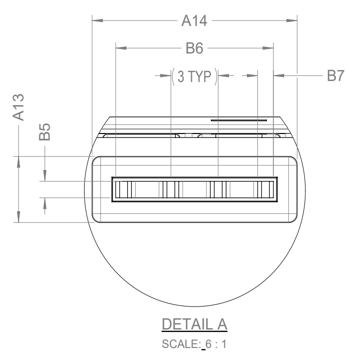




Package Dimensions (mm)







SYMBOL	DIMENSION	TOLERANCE
A1	3.3	±0.65
A2	7.75	±0.50
A3	45	±0.30
A4	49	±0.50
A5	51.6	±0.50
A6	20.4	±0.65
A7	40.8	±0.20
B1	36.4	±0.50
B2	4.4	±0.50
A8	∅4.3	±0.20
A9	∅12.17	±0.50
A10	2.5	±0.30
A11	11.89	$^{+1}/_{-0.65}$
A12	14.64	±0.55
B3	14.99	±0.50
B4	19.79	±0.50
A13	5× 4	±0.50
B5	5× 1	±0.25
A14	3× 13	±0.50
B6	3× 10	±0.50
B7	16× 1	±0.25
ALL CONNECTORS:		±0.75

Supporting Links & Tools

Evaluation Tools & Support

- SpeedFit 2.0 Design Simulator™
- Technical Support Forum
- LTspice and PLECS Models

Dual-Channel Gate Driver Board

- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers
- CGD1700HB2M-UNA: Wolfspeed Gate Driver Board

Application Notes and User Guides

- PRD-07634: Wolfspeed DM Module Mounting User Guide
- PRD-07635: Impact of PCB Design on Wolfspeed DM Module Ampacity
- PRD-07933: Wolfspeed Power Module Thermal Interface Material Application User Guide
- PRD-08333: Wolfspeed Module CIL Evaluation Kits User Guide
- PRD-08376: Thermal Characterization Methods and Applications
- PRD-06379: Environmental Considerations for Power Electronics Systems
- PRD-07845: Power Module Baseplate Capacitance and Electromagnetic Compatibility
- PRD-08710: Measuring Stray Inductance in Power Electronics Systems

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REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

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