

Application Note PRD-08907

Mitigating EMI with SiC Solutions in Renewable Energy & Grid-Connected Power Converters

Application Note PRD-08907

Mitigating EMI with SiC Solutions in Renewable Energy & Grid-Connected Power Converters

Power converters based on wide-bandgap semiconductor technology such as silicon carbide (SiC) MOSFETs unlock higher power density and higher efficiency compared to power converters based on silicon (Si) IGBTs by virtue of SiC’s faster switching speed. However, faster switching speed can lead to higher electromagnetic interference (EMI), which is a crucial problem for circuit designers. In the study, electromagnetic compatibility (EMC) is investigated for a 25kW, three-phase/level T-type neutral-point-clamped, grid-connected bidirectional inverter switching at 60kHz. This inverter is designed for high-power applications like solar inverters, uninterruptible power supplies (UPS) and energy storage systems (ESS). The test setup is based on the IEC-61000-6-3 standard and measures the emissions conducted to the grid by the inverter. Thereafter, a passive EMI filter is designed and implemented to mitigate the inverter’s conducted emissions, and measurements are taken to validate the performance of the filter. It is observed that the measurements are within the limits of the IEC-61000-6-3 standard.

Contents

1. Introduction.....	4
2. T-Type Inverter and EM Noise.....	4
2.1 Three-Level Three-Phase T-Type Inverter.....	4
2.2 EM Noise and Noise Mapping.....	6
3. CONDUCTED EMISSIONS MEASUREMENTS OF CRD-25BDA6512N-K POWER BOARD (EUT)	8
3.1 Ambient Noise	8
3.2 Impact of Auxiliary Components and Gate Loops on Conducted Emissions of EUT	9
.....	10
3.3 Conducted emissions of EUT without EMI Filter Board	10
3.4 Impact of LC Filter’s Choke on Conducted Emissions of EUT.....	12
3.5 Impact of the LC filter’s X capacitor star point connection on Conducted Emissions of the EUT	14
3.6 Impact of Bonding of Heatsink on Conducted Emissions of EUT	14
3.7 Impact of Thermal Interface Material on Conducted Emissions of EUT	15
4. Design of Multi-Stage EMI Filter Board	16
4.1 Components for Filtering.....	16
4.1.1 X capacitor	16

4.1.2 Common-Mode Choke	17
4.1.3 Y capacitor	18
4.2 Introduction to Design Methodology	20
5. Conducted Emissions Results of EUT with EMI Filter Board.....	21
6. PCB Layout & Component Placement	23
6.1 PCB layout techniques.....	23
6.1.1 ‘Optimized’ Gate Loop	23
6.1.2 Counter action against high di/dt.....	24
6.1.3 Counter action against high dv/dt.....	25
6.2 Component Placement	25
7. Conclusion	27
8. References	28

1. Introduction

Power electronic circuits such as an inverter are essential in connecting a renewable energy system to a grid. Grid-connected transformer-less solar inverters have drawn attention due to their high power-density, high efficiency and low cost [1]. Wide-bandgap semiconductor devices such as SiC MOSFETs allow faster switching transients, enabling MOSFETs to switch at higher switching frequencies compared to Si IGBTs resulting in more efficient and compact power converters.

While SiC MOSFETs reduce the size and weight of power converters, higher switching speed causes higher EMI. Designers must meet the EMC conditions described in relevant regulations and standards to ensure that the products are compliant. Passive EMI filters are often used for EMI mitigation of power converters. EMI filter design is a complex and demanding topic for designers, and the solution to the EMI problem is unique to the circuit.

In this study, an EMI filter is designed for Wolfspeed's 25kW high efficiency, high power density bi-directional three-phase/level T-type neutral point clamped inverter ([CRD-25BDA6512N-K](#)). This design demonstrates the performance of Wolfspeed's 650V and 1200V SiC MOSFETs within high power systems such as solar inverters, uninterruptible power supplies (UPS), EV fast chargers, HVDC applications, high power PSU for AI/datacenters and energy storage systems.

2. T-Type Inverter and EM Noise

2.1 Three-Level Three-Phase T-Type Inverter

The output power fluctuation of renewable energy sources and increasing power demand on the electric grid brought by the EV transformation puts increased stress onto the existing grid. A bi-directional converter is crucial to help manage the grid since it is able to transfer energy between the renewable energy source, the storage battery (which can include an EV battery), and the electric grid depending on the demand.

For the inverter stage in a bi-directional system, the two-level three-phase inverter is very popular due to its simplicity and ease of control. Since there are only two voltage levels, two-level inverters have relatively higher output THD. The solar industry's move towards higher bus voltages of 1000V or 1500V to reduce the current flowing in the circuit poses a major challenge in the use of two-level inverters due to the inverter's THD at higher voltages [2]. Multilevel converters help to solve this problem of high THD by employing multiple input voltage levels and can operate at higher switching frequencies, higher voltages, and higher power without compromising on efficiency [3]. This also helps to reduce the size of the system because a smaller EMI filter may be utilized. A T-type converter has a simple structure and lower cost compared to other multilevel topologies due to a lesser number of power devices than are present in other topologies like the I-type and active-NPC. Although operating power converters at higher switching frequency results in higher power density, it also causes unwanted EMI problems. Since EMI filters take approximately one-third of an inverter's total volume, it is important to optimally design the EMI filter.

The CRD-25BDA6512N-K is the inverter stage of the solar PV architecture connected to the AC grid based upon Wolfspeed's 3rd generation SiC MOSFETs- C3M0032120K (1200V, 32m Ω , TO-247-4) in the high-side and low-side switch positions and of all three phases and two C3M0025065K (650V, 25m Ω , TO-247-4) in the T-side position of

all three phases. The bi-directional side switch can be implemented in either a common-drain configuration or a common-source configuration. A common-drain configuration is chosen for this design as can be seen in Figure 1 because it allows for two fewer gate bias power supplies and saves cost and space on the board.

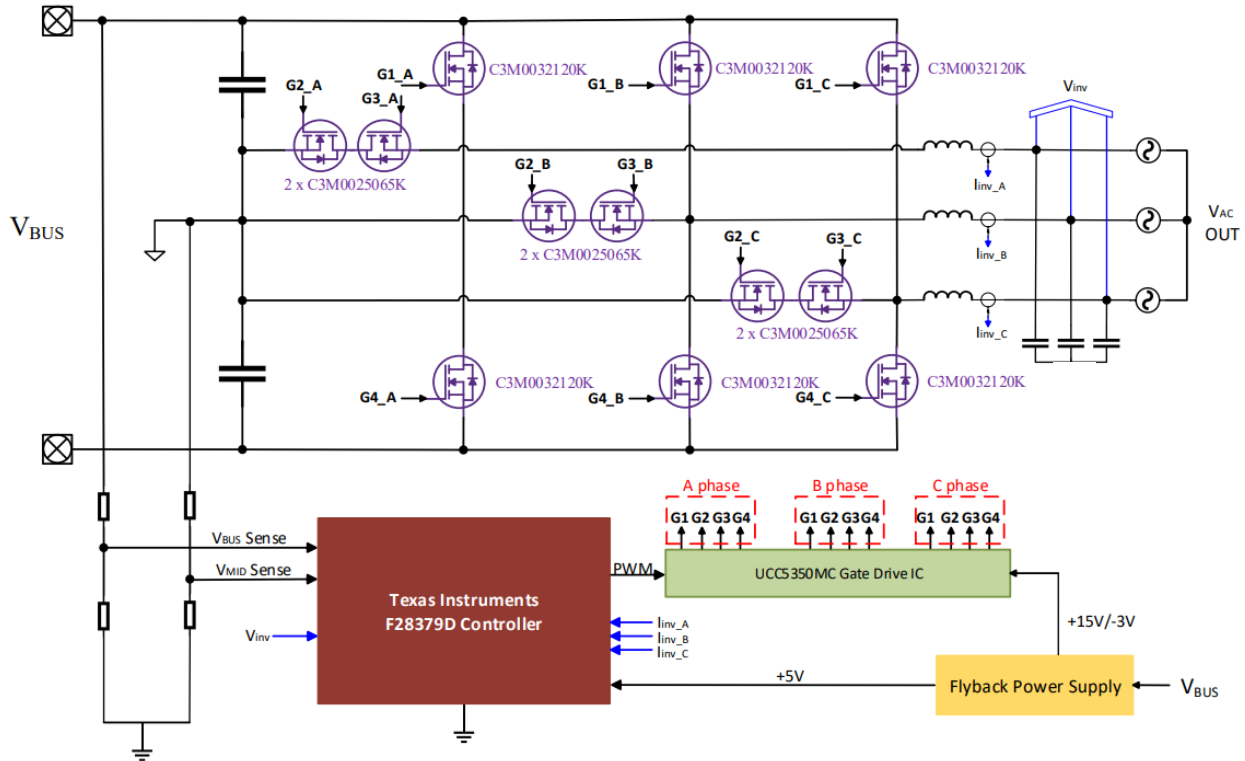


Figure 1: Block Diagram of Wolfspeed's CRD25BDA6512N-K, 25KW Bi-Directional T-Type Inverter

Figure 2 shows the CRD-25BDA6512N-K power board. Included on this single PCB solution is a DC-link bus capacitance with low-inductance power planes, gate drivers, current and voltage sensing, thermal management, various control peripherals, and a three-phase output LC filter. The converter is a bi-directional design, and therefore can operate in inverter mode providing a 3-phase balanced AC voltage on the output when a DC voltage is supplied as input and can operate in PFC mode providing a DC voltage output when a 3-phase AC voltage is supplied at the 3-phase input side.

The design parameters of the T-type PV inverter are given in Table 1. This design shows the SiC MOSFETs switching at a 60kHz switching frequency to achieve a power density of > 6kW/L while still maintaining a peak efficiency of >99%.

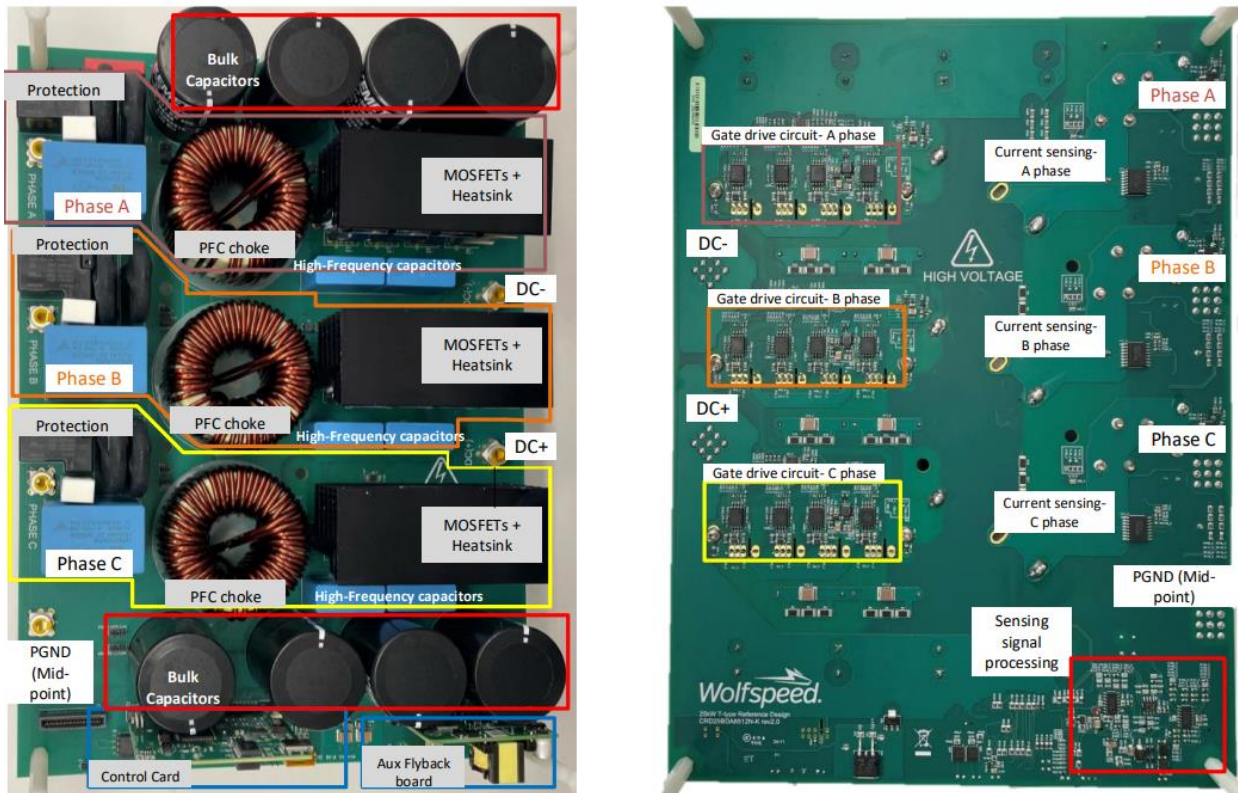


Figure 2: CRD-25BDA6512N-K reference design hardware

Parameter	Nominal Value
Output Power	25 kW
Input DC Voltage	800 V
Output Grid Voltage (line-line RMS)	400 V
Output Line Frequency	50 Hz
Switching Frequency	60 kHz
Output LC Filter	Inductor 105 μ H @ 20kHz/1V
	Capacitor 10 μ
Equivalent Turn-on/Turn-off External Gate Resistance	5 Ω /2.5 Ω
Thermal Interface Material	1 mm thick Aluminium Nitride

Table 1: Parameters of CRD-25BDA6512N-K

2.2 EM Noise and Noise Mapping

Electromagnetic (EM) noise can be divided into “conducted noise” and “radiated noise” depending on how the noise is transmitted. Conducted noise is transmitted along with power or signal through power lines, signal lines and trace patterns on printed circuit boards. Radiated noise requires no physical contact and travels through the air. These emissions happen when devices produce intentional or unintentional EM energy.

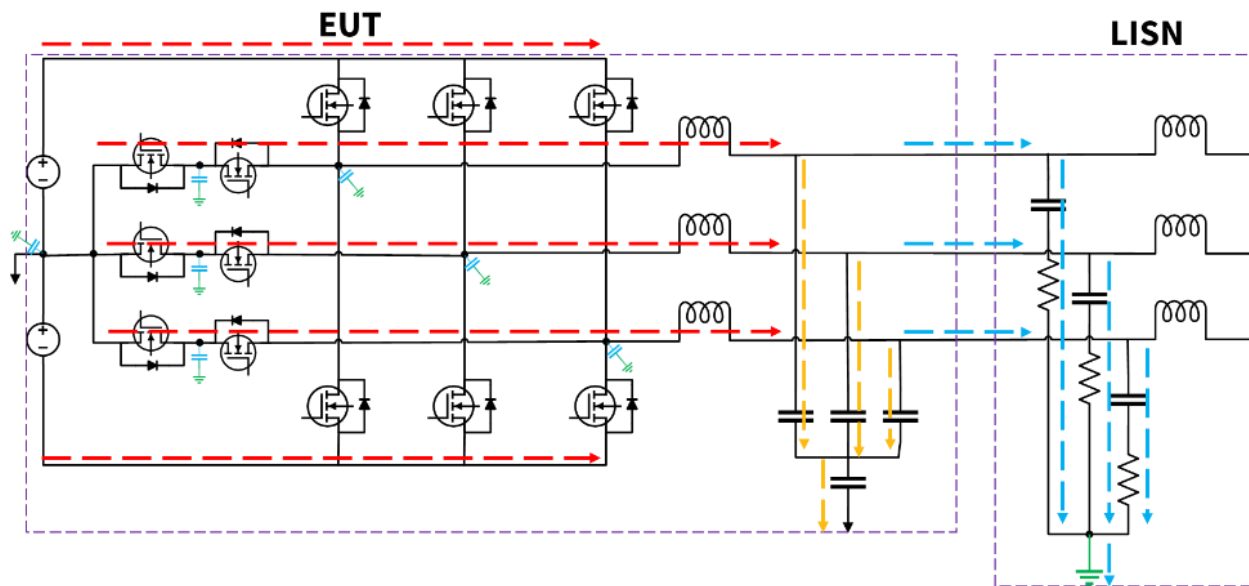


Figure 3: CM noise mapping of three-phase T-Type inverter

Conducted EMI is further divided into two modes according to propagation path: “common mode” (CM) and “differential mode” (DM). CM noise is voltage-driven and generated from voltage fluctuation caused by charging and discharging of stray capacitances between the circuit and the ground. CM current flows from the power lines of the device in the same direction and returns to the source through the ground. DM noise is caused by high di/dt and dv/dt because of MOSFET switching. DM current flows in opposing directions in the power conductors. Detection and reduction of CM noise is relatively more difficult than DM noise in high-power circuits[1].

Figure 3 and Figure 4 show representations of parasitic elements and the resulting CM and DM noise propagation paths for three-phase T-Type inverter.

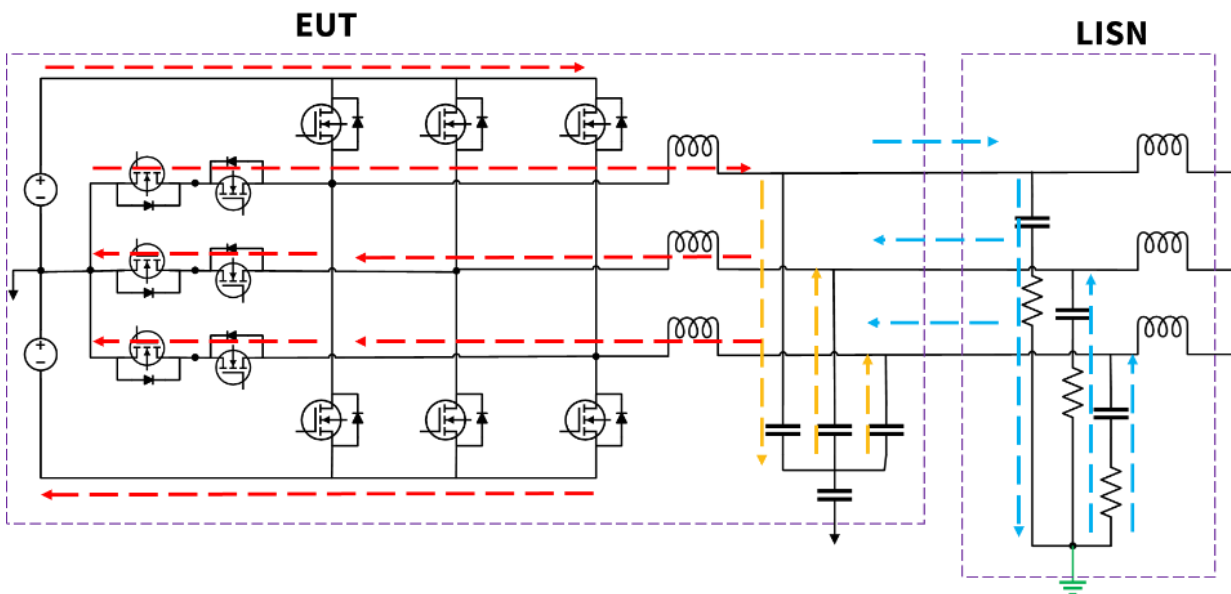


Figure 4: DM noise mapping of three-phase T-Type inverter

3. CONDUCTED EMISSIONS MEASUREMENTS OF CRD-25BDA6512N-K POWER BOARD (EUT)

Grid-connected power converters need to comply with international standards limiting the amplitudes of the low-frequency and the high-frequency current harmonics. This study is focused on mitigating high frequency current harmonics with regards to conducted emissions of the [CRD-25BDA6512N-K](#) 25 kW inverter. The standards limiting the amplitudes of the high-frequency spectral components specify the threshold in terms of conducted noise emission measured in dB μ V. For IEC-6100-6-3, the frequency range of interest is 150kHz to 30MHz.

A pre-compliance test for conducted emissions measurement was built according to the IEC-61000-6-3 standard. The LISN used in the experimental study is ENV432 from Rohde & Schwarz. It is a three-phase LISN capable of 415V AC and 32A. The EMI receiver used in the measurements is ESRP3 from Rohde & Schwarz. Peak (PK) detector is used in the measurement with the EMI receiver. Further, to measure CM and DM currents, EZ-17 current clamps, also from Rohde & Schwarz, are employed. The limit line for the 61000-6-3 EMC standard is marked in experimental results that will follow.

Hereafter in this study, the 25kW T-Type inverter power board that also includes a three-phase output LC filter onboard is referred to as “Equipment Under Test” (EUT). The EUT requires control power to operate, which can be provided by a provisional flyback power supply board or by a benchtop 15V supply. For this study, a benchtop supply is used.

3.1 Ambient Noise

Before measuring the conducted emissions of EUT, a reference level measurement is performed (see Figure 5) to measure the noise level of the system while the EUT is switched off. The EUT is connected to a DC source on the DC side and to a LISN and three-phase resistive load on the AC side. No HV or external 15V supply is applied to the EUT. The heatsink and the star-point of the X capacitors of the LC floating and are not bonded to any potential.

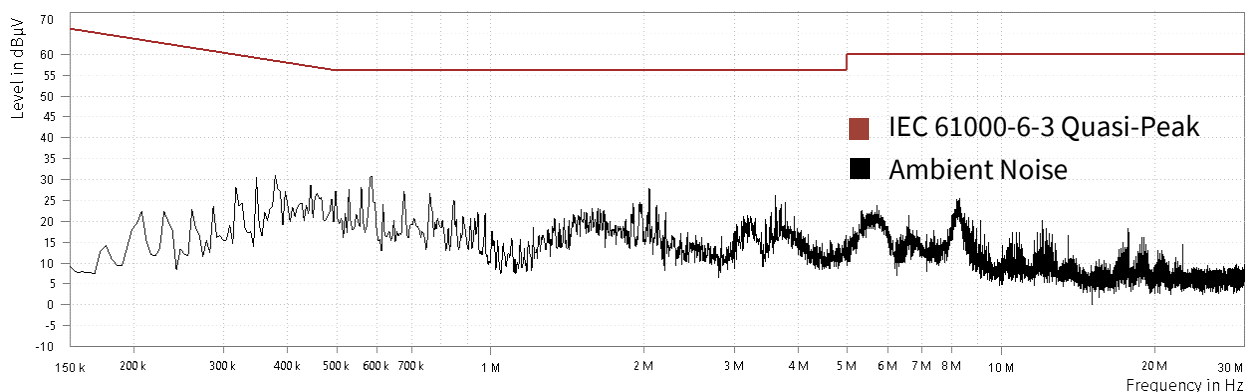


Figure 5: Reference level of conducted emissions with EUT switched OFF

3.2 Impact of Auxiliary Components and Gate Loops on Conducted Emissions of EUT

The bi-directional switch on the T-side position of each phase of the EUT is based on a common-drain configuration. The EUT has a total of 5 gate drive bias power supplies. These circuits generate +15V/-3V for the MOSFETs using a push-pull circuit with TI's SN6507 push-pull transformer driver IC and 750320528 transformer from Wuerth Elektronik. To observe the impact of control/auxiliary components (including gate drive bias power supplies) and the switching gate loops on the conducted emissions of the EUT, following two measurements are performed

- 1) External 15V applied to EUT but still no PWM is applied to MOSFETs.
 - a) This will power the control/auxiliary circuits and generate +15V/-3V for the gate drive of MOSFETs.
 - b) As can be seen in measurement results in Figure 6 (blue curve), we can notice an increase of up to 30dB μ V compared to background noise (black curve) at 545kHz and similar behavior at subsequent harmonics. Upon checking with H-field near field probes, gate drive bias power supplies on the EUT were found to be the emission hotspots.
 - c) As mentioned above, gate drive bias power supply generates +15V/-3V using a push-pull circuit with TI's SN6507 push-pull transformer driver IC and 750320528 transformer from Wuerth Elektronik. The push-pull driver IC is programmed to switch at 550kHz which explains the peaks around 550kHz and subsequent harmonics in the measurement when external 15V is applied to EUT.
 - d) The interwinding capacitance of the transformer for push-pull is ~9pF, which is relatively high and is also a potential cause for higher EMI. For new designs, customers can also consider using an LLC topology for bias power supply generation instead of push-pull. An LLC transformer can offer lower primary-to-secondary capacitance, which reduces the path for parasitic currents to flow

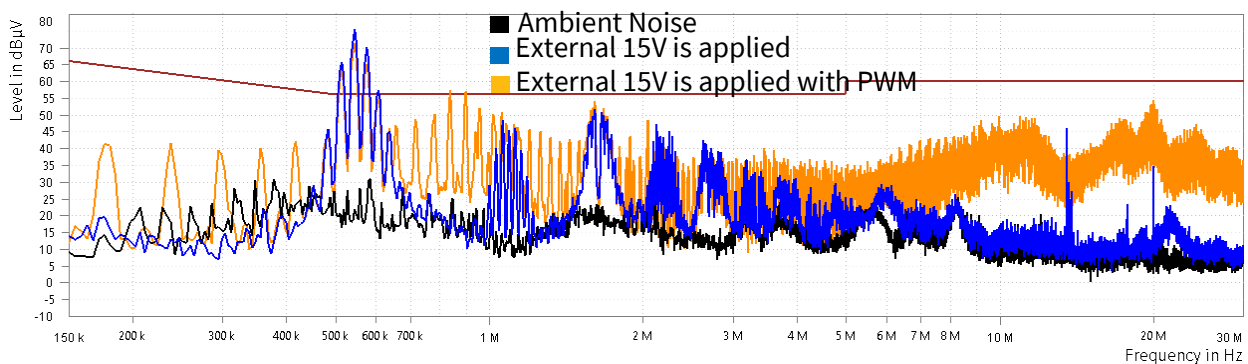


Figure 6 : Conducted emissions of gate drive bias power supplies and gate loops

- e) Some good practices that were followed with regards to low EMI at design stage
 - o Using SMD common-mode choke on the secondary side of gate drive bias supply transformer as shown in Figure 7.

- Strictly following recommendations for low emissions designs and PCB layout guidelines mentioned in TI’s SN6507 push-pull transformer driver IC datasheet.
- 2) Next, in addition to applying external 15V to EUT, PWM switching signals are applied to the MOSFETs as per the control scheme.
- a) It can be seen in Figure 6 that as PWM signals are applied to MOSFETs and they start switching between +15V and -3V, there is a substantial increase in conducted emissions, especially at frequencies higher than 5MHz.
 - b) As confirmed with H-field near-field probes, switching gate loops on the EUT are found to be the emission hotspots. It should be reiterated here that having a compact and optimized gate loop is crucial for a low-emission design. For details on how to ensure a compact and low-emission gate loop, it is encouraged to check out Wolfspeed’s application note- [PCB Layout Techniques for Discrete SiC MOSFETs](#).

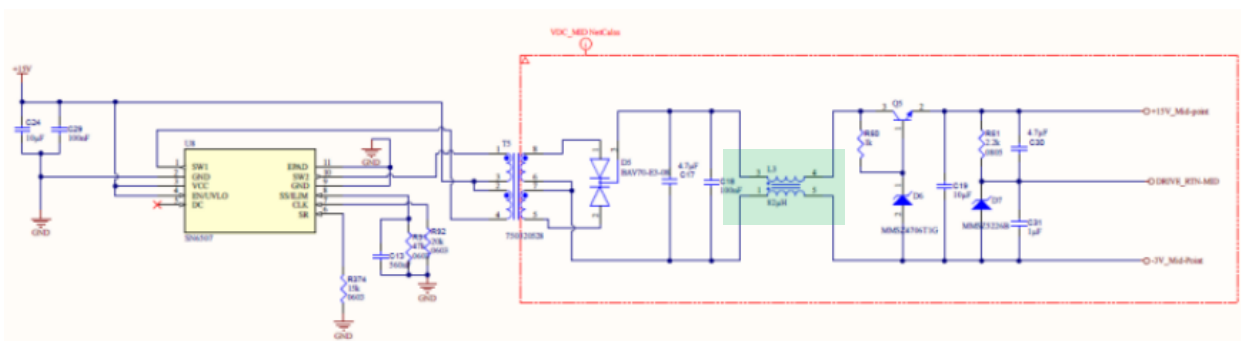


Figure 7 : One of the gate drive bias power supplies of 25kW T-Type with SMD CM choke (marked in green) on the secondary side of gate drive bias transformer to mitigate conducted emissions generated by switching of push-pull gate driver IC

3.3 Conducted emissions of EUT without EMI Filter Board

The LISN used for the study is limited to 415V AC and 32A, meaning that the output power will be limited to 22kW instead of the 25kW that the inverter is rated for. As shown in Figure 8, conducted emissions of EUT are measured for operating conditions as stated in Table 1 except the output power, which is limited to 22kW. Current clamps are used on the AC lines to measure CM and DM noise currents (measured in dBµA) and are shown in Figure 9.

The switching frequency of the inverter is 60kHz. It can be seen in Figure 8 that spikes in conducted emissions of EUT occur at subsequent harmonics of switching frequency. Since, conducted EMI range starts at 150kHz, the first emission peak within the CEMI range belongs to the 3rd harmonic of the switching frequency at 180kHz ($3 \times 60 = 180\text{kHz}$) followed by the 4th harmonic at 240kHz ($4 \times 60 = 240\text{kHz}$) and so on. Conducted emissions at lower frequencies dictate the size and weight of the passive EMI filter. Hence, choosing the right switching frequency becomes critical to strike a balance among power density, EMC, efficiency and cost.

Possible mistakes to avoid while selecting the switching frequency could be:

- 1) Switching frequency too high for high-voltage hard-switching applications
- 2) Non-EMI-friendly switching frequency- As mentioned earlier, conducted EMI range starts at 150kHz.

Hence, it isn't 'EMI-friendly' to choose a switching frequency if its n^{th} harmonic is 150kHz or slightly higher than 150kHz. For example, for a switching frequency of 50kHz, the 3rd harmonic ($3 \times 50 = 150\text{kHz}$) falls within the CEMI range. This would have been avoidable by choosing a switching frequency of 47kHz, wherein the 3rd harmonic is 141kHz, which is outside the CEMI range. Hence, in comparison to 50kHz, a switching frequency of 47kHz would be a better trade-off between power density and EMI.

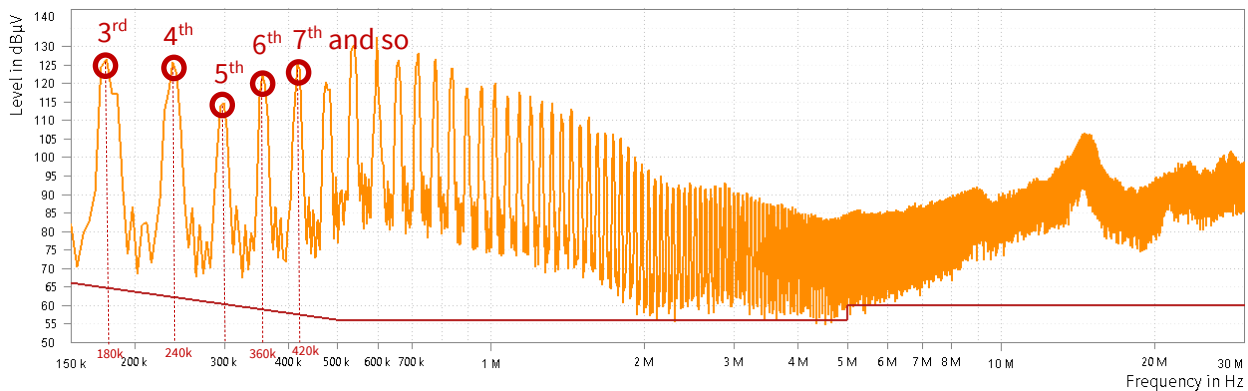


Figure 8: Conducted emissions of EUT at 22kW

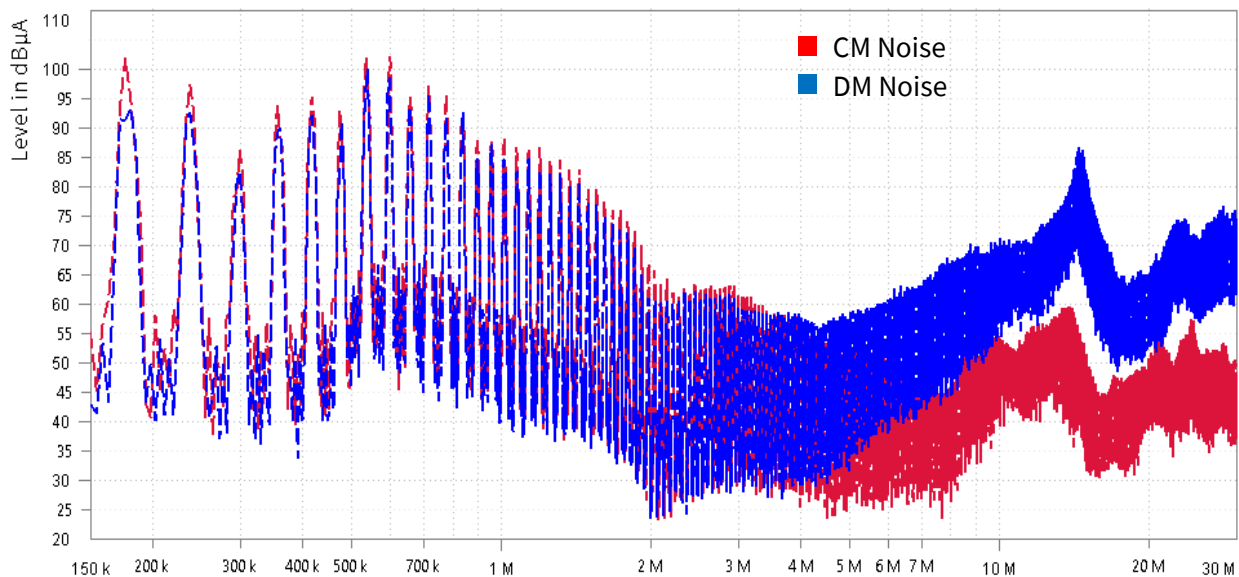


Figure 9: CM (red) and DM (blue) noise spectrum of EUT at 22kW

Example switching frequency ranges for high-voltage hard-switching applications:

- 1) $\leq 47\text{kHz}$ (ensures that the 3rd harmonic isn't in CEMI range while achieving a power density similar to a switching frequency of 50kHz)
- 2) 60~67kHz (ensures that the 2nd harmonic isn't in CEMI range while achieving a power density similar to a switching frequency of 75kHz)
- 3) 120~135kHz (to make sure that switching frequency isn't in CEMI range while achieving a power density similar to a switching frequency of 150kHz)

3.4 Impact of LC Filter's Choke on Conducted Emissions of EUT

To provide nominal noise suppression, the power stage is supplemented with an LC filter on the EUT. Details regarding design and sizing of the LC filter can be found in the user guide of [CRD-25BDA6512N-K](#). It has been observed that the design of the filter's choke can have a substantial impact on the conducted emissions of the EUT. Figure 10 shows three different LC filter DM chokes tested to study their impact on conducted emissions of the EUT.

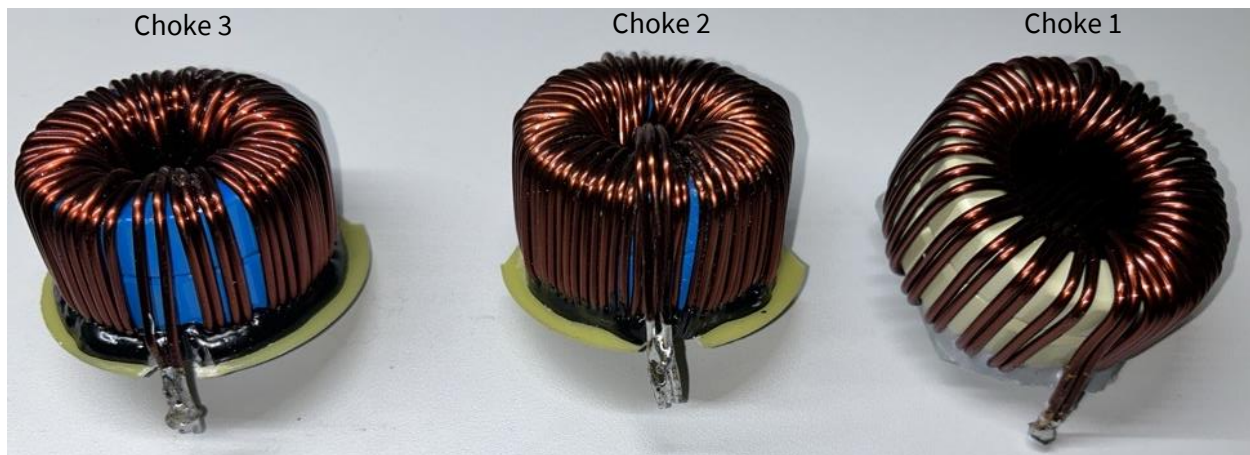


Figure 10: Three different DM Chokes used for studying impact of LC filter's DM choke on conducted emissions of EUT

Three chokes are similar in electrical specifications but differ in mechanical construction as mentioned below:

- 1) Choke 1: Conventional winding, $\phi 2\text{mm} \times 2\text{P}$ wire, 28Turns, $108\mu\text{H}$ @36A
- 2) Choke 2: Butterfly winding, $\phi 1.8\text{mm} \times 3\text{P}$ wire, 30Turns, $105.89\mu\text{H}$ @36A
- 3) Choke 3: Butterfly winding, $\phi 2\text{mm} \times 2\text{P}$ wire, 30Turns, $105\mu\text{H}$ @36A

For Choke 2, butterfly type winding as shown in Figure 11 is employed instead of conventional winding as in Choke 1. This helps reduce the parasitic capacitance among the turns of the choke and possibly, improves the conducted emissions attenuation at higher frequencies. In Choke 3, butterfly type winding is maintained while reducing the number of wires to 2 and increasing the diameter of each wire to 2mm (compared to $\phi 1.8\text{mm} \times 3\text{P}$

wire in Choke 2). This further reduces the parasitic capacitance between turns of Choke 3 and possibly improves performance at higher frequencies.

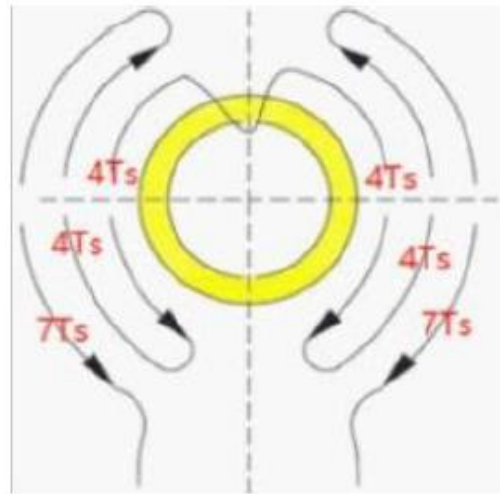


Figure 11: Butterfly type winding structure for Choke 2

A comparison of parasitic capacitances of filter’s chokes at 10MHz, measured from impedance analyzer is shown in Table 2.

DM Choke	Parasitic Capacitance at 10MHz
Choke 1	292pF
Choke 2	49pF
Choke 3	30pF

Table 2: Parasitic capacitances of DM chokes at 10MHz

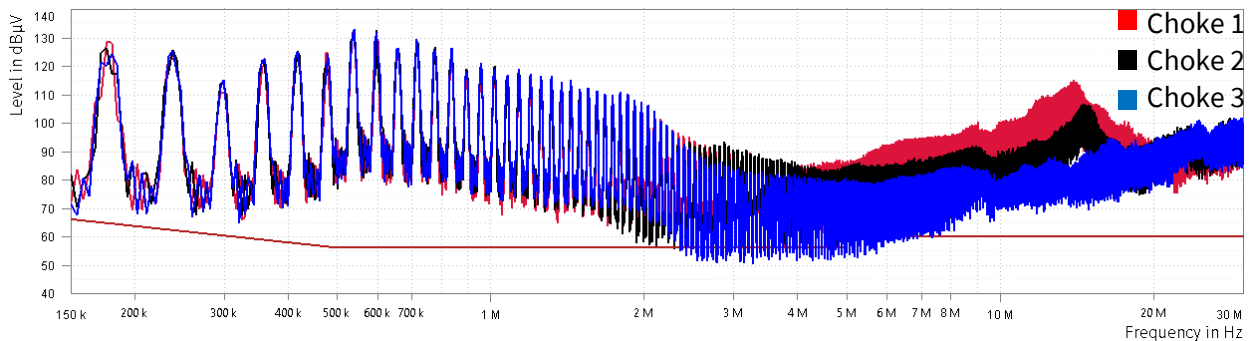


Figure 12: Impact of LC filter’s choke inductor on conducted emissions of EUT at 22kW

Figure 12 shows conducted emissions of EUT with Chokes 1, 2, and 3. Aligning with the discussion points above, an improvement of up to 25dBµV can be seen from Choke 1 to Choke 3 at higher frequencies. Optimizing the

choke inductor of the LC filter can potentially reduce the attenuation requirement from the EMI board and enable higher overall power density. Hereafter Choke 3 is used as the inductor for the EUT’s LC filter.

3.5 Impact of the LC filter’s X capacitor star point connection on Conducted Emissions of the EUT

As will be discussed later in the study, one of the main limitations of a conventional passive EMI filter with regards to CM noise attenuation is the maximum allowed value of Y capacitance connected to protective earth (PE). This limit is imposed by safety standards to limit the maximum allowed current that flows in the protective conductor and subsequent maximum admissible touch current. [4] “A new concept for minimizing high-frequency common-mode EMI of three-phase PWM rectifier systems keeping high utilization of the output voltage” shows that connecting a filtering capacitor between the star point of the LC filter’s X capacitors and mid-point of the DC-link, as compared to connecting three Y capacitors with one connection between each phase, can offer similar EMI attenuation while limiting touch current and also reducing the part count.

Figure 13 shows that when a 2.2 μ F capacitor is connected between the star point of X capacitors and mid-point of DC link, it results in an improvement of up to 30dB μ V. For higher frequencies, the parasitics of the filtering capacitors become dominant and increasingly lower the improvement. Hereafter, the X capacitor’s star point is tied to mid-point of DC-link with a 2.2 μ F capacitor. This reduces filter attenuation requirements at low frequency and enables higher overall power density.

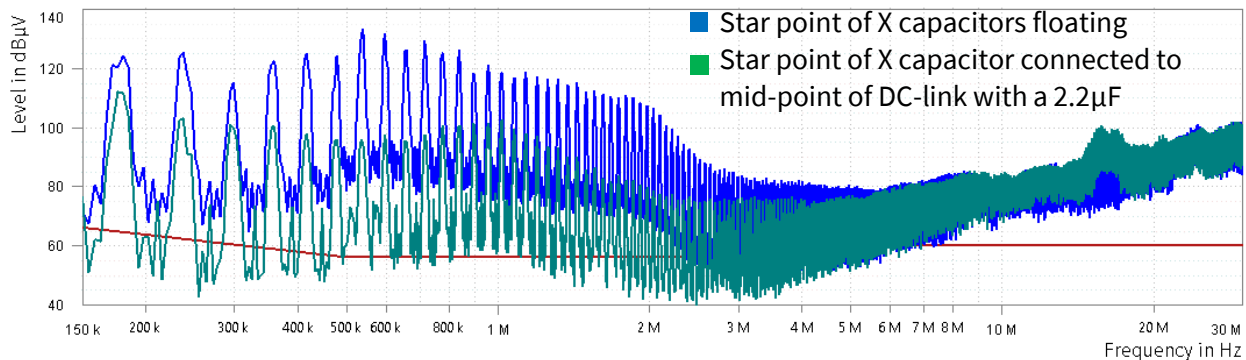


Figure 13: Impact of connection of LC filter's X capacitor's star point on conducted emissions of EUT at 22kW

3.6 Impact of Bonding of Heatsink on Conducted Emissions of EUT

The parasitic capacitances from positive, negative, and mid-point rails of the DC-link to PE are in parallel and can thus be combined into one capacitance, C_g . Impact of C_g on achievable CM noise attenuation is comprehensively discussed in [7]. Referring to the literature, depending on the CM filtering approach, C_g can have significant impact on CM noise attenuation (up to a difference of 32dB μ V). Papers [4] and [7] compare different approaches for bonding the heatsink and concludes the following two options to be not just superior with regards to CM noise attenuation, but also independent of parasitic capacitance between the drain pad of MOSFET and heatsink:

- 1) Connecting heatsink to mid-point of DC-link supplemented with a Y capacitor between the star point of LC filter's X capacitors and mid-point of DC-link
- 2) Earthed heatsink with Y capacitor between each line and PE

As discussed before, [4] shows that connecting a filtering capacitor between the star point of LC filter's X capacitors and mid-point of DC-link as compared to connecting three Y capacitors, one between each phase, offers similar EMI attenuation while limiting touch current and also reducing the part count. Figure 14 explores EUT's conducted emissions with different bonding schemes of the heatsink while the star point of X capacitors is connected to the mid-point of the DC-link with a $2.2\mu\text{F}$ capacitor as previously discussed.

It can be observed in the top image of Figure 14 that the EMI noise increased by up to $30\text{dB}\mu\text{V}$ when the heatsink

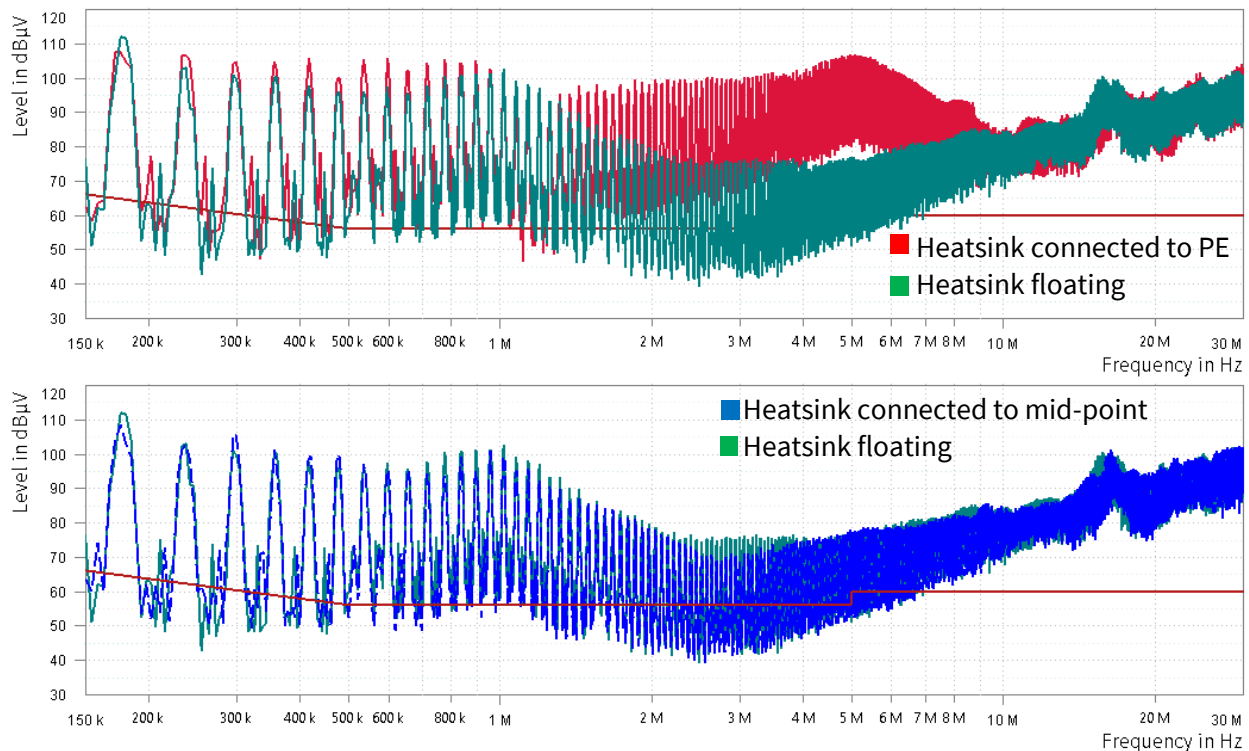


Figure 14: Impact of heatsink bonding on conducted emissions of EUT at 22kW

is connected to PE compared to when it is floating. It can be observed in the bottom image of Figure 14 that the EMI noise is reduced further by $\sim 5\text{dB}\mu\text{V}$ between 2~4MHz when the heatsink is bonded to mid-point of DC-link compared to when it is floating. Hence, best performance is achieved with a heatsink connected to mid-point, although a floating heatsink also yields similar results when compared to being bonded to mid-point. Hereafter, the heatsink is bonded to mid-point while the mid-point of DC-link is capacitively bonded to star point of LC filter's X capacitors with a $2.2\mu\text{F}$ capacitor.

3.7 Impact of Thermal Interface Material on Conducted Emissions of EUT

As power converters are shrinking in volume, thermal management becomes a challenge especially in high-power designs. Thermal interface material (TIM) between the SiC MOSFET and heatsink is crucial to a robust

and reliable operation of power converters. A TIM should not only ensure the required isolation of the MOSFET's drain pad from the heatsink, but it is critical that a low thermal resistance between the case of a MOSFET and heatsink ($R_{th,ch}$) is achieved so that the MOSFET's junction temperature is within its desired derated value. TIM results in a parasitic capacitance between the drain pad (which could be a potential switching node) and the heatsink. This parasitic capacitance becomes a path for CM noise current that flows as a direct result of capacitive coupling of the switching node and PE.

Sil-pads and AlN ceramics are popular choices for the TIM as they provide good electrical isolation and excellent thermal conductivity. Although no EMI measurements are performed with different TIMs in this study, the effective capacitance between the drain tab and heatsink as well as effective thermal resistance between the case of a MOSFET and heatsink ($R_{th,ch}$) of different TIMs is compared in Table 3. The thermal resistance values mentioned below are borrowed from actual testing results as mentioned in Table 4 of Wolfspeed's application note [PRD-05652: Mounting Recommendations and Thermal Measurement for Wolfspeed® SiC Power Devices in Through-Hole Packages](#). It can be seen from comparison below that 1mm AlN TIM offers a good trade-off between better thermals and at the same time lower parasitic capacitance, which eventually translates into better EMI performance.

Thermal Interface Material (TIM)	Thickness (mm)	Parasitic Capacitance (pF)	$R_{th,ch}$ (C/W)
Aluminium Nitride (AlN)	1	14	0.415
	0.5	24	0.406
BERGQUIST SIL PAD TSP 3500	0.38	25	0.964

Table 3: Measured parasitic capacitances and thermal resistance of different thermal interface material

4. Design of Multi-Stage EMI Filter Board

To facilitate in-lab EMI debugging and assist in testing different filter components, a separate three-phase multi-stage EMI filter PCB is designed and used for the testing. For testing, it is connected to EUT after the onboard LC filter with very short cables.

4.1 Components for Filtering

4.1.1 X capacitor

DM noise is suppressed by installing X capacitors across supply line. Connection of X caps influences filter attenuation as they can be connected either directly between phases or to a star point. For X capacitors connected in star, capacitors are connected in series between phases necessitating increased capacitance value to achieve same capacitance between phases. Even though the capacitance needs to be increased but the required voltage levels are reduced, reducing the required size and cost (cost by up to 20% [1]). Hence, X capacitors connected in star enable higher power density for the system.

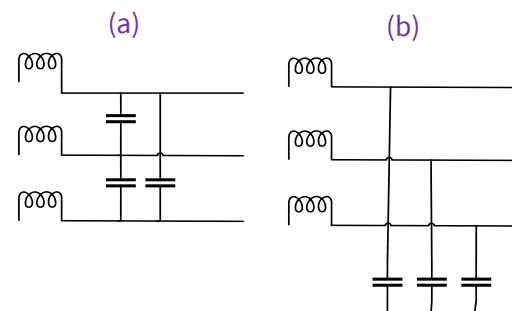


Figure 15: Different possible connections of X capacitors- (a) connected between phases, (b) star connection

At higher frequency (tens of MHz), ESL of X capacitors would increase limiting their capability to attenuate the noise. Hence, it is important to minimize impedance of capacitor branch to ensure that the X capacitors work effectively especially at higher frequency. It is a good practice to parallel a large and smaller X-capacitor to reduce the total ESL of the capacitor branch. Further, as discussed in [11] and shown in Figure 16, for parallel X-capacitors, different capacitor arrangements influence ESL based on the mutual inductance between capacitors. As shown in Figure 17, lowest ESL is achieved with zig-zag arrangement which results in inverse coupling of mutual inductance.

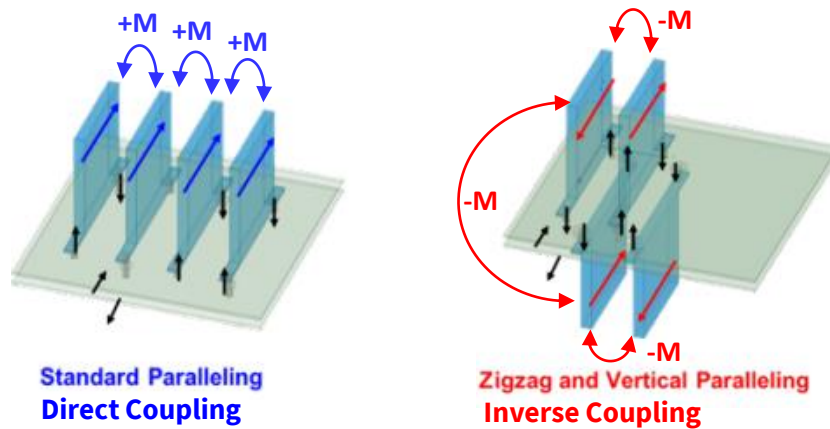


Figure 16: Different parallel arrangements of X capacitors [11]

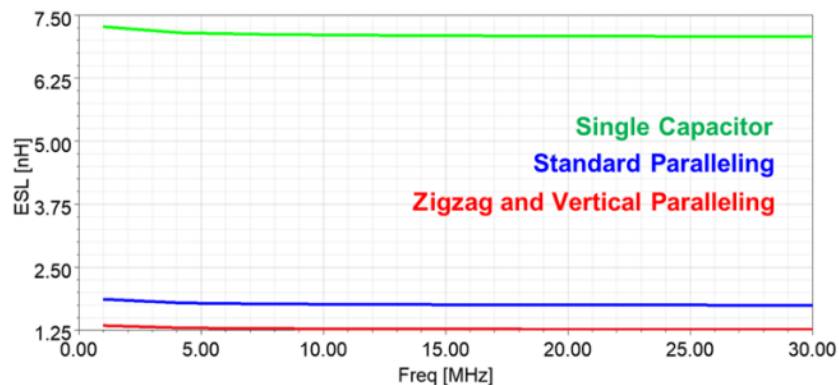


Figure 17: Effective ESL with different parallel arrangements of X capacitors [11]

4.1.2 Common-Mode Choke

CM chokes are vital for CM noise attenuation given limited capacitance values of Y capacitors, as will be discussed next. In three-phase systems, three winding CM chokes as shown in Figure 18 are employed. CM chokes impact CM noise but also DM noise. All the flux produced by a winding does not couple to the other winding. This leakage flux introduces a small DM inductance while DM currents flow through the windings. Excessive leakage inductance may cause saturation of CM choke at low AC current values. An empirically validated approximation for DM inductance is 1% of the CM-inductance [5]. For a good filter design, the leakage

inductance is optimized so it is as big as possible to offer attenuation to DM noise, but small enough to prevent core saturation [6].

[5] “Calculating Parasitic Capacitance of Three-Phase Common-Mode” discusses about different common mode choke materials and that no one material is a “one size fits all” solution for all frequency ranges. The main types of materials are compared in Table 4.

	Ferrites (MnZn, NiZn)	Iron Powder	Nanocrystalline (NC)
Permeability	High	Low	Highest
Saturation	Low	Highest	High
Conductivity	Low	Low	Low
Price	Lowest	Low	Highest

Table 4: Comparison of ferromagnetic materials [5]

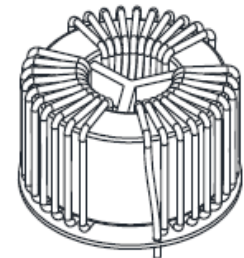


Figure 18: Three-phase Common Mode Choke

Figure 19 shows a comparison of CM impedance of different three-phase CM chokes from Wuerth Elektronik extracted from their online simulation tool. It can be observed that at lower frequencies, CM impedance increases with frequency but at higher frequencies, parasitics dominate and CM inductance consistently decreases supplemented with resonances beyond 10MHz. For this design, as will be discussed later, a two-stage EMI filter employing two identical CM chokes based a nanocrystalline iron core are employed to achieve required noise attenuation at lower frequencies but also improve the response at higher frequencies.

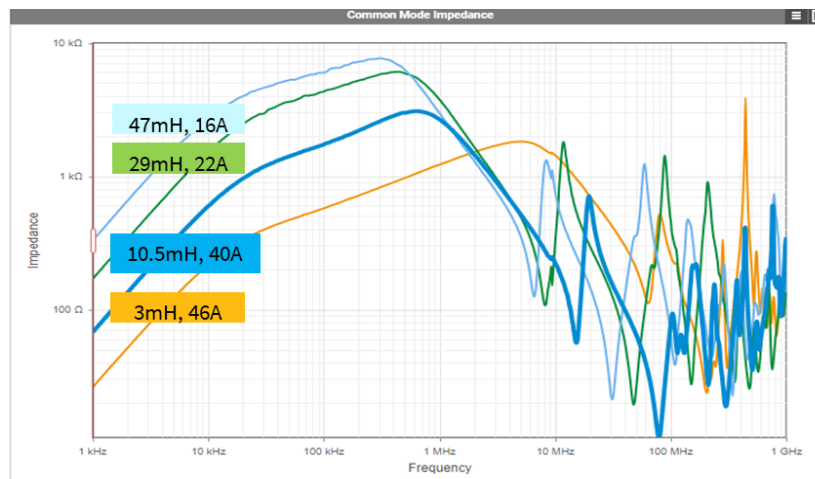


Figure 19: CM impedance of a different three-phase CM chokes

4.1.3 Y capacitor

Y capacitors help to mitigate CM noise at higher frequencies, wherein, owing to parasitics, CM chokes don’t have a significant impact. A low-impedance path for HF noise is created with Y capacitors that are connected

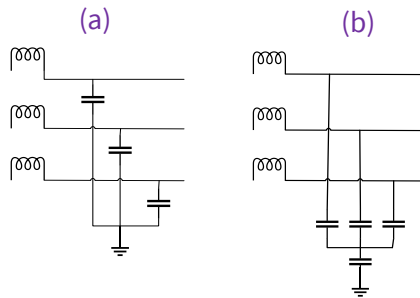


Figure 20: Different possible connections of X capacitors- (a) connected between phases and PE, (b) connected between star point and PE

between supply lines and PE. Y capacitors can be either connected between each phase and PE directly, or between the star point of the X capacitors and PE as shown in Figure 20. Both types of connection offer similar filter attenuation for an earthed heat sink [7].

Since Y capacitors works to attenuate CM noise at higher frequencies, hence, to ensure that they work effectively at tens of MHz, it is critical to ensure a low-impedance path (at tens of MHz) for CM noise between phases and chassis/PE. This includes, minimizing the ESL of X capacitor branch which is discussed section 4.1.1.

The conventional approach is to choose a ceramic disc capacitor as the Y capacitor. These are cost effective but pose risk in terms of safety and reliability [1]. They are not self-healing and are therefore unable to overcome dielectric breakdown with a minimal decrease in capacitance and exhibit short circuits in case of failure. This poses a risk of an electric shock in case connection to PE is lost [8]. Metallized polypropylene (MP) film capacitors, on the other hand, are self-healing, stable over time and temperature changes, and result in an open circuit in case of failure, making them a suitable choice for Y capacitors while ensuring safe and reliable operation. An example of both of the types of Y capacitors is shown in Figure 21.

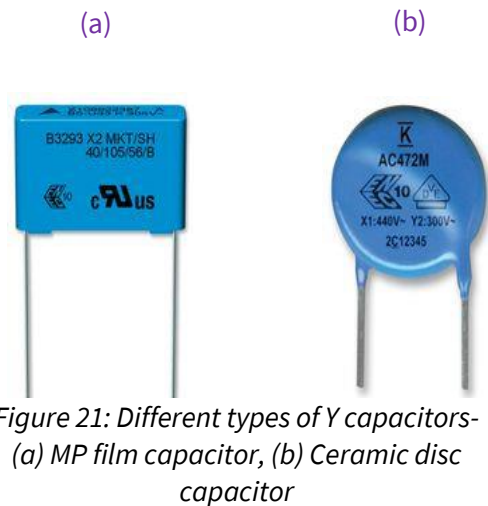


Figure 21: Different types of Y capacitors- (a) MP film capacitor, (b) Ceramic disc capacitor

An example of a capacitor’s (MKP338 1 X1) impedance curve is shown in Figure 22. It can be observed that either a specific Y capacitor or a combination of Y capacitors can be selected to achieve desired CM attenuation at target frequencies.

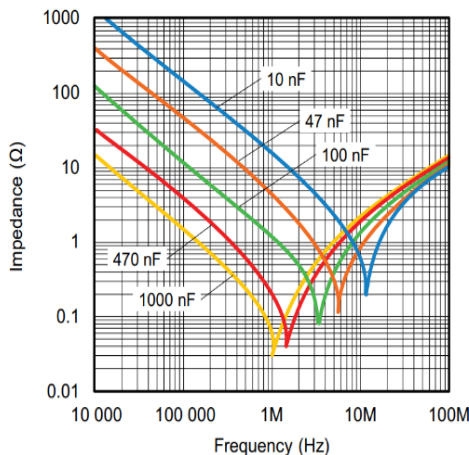


Figure 22: Impedance curves of capacitors (MKP338 1 X1)

As mentioned before, one of the main limitations of a conventional passive EMI filter with regards to CM noise attenuation (besides the parasitics), is the maximum allowed value of Y capacitance connected to PE. This limit exists in order not to exceed maximum allowed protective conductor current and maximum admissible touch current. High Y capacitance values reduces CM noise but also causes an increase in ground leakage current flowing through the PE/chassis. In cases without earthing of chassis or in cases where the bonding of the chassis to PE is lost, this current can flow through a person, possibly causing injury. EN 62920 (product standard for inverters in PV applications) of class B, group 1 limits the touch current for devices used in residential applications to 30 mA. The maximum value of Y

capacitors connected between phases and PE for a touch current limitation of 30mA is calculated for the conditions below to be approximately 268nF.

- $V_{MAINS} = 400\text{VAC grid} + 3\% \text{ tolerance } (V_{MAINS_T})$
- $F_{MAINS} = 50\text{Hz}$
- $C_g = 25\text{nF}$, Parasitic capacitance between DC-link rails (DC+ and DC-), mid-point and PE

$$C_{Ymax} := \frac{i_{tc_pk}}{\left(2 \cdot \pi \cdot f_{MAINS} \cdot (1 + V_{MAINS_tolerance}) \cdot \sqrt{2} \cdot \frac{V_{MAINS}}{\sqrt{3}}\right)} - \frac{6}{\pi^2} \cdot C_g \quad \text{Equation 1}$$

4.2 Introduction to Design Methodology

Insertion loss is a key parameter to measure the suppression capability of an EMI filter. It is the ratio of the power transmitted by the source to the load before and after the filter is connected. Figure 23 (a) shows the ideal insertion loss curve for a single-stage filter. It can be seen that the slope of the insertion loss curve of the filter will turn at frequency point f_o , which is called the corner frequency of the filter. The corner frequency of a single-stage LC filter can be calculated from the resonant frequency of the LC tank as shown below, although the parasitics of passive filter components can substantially impact insertion loss of an EMI filter.

$$f_o = \frac{1}{\sqrt{2\pi LC}} \quad \text{Equation 2}$$

It can be seen in Figure 23 (b) that, between f_o and $10f_o$, the insertion loss curve will basically follow the slope of 20 dB/dec. Between $10f_o$ and $100f_o$, the insertion loss curve will gradually deviate from the theoretical curve, but the insertion loss of 20 dB can still be maintained. After $100f_o$, the suppression effect will gradually deteriorate until there is no effect. Due to the decrease in the high-frequency insertion loss of the filter caused by the high-frequency parasitic parameters, the effective frequency band of the traditional filter is very narrow and might not meet the suppression requirements of the full frequency band. For a defined attenuation, however, the volume of a single-stage filter is substantially larger than the volume of a two-stage filter, cf. pp. 400–403 in [10]. Thus, in industrial applications, two-stage filters are of major interest. [9] “*Design Method of Wide-Band High-Current Air-Core Inductor EMI Filter for High Voltage DC Power of Motor Inverter of Electric Vehicle.*” proposes a novel method for determining the series and corner frequency points of filters suitable for a wide frequency band.

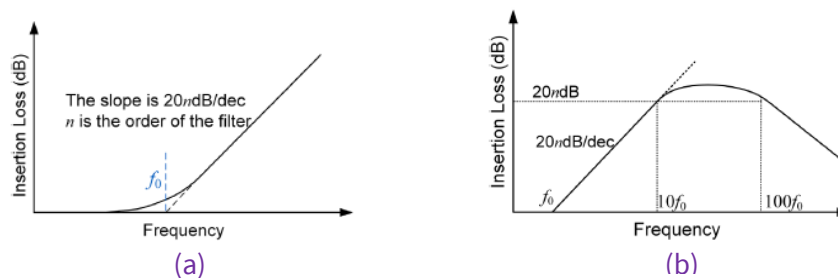


Figure 23: Insertion loss of a single stage filter- (a) Ideal insertion loss curve (b) Non-ideal insertion loss curve [9]

5. Conducted Emissions Results of EUT with EMI Filter Board

For the parameters stated in Table 1, optimization of conducted emissions of EUT without an EMI filter board has been previously discussed. Factors such as PCB layout of the power and gate loop, bonding of the heatsink, connection points of the X and Y capacitors, and selection of the DM choke have proved to be crucial to reduce insertion loss requirements of the EMI filter board. Optimizing these variables on the power board has helped reduce the insertion loss requirement of the EMI filter substantially across the CEMI range. But, as can be seen in Figure 26 in the conducted emissions results without EMI filter, $\sim 45\text{dB}\mu\text{V}$ and $\sim 50\text{dB}\mu\text{V}$ more insertion loss is required at lower and higher frequencies respectively within the CEMI range to achieve pre-compliance.

To handle this, a two-stage passive EMI filter with filter topology LCLC as shown in Figure 24 and Figure 25 is designed and optimized to mitigate conducted emissions of the EUT. Specifications of the EMI filter components are given in Table 5.

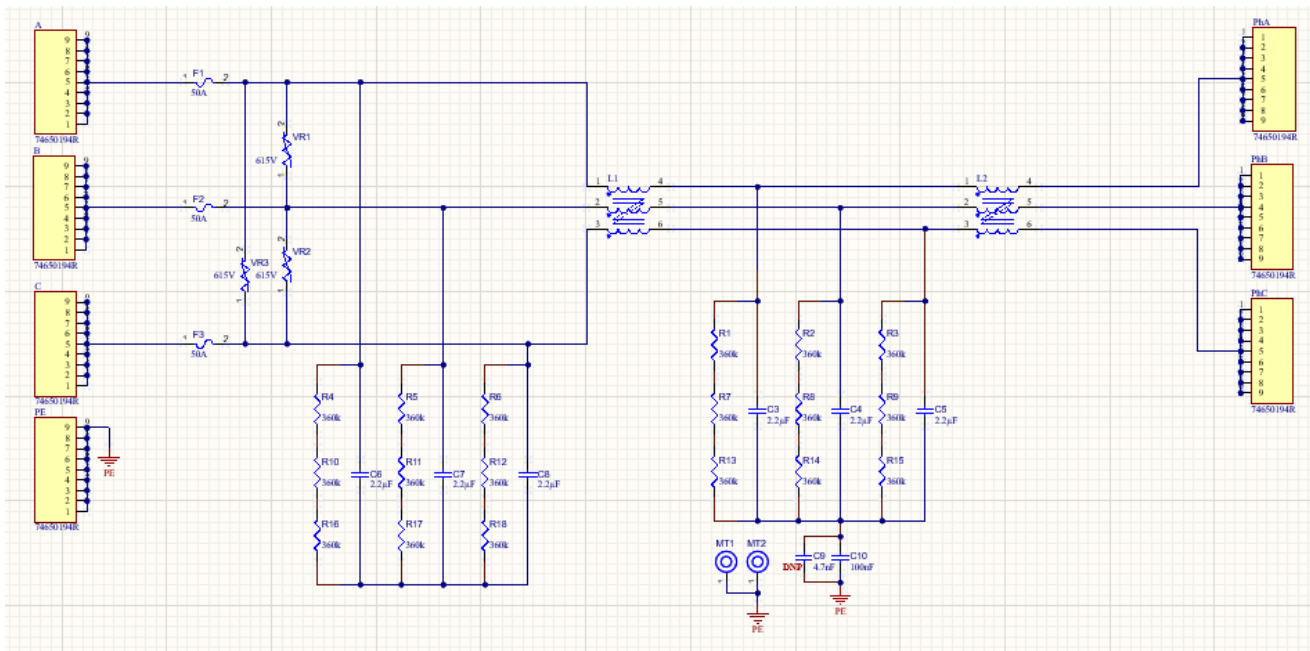


Figure 24: Schematic for 25kW three-phase 2-stage EMI Filter board

We know from Figure 9, that CM and DM noise are similar at lower frequencies while DM noise dominates at higher frequencies. Identical CM chokes based on nanocrystalline iron cores are used in both stages. This helps to mitigate not just CM noise but DM noise effectively across the CEMI range. As discussed before, owing to the increased impact of parasitics, insertion loss of CM chokes reduces at higher frequencies. Hence, a 100nF metallized polypropylene type Y capacitor is used in the first stage of filter, connected between the star point of the X capacitors and PE/chassis to mitigate CM noise at higher frequencies. Further, as can be seen in Figure 25, the CM choke is constructed with single-wire winding, which helps to reduce parasitic capacitance and improves its high frequency response. X capacitors further aid to mitigate DM noise at lower frequencies, which couldn't be tackled with CM chokes. X capacitors are connected to a star point in both stages to improve power density as discussed previously.

Conducted emission results of EUT with and without the EMI filter board are shown in Figure 26 and Figure 27 for 47kHz and 60kHz switching frequency respectively. With the EMI filter board, conducted emissions of the EUT for both switching frequencies are well within the limit line.

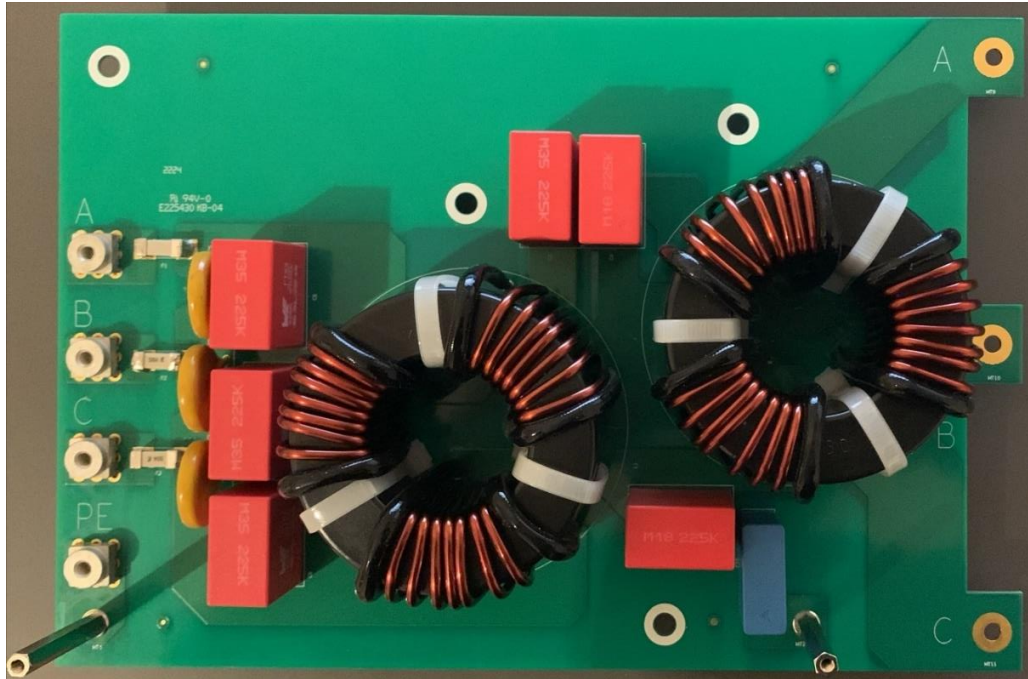


Figure 25: 25kW three-phase 2-stage EMI filter board prototype

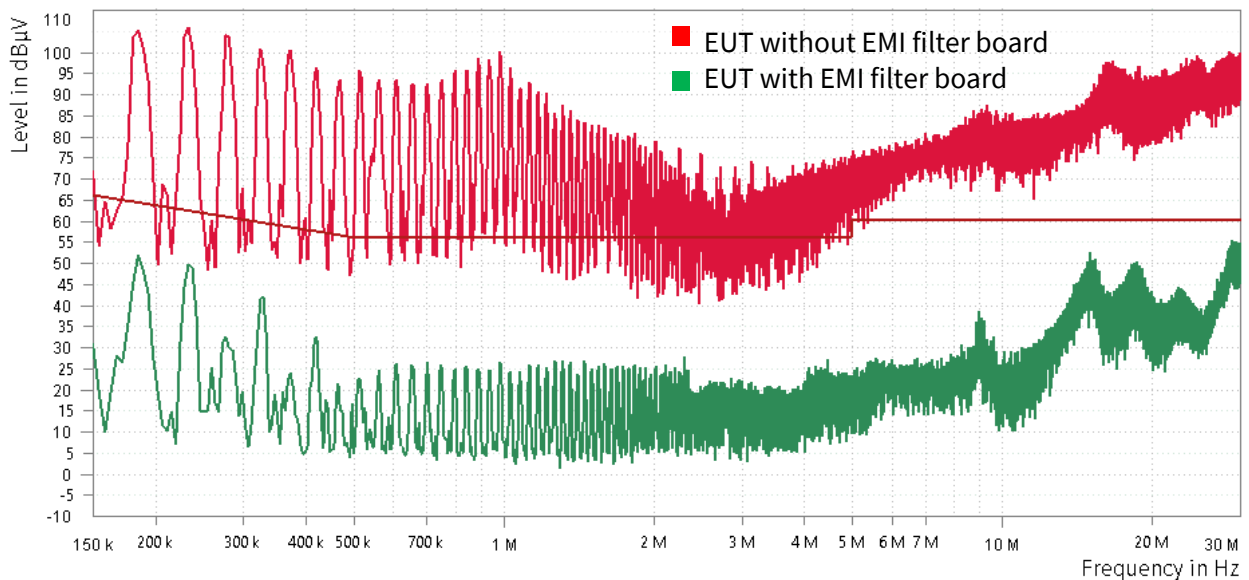


Figure 26: Conducted emissions of EUT without and with EMI filter board at 22kW, 47kHz

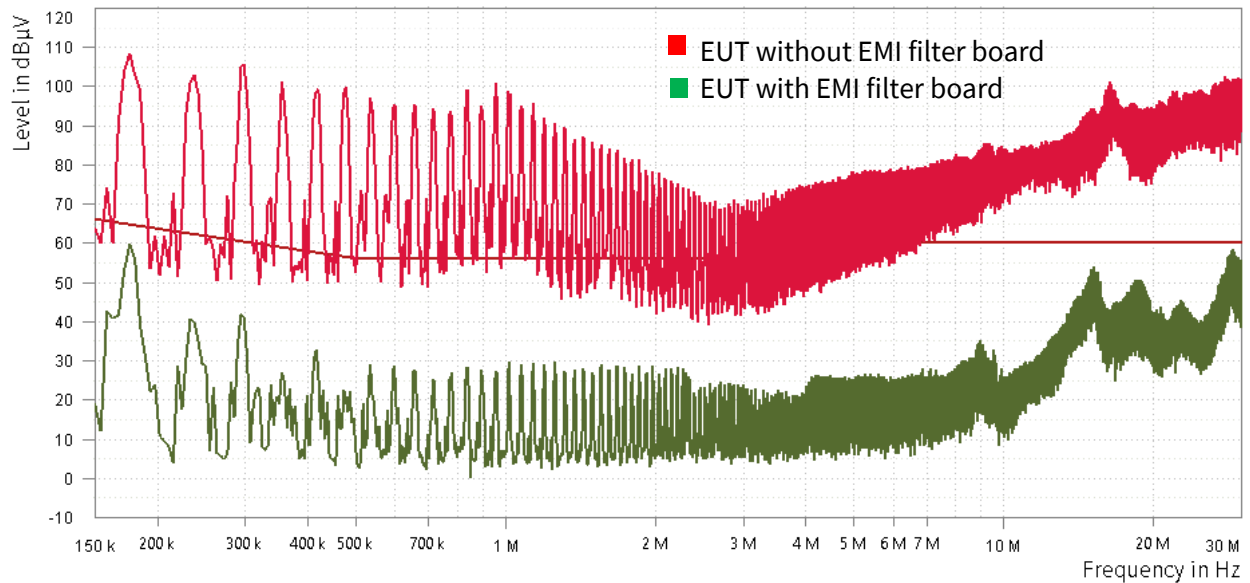


Figure 27: Conducted emissions of EUT without and with EMI filter board at 22kW, 60kHz

	Component	Parameters	Part No.
First Stage (Close to EUT)	CM choke	14.58mH @ 10kHz, 40A, Nanocrystalline core, sectional single layer winding with wire diameter of 2.44mm	Prax Power PI-103471-00
	X Capacitor	2.2µF, X2-Safety Class Capacitor; MKP - Metallized Polypropylene	Wuerth Elektronik 890324026034CS
	Y capacitor	100nF, Y2-Safety Class Capacitor; MKP - Metallized Polypropylene	TDK B32023A3104M189
Second Stage (Close to LISN)	CM choke	14.58mH @ 10kHz, 40A, Nanocrystalline core, sectional single layer winding with wire diameter of 2.44mm	Prax Power PI-103471-00
	X Capacitor	2.2µF, X2-Safety Class Capacitor; MKP - Metallized Polypropylene	Wuerth Elektronik 890324026034CS

Table 5: Specification of EMI Filter components

6. PCB Layout & Component Placement

6.1 PCB layout techniques

PCB layout techniques for SiC MOSFETs follows the same principles as for Si designs.

6.1.1 'Optimized' Gate Loop

- 1) Compact gate drive can be achieved by having the gate driver IC as close to the SiC MOSFET as possible (see Figure 28 (a)). Avoid an overlap between the gate, gate drive circuit, gate drive bias power supply and the drain trace of the MOSFET. Overlap between drain trace and gate circuit of the MOSFET can result in

additional Cgd, which will not only add switching losses but also result in gate oscillations and causes EMI issues

2) Mitigating gate oscillations

- a) Add an external gate-source capacitor and resistor close to the SiC MOSFET (see Figure 28 (b))
- b) A gate-source capacitor is only applicable for packages with KS pin. Wolfspeed does not recommend an external gate-source capacitor for TO-247-3.
- c) A gate-source resistor (typically 10 kΩ) is critical to discharge the gate in case MOSFET is disconnected from the driver. Without this, the FET remains ON, when it should be OFF and could lead to a shoot-through.

6.1.2 Counter action against high di/dt

In addition to a low inductive gate loop, steps could be taken to minimize impact of higher slew rates. Shielding of sensitive gate signals from high magnetic fields (caused due to high di/dt) is important. As shown as an example in Figure 30, if signals and gate drive circuit are routed on top layer, 2nd layer should be return plane connected to source of device. This return plane provides shielding for sensitive signals and gate drive circuit while ensuring shortest possible return paths for gate drive signals to reduce loop area and hence, a low parasitic loop inductance.

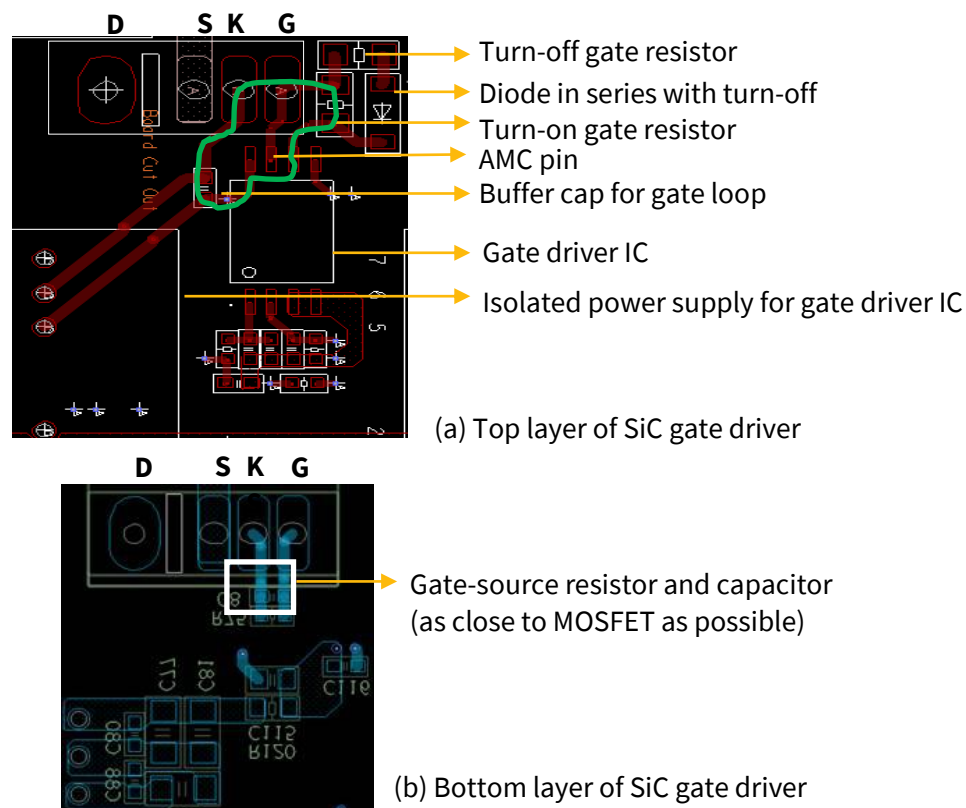


Figure 28: PCB layout example of an 'optimized' gate loop

6.1.3 Counter action against high dv/dt

- 1) With proper component placement (see Figure 29), avoid overlap of gate drive and the drain of MOSFET
- 2) Minimizing overlap between gate drive and power loop ensures reduced external parasitic capacitance (C_{gd} and C_{gs})
- 3) High dv/dt traces (e.g., switching node) should be kept small and only wide enough to carry the current

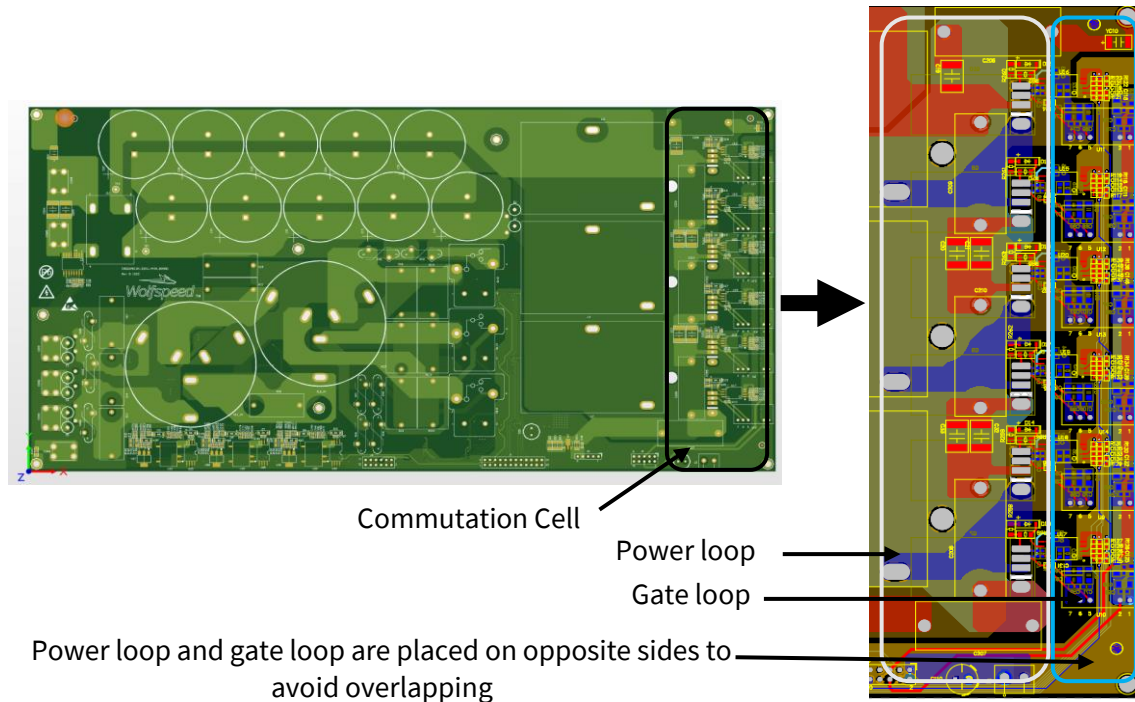


Figure 29 : PCB layout example to minimize overlap between gate and power loop

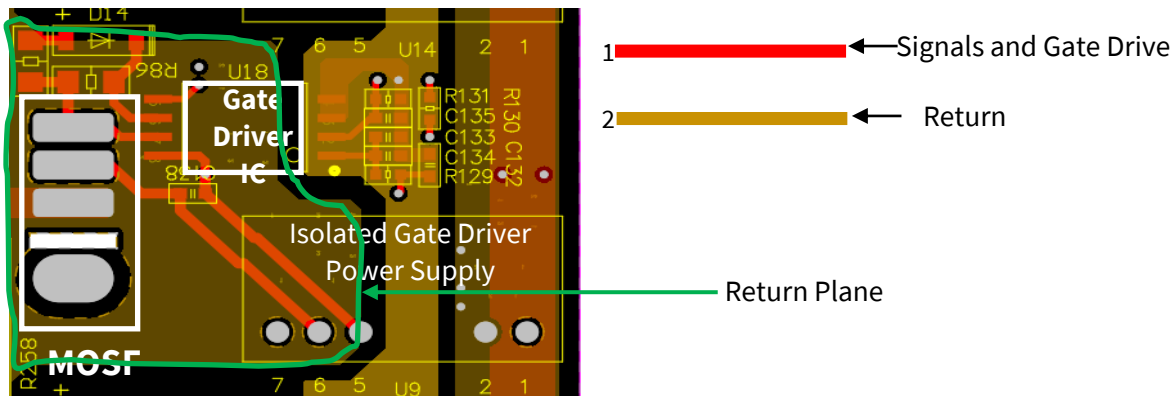


Figure 30 : Return plane of gate drive providing shield to sensitive gate signals

6.2 Component Placement

- 1) Design goals for component placement

- a) Preferably, input and output connector should be placed on opposite side of board to avoid noise coupling. This is critical for EMI
- b) Place a grounded shield between input and output when they are on the same side (see Figure 31)
- c) Input EMI filter and the input/output connectors should be placed far away from high dV/dt traces/nodes to avoid noise coupling.
- d) Sensitive signals (e.g., gate loop, control signals) should be placed far away from the high dV/dt trace
- e) Sensitive signals should be placed far away from the high magnetic field such as PFC choke, DCDC power magnetics

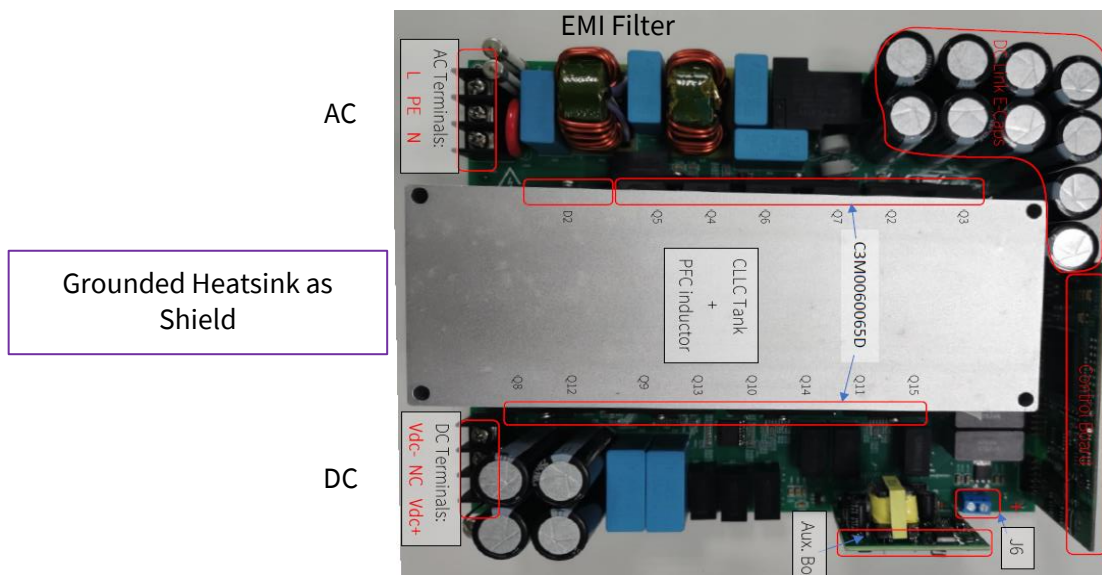


Figure 31: Example of Shielding when input and output are on the same side

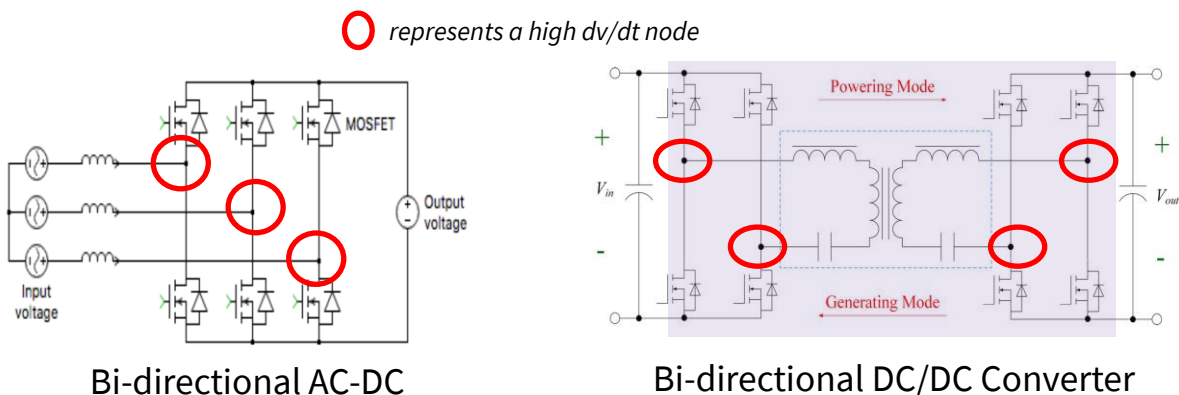


Figure 32: High dV/dt nodes in AC/DC and DC/DC converters

7. Conclusion

EMI filter design is a crucial and challenging topic for power electronics applications. Since the design of an EMI filter is unique to a circuit, it is not possible to suggest a universal solution.

In this study, conducted emissions of a three-phase, three-level, T-type, grid-connected PV inverter is studied. The impact of auxiliary components and gate drive, DM inductor, connection of the heatsink, and connection of the DM capacitors on conducted emissions of the inverter are discussed. Suggestions for optimization to enable a compact EMI filter and improve the overall power density of the converter are provided and verified with measurements.

Further, different components constituting an EMI filter and factors dictating their selection for an optimal and reliable EMI filter are discussed in detail. X capacitors are connected in star configuration to enable higher power density. The leakage inductance of a CM choke is used as a DM inductor to avoid bulky filter design. Also, the filter design with a single Y capacitor between the star point of X capacitors and PE has improved the power density of the inverter.

Conducted EMI for the inverter at two different switching frequencies, 47kHz and 60kHz, up to a power level of 22kW, has been measured and shown to meet the limits specified by the 61000-6-3 standard in a pre-compliance test. With this study, technical experience on a filter design is shared. In addition, good practices for PCB layout and component placement to achieve a low EMI design are discussed in detail. The results and learnings obtained from this study serve as a practical guide for designers.

It should be emphasized here that the solution discussed is one of the many possible approaches to handle conducted EMI for a system. The optimal EMI filter will depend on various factors like trade-off between power density and efficiency, time to market and available resources. However, as the testing demonstrates, conventional design and filtering approaches used in silicon IGBT and MOSFET-based designs apply to SiC-based designs as well.

8. References

- [1] Hizarci, H., Pekperlak, U., & Arifoglu, U. (2021). Conducted emission suppression using an EMI filter for Grid-Tied Three-Phase/Level T-Type solar inverter. IEEE Access, 9, 67417–67431. <https://doi.org/10.1109/access.2021.3077380>
- [2] CRD-25BDA6512N-K: 25kW Bi-Directional T-Type Inverter User Guide
- [3] M. Schweizer, I. Lizama, T. Friedli, and J. W. Kolar, “Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies,” in IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society, 2010, pp. 391–396
- [4] J. W. Kolar, U. Drofenik, J. Miniböck, and H. Ertl, “A new concept for minimizing high-frequency common-mode EMI of three-phase PWM rectifier systems keeping high utilization of the output voltage,” in Proc. IEEE 15th Appl. Power Electron. Conf. Expo., 2000, vol. 1, pp. 519–527.
- [5] Calculating Parasitic Capacitance of Three-Phase Common-Mode Chokes <http://www.stefan-peter-weber.de/publikationen/pcim05.pdf>
- [6] M.Nave, On Modeling the Common Mode Inductor, IEEE Int. Symp. on EMC, pp.452-457, 1991
- [7] Diss. ETH No. 23343 David O. Boillat: Modular High Bandwidth Switch-Mode Three-Phase AC Voltage Source
- [8] KEMET. (2007). EMI Capacitors on the AC Line. [Online]. Available: <https://ec.kemet.com/wp-content/uploads/sites/4/2019/10/201-FY19-Apps-AC-Line-Final-v2.pdf>
- [9] Zhai, Li, et al. “Design Method of Wide-Band High-Current Air-Core Inductor EMI Filter for High Voltage DC Power of Motor Inverter of Electric Vehicle.” IET Power Electronics, 18 June 2022, <https://doi.org/10.1049/pel2.12341>. Accessed 7 Aug. 2022.
- [10] R. W. Erickson and D. Maksimovic, Fundamentals of power electronics, 2nd edition. Norwell, MA: Kluwer Academic, 2001, 881 p.
- [11] S. -Y. Chen et al., "A Compact Three-Phase Multi-Stage EMI Filter with Compensated Parasitic-Component Effects," 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2024