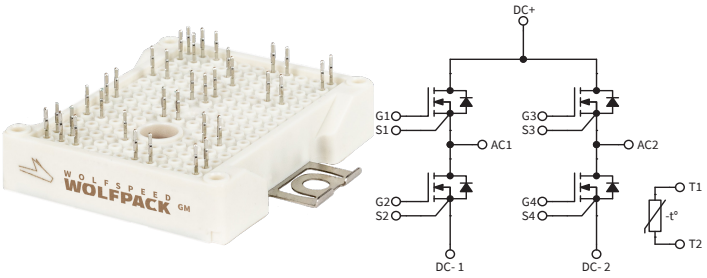
CBB011M12GM4, CBB011M12GM4T

V_{DS}	1200 V
$R_{DS(on)}$	11 mΩ

1200 V, 11 mΩ, Silicon Carbide, Full-Bridge Module



Technical Features

- Ultra-Low Loss
- High Frequency Operation
- Zero Turn-Off Tail Current from MOSFET
- Normally-Off, Fail-Safe Device Operation
- Optional Pre-Applied Thermal Interface Material
- Features Gen4 Technology with Soft Body Diode

Typical Applications

- EV Chargers
- High-Efficiency Converters / Inverters
- Renewable Energy
- Smart-Grid / Grid-Tied Distributed Generation

System Benefits

- Enables Compact, Lightweight Systems
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Voltage	V_{DS}			1200	V	T_{HS} = 25 °C	
Maximum Gate-Source Voltage	$V_{GS(max)}$	-8		+19		Transient	Fig. 33 Note 1
Operational Gate-Source Voltage	$V_{GS(op)}$		-4/15			Static	
DC Continuous Drain Current (T_{VJ} ≤ 150 °C)	I_D			100	A	V_{GS} = 15 V, T_{HS} = 50 °C, T_{VJ} ≤ 150 °C	Notes 2,3,4 Fig. 20
DC Continuous Drain Current (T_{VJ} ≤ 175 °C)				100		V_{GS} = 15 V, T_{HS} = 50 °C, T_{VJ} ≤ 175 °C	
Pulsed Drain Current	I_{DM}			200		t_{Pmax} limited by T_{VJmax} V_{GS} = 15 V, T_{HS} = 50 °C	
Power Dissipation	P_D		292		W	T_{HS} = 50 °C, T_{VJ} ≤ 175 °C	Note 5 Fig. 20
Virtual Junction Temperature	$T_{VJ(op)}$	-40		150	°C	Operation	
		-40		175	°C	Intermittent with Reduced Life	

Note (1): Recommended turn-on gate voltage is 15 V with ±5% regulation tolerance
Note (2): Current limit at T_{HS} = 50°C ,T_{VJ} ≤ 150 °C calculated by $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)}(T_{VJ(max)}, I_{D(max)})}$
Note (3): Current limit at T_{HS} = 50°C, T_{VJ} ≤ 175 °C imposed by package
Note (4): Verified by design
Note (5): $P_D = (T_{VJ} - T_{HS})/R_{TH(JH,typ)}$

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MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	4.0	V	V_{DS} = V_{GS}, I_D = 28 mA	
			2.0			V_{DS} = V_{GS}, I_D = 28 mA, T_{VJ} = 175 °C	
Zero Gate Voltage Drain Current	I_{DSS}		3	300	µA	V_{GS} = 0 V, V_{DS} = 1200 V	
Gate-Source Leakage Current	I_{GSS}		60	1200	nA	V_{GS} = 19 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		11.0	14.9	mΩ	V_{GS} = 15 V, I_D = 100 A	Fig. 2 Fig. 3
			17.6			V_{GS} = 15 V, I_D = 100 A, T_{VJ} = 150 °C	
			19.8			V_{GS} = 15 V, I_D = 100 A, T_{VJ} = 175 °C	
Transconductance	g_{fs}		77		S	V_{DS} = 20 V, I_D = 100 A	Fig. 4
			78			V_{DS} = 20 V, I_D = 100 A, T_{VJ} = 175 °C	
Turn-On Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{On}		1.2 1.1 1.2		mJ	V_{DD} = 600 V, I_D = 100 A, V_{GS} = -4 V/15 V, $R_{G(off)}$ = 0 Ω, $R_{G(on)}$ = 1 Ω L_σ = 24 nH	Fig. 11 Fig. 13
Turn-Off Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{Off}		0.17 0.15 0.12				
Internal Gate Resistance	$R_{G(int)}$		1.4		Ω	f = 100 kHz	
Input Capacitance	C_{iss}		10.1		nF	V_{GS} = 0 V, V_{DS} = 800 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		0.4				
Reverse Transfer Capacitance	C_{rss}		36		pF		
Gate to Source Charge	Q_{GS}		180		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V, I_D = 100 A, Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		96				
Total Gate Charge	Q_G		405				
FET Thermal Resistance, Junction to Heatsink	$R_{th\ JH}$		0.429		°C/W	Measured with Pre-Applied TIM	Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
Body Diode Forward Voltage	V_{SD}		5.8		V	V_{GS} = -4 V, I_{SD} = 100 A	Fig. 7
			5.4			V_{GS} = -4 V, I_{SD} = 100 A, T_{VJ} = 175 °C	
DC Source-Drain Current (Body Diode)	$I_{SD\ BD}$		63		A	V_{GS} = -4 V, T_{HS} = 50 °C, T_{VJ} ≤ 175 °C	Notes 3,4 Fig. 20
Reverse Recovery Time	t_{RR}		20.3		ns	V_{GS} = -4 V, I_{SD} = 100 A, V_R = 600 V di/dt = 16.4 A/ns, T_{VJ} = 175 °C	Fig. 32
Reverse Recovery Charge	Q_{RR}		2.25		µC		
Peak Reverse Recovery Current	I_{RRM}		183		A		
Reverse Recovery Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{RR}		0.38 0.48 0.66		mJ	V_{DD} = 600 V, I_D = 100 A, V_{GS} = -4 V/15 V, $R_{G(on)}$ = 1.0 Ω, L_σ = 24 nH	Fig. 14

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Package Resistance, M1 (High-Side)	R_{HS}		2.98		mΩ	T_{HS} = 125°C, Note 5
Package Resistance, M2 (Low-Side)	R_{LS}		3.18			
Stray Inductance	L_{Stray}		16.8		nH	Between DC- and DC+, f = 10 MHz
Case Temperature	T_C	-40		125	°C	
Mounting Torque	M_S		2.0	2.3	N-m	M4 bolts
Weight	W		39		g	
Case Isolation Voltage	V_{isol}	3			kV	AC, 50 Hz, 1 minute
Comparative Tracking Index	CTI	200				
Clearance Distance			5.0		mm	Terminal to Terminal
			10.0			Terminal to Heatsink
Creepage Distance			6.3			Terminal to Terminal
			11.5			Terminal to Heatsink

Note (5): Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance

Temperature Sensor (NTC) Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rated Resistance	R_{NTC}		5.0		kΩ	T_{NTC} = 25°C
Resistance Tolerance at 25 °C	ΔR/R	-5		5	%	
Beta Value (T_2 = 50 °C)	$ß_{25/50}$		3380		K	
Beta Value (T_2 = 80 °C)	$ß_{25/80}$		3468		K	
Beta Value (T_2 = 100 °C)	$ß_{25/100}$		3523		K	
Power Dissipation	P_{Max}			10	mW	T_{NTC} = 25°C

Typical Performance

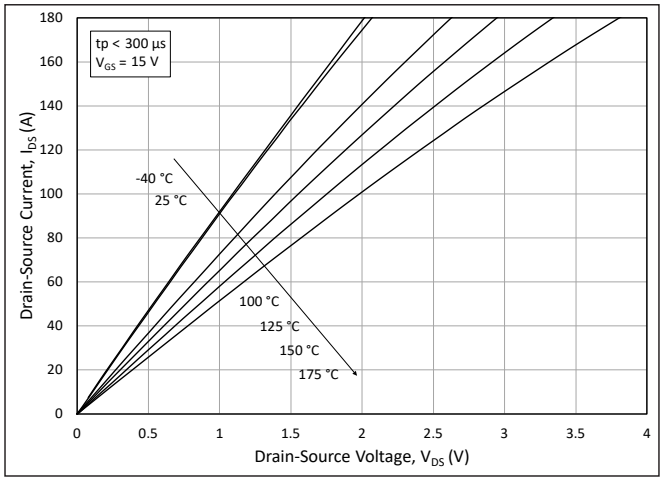


Figure 1. Output Characteristics for Various Junction Temperatures

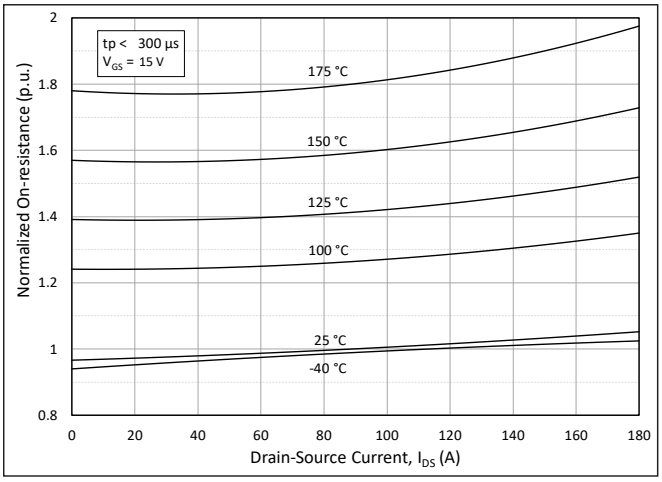


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

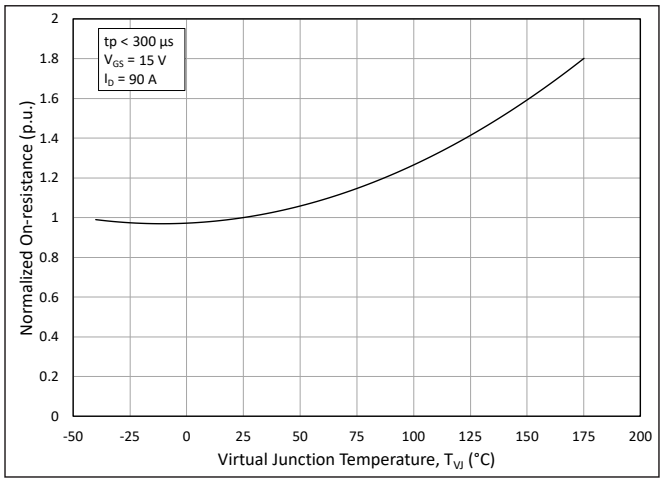


Figure 3. Normalized On-State Resistance vs. Junction Temperature

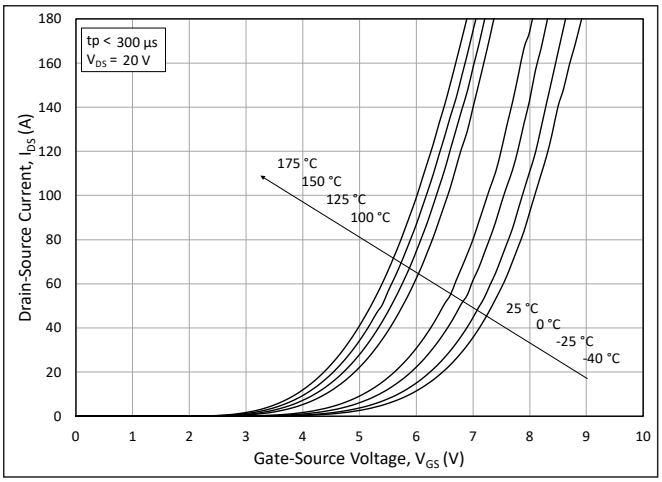


Figure 4. Transfer Characteristic for Various Junction Temperatures

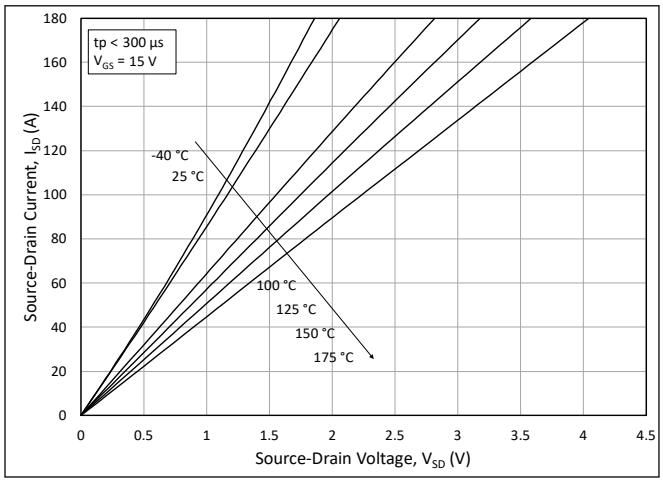


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

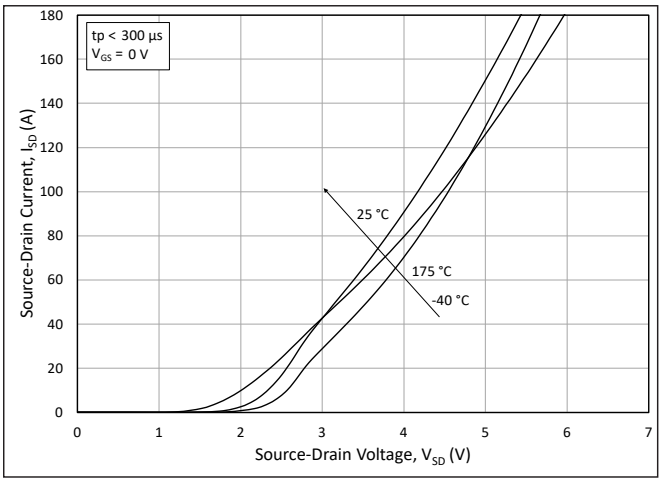


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Body Diode)

Typical Performance

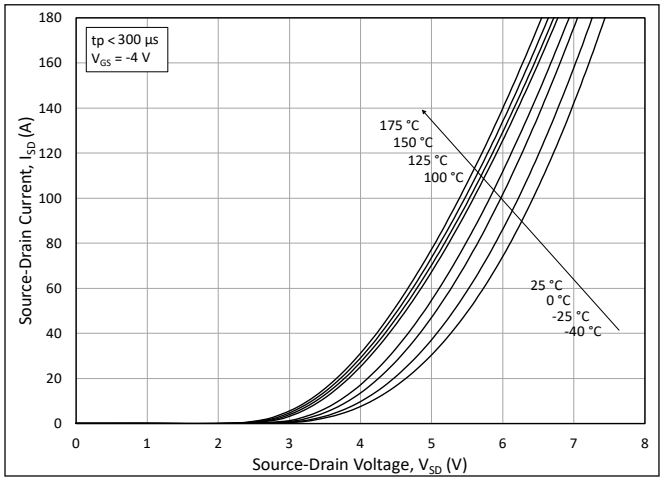


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = - 4 V (Body Diode)

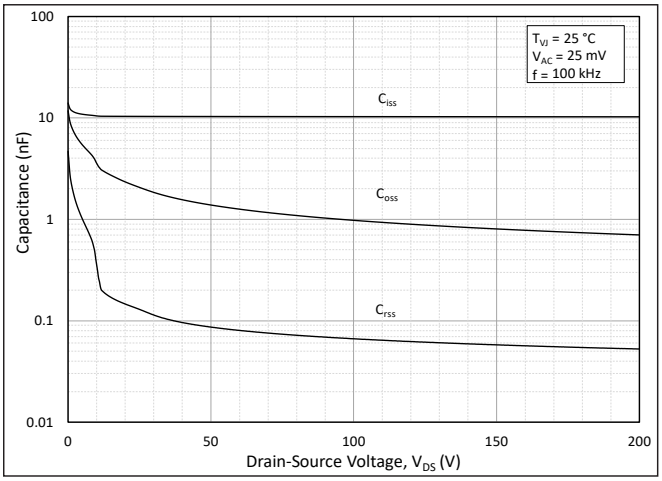


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

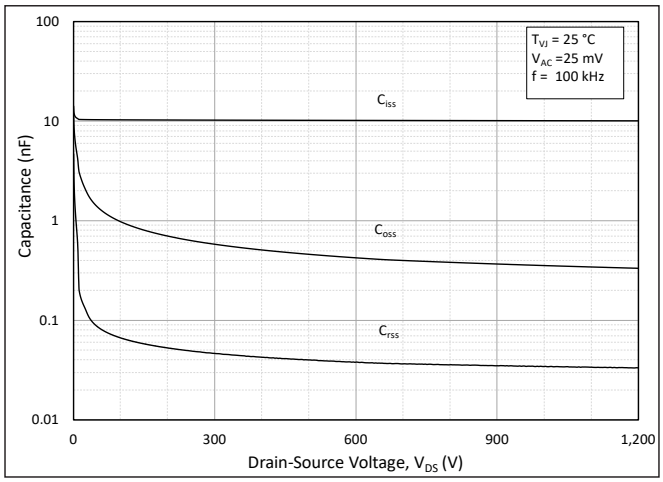


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

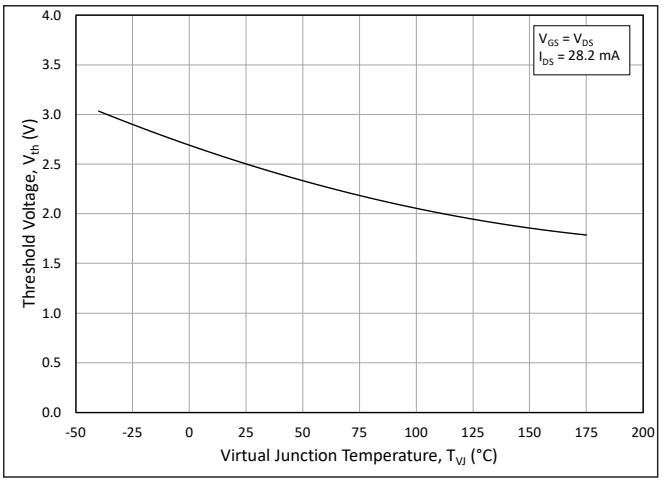


Figure 10. Threshold Voltage vs. Junction Temperature

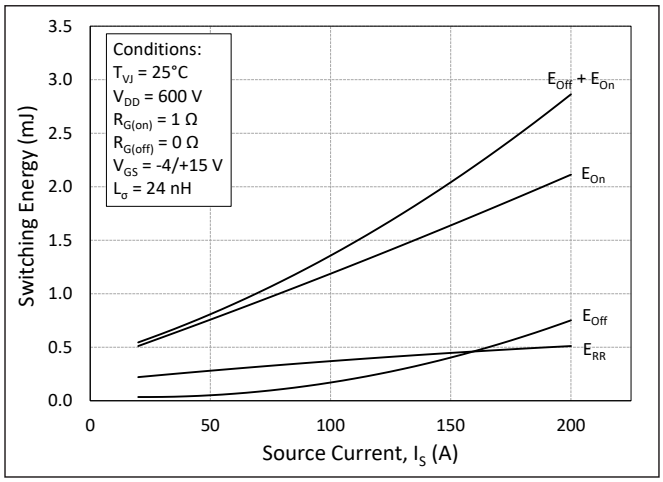


Figure 11. Switching Energy vs. Drain Current (V_{DD} = 600 V)

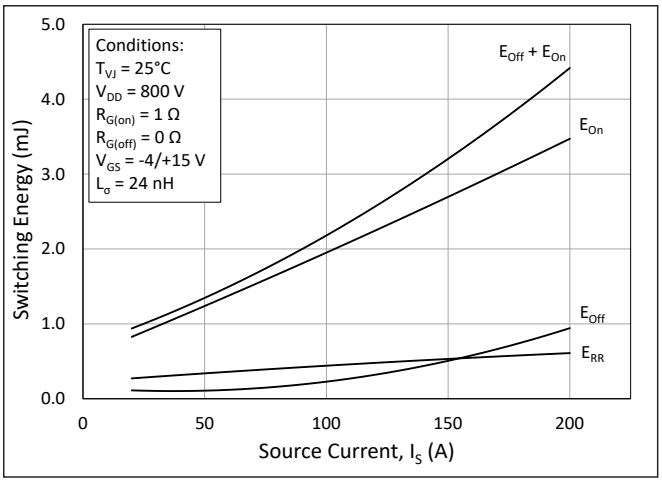


Figure 12. Switching Energy vs. Drain Current (V_{DD} = 800 V)

Typical Performance

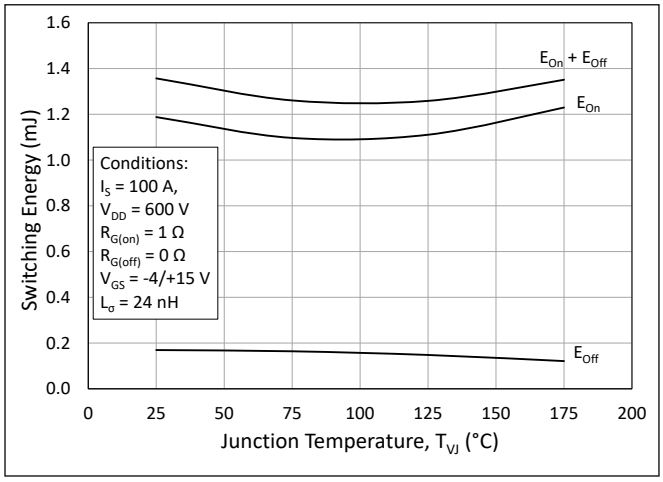


Figure 13. MOSFET Switching Energy vs. Junction Temperature

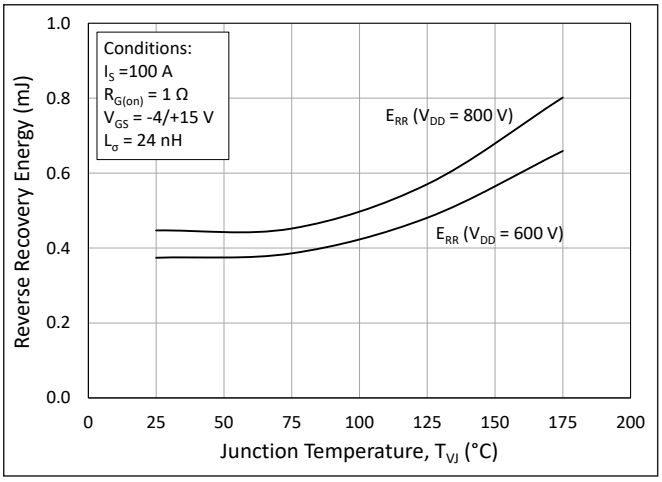


Figure 14. Reverse Recovery Energy vs. Junction Temperature

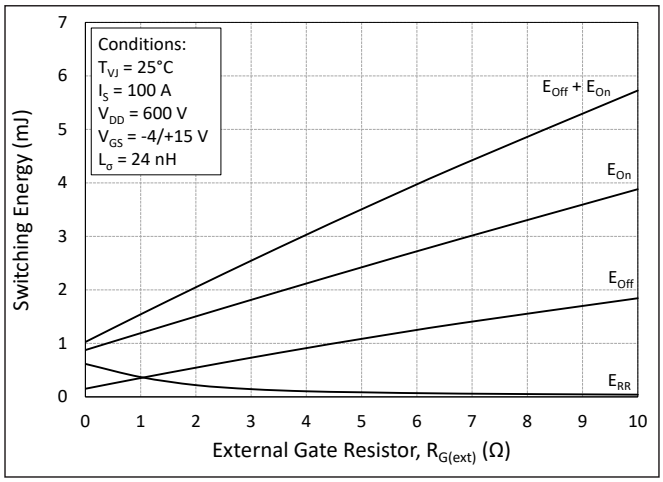


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

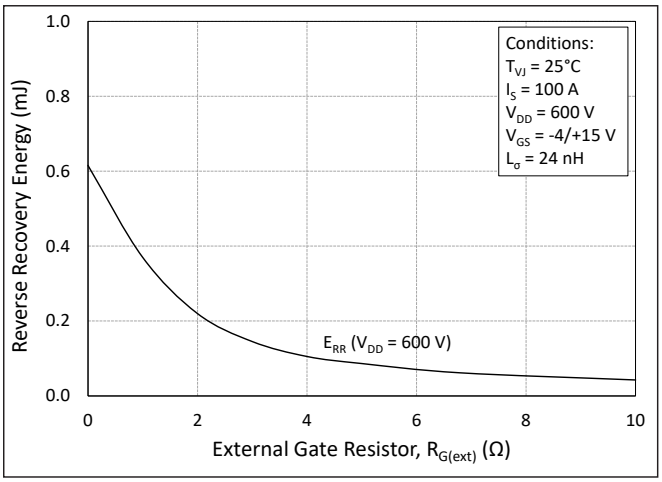


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

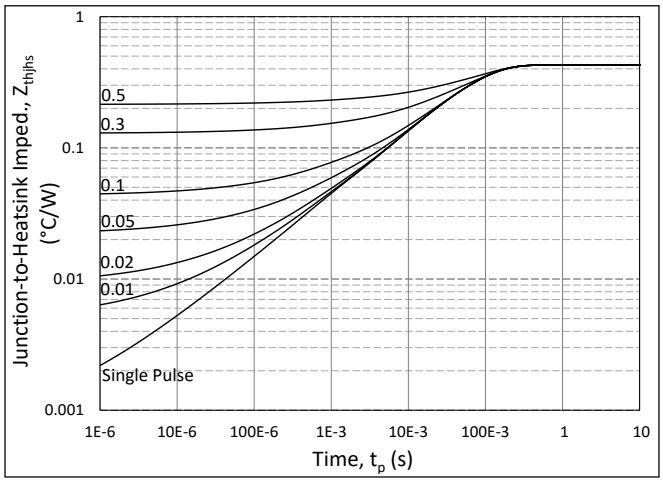


Figure 17. MOSFET Junction to Heatsink Transient Thermal Impedance, $Z_{th\ JHS}$ (°C/W)

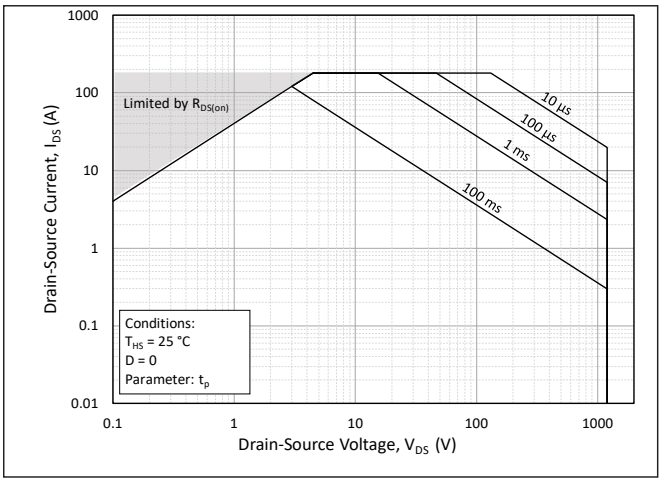


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

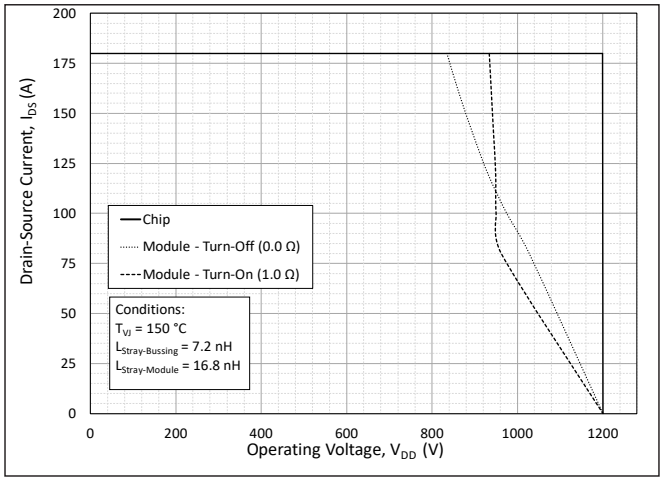


Figure 19. Switching Safe Operating Area

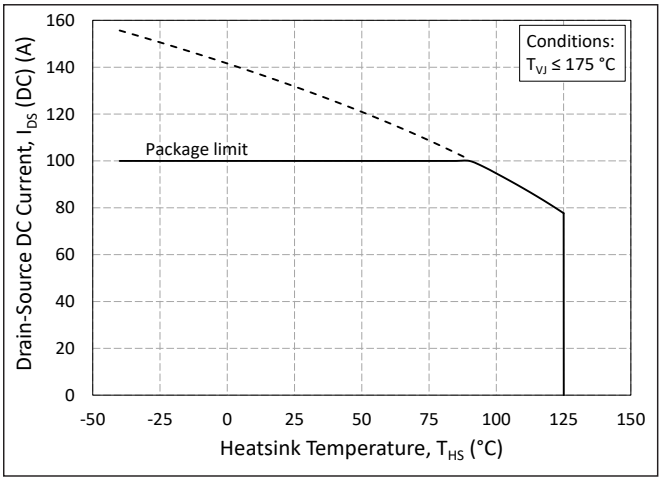


Figure 20. Continuous Drain Current Derating vs. Heatsink Temperature

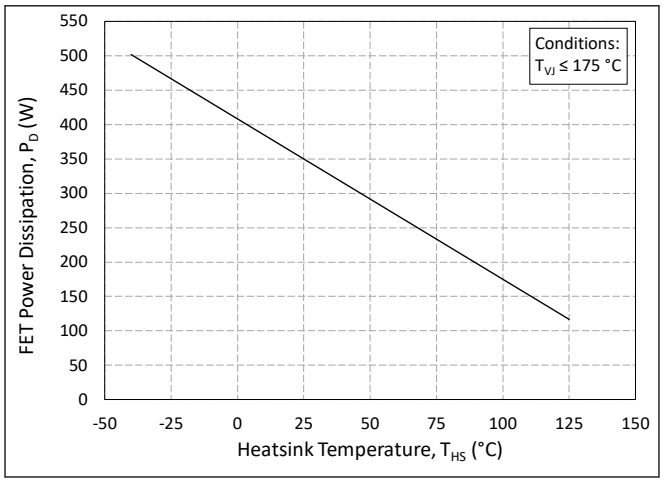


Figure 21. Maximum Power Dissipation Derating vs. Heatsink Temperature

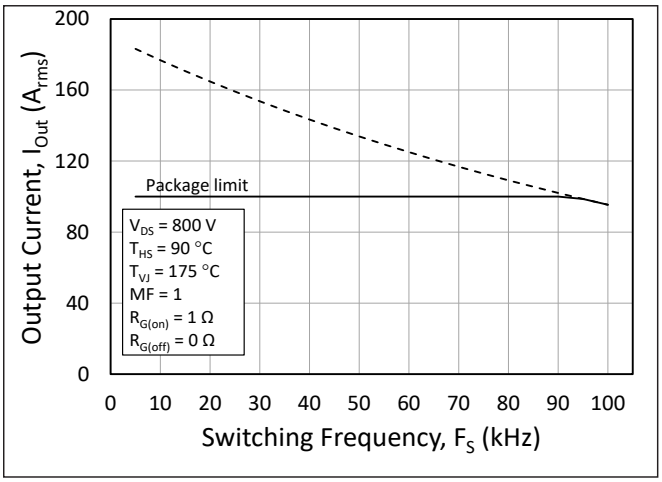


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

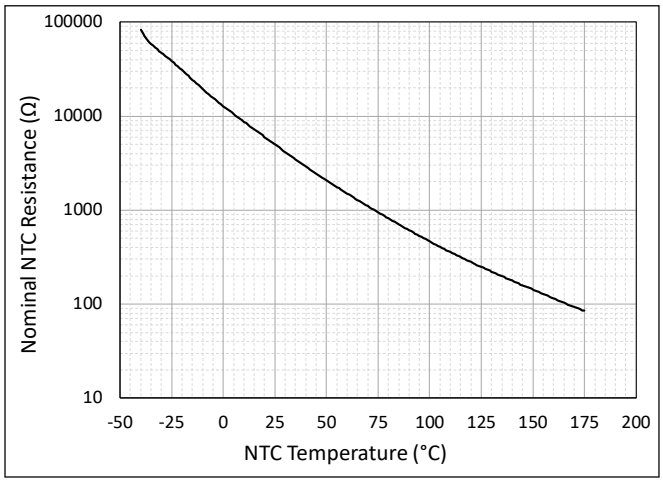


Figure 23. Nominal NTC Resistance vs. NTC Temperature

Timing Characteristics

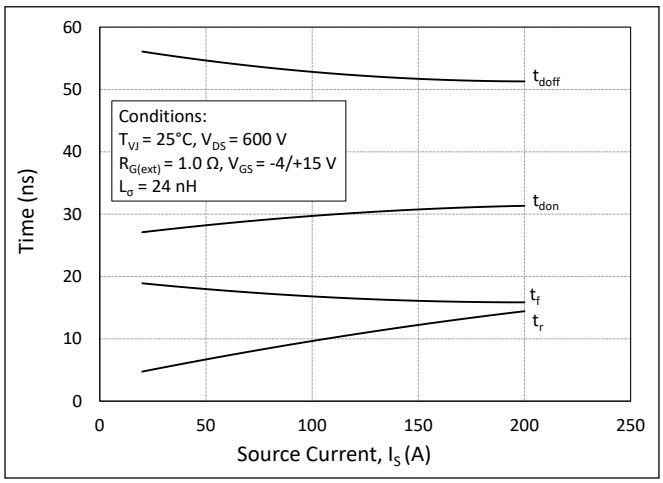


Figure 24. Timing vs. Source Current

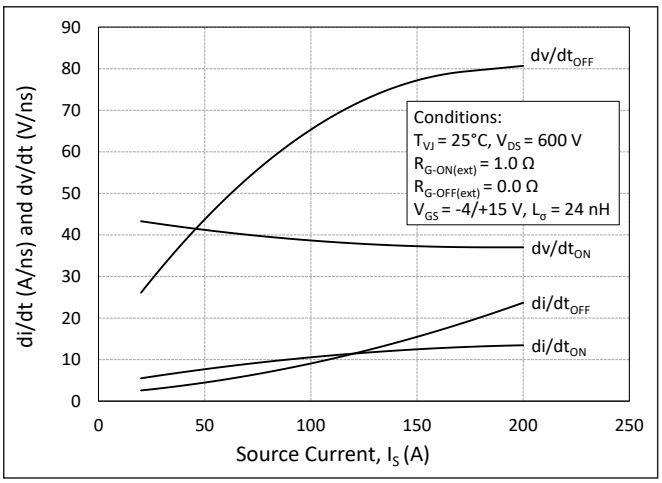


Figure 25. dv/dt and di/dt vs. Source Current

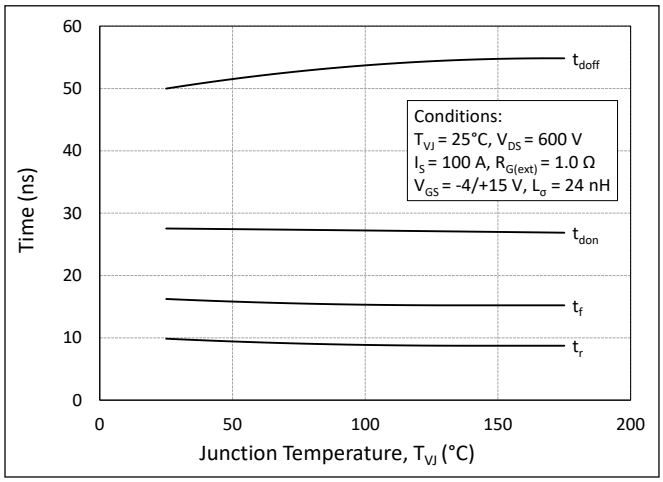


Figure 26. Timing vs. Junction Temperature

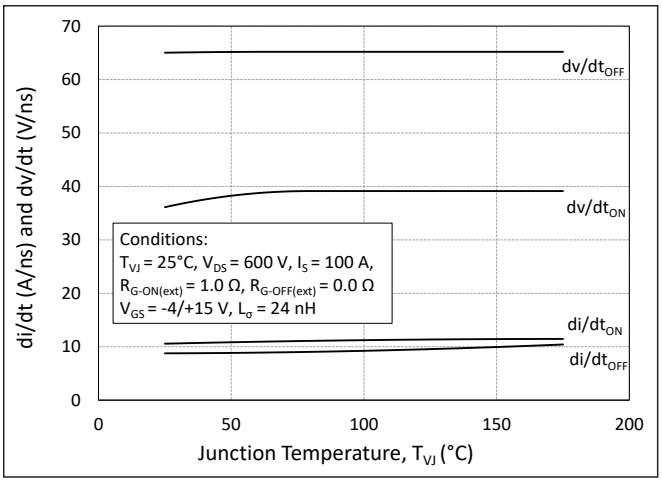


Figure 27. dv/dt and di/dt vs. Junction Temperature

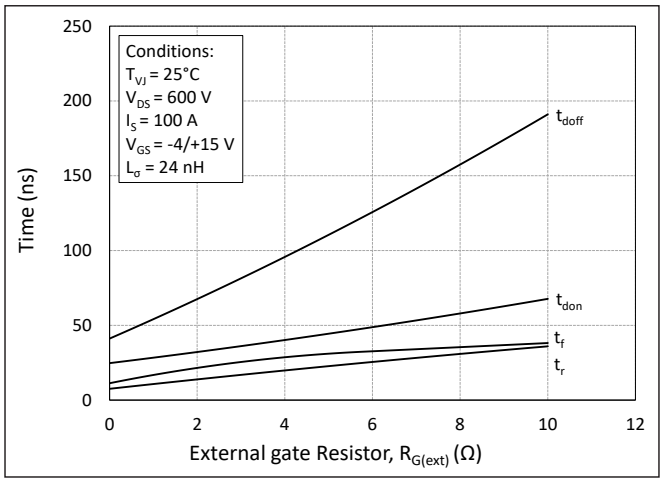


Figure 28. Timing vs. External Gate Resistance

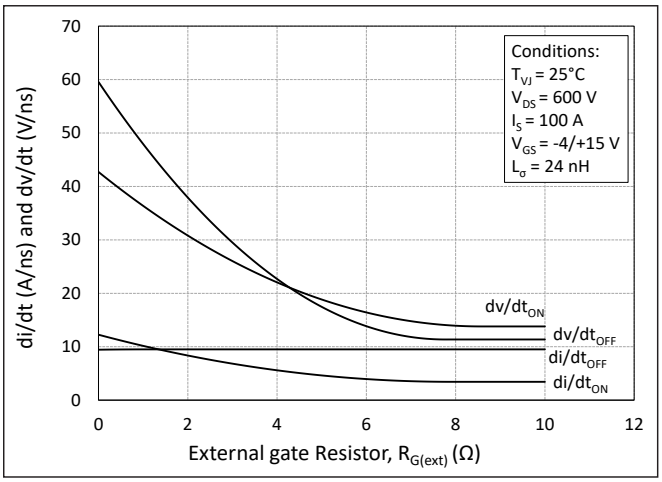


Figure 29. dv/dt and di/dt vs. External Gate Resistance

Definitions

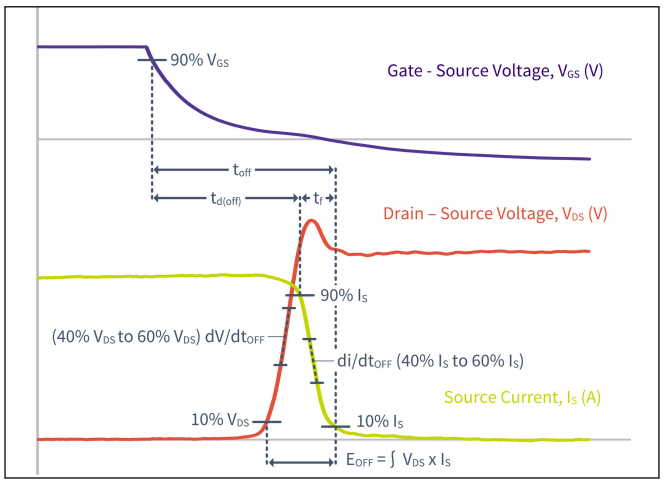


Figure 30. Turn-off Transient Definitions

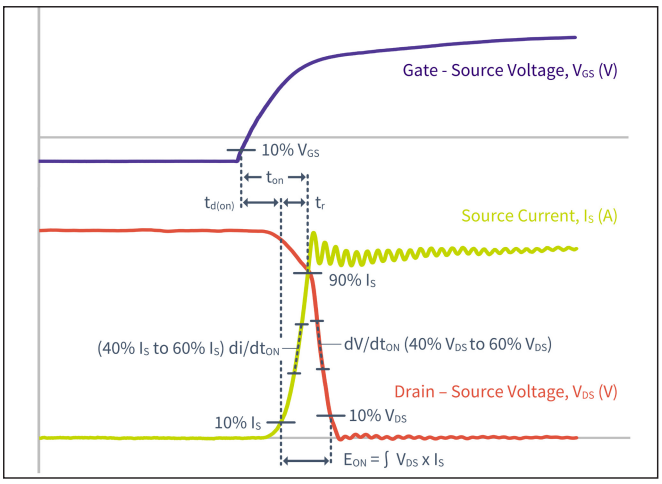


Figure 31. Turn-on Transient Definitions

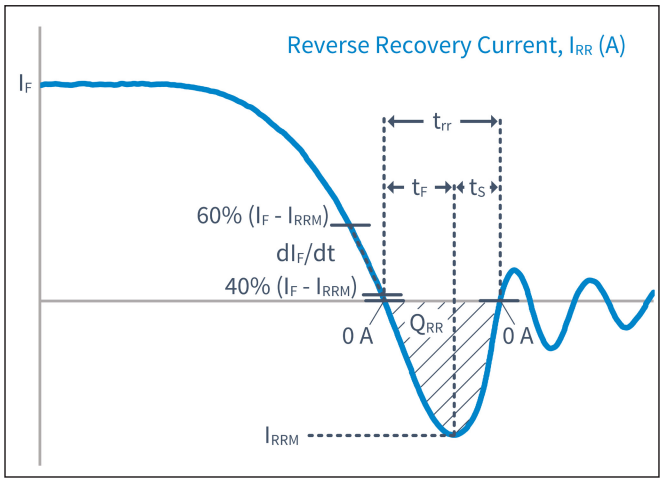


Figure 32. Reverse Recovery Definitions

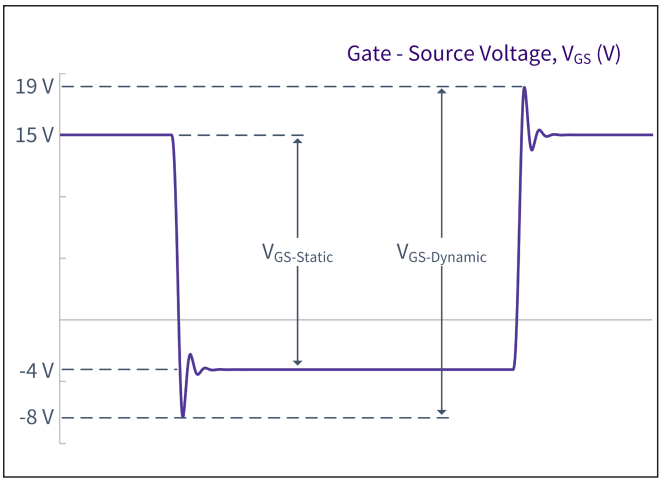
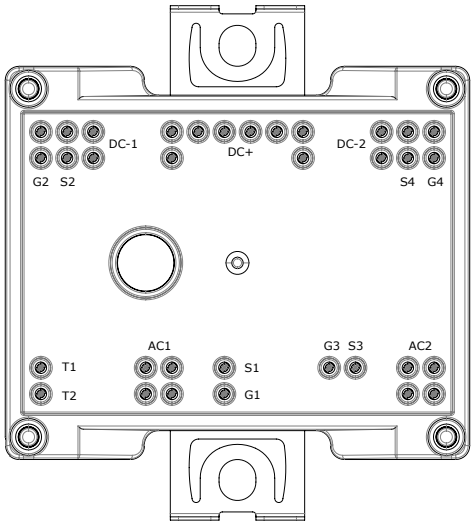
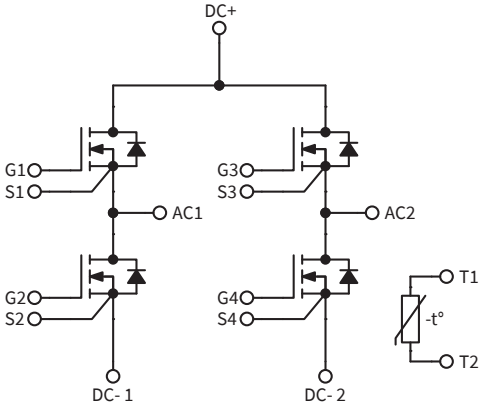


Figure 33. V_{GS} Transient Definitions

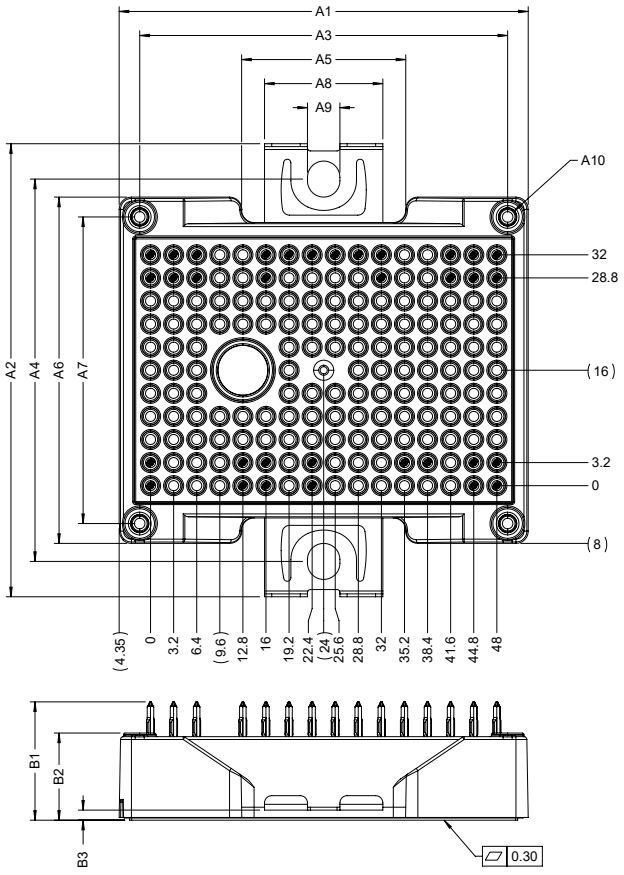
Note (6): The CGD1700HB2M-UNA, which features the UCC21710 gate driver IC from Texas Instruments, was used to evaluate dynamic performance. The typical parasitic turn-on resistance of 2.5 Ω and the parasitic turn-off resistance of 0.3 Ω are not included in the $R_{G(ext)}$ values on this datasheet.

Schematic and Pin Out





Package Dimension (mm)



DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	56.7	±0.30
A2	62.8	±0.50
A3	51	±0.15
A4	(53)	REF.
A5	22.7	±0.30
A6	48	±0.30
A7	42.5	±0.15
A8	16.4	±0.20
A9	4.5	±0.10
A10	⌀2.3 ↧8.5	⌀: $^{+0}_{-0.10}$ ↧: ±0.30
B1	16.4	±0.50
B2	12.0	±0.35
B3	1.4	±0.20
ALL PIN LOCATIONS		±0.40

Product Ordering Code

Part Number	Description
CBB011M12GM4	Without Pre-Applied Phase Change Thermal Interface Material
CBB011M12GM4T	With Pre-Applied Phase Change Thermal Interface Material

Supporting Links & Tools

Evaluation Tools & Support

- All LTSpice Models
- All PLECS Models
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum

Dual-Channel Gate Driver Board

- EVAL-ADUM4146WHB1Z: Analog Devices® Gate Driver Board
- Si823H-AxWA-KIT: Skyworks® Gate Driver Board
- ACPL-355JC: Broadcom® Gate Driver Board
- CGD1700HB2M-UNA: Wolfspeed Gate Driver Board
- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

Application Notes

- CPWR-AN41: Mounting Instructions and PCB Requirements
- CPWR-AN42: Thermal Interface Material Application Note
- CPWR-AN45: Dynamic Performance Application Note

Notes & Disclaimers

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