

CAB5R0A23GM4, CAB5R0A23GM4T

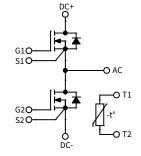
 $\begin{array}{c} V_{DS} & 2300 \, V \\ R_{DS(on)} & 5.0 \, m\Omega \end{array}$

2300 V, 5.0 mΩ, Silicon Carbide, Half-Bridge Module

Technical Features

- Ultra-Low Loss
- High Frequency Operation
- Zero Turn-Off Tail Current from MOSFET
- Normally-Off, Fail-Safe Device Operation
- Aluminium Nitride Substrate
- Optional Pre-Applied Thermal Interface Material





Typical Applications

- DC Fast Chargers
- Energy Storage Systems
- High-Efficiency Converters / Inverters
- Renewable Energy
- Smart-Grid / Grid-Tied Distributed Generation
- Solar Inverters

System Benefits

- Enables Compact, Lightweight Systems
- Enables Two-Level Conversion for 1500 VDC Systems
- Increased System Efficiency due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

Key Parameters

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Conditions	Note	
Drain-Source Voltage	V _{DS}			2300				
Maximum Gate-Source Voltage	V _{GS(max)}	-8		+19	V	Transient	Fig. 33	
Operational Gate-Source Voltage	V _{GS(op)}		-4/15			Static	Note 1	
DC Continuous Drain Current (T _{VJ} ≤ 150 °C)	I _D			150	A	$V_{GS} = 15 \text{ V}, \ T_{HS} = 75 \text{ °C}, T_{VJ} \le 150 \text{ °C}$	Notes 2,3,4	
Pulsed Drain Current	I _{DM}			300		t _{Pmax} limited by T _{VJmax} V _{GS} = 15 V, T _{HS} = 75 °C	Fig. 20	
Power Dissipation	P _D		710		W	T _{HS} = 75 °C, T _{VJ} ≤ 150 °C	Note 5 Fig. 21	
Virtual Junction Temperature	T _{VJ(op)}	-40		150	°C	Operation		

Note (1): Recommended turn-on gate voltage is 15 V with $\pm 5\%$ regulation tolerance

Note (2): Current limit at T_{HS} = 75°C, $T_{VJ} \le 150$ °C imposed by package

Note (3): Continuous DC operational limit set by DC- pins. See Figure 22 for implementable AC current

Note (4): Verified by design

Note (5): $P_D = (T_{VJ} - T_{HS})/R_{TH(JH,typ)}$

MOSFET Characteristics (Per Position) (T_{vJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Conditions	Note	
Drain-Source Breakdown Voltage	V _{(BR)DSS}	2300				V _{GS} = 0 V, T _{VJ} = -40 °C		
Cata Threada and Walta an	N.	1.8	2.5	4.0	V	$V_{DS} = V_{GS}$, $I_{D} = 114 \text{ mA}$		
Gate Threshold Voltage	$V_{GS(th)}$		2.1			$V_{DS} = V_{GS}$, $I_D = 114$ mA, $T_{VJ} = 150$ °C		
Zero Gate Voltage Drain Current	I _{DSS}		15	900	μΑ	V _{GS} = 0 V, V _{DS} = 2300 V		
Gate-Source Leakage Current	I _{GSS}		75	1500	nA	V _{GS} = 15 V, V _{DS} = 0 V		
Drain-Source On-State Resistance	В		5.0	7.0	0	$V_{GS} = 15 \text{ V}, I_D = 240 \text{ A}$	Fig. 2	
(Devices Only)	R _{DS(on)}		11.9		mΩ	$V_{GS} = 15 \text{ V}, I_D = 240 \text{ A}, T_{VJ} = 150 \text{ °C}$	Fig. 3	
Transconductance	_		235			$V_{DS} = 20 \text{ V}, I_{D} = 240 \text{ A}$	Fig. 4	
Transconductance	g _{fs}		230		S	$V_{DS} = 20 \text{ V}, I_{D} = 240 \text{ A}, T_{VJ} = 150 \text{ °C}$		
Turn-On Switching Energy, $T_{VJ} = 25 ^{\circ}\text{C}$ $T_{VJ} = 125 ^{\circ}\text{C}$ $T_{VJ} = 150 ^{\circ}\text{C}$	E _{On}		4.5 5.0 5.2			$V_{DD} = 1200 \text{ V},$ $I_{D} = 240 \text{ A},$	Fig. 11 Fig. 13	
Turn-Off Switching Energy, $T_{VJ} = 25 ^{\circ}\text{C}$ $T_{VJ} = 125 ^{\circ}\text{C}$ $T_{VJ} = 150 ^{\circ}\text{C}$	E _{off}		4.3 4.6 4.7		mJ	$\begin{aligned} &V_{GS} = -4 \text{ V/15 V,} \\ &R_{G(OFF)} = 0.0 \Omega, R_{G(ON)} = 0.0 \Omega, \\ &L_{\sigma} = 18 \text{ nH} \end{aligned}$		
Internal Gate Resistance	R _{G(int)}		1.1		Ω	f = 100 kHz		
Input Capacitance	C _{iss}		36.6		25		Fig. 9	
Output Capacitance	C _{oss}		0.60		nF	$V_{GS} = 0 \text{ V}, V_{DS} = 1500 \text{ V},$ $V_{AC} = 25 \text{ mV}, f = 100 \text{ kHz}$		
Reverse Transfer Capacitance	C _{rss}		48		pF	VAC 25 IIIV, I 100 KII2		
Gate to Source Charge	Q _{GS}		275			$V_{DS} = 1500 \text{ V}, V_{GS} = -4 \text{ V}/15 \text{ V},$		
Gate to Drain Charge	Q_{GD}		235		nC	I _D = 240 A,		
Total Gate Charge	Q_{G}		880			Per IEC60747-8-4 pg 21		
FET Thermal Resistance, Junction to Heatsink	R _{th JHS}		0.105		°C/W	Measured with Pre-Applied TIM	Fig. 17	

Diode Characteristics (Per Position) (T_{vJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Conditions	Notes	
B B: E W	V		5.8		· V	$V_{GS} = -4 \text{ V}, I_{SD} = 240 \text{ A}$	Fig. 7	
Body Diode Forward Voltage	V_{SD}		5.3			$V_{GS} = -4 \text{ V}, I_{SD} = 240 \text{ A}, T_{VJ} = 150 \text{ °C}$	7 Fig. /	
DC Source-Drain Current (Body Diode)	I _{SD BD}		130		A	$V_{GS} = -4 \text{ V}, \ T_{HS} = 75 \text{ °C}, T_{VJ} \le 150 \text{ °C}$	Note 5 Fig. 20	
Reverse Recovery Time	t _{RR}		395		ns		Fig. 32	
Reverse Recovery Charge	Q _{RR}		11.6		μC	$V_{GS} = -4 \text{ V}, I_{SD} = 240 \text{ A}, V_{R} = 1200 \text{ V}$ $di/dt = 20 \text{ A/ns}, T_{VI} = 150 ^{\circ}\text{C}$		
Peak Reverse Recovery Current	I _{RRM}		290		Α			
Reverse Recovery Energy, $T_{VJ} = 25 ^{\circ}\text{C}$ $T_{VJ} = 125 ^{\circ}\text{C}$ $T_{VJ} = 150 ^{\circ}\text{C}$	E _{RR}		2.3 8.2 12		mJ	$\begin{split} &V_{DD} = 1200 \text{ V}, \ I_D = 240 \text{ A}, \\ &V_{GS} = -4 \text{ V}/15 \text{ V}, \ R_{G(ON)} = 0.0 \ \Omega, \\ &L_{\sigma} = 18 \text{ nH} \end{split}$	Fig. 14	

Module Physical Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Package Resistance, M1 (High-Side)	R _{pkg1}		1.5		0	T = 135°C Note C
Package Resistance, M2 (Low-Side)	R _{pkg2}		1.4		mΩ	T _c = 125°C, Note 6
Stray Inductance	L _{Stray}		11		nH	Between DC- and DC+, f = 10 MHz
Case Temperature	T _C	-40		125	°C	
Mounting Torque	Ms		2.0	2.3	N-m	M4 bolts
Weight	W		36		g	
Case Isolation Voltage	V _{isol}	5			kV	AC, 50 Hz, 1 minute
Comparative Tracking Index	СТІ	600				
Classica Bistoria			8.1			Terminal to Terminal
Clearance Distance			13.2			Terminal to Heatsink
Creepage Distance			9.8		mm	Terminal to Terminal
			14.9			Terminal to Heatsink

Note (6): Total Effective Resistance (Per Switch Position) = MOSFET R_{DS(on)} + Switch Position Package Resistance

Temperature Sensor (NTC) Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Rated Resistance	R _{NTC}		5.0		kΩ	T _{NTC} = 25°C
Resistance Tolerance at 25 °C	ΔR/R	-5		5	%	
Beta Value (T ₂ = 50 °C)	ß _{25/50}		3380		K	
Beta Value (T ₂ = 80 °C)	ß _{25/80}		3468		K	
Beta Value (T ₂ = 100 °C)	ß _{25/100}		3523		K	
Power Dissipation	P _{Max}			10	mW	T _{NTC} = 25°C

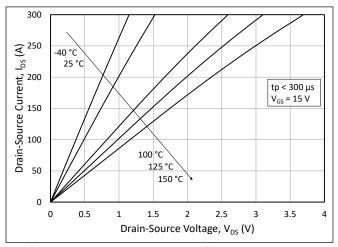


Figure 1. Output Characteristics for Various Junction Temperatures

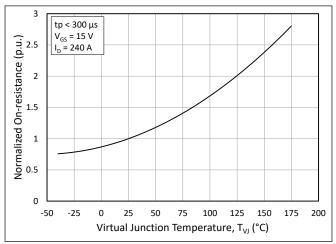


Figure 3. Normalized On-State Resistance vs. Junction Temperature

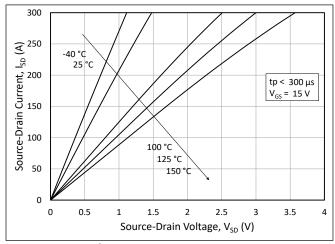


Figure 5. 3^{rd} Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 15 \text{ V}$

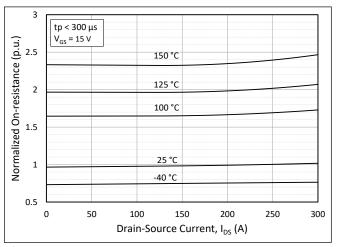


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

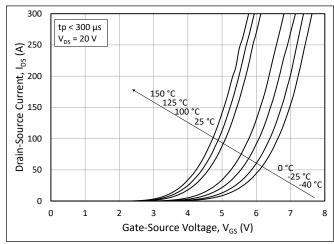


Figure 4. Transfer Characteristic for Various Junction Temperatures

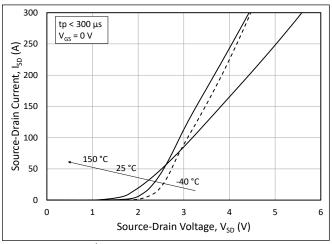


Figure 6. 3^{rd} Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 0$ V (Body Diode)

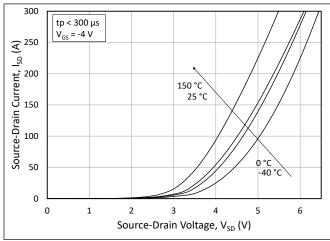


Figure 7. 3^{rd} Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = -4 \text{ V (Body Diode)}$

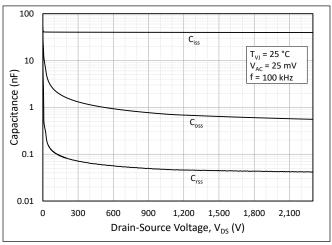


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 2300V)

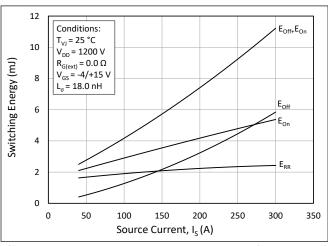


Figure 11. Switching Energy vs. Drain Current (V_{DD} = 1200 V)

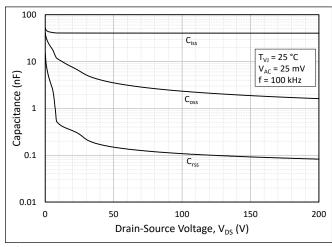


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

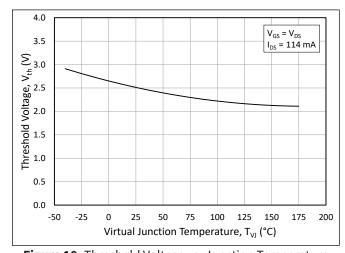


Figure 10. Threshold Voltage vs. Junction Temperature

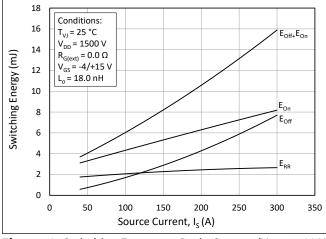


Figure 12. Switching Energy vs. Drain Current (V_{DD} = 1500 V)

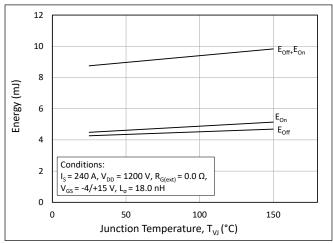


Figure 13. MOSFET Switching Energy vs. Junction Temperature

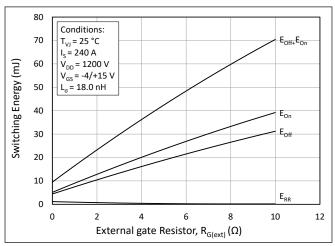


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

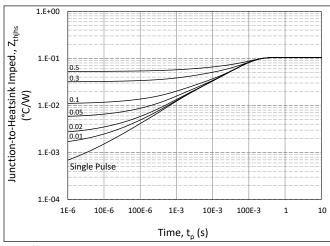


Figure 17. MOSFET Junction to Heastsink Transient Thermal Impedance, $Z_{th JHS}$ (°C/W)

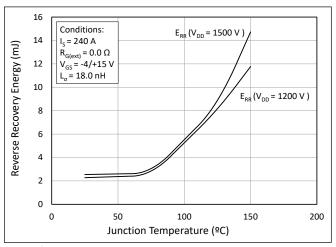


Figure 14. Reverse Recovery Energy vs. Junction Temperature

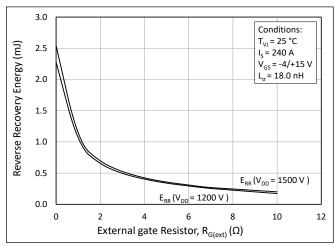


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

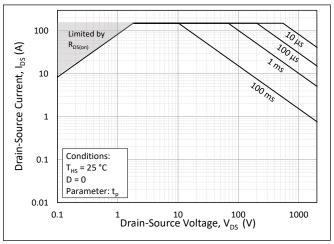


Figure 18. Forward Bias Safe Operating Area (FBSOA)

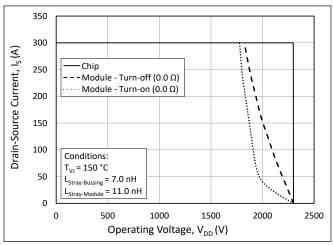


Figure 19. Switching Safe Operating Area

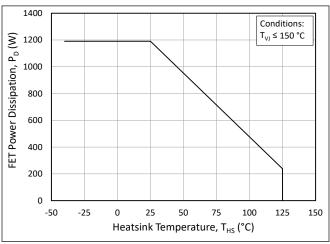


Figure 21. Maximum Power Dissipation Derating vs. Heatsink Temperature

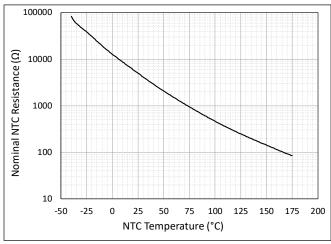


Figure 23. Nominal NTC Resistance vs. NTC Temperature

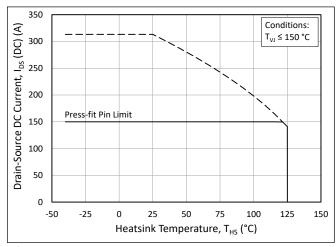


Figure 20. Continuous Drain Current Derating vs. Heatsink Temperature

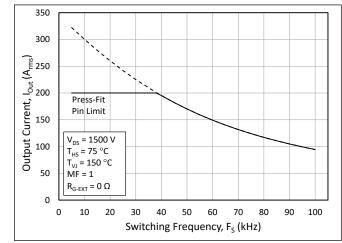


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

Timing Characteristics

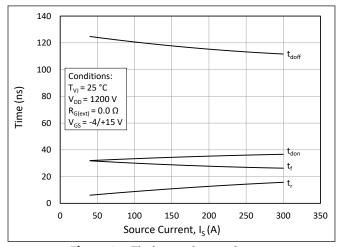


Figure 24. Timing vs. Source Current

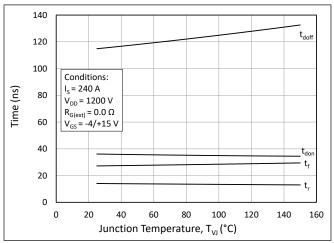


Figure 26. Timing vs. Junction Temperature

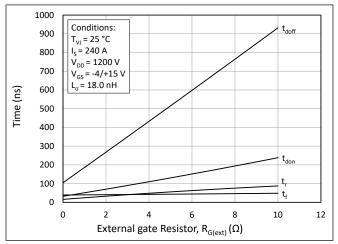


Figure 28. Timing vs. External Gate Resistance

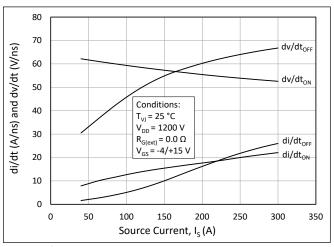


Figure 25. dv/dt and di/dt vs. Source Current

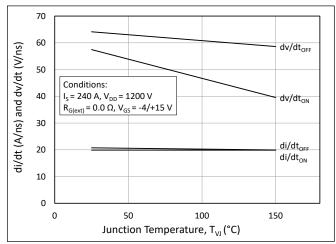


Figure 27. dv/dt and di/dt vs. Junction Temperature

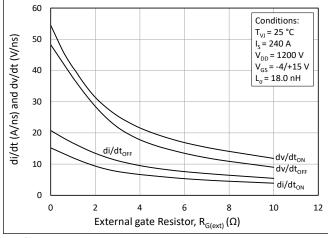


Figure 29. dv/dt and di/dt vs. External Gate Resistance

Definitions

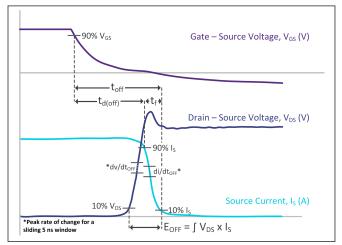


Figure 30. Turn-off Transient Definitions

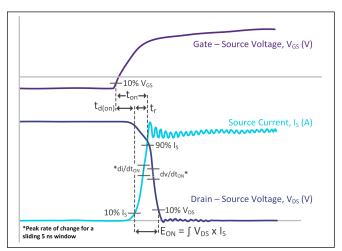


Figure 31. Turn-on Transient Definitions

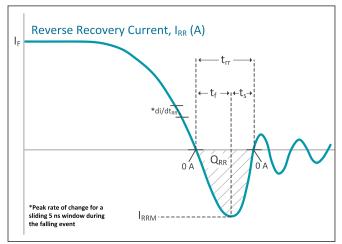


Figure 32. Reverse Recovery Definitions

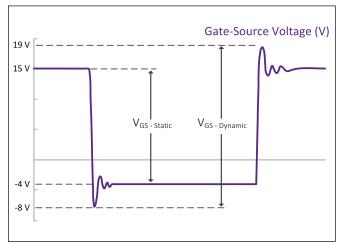
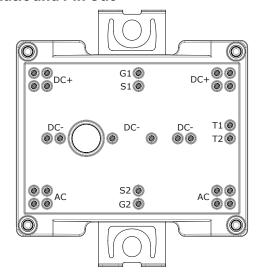
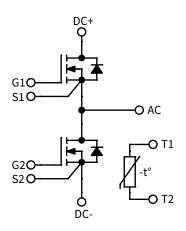


Figure 33. V_{GS} Transient Definitions

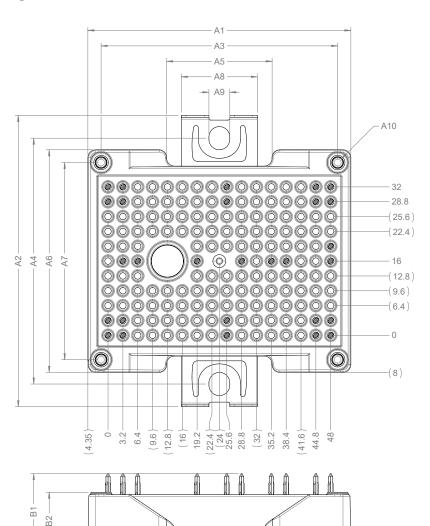
Note (7): A gate driver featuring the IXDD614SI gate driver IC was used to evaluate dynamic performance. The typical driver high-state output resistance of $0.4\,\Omega$ and low-state output resistance of $0.3\,\Omega$ are not included in the RG(ext) values on this datasheet.

Schematic and Pin Out





Package Dimension (mm)



DIMENSION TABLE							
SYMBOL	DIMENSION	TOLERANCE					
A1	56.7	±0.30					
A2	62.8	±0.50					
A3	51	±0.15					
A4	(53)	REF.					
A5	22.7	±0.30					
A6	48	±0.30					
A7	42.5	±0.15					
A8	16.4	±0.20					
A9	4.5	±0.10					
A10	Ø2.3 ⊽8.5	Ø: -0.10 ▼: ±0.30					
B1	16.4	±0.50					
B2	12.33	±0.35					
B4	1.8	±0.20					
ALL PIN	LOCATIONS	±0.40					

B4

Product Ordering Code

Part Number	Description
CAB5R0A23GM4	Without Pre-Applied Phase Change Thermal Interface Material
CAB5R0A23GM4T	With Pre-Applied Phase Change Thermal Interface Material

Supporting Links & Tools

Simulation Tools & Support

- All LTSpice Models
- All PLECS Models
- SpeedFit 2.0 Design Simulator™
- <u>Technical Support Forum</u>

Compatible Evaluation Hardware

- EVAL-ADUM4146WHB1Z: Analog Devices® Gate Driver Board
- UCC21710QDWEVM-054: Texas Instruments® Gate Driver Board
- CGD1700HB2M-UNA: Wolfspeed Gate Driver Board
- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

Application Notes

- PRD-02302: Wolfpack Mounting Instructions and PCB Requirements
- PRD-06379: Environmental Considerations for Power Electronics
- PRD-07845: Power Module Baseplate Capacitance and Electromagnetic Compatibility
- PRD-07933: Wolfspeed Power Module Thermal Interface Material Application User Guide
- PRD-07968: Wolfspeed WolfPACK™ Dynamic Performance
- PRD-08376: Thermal Characterization Methods and Applications
- PRD-08710: Measuring Stray Inductance in Power Electronics Systems

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