Application Note PRD-08710

Measuring Stray Inductance in Power Electronics Systems

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In power electronics systems, parasitic inductance degrades performance by contributing to voltage overshoots and electromagnetic interference. Minimizing this inductance is critical to maximizing system efficiency and lifetime. Developing mitigation techniques or modeling systems often requires a method to accurately characterize the inductance of an existing system. This document identifies the commutation paths of a typical system and provides a clear and detailed methodology for measuring these inductances using an impedance analyzer.

Contents

1. Introduction

The fast switching of silicon carbide semiconductors enables more efficient systems with increased power density. As with all power electronics systems (even those using silicon), proper system design is important to maximize the performance of the switching semiconductors. Minimizing the stray inductance is a particularly important parameter for system design because the fast changes in current through the device induce voltage overshoots and oscillations in the system. Systems leveraging silicon carbide devices are particularly sensitive to the effects of parasitic inductance due to their fast edge rates that enable more efficient switching. In fact, the switching speed of silicon carbide is generally not limited by the device itself, but by these inductance-induced voltage overshoots and oscillations. An example of how faster switching affects system dynamics is shown in Figure 1. Here, a SiC power module is switched under identical conditions but with a 0 Ω gate resistance in Figure 1 (a) and a 10 Ω gate resistance in Figure 1 (b). The larger gate resistance results in the voltage slew rates decreasing from 67 V/ns to 12 V/ns, and the current slew rates decreasing from 49.1 A/ns to 9.8 A/ns. At 0 Ω, the system shows a 430 V overshoot that causes the part to exceed its rated voltage of 1200 V, while switching at 10 Ω shows a 120 V overshoot. In terms of ringing, the part switched at 0 Ω has 60 MHz oscillations that persist for several hundred nanoseconds, while the 10 Ω system shows no ringing. Of course, this comes with the caveat that the device switched at 10 Ω will have significantly higher switching losses; it is generally desired to switch as fast as possible while remaining in the SiC device's safe operating area. By reducing the parasitic inductance, the part can be switched faster while behaving within its ratings.

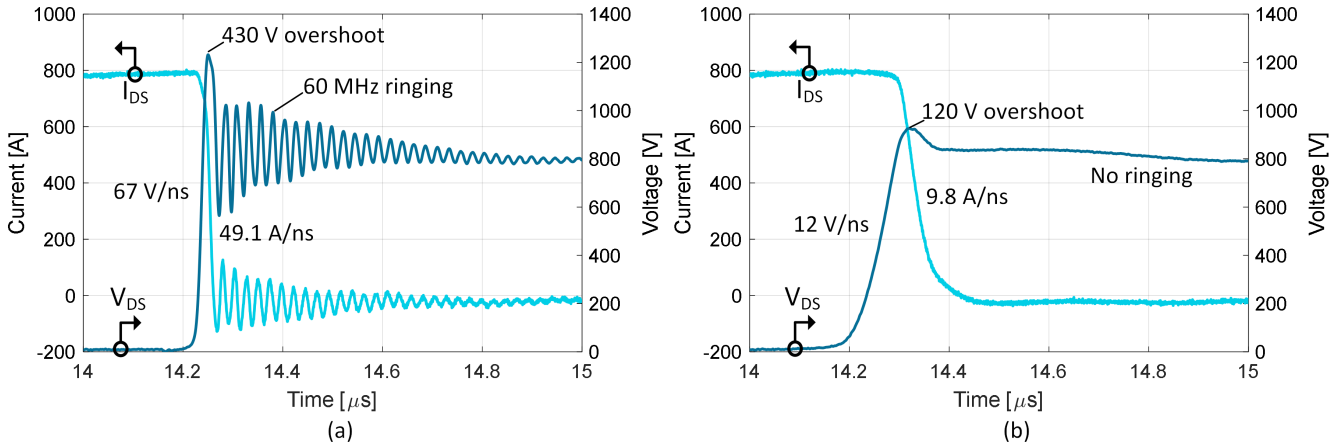

Figure 1: Comparison of power module switching at (a) 0 Ω R_G and (b) 10 Ω R_G

1.1 Characterization Methods

Minimizing and predicting the influence of parasitic inductance requires methods to characterize it. There are many approaches to accomplish this. The first class of methods use finite element analysis (FEA) simulation to predict the inductance of a given 3D geometry. The primary advantage of FEA is that it does not require a physical sample, is not affected by measurement errors, and can measure quantities that would be difficult or impossible to do empirically. However, FEA requires detailed knowledge of the 3D structure, a paid license for FEA software, and expertise to configure the simulations. For more information on inductance theory and performing FEA simulations, see Wolfspeed's document PRD-08734.

The second class of methods used to quantify parasitic inductance are empirical ones. These include using vector network analyzers, impedance analyzers (ZAs), or analysis of time-domain switching waveforms. For power electronics systems, Wolfspeed recommends using impedance analyzers for detailed characterization, and analyzing time-domain waveforms for quick estimations or verification. Both methods will be discussed in this document.

1.2 Identifying Commutation Paths

The influence of stray inductance in a power electronics system depends on the system topology and its location in the circuit. Stray inductance that is present in loops that contain high-frequency currents (where the di/dt events from Figure 1 are present) are of the most concern. These loops are often referred to as *commutation paths*. For example, consider the buck converter in Figure 2. Here, the commutation path is defined from the input voltage (+), through the bussing, through the half-bridge module, and back to the input voltage (-). Any inductance in this path will contribute to ringing and voltage overshoots caused by the device switching edges. Contrastingly, the output path from the AC terminal of the module includes a large filter to provide a DC-like output voltage and current. As such, the di/dt in the output path is very small, and thus any stray inductance will have minimal effect. The output of power modules are also often connected to an inductive load (such as motor windings or filter inductors) that are on the order of µH – mH, which dominate any nH inductance in series.

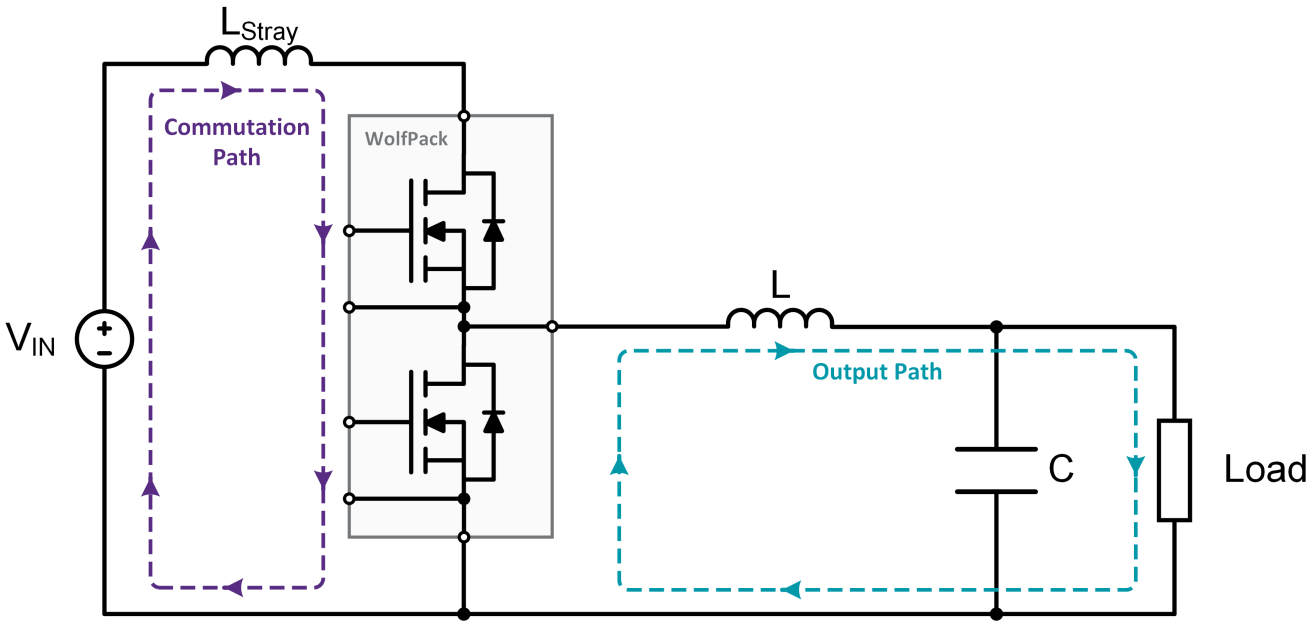

Figure 2: Commutation path for a buck converter system

As shown in Figure 2, the commutation path includes both the system and the module. These are typically measured separately as partial inductances and combined to represent the complete loop. For this reason, it is important to have both an optimized system and an optimized module; for example, using a 6 nH module with a 100 nH bus will result in a 106 nH loop, therefore negating the optimization of the module. The commutation path (provided as stray inductance in datasheets) of power modules is typically defined from its DC+ to DC- terminals, as shown for the half-bridge module in Figure 3 (b) and the six-pack module in Figure 3 (c). For

discrete parts such as the one in Figure 3 (a), the stray inductance is provided from the drain to source terminals, but the total commutation path will include at least two parts in series and any system interconnections.

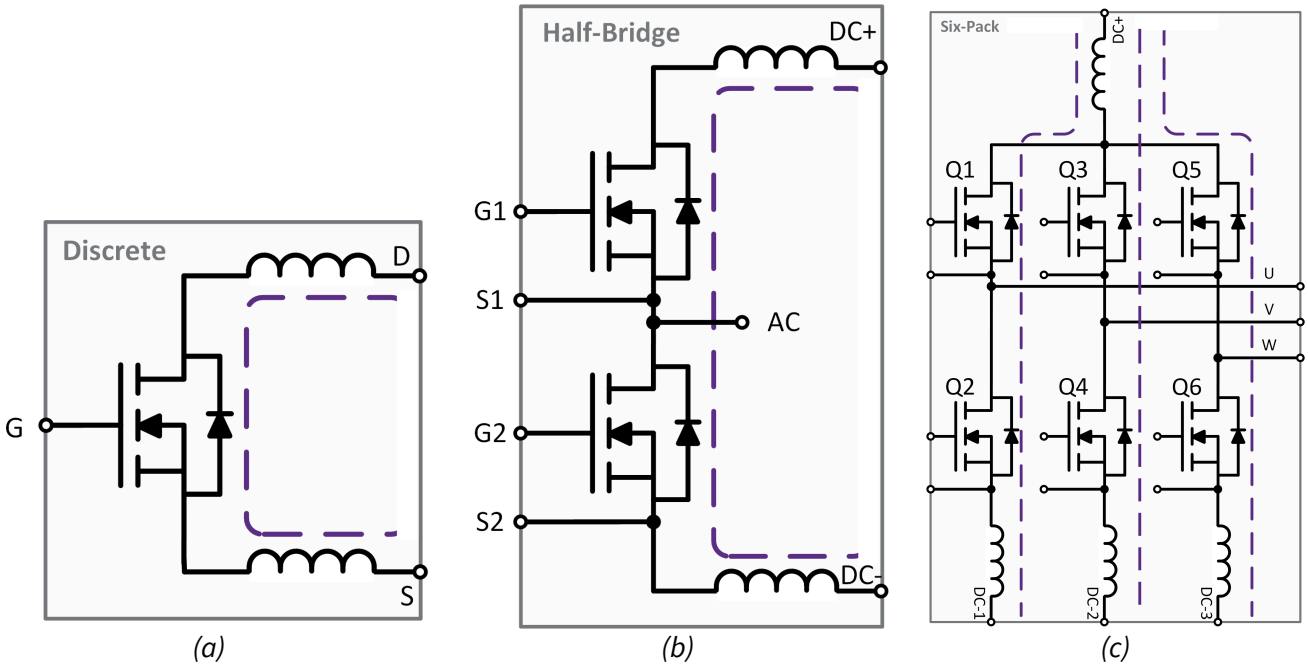

Figure 3: Typical commutation paths for a (a) discrete part, (b) half-bridge module, and (c) six-pack module

The commutation paths described apply to most systems. However, there can be cases where the commutation paths are not intuitive, or when they include the AC terminal of the power module. For example, in neutral point clamped (NPC) inverters using half-bridge power modules, the commutation path can include the AC terminal inductance of two of the three power modules.

1.3 Frequencies of Interest

One crucial concept to comprehend is the frequency-dependence of inductance. Due to proximity and skin effect (described in PRD-08734), in which high-frequency current crowds to the interior of a conducting loop, inductance will decrease as the frequency increases [1]. A notional inductance-across-frequency waveform is shown in Figure 4. At low frequency (here, below 10 kHz), the inductance is flat at around 24 nH. However, between 10 kHz – 1 MHz, the frequency rapidly decreases to about 15 nH, at which point the inductance plateaus. The reason for this plateau in frequency is that there is a limit to how much the current can crowd on the inner loop of a conductor.

For inductance extraction, the implication of this is that the inductance must be extracted at a specific frequency, and this frequency should be selected appropriately. It is recommended to select a frequency that is 1) within the high-frequency plateau region of the inductance curve and 2) within the high-accuracy region of the impedance analyzer (frequencies >50 MHz can often have measurement errors). Wolfspeed recommends 10 MHz, but the optimal frequency can change depending on the system. The reason that measuring inductance at high frequency is preferred is that high-performance MOSFET switching occurs in this domain. Also, consider

that the impedance of a 24 nH conductor at 10 kHz is 0.0015 Ω, while the impedance of a 15 nH conductor at 10 MHz is 94.24 Ω – even though the inductance is smaller, its influence on the overall impedance is much greater.

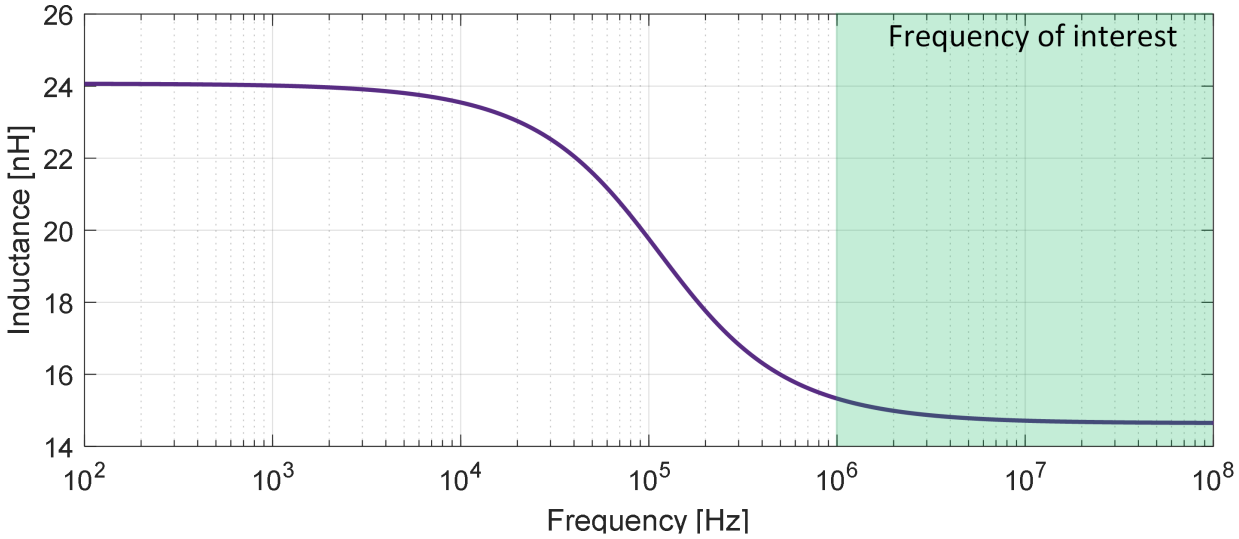

Figure 4: Notional frequency dependence of inductance and typical frequency of interest

2. General Inductance Measurement Approach

This section will thoroughly describe how to use an impedance analyzer to measure the parasitic inductance of power modules and system bussing. The impedance analyzer used here is the E4990A impedance analyzer shown in Figure 5 (this instrument is used to measure the stray inductance for Wolfspeed datasheets). The instrument is capable of measuring from 20 Hz to 120 MHz.

Figure 5: Keysight Technologies® E4990A Impedance Analyzer [2]

2.1 MOSFET Biasing

When measuring a power module, it is necessary to measure through the drain-source path of the MOSFETs. During the off-state, the MOSFETs inhibit measurement by presenting a high-impedance capacitance (C_{OSS}) in series with the parasitic inductance. This series impedance reduces the available extraction range of the inductance and yields less accurate measurements. Thus, it is beneficial to introduce a voltage to bias the parts

on to eliminate the capacitive effects [3]. To demonstrate this procedure, consider the test setup schematic of a generic MOSFET power module using the impedance analyzer shown in Figure 6 below. The impedance analyzer is connected across the DC+/DC- terminals of the half-bridge module, and a voltage is applied across the gate-source of each MOSFET.

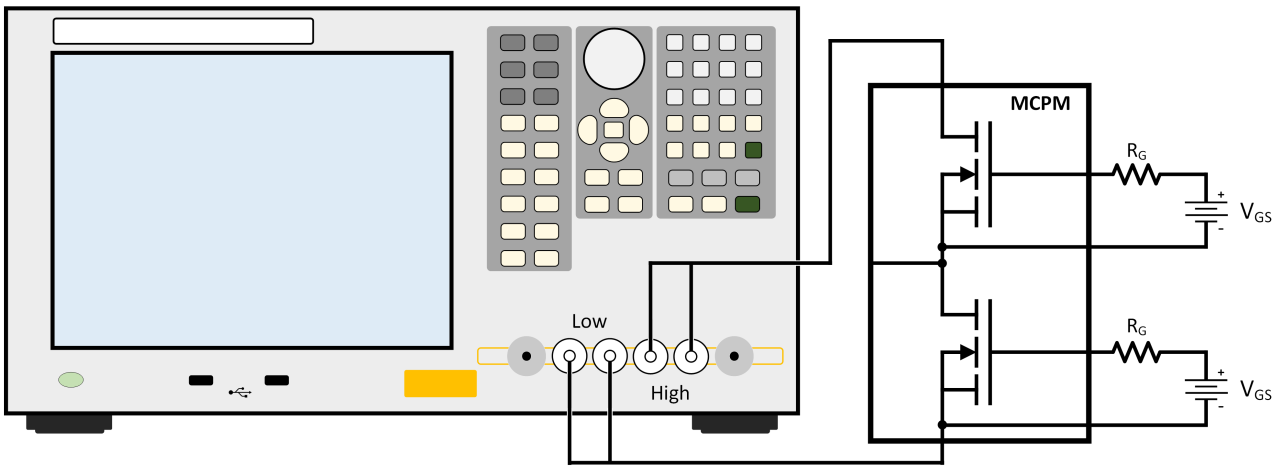

Figure 6: Example ZA Measurement with device gated OFF/ON (V_{GS} = 0 V/ 12V)

Condition 1: No Bias Applied

With the device gated OFF (V_{GS} = 0V), the impedance analyzer measures through the MOSFET's output capacitance (C_{OSS}), along with any series resistance and parasitic inductance, which results in the series R-L-C circuit shown in Figure 7. As shown in this result, the C_{OSS} dominates the measurement results below 70 MHz. At 70 MHz, a resonance occurs, and the system becomes inductance dominated. However, the available region to extract the inductance is at very high frequencies where accuracy may be limited. In addition, because fewer data points are available, it can be more difficult to tell if measurement errors have occurred. The resonance can be used to determine the inductance, but the yielded result is less accurate than using the biasing technique described next.

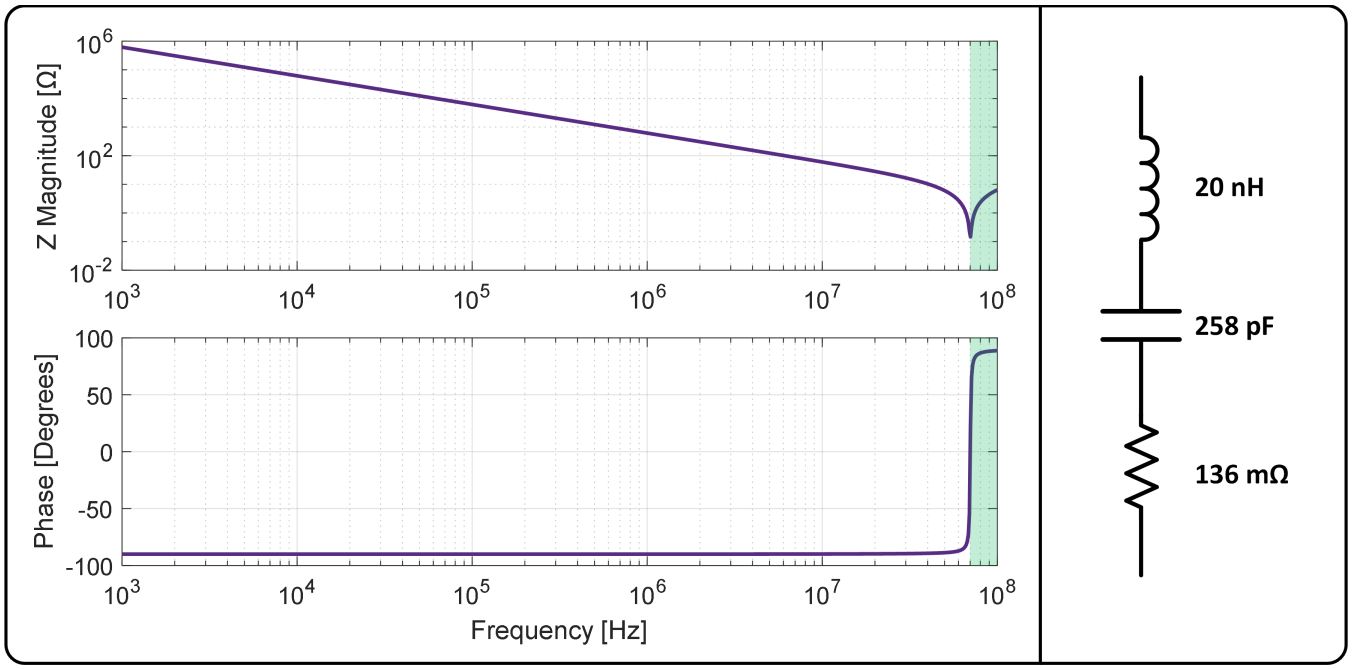

Figure 7: Example ZA Measurement with device gated OFF (VGS = 0 V), (a) Impedance vs. Frequency, (b) equivalent circuit

Condition 2: With Bias Applied

To eliminate the influence of the C_{OSS}, the MOSFET device must be gated ON during the measurement to achieve reliable results. Gating ON the device can be achieved by:

- Connecting batteries across the Gate-Source (G-S) of every switch position. (It is recommended that a >100 Ω resistor is placed in series to the battery connection to prevent accidentally short circuiting the battery during testing.)
- Charging C_{GS} by momentarily applying voltage with a power supply, then removing the power leads. **Please note that an external power supply (even an isolated power supply) can provide additional paths for the stimulus current and must be removed from the system during test.**

The result of condition 2 is shown by the R-L circuit response of Figure 8. The measurement results consist of the parasitic inductance and the Drain-Source Resistance ($R_{DS(ON)}$) of the power module as shown in the equivalent circuit of Figure 8. This measurement procedure is ideal because it allows the extraction of the effective inductance across a wide frequency range due to the low series impedance of the MOSFET. This is useful for determining the frequency-dependence of the inductance as described in section 1.3.

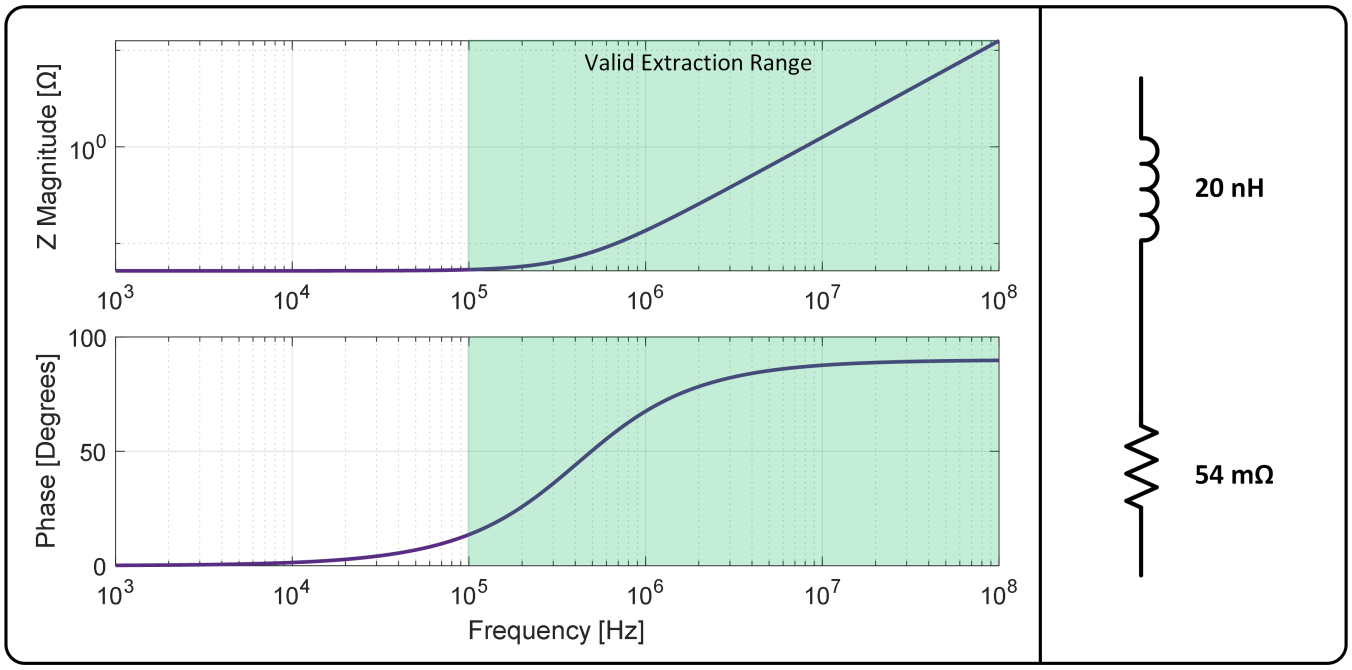

Figure 8: Example ZA measurement with device gated ON (VGS = 12 V), (a) Impedance vs. Frequency, (b) equivalent circuit

2.2 Fixturing and Compensation

Performing measurements with an impedance analyzer requires using a fixture to interface between the DUT and the instrument. Selecting an appropriate fixture is essential to accurately measure the parasitic inductance of power electronics systems. Fixtures are typically selected on how easily they interface with the geometry of the device. For power modules, which have varied geometry, different fixturing methods must be used for different module packages. In addition, the fixture is not ideal; it contains some portion of resistance, inductance, and capacitance that will add to the measurement of the DUT. Thus, compensation methods are necessary to remove the contribution of the fixture to isolate the DUT impedance.

The stray inductance of DC link bus bars and SiC power modules are extremely small, often on the order of 5 nH – 25 nH. The impedance of these inductances is on the fringe of what is possible with modern measurement equipment. For example, consider the manufacturer-specified error of the Keysight Technologies® 42941a impedance probe (more details on this probe will be provided later) in Figure 9. The impedance magnitude of inductances between 5 nH – 25 nH is highlighted in gray. At 25 nH, the error at high frequency (above 10 MHz) is approximately 3 %, while 5 nH lies outside the 10 % specified error region only above 5 MHz. Below 100 kHz, the specified error is greater than 10 % for both inductances. Accurate measurements of inductance in this range are not guaranteed by the manufacturer even with this instrument. Techniques that will be explained in this document can be applied to improve this error, but it demonstrates that care must be taken when measuring small inductances for accurate results.

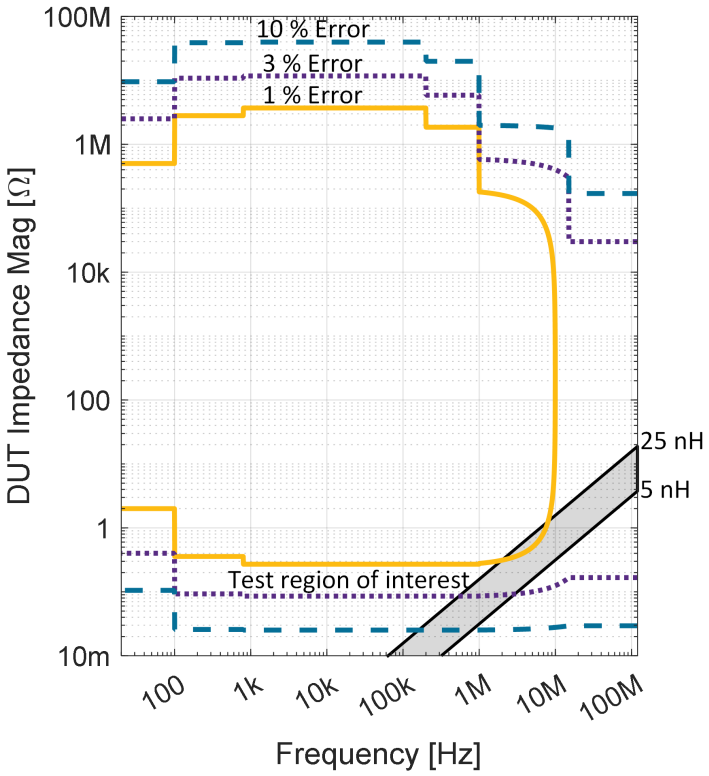

Figure 9: Manufacturer-specified error of the Keysight Technologies® E4990A impedance analyzer [2]

2.2.1 Selecting an Appropriate Fixture

The available fixtures can be broadly separated into two categories: manufacturer and user-fabricated. Manufacturer fixtures are those that are developed, manufactured, and sold by the equipment vendor for interfacing with the impedance analyzer. These fixtures provide the highest level of accuracy and consistency when used properly. User-fabricated fixtures (also referred to as custom fixtures) are those that are built by the user for a measurement. Developing custom fixtures is challenging and requires a detailed understanding of the equipment. Custom fixtures are not recommended for parasitic inductance extraction because the errors associated with these fixtures are too large for measuring small inductances.

For all fixture types, it is essential to avoid loose cabling and clips. Measurements of small nH inductances are impossible with these devices. Instead, fixtures must be rigid such that consistent contact and geometry can be maintained. The fixtures recommended by Wolfspeed for parasitic inductance extraction are the 42941a impedance probe in Figure 10 (a) and the 16047e test fixture in Figure 10 (b). The 42941a fixture supports analysis up to 120 MHz, includes a 1.5-meter cable, and features a maximum adjustable jaw width of 15 mm. Note here that the cable does not present an issue with performing measurements because 1) the cable is designed by the manufacturer for this analysis and includes proper shielding, 2) the manufacturer includes a compensation process specific for this cable, and 3) the cable occurs before the measurement head. However, one adjustment made to the probe is that it is mounted to an adjustable arm that can be moved in the vertical direction. This allows the probe head to descend on the measurement and be held in place. Holding the probe by hand is not appropriate for these measurements. The 16047e fixture connects directly to the E4990a

instrument and uses two adjustable clamps to contact the DUT. This fixture is extremely accurate and can support terminal widths up to 62 mm.

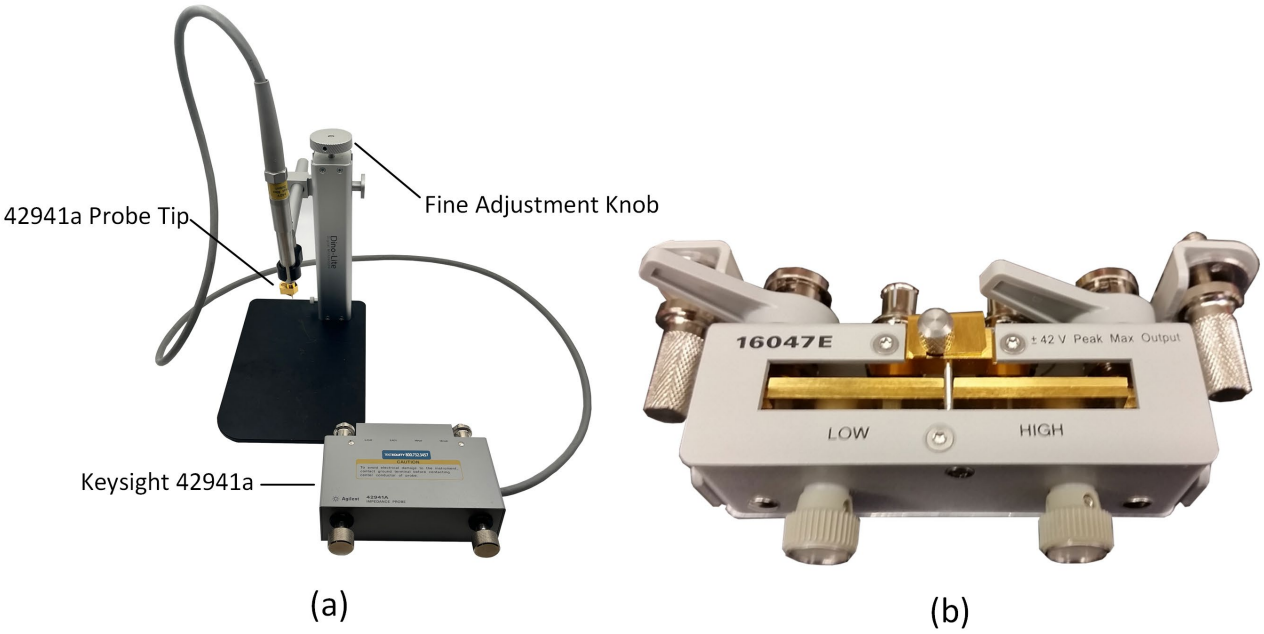

Figure 10: Recommended manufacturer fixtures, (a) Keysight Technologies® 42941a [4], (b) Keysight Technologies® 16047e [5]

An example measurement using the 42941a impedance probe is shown in Figure 11. The impedance probe is useful for making measurements across flat surfaces with spacing under 15 mm, especially on large geometries that cannot be mounted onto the impedance analyzer. The example in Figure 11 is of a CIL evaluation kit, which is a large PCB that contains DC link capacitors and a bar current shunt. The impedance probe tip is placed across the PCB terminals to perform the measurement. **Please note that some metals placed directly underneath an inductance measurement setup can interfere with the magnetic fields of the measurement and cause an underprediction in the measured value.**

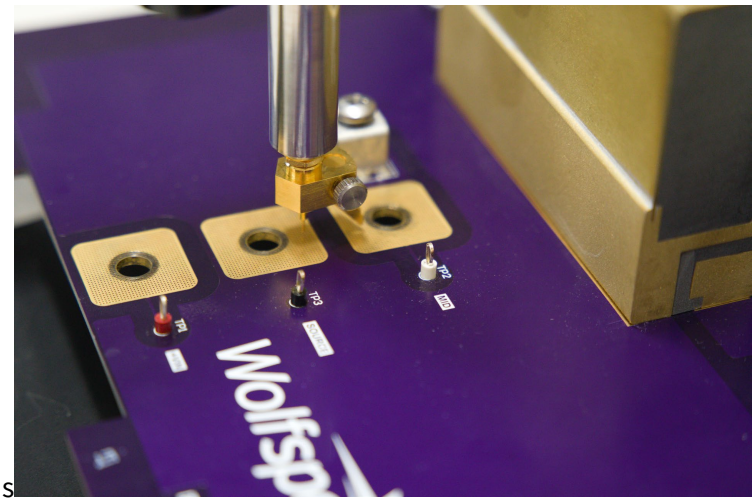

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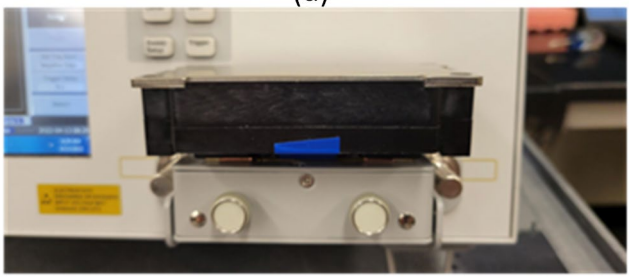
Figure 11: Example measurement using the 42941a impedance probe

An example measurement of a 62 mm Wolfspeed power module using the 16047e test fixture is shown in Figure 12. Copper foil is attached to the module terminals in Figure 12 (a) to provide a clamping point for the test fixture. The module is placed flush with the 16047e fixture in Figure 12 (b) to make the measurement. This setup provides a very direct and accurate measurement with the fixture. *If devices can be placed in the 16047e test fixture's terminals, it provides the most accurate measurements possible.*

(a)



(b)

Figure 12: Example measurement using the 16047e test fixture [6]

In some cases, it may be necessary to design a PCB or other structure to interface between the DUT and manufacturer fixture. An example of an adapter fixture used to measure a Wolfspeed WolfPACK™ power module with the 42941a impedance probe is shown in Figure 13. This PCB is necessary because it is difficult to make contact between the probe tip and the press-fit module pins. These setups can provide accurate results if the compensation is handled correctly. More details on compensation will be provided in later sections.

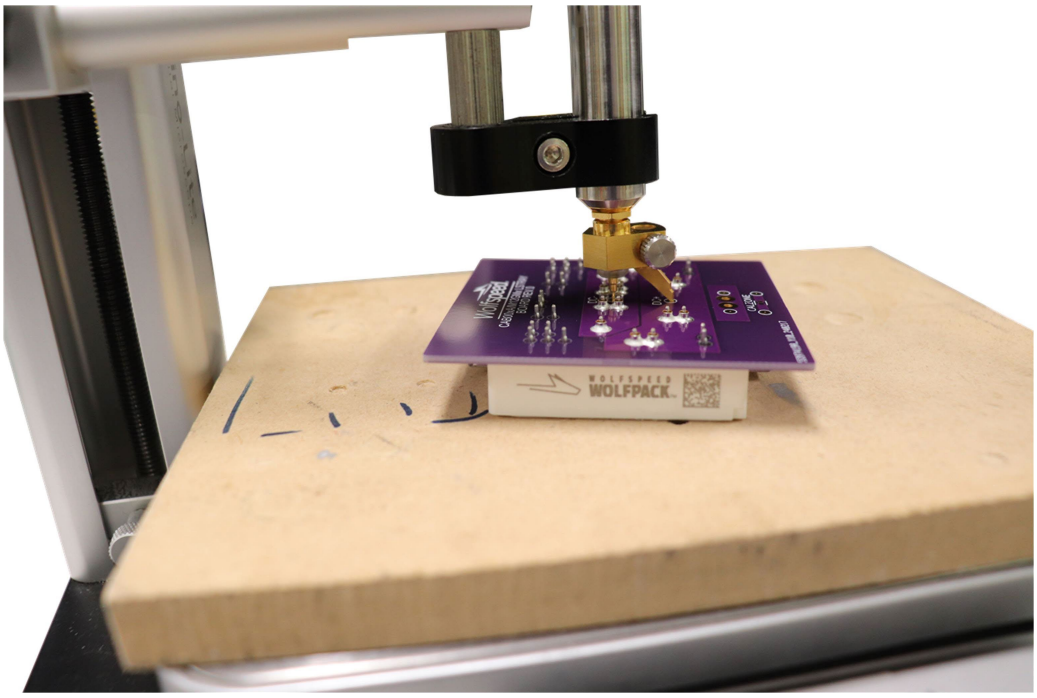


Figure 13: Example adapter fixture between 42941a impedance probe and Wolfspeed WolfPACK power module

Custom Fixtures

While custom fixtures are not generally recommended, they can be necessary when 1) the DUT is too large for any manufacturer fixtures, and 2) it is not possible to perform FEA analysis due to unknown module geometries. An example of a custom fixture for measuring a 62 mm power module is shown in Figure 14. Because the design and techniques for implementing these fixtures are complex, it is discussed in Section 4.

Figure 14: Example custom fixture for measuring a 62 mm power module [6]

2.2.2 Compensation Theory

Compensation describes the process used to remove the impedance contributions of the fixture from the measurement. Figure 15 shows a general connection setup for impedance measurements using the E4990A impedance analyzer. Here, the DUT is denoted by the impedance block Z_L. When measuring, the stimulus current will flow through both the fixture and the DUT and measure their combined impedance. The typical compensation (or calibration) standards are shown in the right of Figure 15. During a compensation measurement, the DUT is removed and is replaced by one of the calibration standards. Z_{SC} denotes a short circuit, where the measurement terminals of the fixture are shorted together. This compensation removes the series impedance and series inductance of the fixture. Z_{OC} denotes an open circuit, where the measurement terminals of the fixture are left open. This compensation removes the parallel capacitance and resistance of the fixture. Finally, Z_{ST} denotes a load compensation, where a known impedance is used to solve for the remaining variables in the fixture transmission matrix, reducing the influence of other systemic errors.

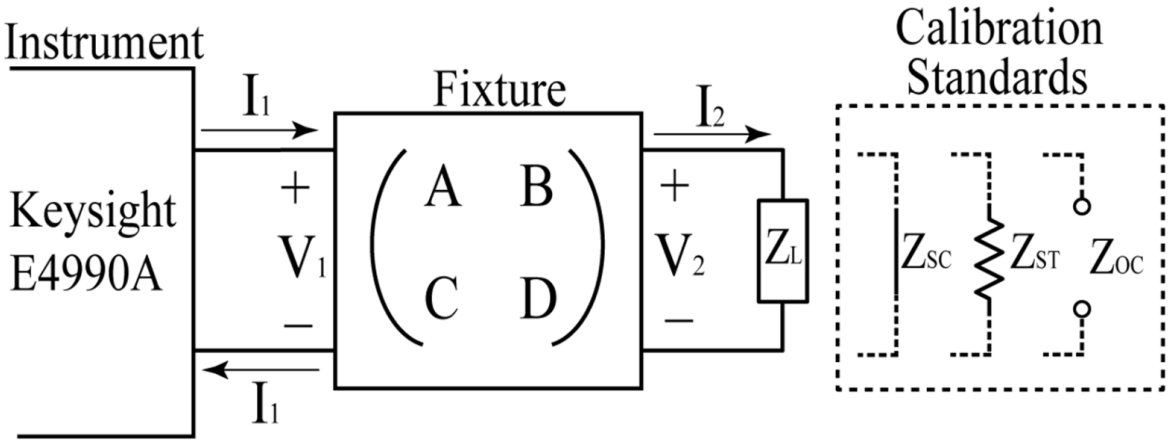


Figure 15: Configuration of E4990A measurements and compensation standards [7]

It is not necessary to apply all three compensation standards to every DUT measurement; they can be strategically applied when necessary for a particular measurement. In addition, it is important to perform the compensation methods properly to minimize errors. This requires understanding several fundamental concepts of impedance analysis.

2.2.3 Applying Compensation Methods

A typical compensation procedure involves only the short and open compensation methods. The load compensation is an additional measurement that can be used to further improve measurement accuracy. The method involves measuring a known impedance, such as a 50 Ω resistor. The instrument then compares the measurement of this known impedance to its theoretical value and adjusts the compensation network accordingly. Any differences between the theoretical load impedance and the actual load impedance will result in additional error. The load compensation is described as an optional procedure by the manufacturer and specifies criteria in which the load compensation is necessary. For the procedures outlined in this document, a relevant specified criterion is to apply the load compensation when a user-fabricated fixture is used to perform a measurement. Given the difficulty of performing the load compensation correctly (where incorrectly selecting

a load standard can increase error), and that it is optional for most measurements, it is preferred to skip the load compensation entirely in most measurements with manufacturer fixtures.

The short and open compensations are required for all impedance analyzer measurements. However, the sensitivity of the standard on the resulting DUT measurement is dependent on the DUT impedance. For example, consider measuring a 10 pF capacitor, which will have an impedance of 1590 Ω at 10 MHz. A stray fixture inductance of 5 nH will only have an impedance of 0.31 Ω at this frequency. Thus, the short compensation has a small influence on this measurement, while the open compensation will have a larger influence. For measuring small impedances, such as the stray parasitic inductance of a power module, the measured result is very sensitive to the short compensation which must be considered carefully.

In this document, the short compensation is scrutinized heavily for two reasons. One, as stated above, it is most influential on the measurement of small stray inductances. Two, it involves the insertion of a shorting standard to perform the measurement. This provides an additional avenue for error, unlike the open compensation which involves simply disconnecting the DUT and keeping any cabling in a fixed position.

An example compensation technique is shown in Figure 16. The open compensation in Figure 16 (a) is performed by closing the clamps together with nothing connected. The short compensation technique in Figure 16 (b) is performed by placing the provided shorting bar in the fixture. The optional load compensation technique in Figure 16 (c) is performed with a leaded precision 50 Ω resistor. A close-up photo with the 16047e short compensation connected to the E4990A impedance analyzer is shown in Figure 17.

(a) (b) (c)

Figure 16: Example compensation using 16047e fixture, (a) open compensation, (b) short compensation, (c) load compensation [8]

Figure 17: 16047e fixture attached to the E4990a impedance analyzer with the shorting bar attached

2.3 Maximizing Measurement Accuracy

The typical process for measuring a DUT with an impedance analyzer is as follows. First, the fixture is connected to the instrument. Then, each compensation standard is connected, and the instrument performs a single internal measurement and stores the information. Then, the DUT is connected, and a single measurement is made. The instrument will perform the necessary equations to remove the fixture contribution and display the DUT impedance. This process is simple but can be modified to reduce error for measuring small inductances.

2.3.1 Repeatability

When making measurements, there is an inherent variation associated with each individual measurement referred to as repeatability [7]. This variation can be caused by noise in the instrumentation, variations in contact resistance, variations in the position of the device, environmental conditions, and any other factors that can make a seemingly identical measurement vary [9].

Errors associated with repeatability can be minimized by applying an averaged external compensation technique. Effectively, by repeating each compensation and DUT measurement multiple times, outlier removal and averaging can be applied to reduce repeatability error. This technique requires performing compensation externally – that is, saving all the data separately and applying the compensation equations in a separate software. The equations needed to perform any combination of short, open, and load compensations are provided in Table 1. *Note: when applying compensation, decompose the impedance into real and imaginary components. The equations will not work with impedance magnitude and phase.*

Table 1: Equations to perform external compensation

Compensation Type	Equation
Short, Open, and Load	$Z_L = \frac{(Z_{XM} - Z_{SC})(Z_{OC} - Z_{SM})}{(Z_{OC} - Z_{XM})(Z_{SM} - Z_{SC})} Z_{ST}$
Short	$Z_L = Z_{XM} - Z_{SC}$
Open	$Z_L = \frac{Z_{OC} Z_{XM}}{Z_{OC} - Z_{XM}}$
Load	$Z_L = \frac{Z_{ST} Z_{XM}}{Z_{SM}}$
Short and Open	$Z_L = \frac{Z_{OC}(Z_{XM} - Z_{SC})}{Z_{OC} - Z_{XM}}$
Short and Load	$Z_L = \frac{Z_{ST}(Z_{XM} - Z_{SC})}{Z_{SM} - Z_{SC}}$
Open and Load	$Z_L = \frac{Z_{ST} Z_{XM}(Z_{OC} - Z_{ST})}{(Z_{OC} - Z_{XM}) Z_{ST}}$
Z_{XM}	Measured impedance of the DUT
Z_{OC}	Measured impedance of the open calibration standard
Z_{SC}	Measured impedance of the short calibration standard
Z_{SM}	Measured impedance of the load calibration standard
Z_{ST}	True impedance of load the calibration standard

The averaging process is described as follows, where *n* is the number of measurements desired.

1. Measure and save the short compensation
   a. Lift probe, place back into position, repeat for *n* measurements
   b. Eliminate any outliers
   c. Average remaining measurements
2. Measure the DUT
   a. Lift probe, place back into position, repeat for *n* measurements
   b. Eliminate any outliers
   c. Average remaining measurements
3. Perform compensation
   a. Taking the results of 1-c and 2-c, with the appropriate equation from Table 1, calculate an impedance estimate

An example of this process for a short compensation measurement using the 42941a probe is shown in Figure 18. The 42941a is particularly susceptible to repeatability errors because of the contact resistance between the surface and the probe tip. It is highly recommended to use the averaging method with the 42941a probe. Figure 18 (a) shows 25 raw measurements for the short compensation standard converted to inductance. Most measurements follow a similar trajectory, but 4 measurements are clear outliers. If more than 10% of the datapoints in a given measurement result are greater than two standard deviations from the mean, the entire measurement result is discarded. The outliers are most likely caused by poor contact between the probe tip and the compensation plane. The remaining valid measurements in Figure 18 (b) show good agreement but have high levels of variation at low frequency. By averaging the remaining measurements, this variation can be reduced and yields the result in Figure 18 (c). This waveform represents the short compensation that will be applied to the DUT measurement using the equations in Table 1.

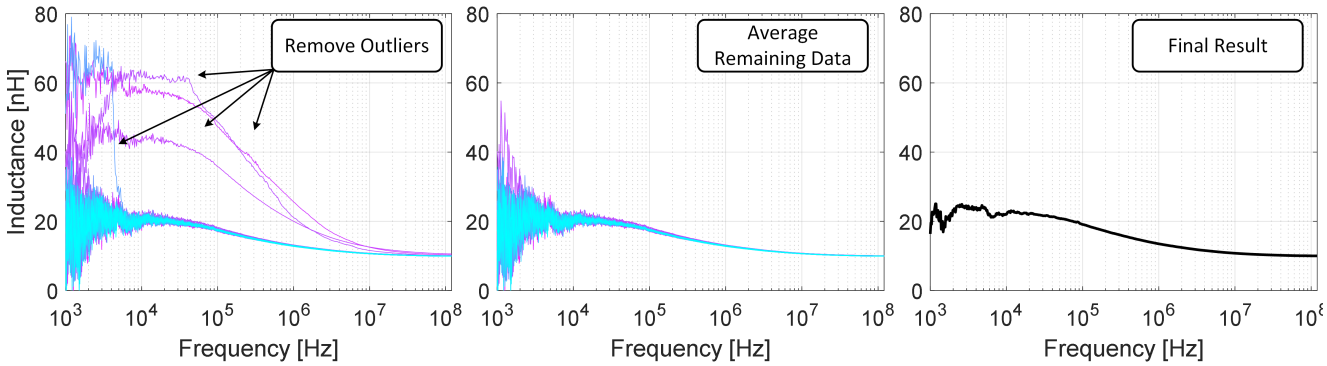


Figure 18: Example flow of data processing for the short compensation measurement

2.3.2 Residual Impedance

When performing the short compensation, a shorting structure must be added to the fixture to close the inductance loop. However, what is desired is the partial inductance of the fixture; the shorting structure adds some impedance to the measurement that is not included in the DUT measurement. Effectively, an assumption is made that the shorting structure applied has zero impedance. For most measurements, this assumption does not affect the measured result in any noticeable way. However, for very low inductance parts (such as in SiC

power modules), the impedance of the short standard is not insignificant. Determining the impedance of the shorting structure is impossible empirically, but FEA tools can be used to estimate its residual impedance. Figure 19 shows a 3D geometry of the 16047e shorting bar implemented in ANSYS Q3D (an FEA extraction software). Simulation estimates the residual inductance of the shorting bar to be 0.55 nH. Thus, this 0.55 nH can be added back to the measurement in post-processing.

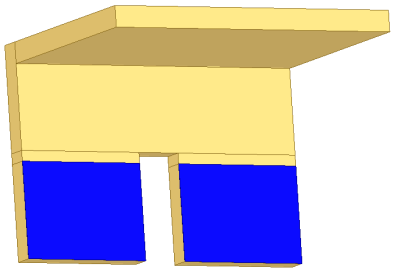


Figure 19: 3D geometry of the 16047e shorting structure evaluated in ANSYS Q3D [6]

For example, consider the commutation inductance measurement of the WAB400M12BM3 power module using the 16047e setup shown in Figure 12. This measurement setup uses the 16047e shorting bar for the short compensation, which was simulated to have a residual impedance of 0.55 nH. Figure 19 shows a comparison of the WAB300M12BM3 commutation inductance extracted in ANSYS Q3D and the empirical measurements with the 16047e fixture. When the residual impedance is not included, the measurement underpredicts the simulation result in the region of interest (1 MHz – 10 MHz). However, after adding the residual impedance back to the measurement, the measurement and simulation result overlap.

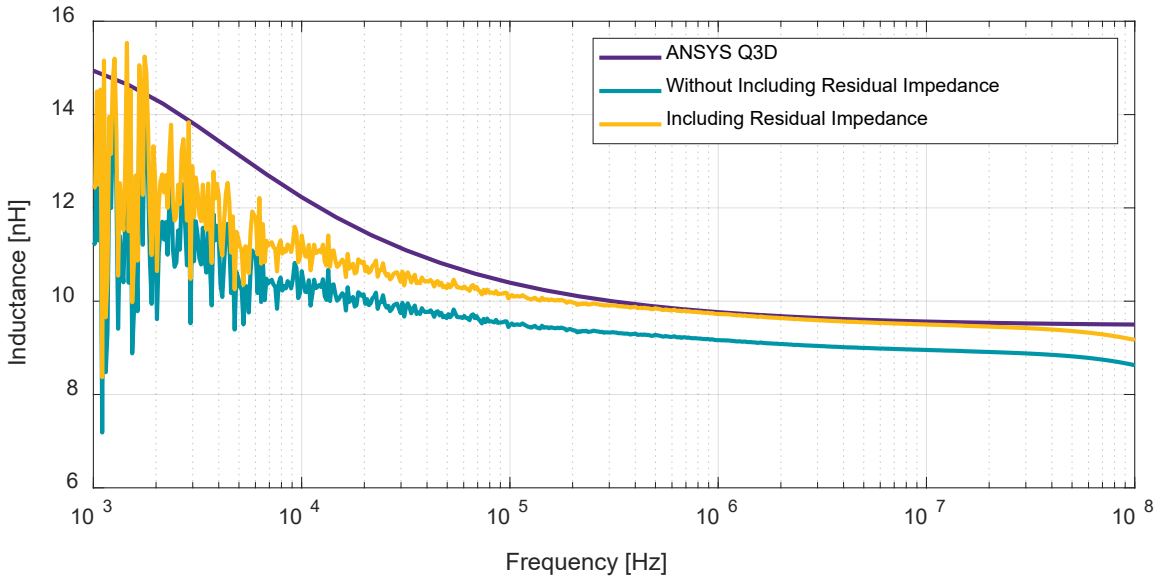


Figure 20: Commutation inductance measurement of a WAB400M12BM3 power module compared to FEA, with and without the residual impedance removal

2.3.3 Consistency Between Compensation and Measurement

Maintaining a consistent configuration between compensation and measurement is a critical factor in making accurate impedance measurements [9]. The short compensation must either 1) represent the smallest possible impedance between the fixture terminals or 2) be controlled such that the impedance is deterministic in FEA. The fixture geometry and placement must also be identical between the short compensation and the DUT measurement. An example of a proper short compensation and measurement is shown in the measurement of a surface mount inductor in Figure 21. The jaw width between the compensation measurement in Figure 21 (a) is identical to the width in Figure 21 (b). Changing the jaw width between them would invalidate the measurement. Other factors, such as the surface finish, are kept consistent. Here, the short calibration standard is defined as a small strip of the same geometry as the DUT; this strip can then be imported into FEA software and analyzed to determine the residual inductance.

Figure 21: Metrology for test case inductors (a) short compensation and (b) DUT measurement

As stated, another option for applying the compensation is to create the lowest inductance path between the fixture leads. For the 42941a fixture, a large, polished copper plane provides an ideal surface for compensation, as shown in Figure 22.

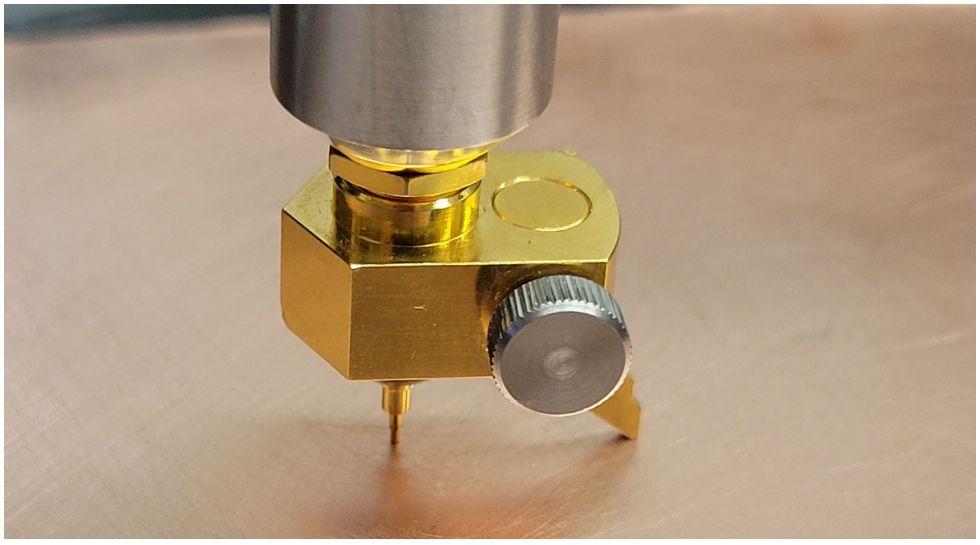
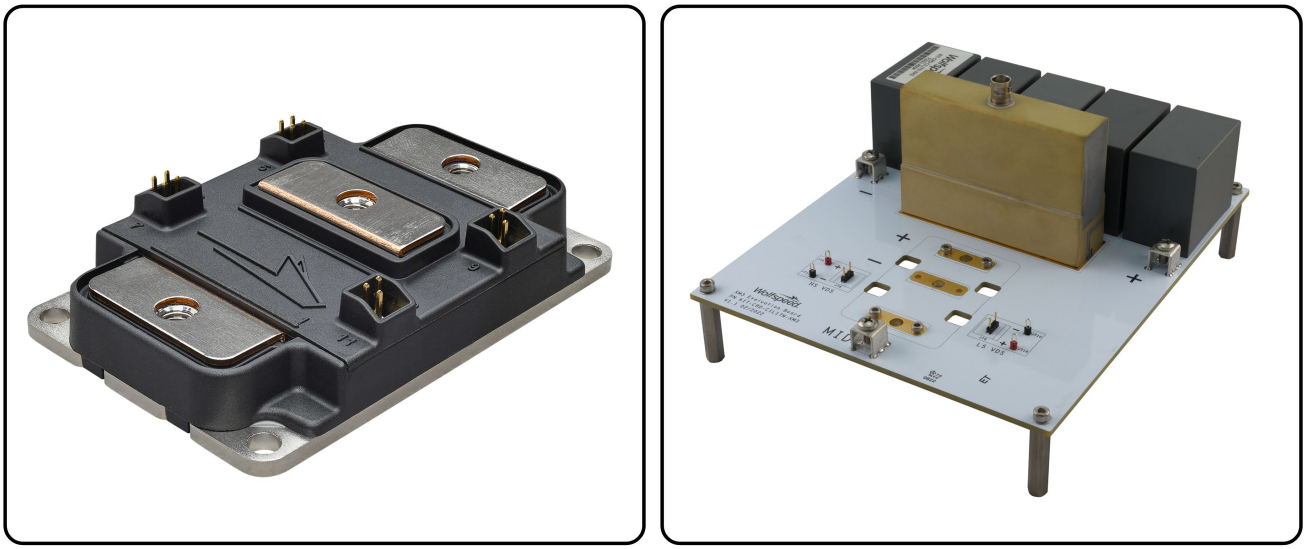


Figure 22: Example of a short compensation using a polished copper plane

3. Application of Measurement Techniques

The measurement methods outlined in Section 1 are applied to a Wolfspeed KIT-CRD-CIL17N-XM3 and a CAB320M17XM3 half-bridge power module shown in Figure 23 (a) and (b), respectively. Each measurement constitutes a partial inductance, but the combined inductance of these devices yields the full commutation inductance of the system during a double pulse test (DPT).



(b) (a)

Figure 23: Inductance will be characterized for (a) the CAB320M17XM3 and (b) the KIT-CRD-CIL17N-XM Eval Kit

3.1 XM Power Module Measurements

The first measurement discussed is of the XM power module. The commutation loop inductance for half-bridge modules is obtained by measuring across the DC+ and DC- terminals. The device is biased ON during all measurements by applying a 12 V battery across the G-K terminals of both switch positions. The XM module provides additional challenges when measuring due to the differences in height between the DC+ and DC- terminals.

Both the 42941a and 16047e manufacturer fixtures can be used to measure the XM power module. A picture of the measurement setup using the 16047e fixture is shown in Figure 24. Similar to the method for the 62 mm module in Figure 12, copper foil is added to the measurement terminals to provide a vertical structure for the 16047e to clamp to. The probe leads apply the 12 V battery source to the XM module terminals to bias the device ON. The short compensation is performed with the standard shorting bar in Figure 17. The averaging and external compensation techniques in 2.3 are all applied.

A picture of the measurement setup using the 42941a fixture is shown in Figure 25. To account for the vertical height differences in the terminals, the “ground” terminal of the 42941a probe head is unscrewed, brought down in height, and retightened. Because the probe head cannot be compensated using a flat plane, the short compensation was done by adding a copper shorting strap between the module terminals, shown in Figure 25 (a). This allows for the exact same geometry to be used between the short compensation and the XM3 measurement in Figure 25 (b).

Figure 24: XM module measurement with 16047e fixture

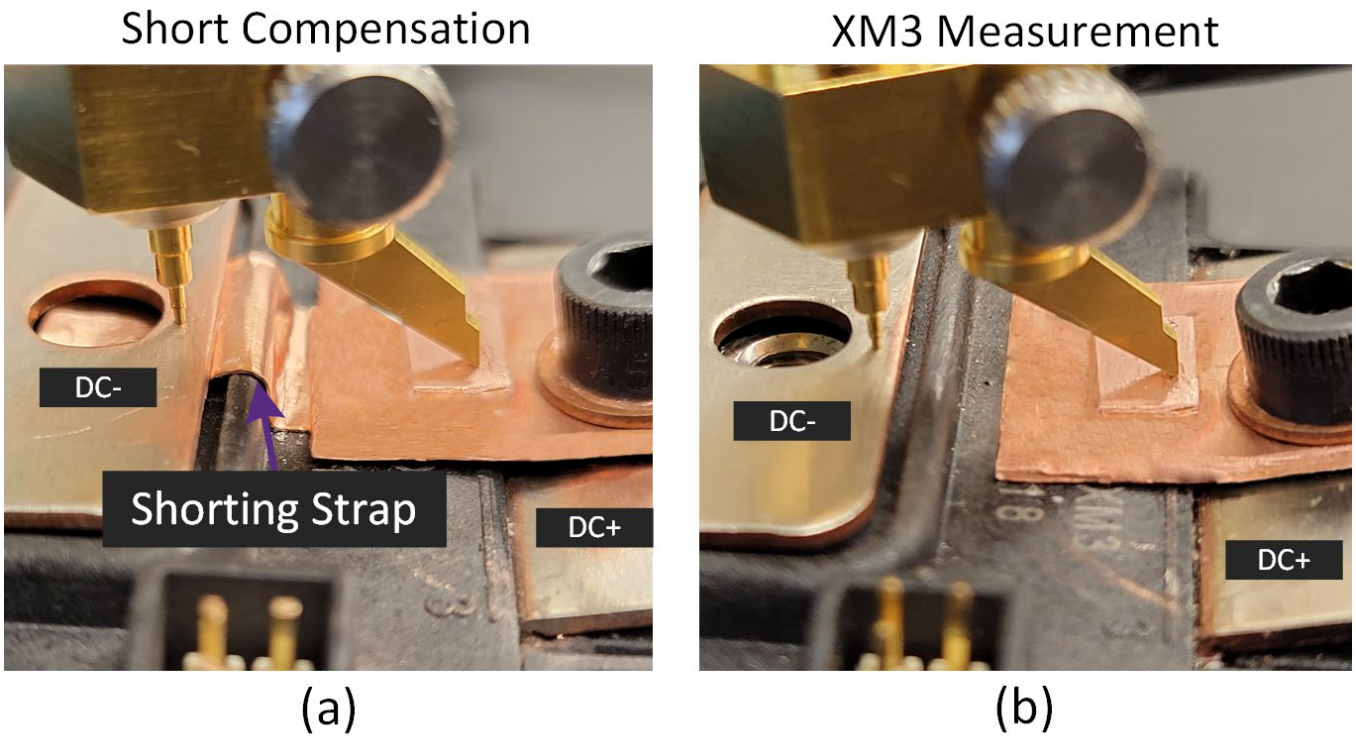


Figure 25: XM module measurement with 42941a fixture, (a) short compensation configuration and (b) XM measurement configuration [10]

The measurement results from the above configurations were processed in MATLAB to remove outliers, average the data, and apply the compensation equations. The XM3 power module geometry was imported into ANSYS Q3D to provide a reference to the measured data. Figure 26 shows the results of this comparison. All three methods agree, especially in the region of interest (1 MHz – 10 MHz). Interestingly, the results do not show a significant decrease in inductance over frequency; this suggests that the current paths in the XM power module are balanced (there is no significant crowding to an inner region of the conductor). The simulated and measured results are roughly 6.7 nH at 10 MHz.

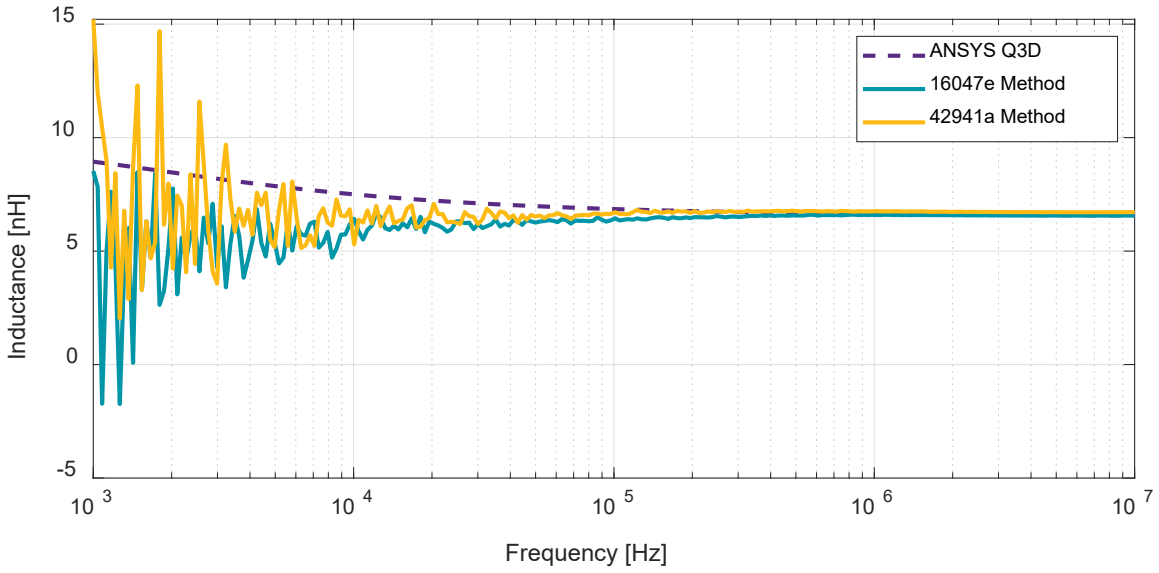


Figure 26: XM module measurement results compared to ANSYS Q3D

3.2 DC Link Measurements

Characterizing the impedance of CIL evaluation kits has additional complexities due to the large geometry and additional components on the PCB. The evaluation kit features bulk capacitors that store most of the energy required during testing. These capacitors contribute their own parasitic inductance to the measurement and should be included. Often, smaller high-frequency capacitors are placed on the PCB closer to the module, providing a low-impedance path for high-frequency current. The DC+ and DC- layers on the PCB are also often overlapped to provide flux cancelation and decrease the inductance, but this structure forms a parasitic parallel plate capacitance close to the module. The current-viewing resistor also contributes some inductance to the system and should be included during measurement. Considering these paths, the simplified circuit network of a typical CIL evaluation kit is shown in Figure 27 (a more complex circuit would consider the individual capacitors, but this is unnecessary for most analysis). The measurement should be made across the DC+ and DC- terminals in Figure 27 (where the module would be connected).

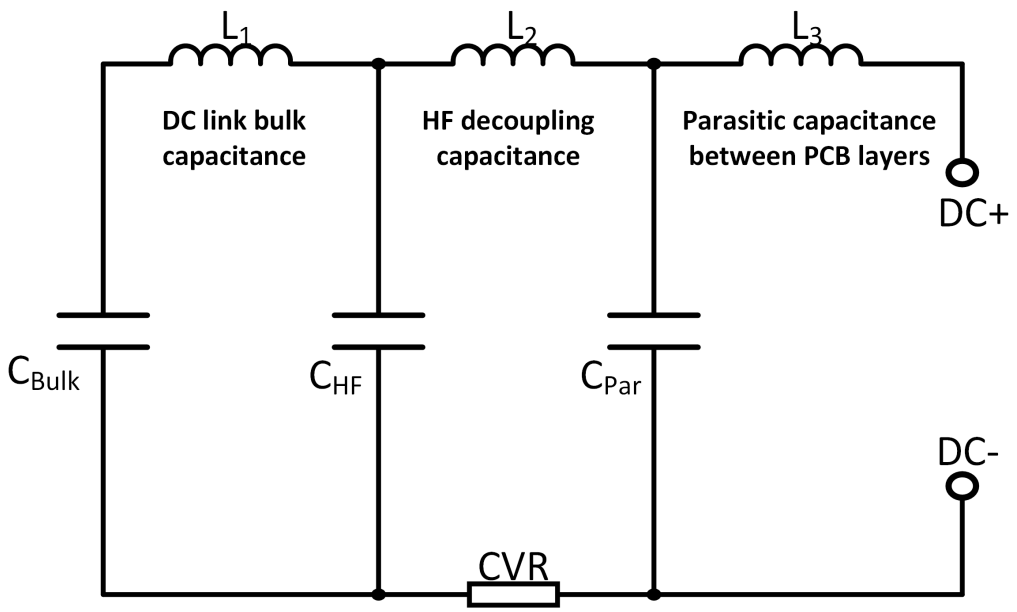


Figure 27: Circuit network of typical CIL evaluation kit

Because of the large size of the evaluation kit, it is not possible to mount on the impedance analyzer. Instead, the 42941a impedance probe provides the easiest measurement configuration. Figure 28 shows the 42941a impedance probe placed onto the evaluation kit during measurement. The probe is placed on the bottom side of the PCB where the module attaches to more accurately replicate the location of the module attachment. In the bottom view, the high-frequency capacitors are visible. In total, the KIT-CRD-CIL17N-XM evaluation board has five parallel 22 µF bulk capacitors (110 µF), thirty parallel 0.047 µF high-frequency capacitors (1.4 µF), and a 2.5 mΩ bar shunt current-viewing resistor.

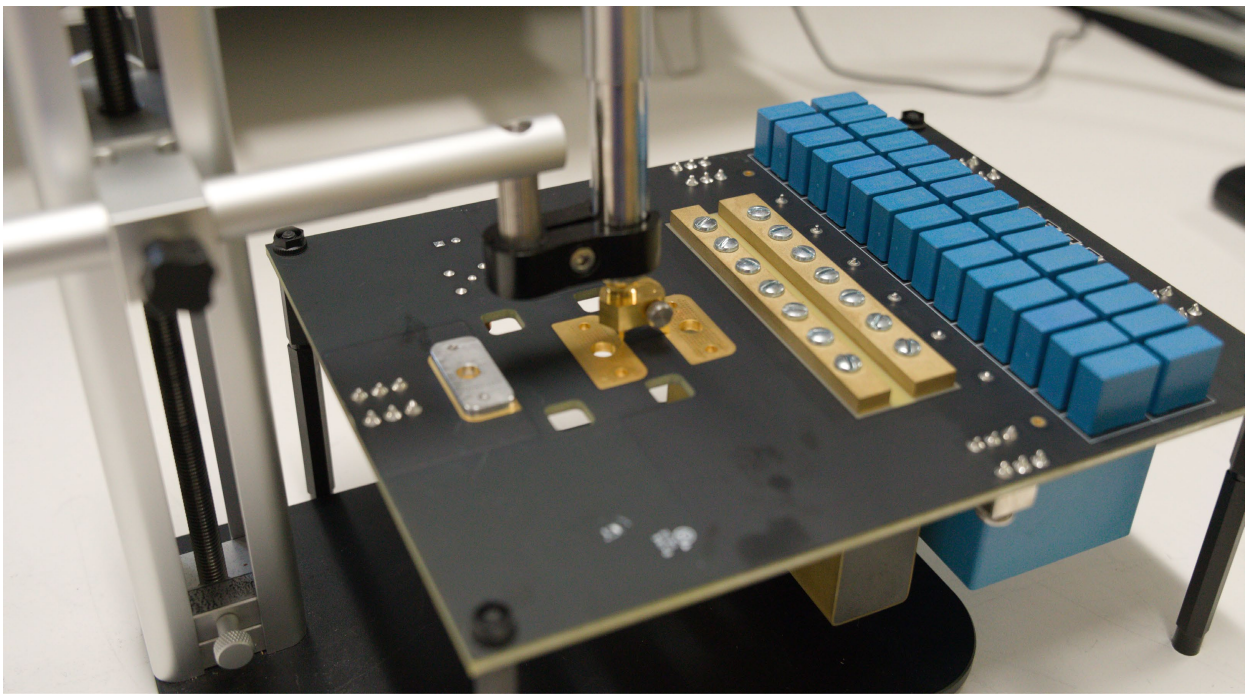


Figure 28: KIT-CRD-CIL17N-XM commutation inductance measurement setup from DC+ to DC-

The CIL evaluation board measurements were processed using the averaging external compensation technique and the results are shown in Figure 29. The impedance profile across frequency shows several resonances due to the multiple LC elements that represent the system. Because the inductance across the system is not constant, it can be difficult to select a single inductance to represent the commutation inductance. Wolfspeed recommends extracting the inductance at 10 MHz, but this may not always be possible (for example, if a resonance exists at this frequency). In addition, there may be multi-modal ringing in the system – often, the voltage overshoot is determined by the inductance $L_2 + L_3$, but high-frequency oscillations are determined by C_{Par} and L_3.

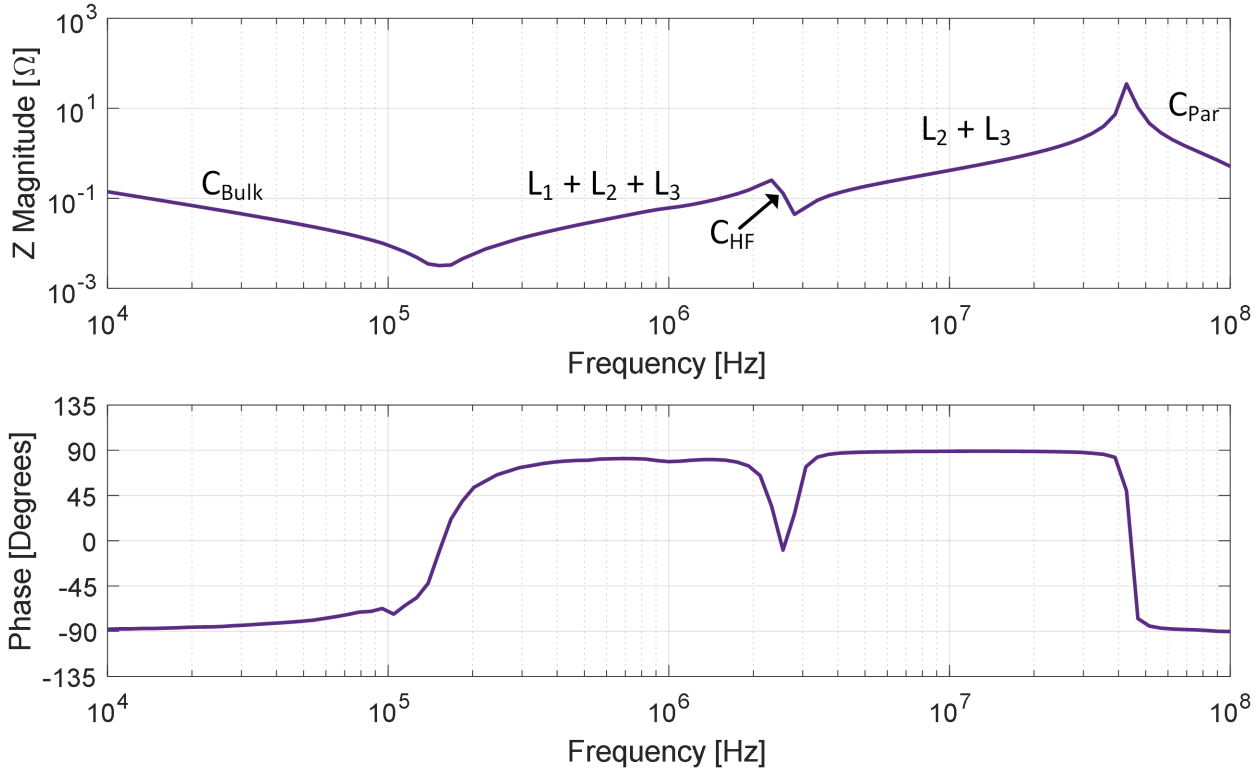


Figure 29: KIT-CRD-CIL17N-XM impedance measurement results

To actually quantify the system parasitics, there are several approaches. One approach would be to use the impedance, phase, and frequency at specific points to calculate the inductance (select points where the phase is ~90 degrees). Another method is to implement the full parasitic model in simulation and extract the frequency response. An SPICE simulation of the CIL evaluation kit parasitic model is shown in Figure 30. The values were tuned to match the measured impedance data, the results of which are presented in Figure 31. The parasitic model shows good agreement with the empirical data. Here, the high-frequency current loop through the high-frequency capacitors is 6.5 nH.

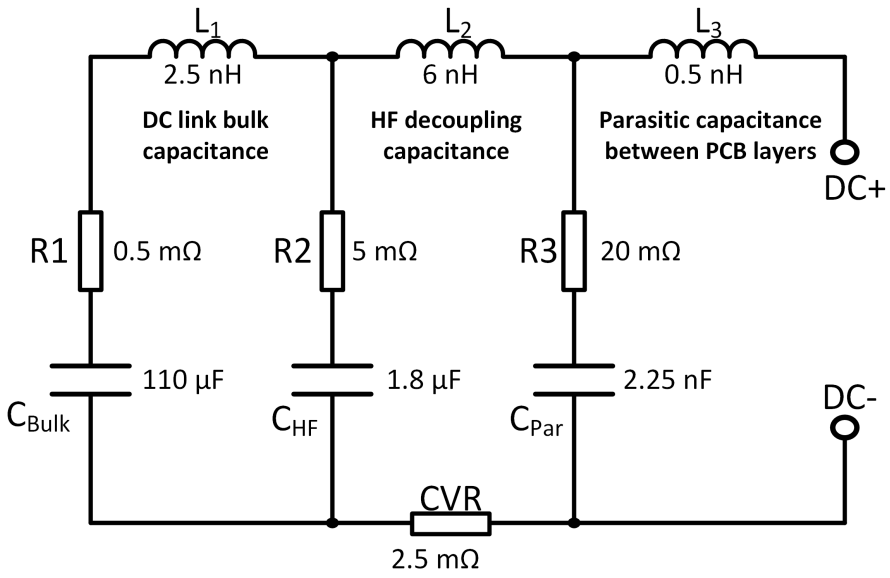


Figure 30: SPICE circuit of CIL evaluation board parasitics

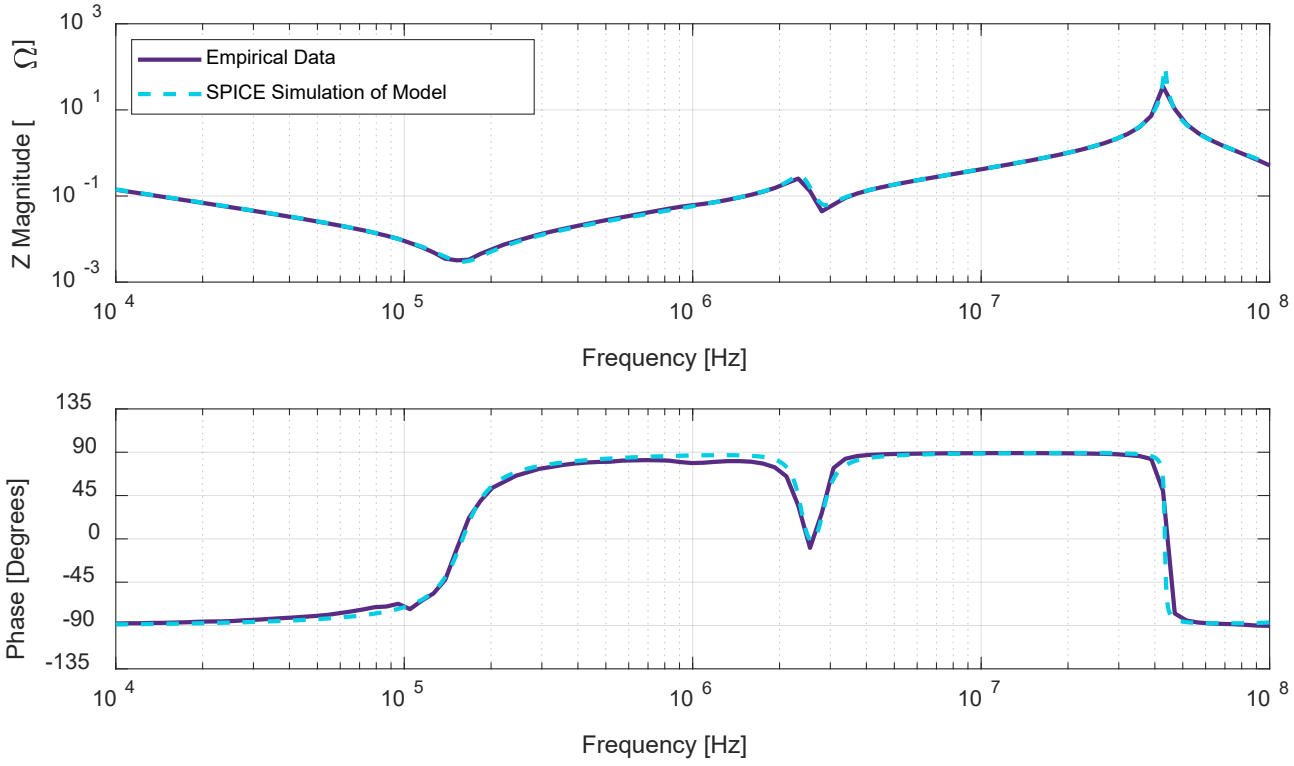


Figure 31: Overlay of empirical impedance data and LTspice simulation of the parasitic model

3.3 Time-Domain Extraction

An alternative method to impedance analysis that can be used to estimate the commutation inductance of a full system is through analysis of the time-domain DPT waveforms. This method requires measurements with accurate de-skew and high bandwidth of the drain-source voltage and drain-source current during the DPT (see document PRD-08333). An annotated view of the fully assembled KIT-CRD-CIL17N-XM evaluation kit is shown in Figure 32. A CAB320M17XM3 power module was connected to the evaluation board and a CGD1700HB2P-XM3 gate driver is used to control switching. This configuration was used to measure DPT waveforms of the CAB320M17XM3 power module.

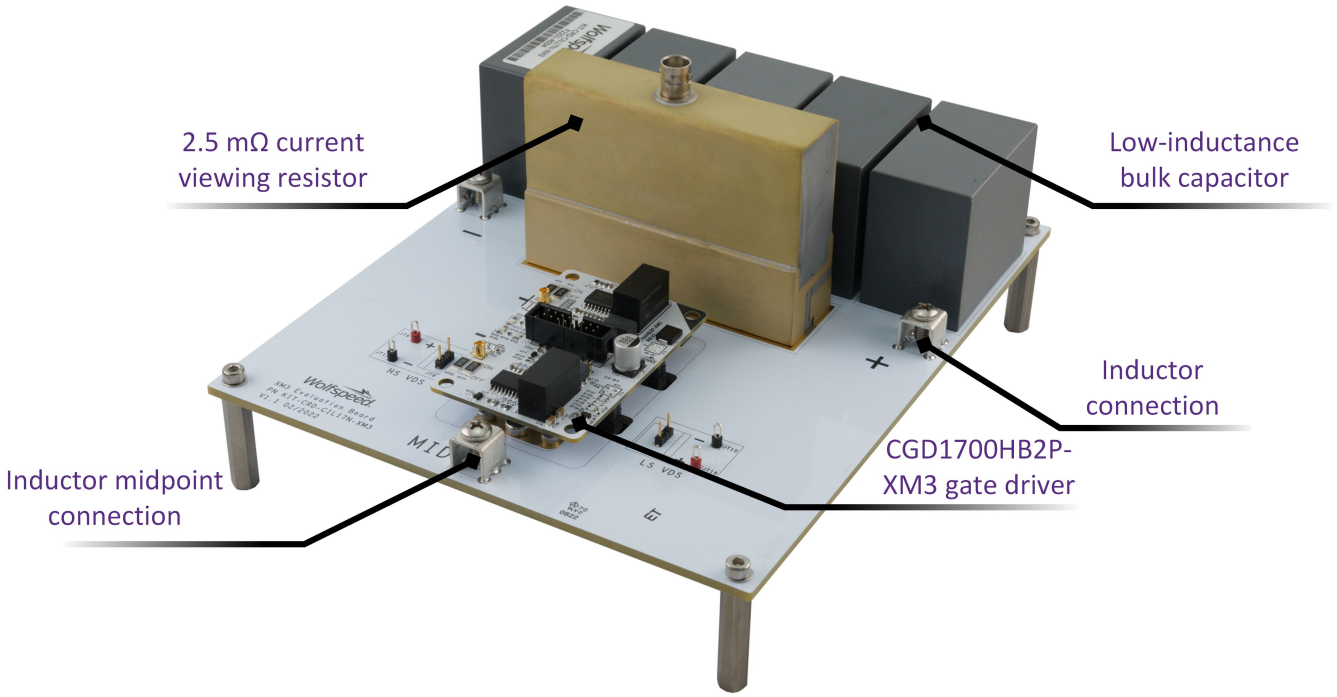


Figure 32: KIT-CRD-CIL17N-XM evaluation kit

During a DPT, the drain-source voltage (V_{DS}) waveforms will be affected by changes in the drain-source current (I_{DS}). The perturbations in the drain-source voltage are equal to the derivative of the drain-source current multiplied by the commutation inductance, as shown in equation (1). A common example of this is the voltage overshoot observed at turn-off – a faster device or higher parasitic inductance will result in higher overshoot. In effect, the V_{DS} and I_{DS} waveforms can be used to estimate the commutation inductance.

$$V_{DS,act} = V_{DS,meas} + L * \frac{dI_{DS}}{dt} \qquad (1)$$

This method can be applied to both the turn-on and turn-off waveforms. Figure 33 demonstrates the process on the turn-on waveforms measured at 900 V, 500 A, 25°C, and 1 Ω R_G. In Figure 33 (a), the V_{DS} waveform (teal) has a region of slow, linear decrease before the device fully turns on. This region is known as the "knee" and is caused by the di/dt event inducing a voltage drop across the commutation inductance in the system. In software such as MATLAB, equation (1) can be calculated and overlaid with the original V_{DS} waveform. The knee will be removed when *L* is tuned properly. *Tips: use the "gradient()" function to calculate the derivative,*

"circshift()" to adjust the deskew, and "smooth" to add filtering if necessary. Figure 33 (b) shows an example of this process. With *L* set to 11 nH, the modified V_{DS} waveform (purple) shows a flat response during the knee region (if *L* is too low, the knee will have a negative, and if *L* is too large, the knee will have a positive slope).

The estimate of 11 nH slightly underpredicts the actual inductance of 13 nH; this is because this method only considers the inductance that is both in the commutation loop and *not* in the V_{DS} measurement path. For a low-side DPT measurement, this means that the source inductance of the module is not considered (and vice-versa, a high-side measurement would not include the drain inductance of the module). Thus, this method will underpredict the actual commutation inductance of the system but will provide a reasonable estimate.

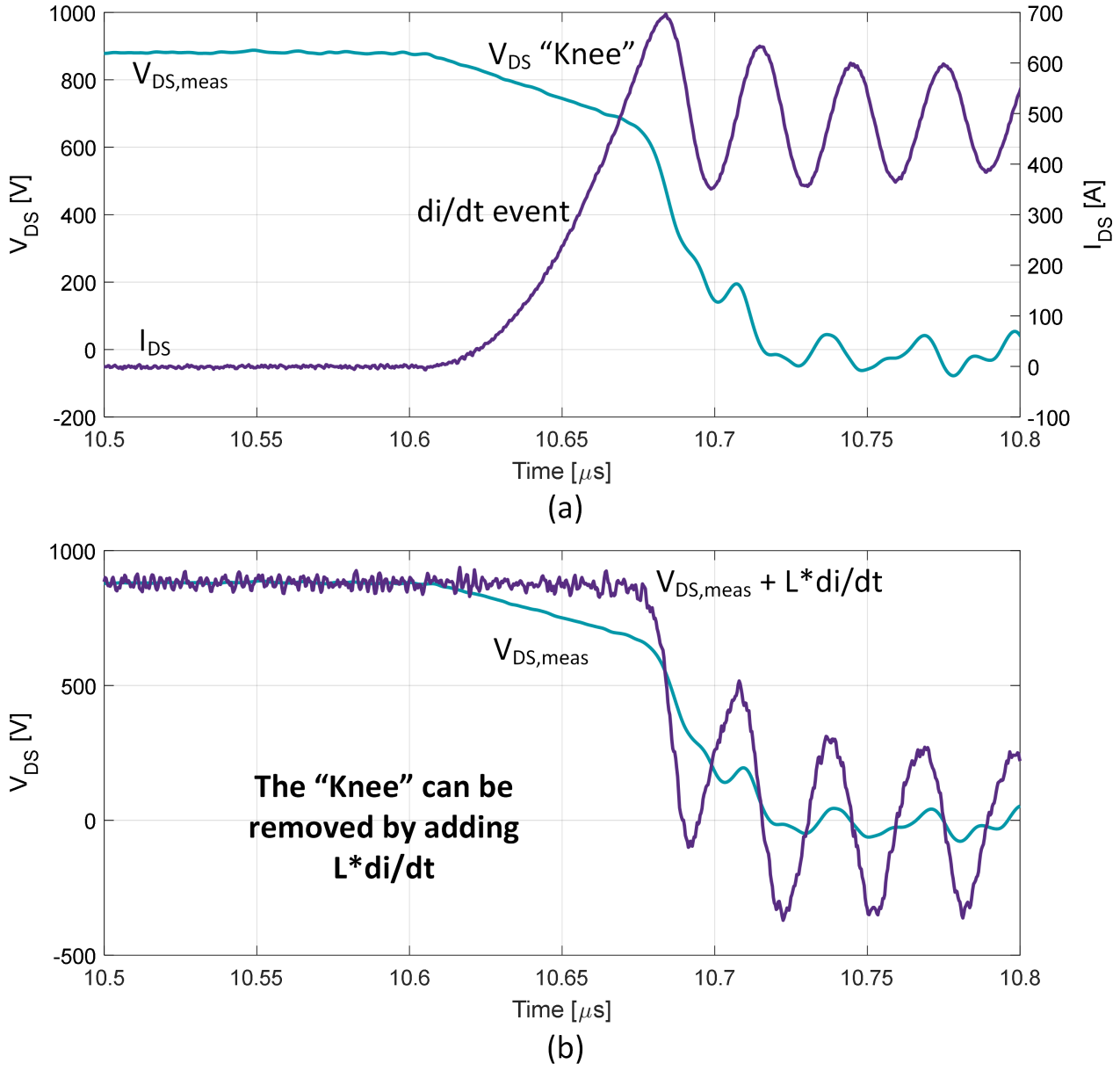


Figure 33: Time-domain inductance extraction method using the turn-on event, (a) V_{DS} and I_{DS} waveforms, (b) V_{DS} and "corrected" V_{DS} waveform

Figure 34 demonstrates the technique applied to a turn-off waveform. A V_{DS} measurement at turn-off usually shows a large voltage spike after the transition because of the di/dt event; however, after applying the L * di/dt removal (with 11 nH) the dynamics of the transition are removed.

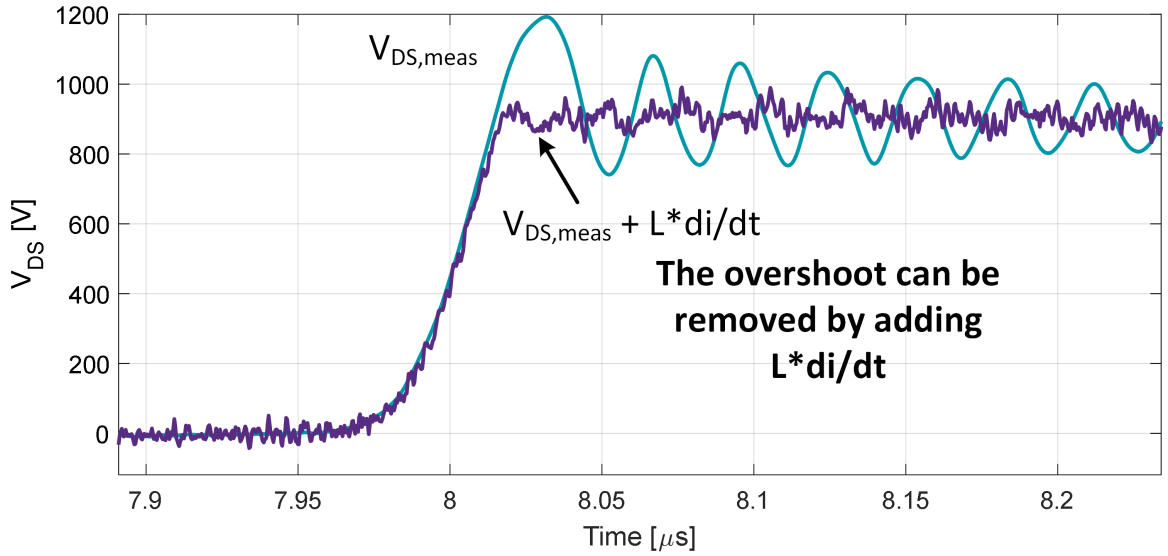


Figure 34: Time-domain inductance extraction method using the turn-of event: V_{DS} and "corrected" V_{DS} waveform

4. Custom Fixture Design and Implementation

In general, Wolfspeed recommends using the previously discussed manufacturer-designed fixtures or FEA analysis when possible. However, for some geometries (such as those with terminal distances greater than 62 mm), and when FEA is not possible, fully custom fixtures may be necessary. Designing proper fixtures and applying correction procedures is laborious but can yield reasonable results.

Two custom fixture designs are practical for SiC module measurements: one using the four-terminal-pair (4TP) technique, and one using a four-terminal (4T) technique [11]. While the 4TP measurement is described as more accurate than the 4T measurement [11], it is noted that improperly terminating the shield in the 4TP setup will yield invalid results. The 4T technique, however, is not prone to this issue. Therefore, both techniques are compared herein.

A detailed diagram describing the E4990A 4T and 4TP measurement techniques is shown in Figure 35. The E4990A has four terminals; the HC and LC terminals provide the stimulus current, while the HP and LP terminals measure the voltage potential drop across the measurand [12]. The stimulus current flows from the HC terminal through the device under test (DUT) and finally to the current collection terminal, LC. The current then flows through the return path until it terminates through the shield of the HC terminal. It is noted that during compensation, the DUT is replaced with a shorting structure or "short standard," but the current paths are unchanged. The primary difference between the 4T and 4TP techniques is the shield connection. The 4T measurement terminates the shield of each terminal directly at the instrument attachment, whereas the 4TP measurement configures the shield so that it follows the signal traces and connects at the DUT.

For the 4TP measurement, the signal traces and shield are intended to be implemented as 50 Ω impedance-matched striplines. The shield traces should not connect to the module terminals and should be galvanically isolated from the signal trace across the entire PCB. For both fixtures, the HC/LC and HP/LP test signal traces should terminate close together on the module terminals to reduce the influence of current flow along the terminal during a measurement.

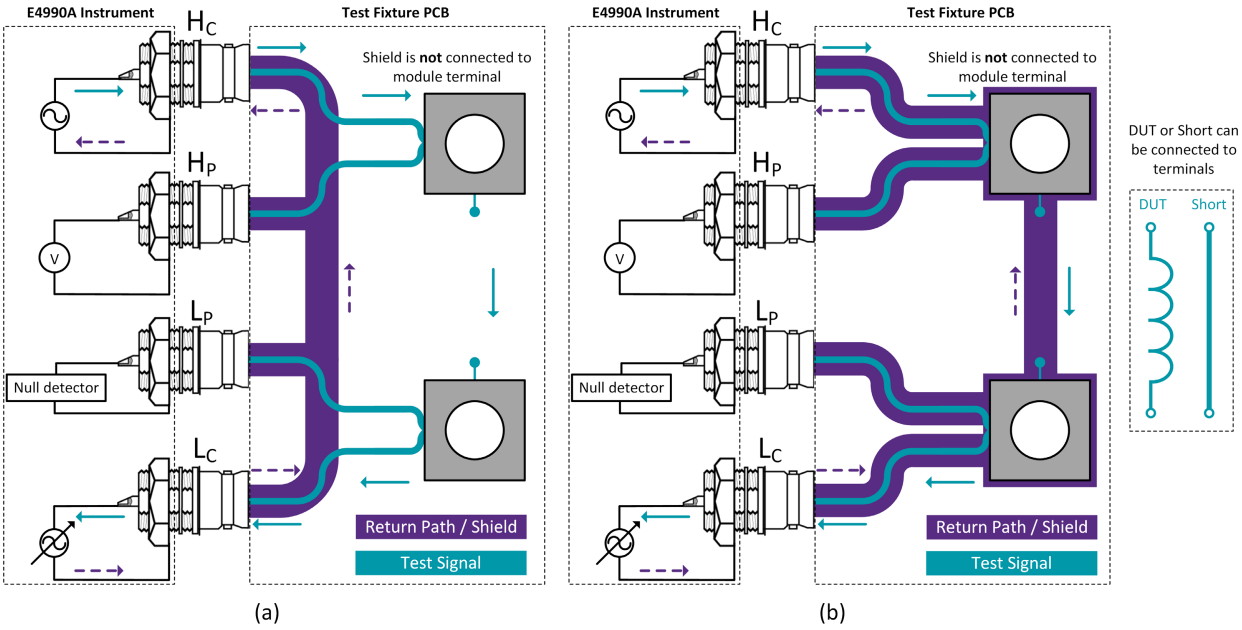


Figure 35: (a) Four-terminal measurement technique, (b) four-terminal pair measurement technique

Figure 36 presents the PCB layout for the two fixtures designed for the BM3 power module based on the 4T and 4TP measurement techniques. The red traces indicate bottom layer copper, and the blue traces indicate top layer copper. Each measurement requires two fixtures: one to perform a short compensation, and the other to perform the DUT measurement. Using a dedicated fixture to apply the short standard provides a much more consistent and controlled compensation compared to “external” approaches (e.g., soldered copper foil). Additionally, a fabricated short compensation fixture can be imported into FEA software for analysis. Both PCBs shown in Figure 36 consist of two electrical layers with 1.6 mm spacing and 1-ounce copper thickness. Both PCBs are designed to mount on top of the BM3 module. On the long sides of the fixtures, a set of four BNC connectors are used to interface directly with the E4990A impedance analyzer.

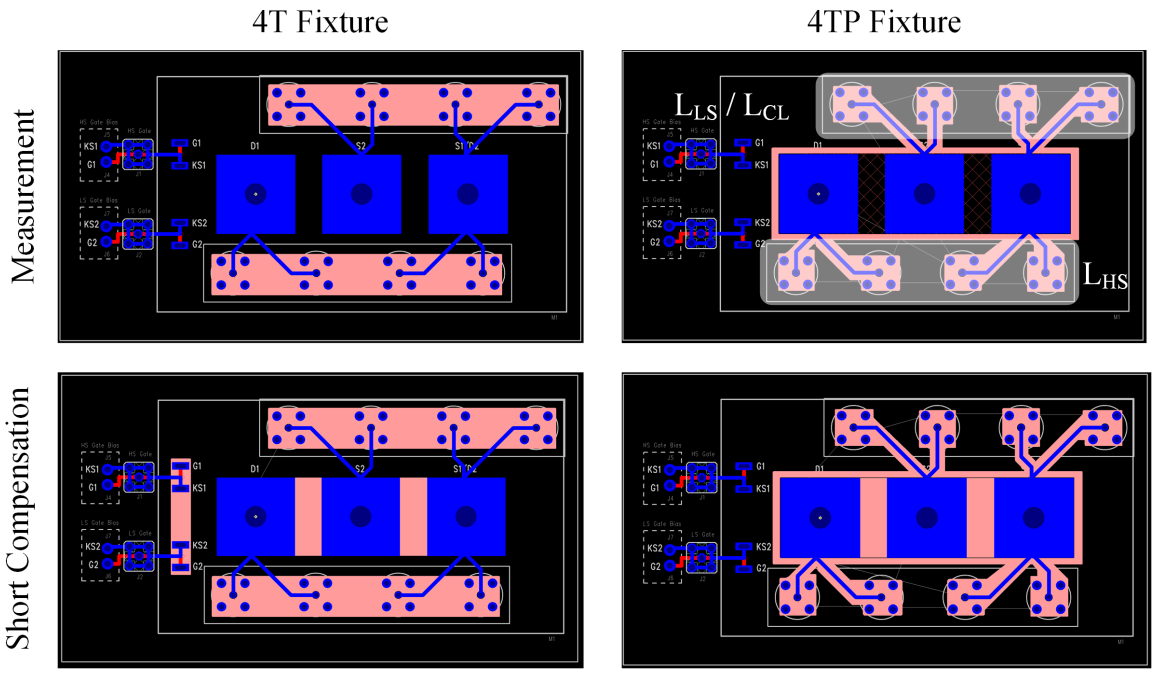
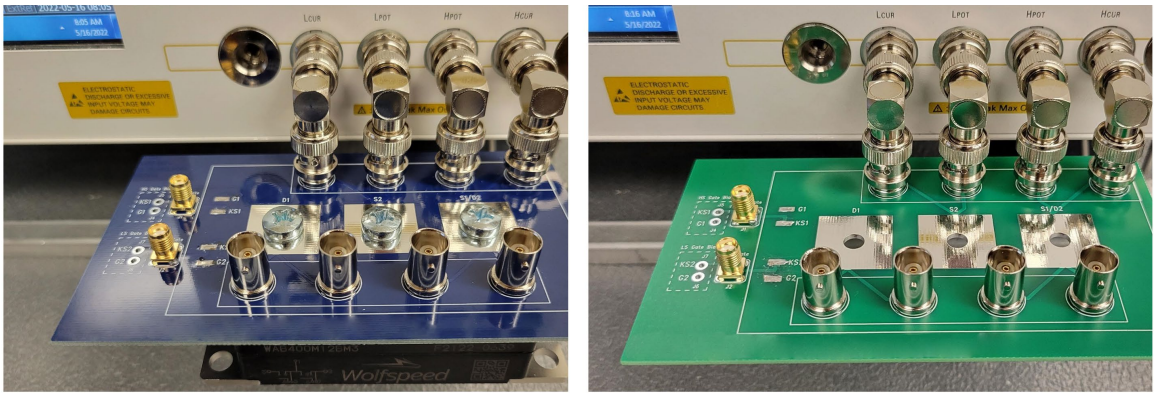


Figure 36: 4T and 4TP fixture designs for BM3 module measurements (short and measurement fixtures)

An important, but subtle, feature of these fixtures is how current is designed to flow to the module terminals. The blue traces for the stimulus signal terminate on the edge of the module terminals, which is not the desired location for measurement. Ideally, the current would be equally distributed on the face of the terminals. To resolve this issue, the signal traces are routed on the top layer of the board. The current then must flow through the annular ring in the center of each pad to reach the top face of the module terminals. Because the current flow for the short compensation and the module measurements are identical up to this point (as the shorting structure is located on the bottom layer of the PCB), its contribution to the measurement is removed in compensation.

Figure 37 shows the 4TP fixture configurations used to measure the BM3 power module. In Figure 37 (a), the BNC connectors on the PCB are connected to the E4990A impedance analyzer using right-angle adapters for a direct, cableless connection. The BM3 module is mounted using bolts at each terminal. In Figure 37 (b), the 4TP short compensation fixture is similarly attached to the E4990A and measured. Each measurement is performed 25 times. These measurements are averaged to produce a result with the aid of external compensation. Reconnecting the PCB or module between each measurement is unnecessary because of the consistency of these interfaces.



(a) (b)

Figure 37: Custom fixture measurement example, (a) 4TP measurement, (b) 4TP short compensation

Before discussing the results, it is important to understand the different measurements that can be made on a half-bridge module. The most important measurement discussed thus far is the commutation inductance from DC+ to DC-. However, measurements can also be made from DC+ to phase, and from phase to DC-. The nuances of when to measure these quantities is not discussed in this document, but for the BM3 case study the measurement from DC+ to phase requires measuring across the full length of the module. Because measurements with long terminal distances are the primary application of custom fixtures, this measurement from DC+ to phase is used as the test case for the developed custom fixtures.

Measurement results for the WAB400M12BM3 DC+ to phase measurement using the 4T and 4TP custom fixture are shown in Figure 38. The 4TP measurement overpredicts the FEA simulation, while the 4T measurement underpredicts the FEA simulation. Overall, the 4TP method demonstrates greater accuracy.

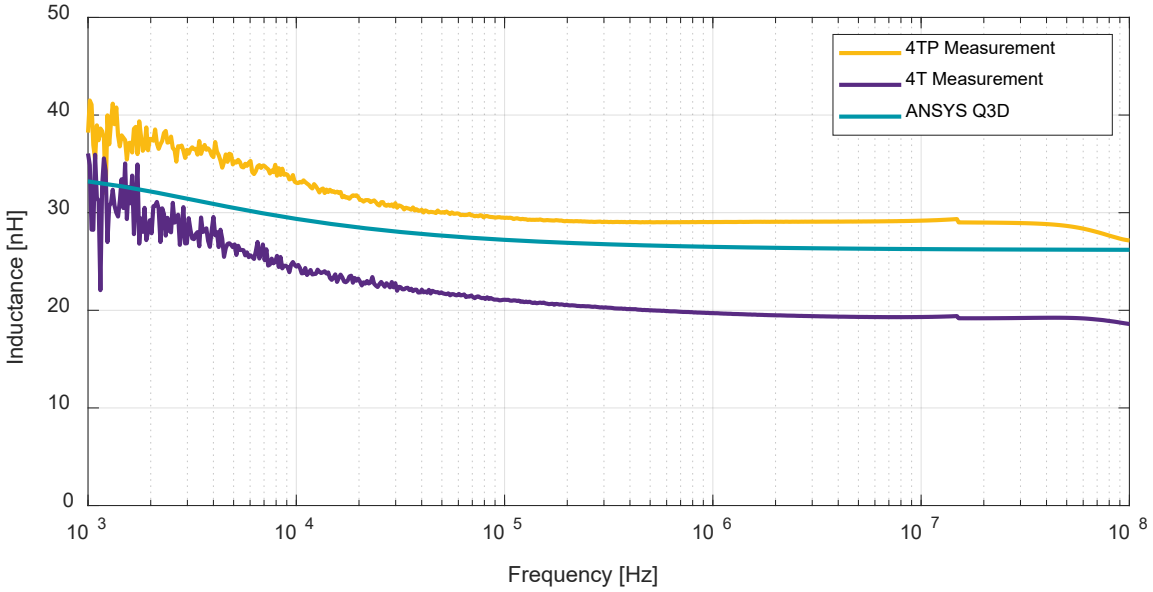


Figure 38: 4TP measurement comparisons for commutation loop, low side, and high side

4.1 Error Analysis: Residual Removal

The residual removal techniques discussed in section 2.3 can be applied to custom fixtures as well. However, the procedure differs for 4T and 4TP fixtures. For the 4T fixture, the residual impedance removal is identical to that of the manufacturer fixture, as shown in Figure 39 (a). The DUT measurement is described by L_{Meas}, which includes the self-inductance of the module (L_{Module}) as well as the self-inductance of the return shield path (L_{Return}). The total inductance (L_{Meas}) is the sum of these two quantities as given in equation (2). The short compensation measurement (L_{SC}) includes the residual inductance of the short standard (L_{Short}) and the self-inductance of the return shield path (L_{Return}). The total inductance L_{SC} is the sum of these two quantities, as given in equation (3). The final compensated result ($L_{compensated}$) is the difference between these two quantities, as given in equation (4). Here, the residual impedance of the short standard is the only source of error, per equation (5).

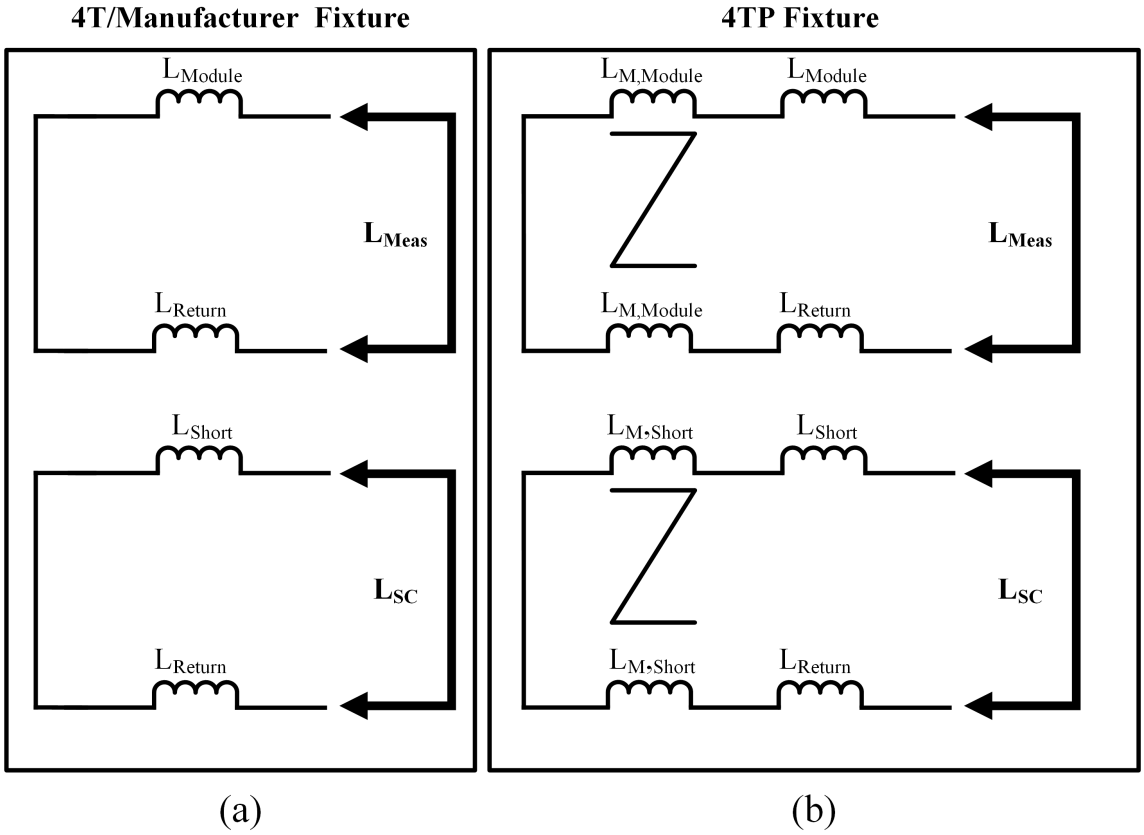


Figure 39: Measurement error analysis for (a) 4T and manufacturer fixtures, (b) 4TP fixtures [12]

$$L_{Meas} = L_{Module} + L_{Return} \quad (2)$$

$$L_{SC} = L_{Short} + L_{Return} \quad (3)$$

$$L_{compensated} = L_{Meas} - L_{SC} = L_{Module} - L_{Short} \quad (4)$$

$$L_{err} = L_{Short} \quad (5)$$

The error contributions of the 4TP pair fixture in Figure 39 (b) are more complex due to the placement of the shield return path near the DUT. Because the shield follows the path of the DUT and the short compensation, there is potential for mutual coupling between these paths. In the manufacturer fixture and the 4T fixture, the shield is located far away from the DUT, and these mutual coupling terms are negligible.

For the 4TP fixture in Figure 39 (b), the DUT measurement includes the partial self-inductance of the module (L_{Module}), the partial self-inductance of the return path (L_{Return}), and the mutual coupling between these paths ($L_{M,Module}$). The total inductance of this measurement (L_{Meas}) is given in equation (6). Conversely, the short compensation measurement includes the partial self-inductance of the shorting structure (L_{Short}), the partial self-inductance of the return path (L_{Return}), and the mutual coupling between these paths ($L_{M,Short}$). The total inductance of this measurement (L_{SC}) is given in equation (7). The final compensated measurement of the module is obtained by subtracting the short measurement (L_{SC}) from the module measurement (L_{Meas}), as given in equation (8). The error terms from equation (8) are resolved to produce an expression for total error (L_{error}) in equation (9). If the mutual coupling terms are equal or negligible, then the error for the 4TP fixture is identical to that of the 4T fixture.

The error contributions of the 4TP fixture measurement technique are significantly more complex than those of the manufacturer or 4T approaches. In addition, the mutual coupling between the return shield path and the module is challenging to quantify as it can only be estimated via FEA with an accurate CAD model of the DUT and access to appropriate FEA software. If both are available, then FEA software can be used to estimate the module inductance parameters directly in lieu of implementing a custom fixture. Thus, the 4TP measurement technique is not recommended due to its complex error contributions and the resulting difficulty in performing error removal without an accurate model of the DUT.

$$L_{Meas} = L_{Module} + L_{Return} - 2L_{M,Module} \quad (6)$$

$$L_{SC} = L_{Short} + L_{Return} - 2L_{M,Short} \quad (7)$$

$$L_{compensated} = L_{Meas} - L_{SC} = L_{Module} - L_{Short} - 2L_{M,Module} + 2L_{M,Short} \quad (8)$$

$$L_{error} = L_{Short} - 2L_{M,Short} + 2L_{M,Module} \quad (9)$$

Conversely, the manufacturer and 4T measurement techniques only require a 3D model of the fixture geometry to estimate the residual impedance. For the 16047e measurements, the shorting bar was measured with calipers and a simple 3D model was created, as shown in Figure 40. The blue shaded regions represent the source and sink locations of the model. This geometry was simulated in Q3D across frequency to estimate the residual impedance of the 16047e short standard.

For the custom 4T fixture, the residual impedances are more complex as they differ for each measurement. Figure 40 describes the regions of the short compensation standard that contribute the residual impedances of the short compensation. The measurement terminals are provided for clarity but are not included in the simulation. Only the region between the module terminals for each simulation is included, because Q3D makes use of the entire top face of the adjoining terminals for the source and sink. Note that the region of residual impedance is the same length as the module; this is why the errors are large for terminals with far-apart distances.

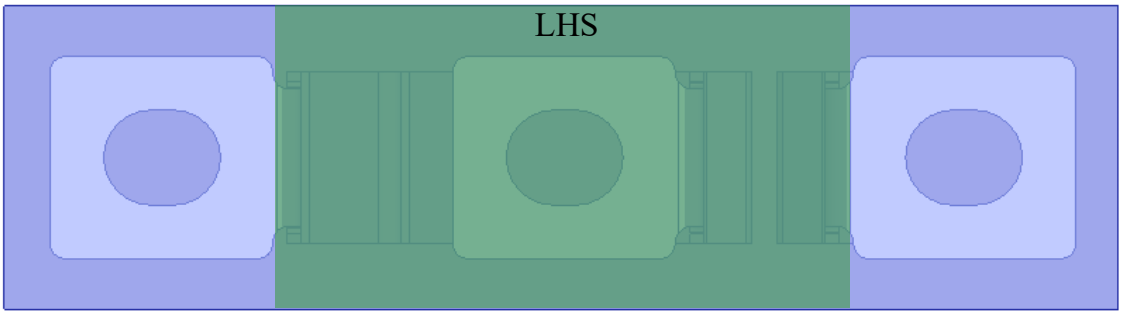


Figure 40: 3D geometry of the 4T short standard residuals. Colored regions represent the portion of the short standard that must be removed from the measurement

The residual short impedance for the 4T fixture is shown in Figure 41. The residual impedance is quite large, being 14 nH at 1 kHz and 10.5 nH at 10 MHz. The residual inductance in Figure 41 was added to the 4T measurement result in Figure 38, the result of which is presented in Figure 42. After applying the residual inductance removal, the 4T measurement shows improved accuracy when compared to the FEA results and is similar to the 4TP measurement. However, while this test case shows similar results between the 4T and 4TP techniques, the 4T technique with residual removal is overall more accurate than the 4TP technique.

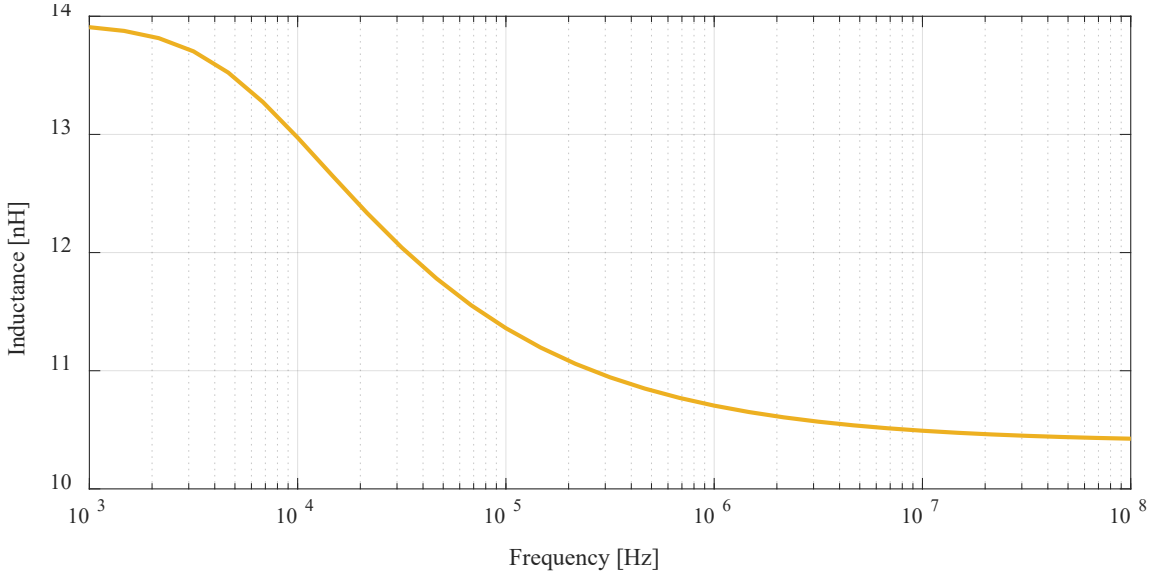


Figure 41: Residual short compensation impedance for the 4T measurement fixture

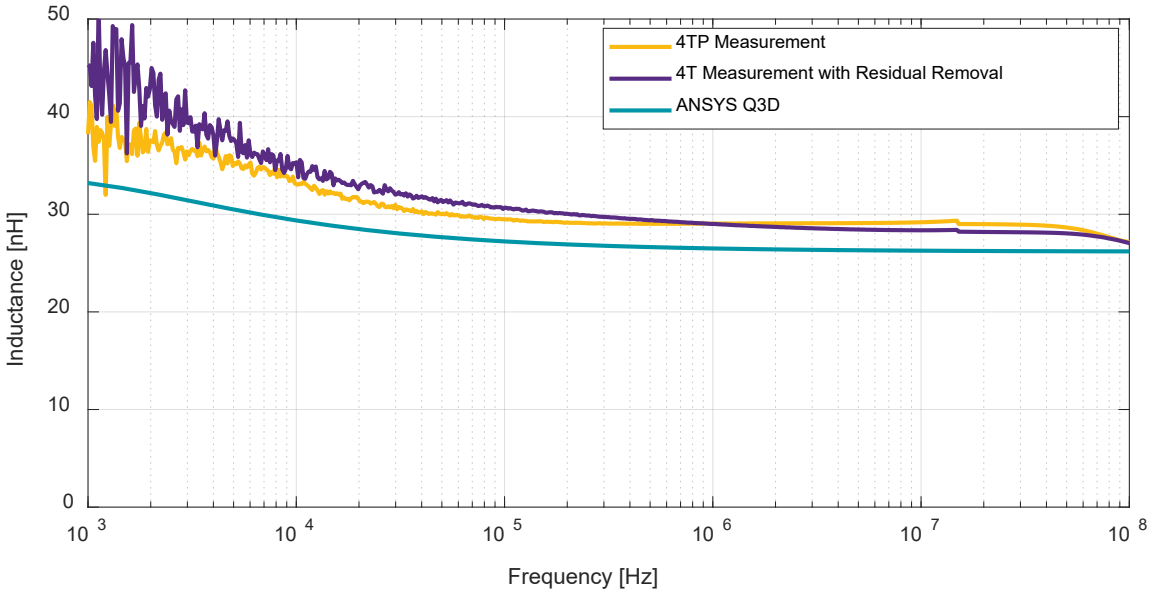


Figure 42: Corrected 4T custom fixture measurements with residual short impedance removed

5. Summary

Improperly designed systems with excessive parasitic inductance in the commutation path can cause voltage overshoots and oscillations that can only be managed by increasing gate resistance. However, this will increase switching losses and reduce efficiency. In order to take full advantage of the performance of SiC, it is necessary to design systems for minimal stray inductance. Developing capabilities to quantify inductance of both systems and modules is invaluable to designing and modeling these systems. This document describes in detail multiple methods for quantifying parasitic inductance that can be applied across a wide range of parts and geometries.

Revision History

Date	Revision	Changes
July 2024	1	Initial Release

References

[1] M. Olimmah, "Modeling and Simulation of Frequency Dependent Impedance of Conductors in Wide-band Gap Applications for Power Electronics," in *M.S. thesis, Univ. of Alabama*, Tuscaloosa, AL, 2020.

[2] Keysight Technologies, "E4990A Impedance Analyzer 20 Hz to 10/20/30/50/120 MHz," *5991-3890EN datasheet,* 2016.

[3] B. Nelson, A. Lemmon, B. DeBoi, M. Olimmah and K. Olejniczak, "Measurement-Based Modeling of Power Module Parasitics with Increased Accuracy," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020.

[4] Keysight Technologies, "Keysight 42941A Impedance Probe Kit," *Operation and Service Manual,* 2015.

[5] Keysight Technologies, "16047E Test Fixture, 40 Hz to 110 MHz Operation and Service Manual," in *Operation and Service Manual, 16047-90040*, 2018.

[6] B. T. DeBoi, "Characterization and Modeling of SiC Multi-Chip Power Modules," in *PhD Dissertation, University of Alabama*, Tuscaloosa, AL, 2022.

[7] B. W. Nelson, A. N. Lemmon, B. T. DeBoi and T. J. Freeborn, "Modeling and Validation of Fixture-Induced Error for Impedance Measurements," *IEEE Transactions on Power Electronics,* vol. 68, pp. 129-137, 2019.

[8] B. T. DeBoi, "On the Accuracy of Impedance Measurements and the Influence of Fixturing," in *M.S. thesis, Univ of Alabama*, Tuscaloosa, AL, 2019.

[9] B. T. DeBoi, A. N. Lemmon, B. W. Nelson, C. D. New and D. M. Hudson, "Improved Methodology for Parasitic Characterization of High-Performance Power Modules," *IEEE Transactions on Power Electronics,* vol. 35, pp. 13400-13408, 2020.

[10] B. T. DeBoi, A. N. Lemmon, B. McPherson and B. Passmore, "Improved Methodology for PArasitic Anaylsis of High-Performance Silicon Carbide Power Modules," *IEEE Transactions on Power Electronics,* vol. 37, pp. 12415-12425, 2022.

[11] Keysight Technologies, "Impedance Measurement Handbook, A guide to measurement technology and techniques, 6th Ed," 2016. [Online]. Available: https://www.keysight.com/us/en/assets/7018-06840/application-notes/5950-3000.pdf. [Accessed 16 06 2024].

[12] B. T. DeBoi, A. N. Lemmon and C. D. New, "Analysis of Fixture Design for Impedance Characterization of Multi-Chip Power Modules," in *PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2022.