User Guide **PRD-08613**

CRD-25BDA6512N-K: 25kW Bi-Directional T-Type Inverter User Guide

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This user guide provides an overview of Wolfspeed's CRD-25BDA6512N-K 25kW Bi-Directional T-Type Inverter reference design including key system specifications, system design, hardware setup and test procedure, and test results. CRD-25BDA6512N-K is designed with 25mΩ 650V and 32mΩ 1200V SiC MOSFETs. Utilizing SiC MOSFETs in this topology for solar PV inverters, uninterruptible power supplies (UPS), and other similar applications may boost system efficiency and power density compared to Si-based solutions.

Contents

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CAUTION

PLEASE CAREFULLY REVIEW THE FOLLOWING PAGES, AS THEY CONTAIN IMPORTANT INFORMATION REGARDING THE HAZARDS AND SAFE OPERATING REQUIREMENTS RELATED TO THE HANDLING AND USE OF THIS BOARD

警告

请认真阅读以下内容，因为其中包含了处理和使用本板子有关的危险和安全操作要求方面的重要信息。

警告

ボードの使用、危険の対応、そして安全に操作する要求などの大切な情報を含むので、以下の内容をよく読んでください。

CAUTION

DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE BOARD. THERE CAN BE VERY HIGH VOLTAGES PRESENT ON THIS EVALUATION BOARD WHEN CONNECTED TO AN ELECTRICAL SOURCE, AND SOME COMPONENTS ON THIS BOARD CAN REACH TEMPERATURES ABOVE 50˚ CELSIUS. FURTHER, THESE CONDITIONS WILL CONTINUE FOR A SHORT TIME AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED.

Please ensure that appropriate safety procedures are followed when operating this board, as any of the following can occur if you handle or use this board without following proper safety precautions:

- Death
- Serious injury
- Electrocution
- Electrical shock
- Electrical burns
- Severe heat burns

You must read this document in its entirety before operating this board. It is not necessary for you to touch the board while it is energized. All test and measurement probes or attachments must be attached before the board is energized. You must never leave this board unattended or handle it when energized, and you must always ensure that all bulk capacitors have completely discharged prior to handling the board. Do not change the devices to be tested until the board is disconnected from the electrical source and the bulk capacitors have fully discharged.

警告

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操作板子时应确保遵守正确的安全规程，否则可能会出现下列危险：

- 死亡
- 严重伤害
- 触电
- 电击
- 电灼伤
- 严重的热烧伤

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ボードを操作するとき、正確な安全ルールを守るのを確保すべきです。さもないと、以下の危険がある可能性があります:

- 死亡
- 重症
- 感電
- 電撃
- 電気の火傷
- 厳しい火傷

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1. Introduction

This user guide overviews the design theory, schematic, artwork and test setup necessary to evaluate Wolfspeed's CRD25BDA6512N-K, 25KW Bi-Directional T-Type Inverter for solar inverters, uninterruptible power supplies (UPS), and similar applications. In conjunction with this user guide, the complete suite of reference design files including schematics, PCB layout, Gerber files, BOM, and firmware are available for download from the CRD-25BDA6512N-K product page on Wolfspeed's website.

The CRD-25BDA6512N-K is the inverter stage of the solar PV architecture connected to the AC grid based upon Wolfspeed's 3rd generation SiC MOSFETs - C3M0032120K (1200V, 32mΩ, TO-247-4) and C3M0025065K (650V, 25mΩ, TO-247-4). Included on this single PCB solution is a DC-link bus capacitance with low-inductance power planes, gate drivers, current and voltage sensing, thermal management, various control peripherals and output LC filter. The converter is a bi-directional design, and therefore can operate in inverter mode providing a 3-phase balanced AC voltage on the output when a DC voltage is supplied as input and can operate in PFC mode providing a DC voltage output when a 3-phase AC voltage is supplied at 3-phase input side.

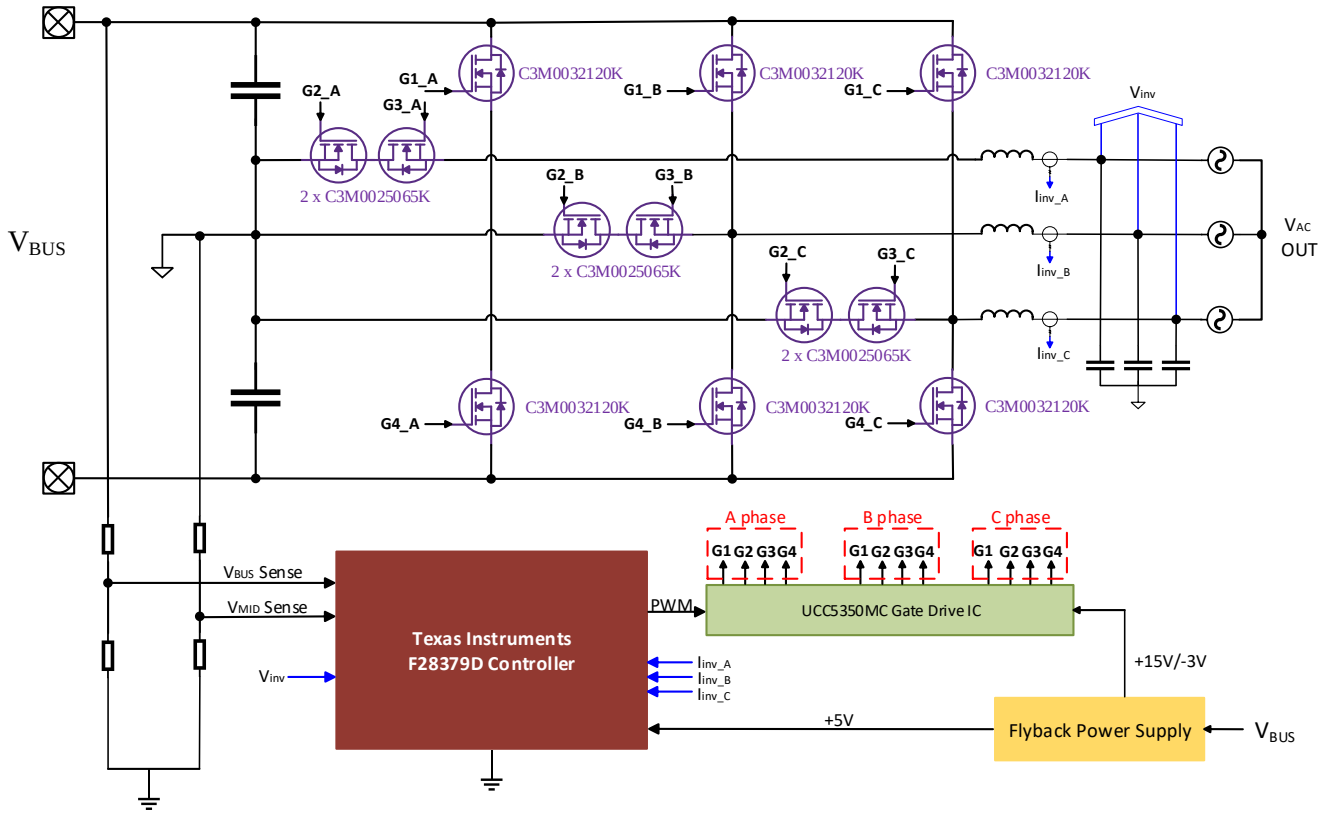


Figure 1: Block Diagram of Wolfspeed's CRD25BDA6512N-K, 25KW Bi-Directional T-Type Inverter

The output power fluctuation of renewable energy sources and increasing power demand on the electric grid bought by the EV transformation puts increased stress onto the existing grid. A bi-directional converter is crucial

to help manage the grid since it is able transfer energy between the renewable energy source, the storage battery (which can include an EV battery), and the electric grid depending on the demand.

For the inverter stage in a bi-directional system, the two-level three-phase inverter is very popular due to its simplicity and ease of control. Since there are only two voltage levels, two-level inverters have relatively higher output THD. The solar industry's move towards higher bus voltages of 1000V or 1500V to reduce the current flowing in the circuit poses a major challenge in the use of two-level inverters due to the inverter's THD at higher voltages. Multilevel converters help to solve this problem of high THD by employing multiple input voltage levels and can operate at higher switching frequencies, higher voltages, and higher power without compromising on efficiency [2]. This also helps to reduce the size of the system because a smaller EMI filter may be utilized. A T-type converter has a simple structure and lower cost compared to other multi-level topologies due to a lesser number of power devices than other multi-level topologies like the I-type and active-NPC.

Utilization of SiC MOSFETs in T-type inverters can improve efficiency and power density [3]. This design shows the SiC MOSFETs switching at a 60kHz switching frequency to achieve a power density of > 6kW/L while still maintaining a peak efficiency of >99%.

2. Description

The CRD-25BDA6512N-K reference design board uses Wolfspeed's 3rd generation SiC MOSFETs - C3M0032120K (1200V, 32mΩ, TO-247-4) in the high-side and low-side switch positions of all three phases and two C3M0025065K (650V, 25mΩ, TO-247-4) in the T-side position of all three phases.

In inverter mode, this board can be tested by using DC source at the input and 3-phase resistive load at the output. This design uses third harmonic injection pulse width modulation (THI PWM) technique for wide input voltage range in inverter mode. This unit has not been tested with a grid –connection, and a grid-connection algorithm is not tested in the firmware currently. In PFC mode, this board can be tested using a 3-phase AC source at the input and a DC resistive or E-load in constant R mode at the output.

The firmware is built and loaded into the control card using Texas Instrument's Code Composer Studio integrated development environment (IDE). There is no GUI for this design. The details of using the firmware in CCS are shared in Hardware Testing Section 4.2.

2.1 Key Electrical Specifications

Table 1: Specifications of Wolfspeed's CRD-25BDA6512N-K, 25kW Bi-Directional T-Type Inverter

Parameter		Test Conditions	Min.	Nom.	Max.	Units
Inverter DC Input Characteristics						
$V_{IN(DC)}$	Input voltage		670	800	900	V_{rms}
f_{sw}	Switching frequency			60		kHz
PFC DC Output Characteristics						
$V_{out(DC)}$	Input voltage		670	800	900*	V_{rms}
f_{sw}	Switching frequency			60		kHz
AC Side Input/Output Characteristics						
$V_{OUT(AC)}$	Output L-L RMS voltage		380	400	480*	V

$I_{OUT(RMS)}$	Output RMS current	V_{IN} = 800V, P_{OUT} = 25kW		36		A
$P_{OUT\ max}$	Output Power				25000	W
f_{ac}	Output Line Frequency			50/60		Hz
DC-AC System Characteristics						
η_{peak}	Peak efficiency	V_{IN} = 800V, V_{OUT} = 400$V_{L\text{-}L\ RMS}$, I_{OUT} = 40% of $I_{OUT(nom)}$		99%		
$\eta_{full\ load}$	Full load efficiency	V_{IN} = 800V, V_{OUT} = 400 $V_{L\text{-}L\ RMS}$, I_{OUT} = 100% of $I_{OUT(nom)}$		98.5%		
AC-DC System Characteristics						
η_{peak}	Peak efficiency	V_{IN} = 480 $V_{L\text{-}L\ RMS}$, V_{OUT} = 800V, I_{OUT} = 50% of $I_{OUT(nom)}$		99.25%		
η_{peak}	Peak efficiency	V_{IN} = 400 $V_{L\text{-}L\ RMS}$, V_{OUT} = 800V, I_{OUT} = 50% of $I_{OUT(nom)}$		99%		
$\eta_{full\ load}$	Full load efficiency			98.5%		
Mechanical						
	Dimensions	Width Length Component height		235 320 50		mm
*Output voltage is derated at low-line input voltage						

2.2 Applications

The primary applications for Wolfspeed's CRD-25BDA6512N-K reference design board are solar inverters, uninterruptible power supplies (UPS), fast charging, industrial power supplies, and other energy storage systems. Using a DC input from the solar panel array, this design provides a non-isolated AC output that can supply power to various commercial/residential loads or to the AC grid.

2.3 Features

Some of the features of Wolfspeed's CRD-25BDA6512N-K reference design board are listed below:

- Bi-directional operation with 25kW output in both power flow modes
- Peak efficiency > 99%
- Power density > 6kW/L
- Third Harmonic Injection Pulse Width Modulation (THI PWM) for inverter mode
- Protection functions listed in Table 3
- Programmable switching frequency from 47 to 60kHz

- Electrical performance of the inverter can also be evaluated in open-loop

3. System Design

3.1 Topology Selection

A T-type NPC inverter is a multi-level inverter for 3-phase converters. For an 800V DC bus system, the main leg devices must block the full DC link voltage and therefore must be 1200V rated devices as shown in figure 2. The side bi-directional devices only need to block half the DC link voltage and are therefore 650V rated devices. The bi-directional switch can be implemented in either a common-drain configuration or a common-source configuration. A common-drain configuration is chosen for CRD-25BDA6512N-K due to being able to use two fewer gate bias power supplies and saving cost and space on the board, more details of which are shared in Section 4.

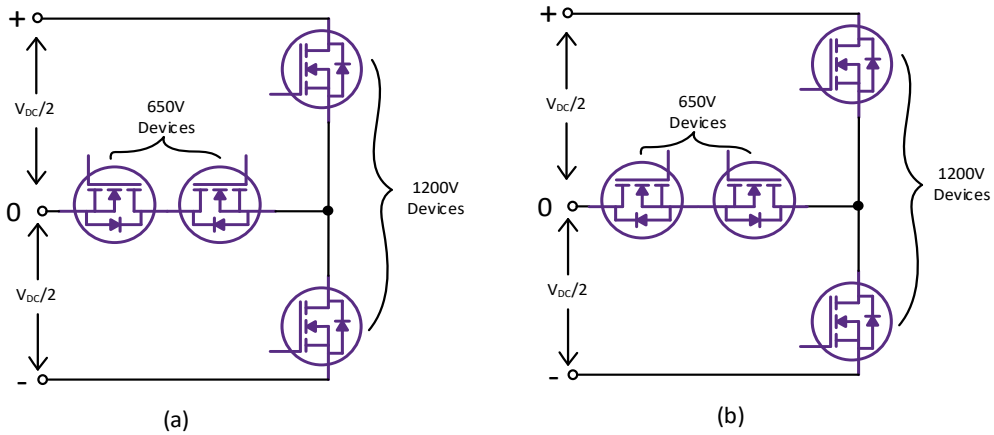


Figure 2: Single leg of the T-type Inverter topology (a) Bi-directional switch Common-Drain configuration (b) Bi-directional switch Common-Source configuration

For a single phase of the T-type inverter topology, three voltage states are possible: DC+, DC- and 0V. As a three-level topology, it exhibits good total harmonic distortion (THD) performance, allowing for smaller output inductors. With fewer components and superior conduction losses compared to NPC topology, TNPC was selected for the CRD-25BDA6512N-K reference design board.

3.2 MOSFET Selection

Traditional switching devices like Si IGBT technology have low “on-state” static losses but have slow switching performance and therefore much higher dynamic or switching losses. This limits their application to low switching frequencies which require bulky and large magnetics. SiC MOSFETs can switch much faster than Si IGBTs and therefore have lower switching losses. Table 2 compares the power losses for SiC MOSFETs and Si IGBTs in 25kW T-type inverter simulation.

Table 2: Comparing power loss for SiC MOSFET and Si IGBT at 25kW power

		Inverter Mode		*PFC Mode*	
Power Device		**DC-link MOSFET:** 32mΩ 1200V SiC **Side MOSFET:** 25mΩ 650V SiC	**DC-link IGBT:** 50A 1200V Si **Side IGBT:** 50A 650V Si	**DC-link MOSFET:** 32mΩ 1200V SiC **Side MOSFET:** 25mΩ 650V SiC	**DC-link IGBT:** 50A 1200V Si **Side IGBT:** 50A 650V Si
Switching Frequency		60kHz	24kHz	60kHz	24kHz
Heatsink Temperature		85°C	85°C	85°C	85°C
$R_{th,ch}$		0.5 °C/W	0.5 °C/W	0.5 °C/W	0.5 °C/W
Efficiency*		**98.9%**	**98.85%**	**99.06%**	**98.65%**
DC-Link MOSFET	**Switching Losses**	75.79 W	127.14 W	0 W	0 W
	Conduction Losses	129.17 W	104.16 W	115.86 W	138.55 W
	Total Losses	204.96 W	231.3 W	115.86 W	138.55 W
Side MOSFET	**Switching Losses**	0 W	0 W	50.16 W	97.44 W
	Conduction Losses	70.1 W	55.5 W	67.34 W	99.13 W
	Total Losses	70.1 W	55.5 W	117.5 W	196.6 W
Total Losses		275.06 W	286.8	233.36 W	335.12W
Tj of DC-Link Device		134.9 °C	134.7 °C	114.3 °C	115.1 °C
Tj of Side Device		97.7 °C	91.8 °C	109.1 °C	125.4 °C
** Efficiency is for power devices only. EMI filter, PFC choke, Aux power and control circuit are not included*					

From Table 2, it is noted that even though the switching frequency for Si IGBTs is 24kHz, which is much lower than that of SiC MOSFETs, the power loss for both inverter and PFC modes are higher than that of SiC MOSFETs. This clearly shows that the inverter will have much higher efficiency with SiC MOSFETs even after including the system magnetics, which will be smaller with SiC. Fig. 3 shows a weight and size comparison between the two chokes that would be needed for switching frequency of 60kHz for SiC and 24kHz for IGBTs. A SiC solution provides higher efficiency, lower magnetics cost, and reduced size and weight, and is therefore a higher-power-density solution for bi-directional grid-tied inverters.

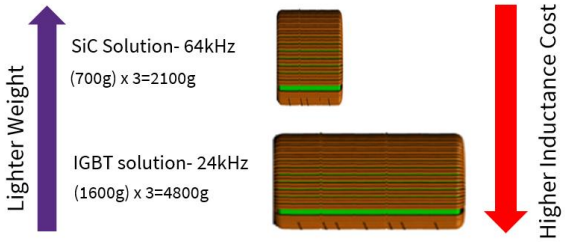


Figure 3: Weight of PFC choke comparison for SiC and IGBT switching frequency

3.3 Gate Driver IC

For the gate driver IC, the design uses the Texas Instruments UCC5350MC isolated gate driver, which has a sink/source drive strength of ±5 A. The selected gate driver IC includes an active Miller clamp. The active Miller-clamp function helps to prevent a false turn-on of the power switches caused by Miller current. The Miller-clamping function is implemented by adding a low-impedance path between the gate of the power device and the VEE2 supply. Miller current sinks through the clamp pin, which clamps the gate voltage to be lower than the turn-on threshold value for the gate. The gate driver IC also includes other built-in functionalities such as undervoltage lockout, low propagation delay, and high common-mode transient immunity. More details about the built-in features of the gate driver IC can be found in the Texas Instruments UCC5350MC datasheet.

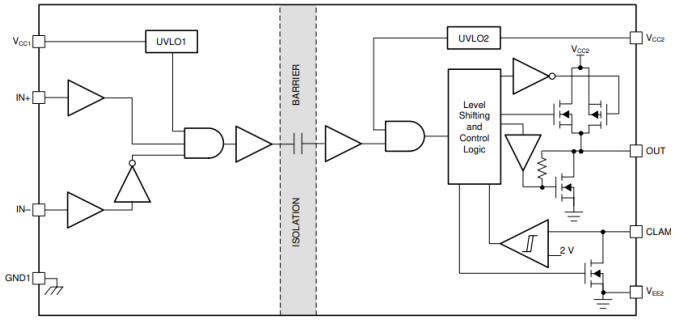


Figure 4: UCC5350MC functional block diagram

3.4 LC Filter Design

The EMI filter is intended to remove any high-frequency noise propagating to the grid and address the issue of common-mode noise. A standard procedure to eliminate differential noise in grid-connected systems is incorporating an LC filter [4]-[6] topology shown in figure 5. Proper damping needs to be applied to ensure resonant peak is kept under control. A review of various damping topologies for the LC filter has been evaluated in [7]. Following the step-by-step methodology provided in [4], the LC filter component sizes have been determined. The input parameters utilized for this calculation are:

- P_{out}= 25kW
- F_{ac}= 50Hz
- F_{sw}= 64kHz
- E_n= 230V

This yields the following parameters for the L_{INV} and C_{DM}:

- L_{INV} = 102uH
- C_{DM}= 24.9 uF

Even though using this calculation and methodology derives a higher C_{DM}, only 10uF is used as the goal of this filter is to provide only nominal noise suppression and not be in compliance with any EMI standards. A separate

EMI filter board that is an add-on to the CRD-25BDA6512N-K board has been designed and optimized to IEC 61000-6-3, standard for emissions. The user can request more details about this on Wolfspeed Power Applications Forum.

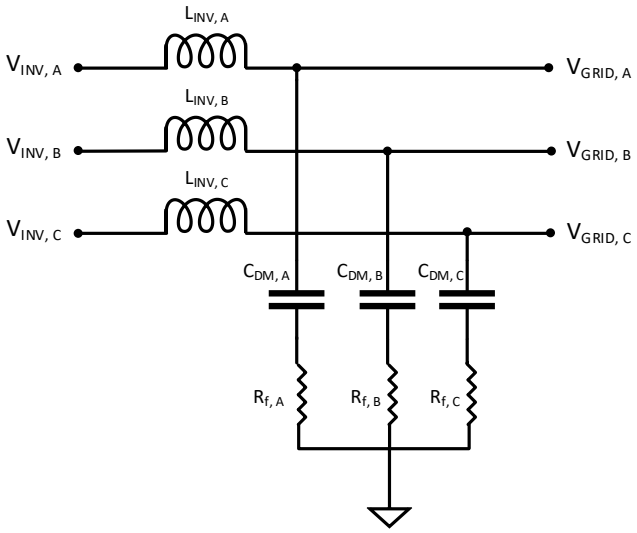


Figure 5: LC filter topology

The inductor design for the selected value is based on the following constraints:

- Height of the component needs to be ≤ 40 mm
- Volume of the inductor needs to be minimized
- Inductor power loss needs to be minimized
- Temperature of the PFC choke needs to be ≤ 120^0C
- No-load inductance is not too high

The area-product method has been utilized to find out if a core is compatible with the design. The eligible cores from the previous step have been run through the design procedure provided by [8]-[9]. A user can request more details about the magnetics design and request a datasheet on Wolfspeed Power Applications Forum.

3.5 Controller Selection

Texas Instruments TMS320F280039C is chosen as the controller IC for this design. It is a member of the C2000™ real-time microcontroller family by Texas Instruments. The user can read more about features of this controller in TMS320F28003x's datasheet.

For simplicity of design, the control card TMDSCNCD280039C is directly used in CRD-25BDA6512N-K. Although the height of this control card is taller than the 40mm specification for this design, the control card can easily be re-designed to lower the height by connecting only the necessary pins used for the design.

3.6 Thermal Design

Power switches of each phase are placed on a heatsink. Forced air cooling is used for this design. As seen from Table 2, in the inverter mode the 1200V switches have more power losses than the 650V switches (and therefore

higher temperature), and vice-versa in PFC mode. Placing these devices on the same heatsink next to each other allows for thermal coupling, providing more area to cool the hotter switch. Figure 6 shows the placement of devices on the heatsink, showing each 1200V and 650V switch placed alternatively for thermal coupling, to minimize the switching node trace and to minimize the gate loop. This design also allows for the same air from the heatsink to flow over to the PFC choke for cooling.

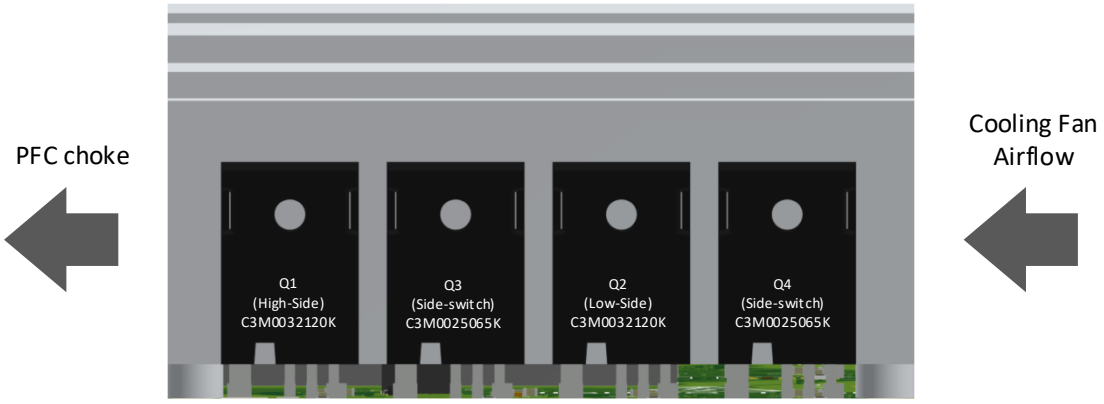


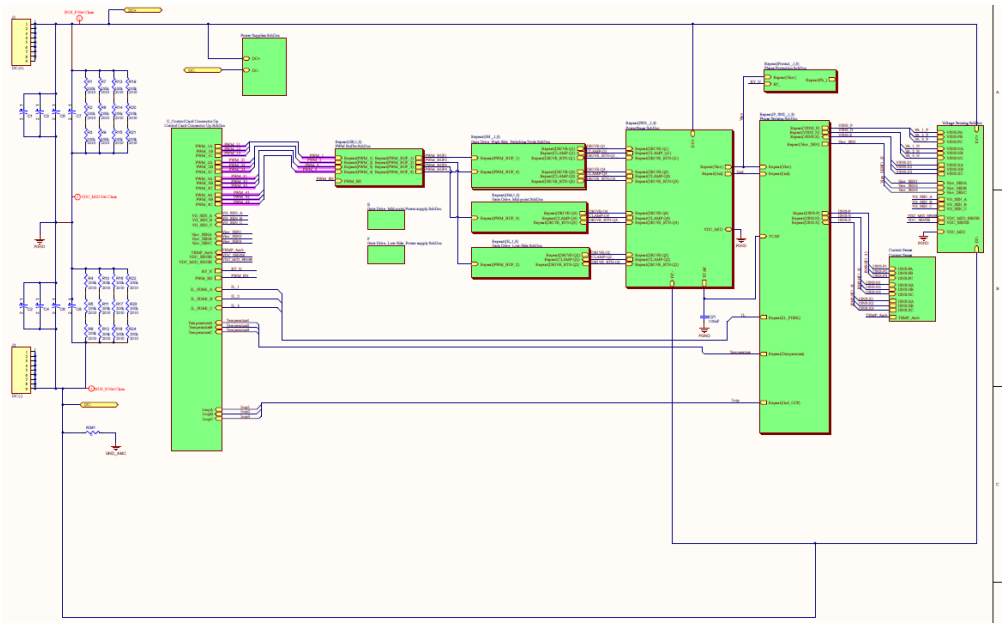
Figure 6: Position of devices on heatsink

AlN ceramics of 1mm width are chosen for the thermal interface material (TIM) for each switch as it provides excellent thermal conductivity. Based on the power loss estimation for each device, the thermal impedance of the MOSFET from junction to case and the thermal impedance of the TIM, analysis is carried out to select the right heatsink offering the optimum thermal impedance to keep the junction temperature of the MOSFET below 135^0C. BOYD 780453B extrusion profile was selected with Max Clip MAX03NG-ND mounting for each switch based on this analysis. A user can refer to the section 3 in Thermal Management of Bottom-Side Cooled Surface Mount Devices and Design Considerations application note to understand more about how these thermal calculations are performed.

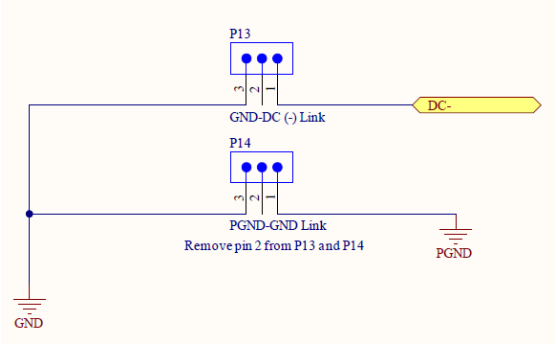
4. Schematics

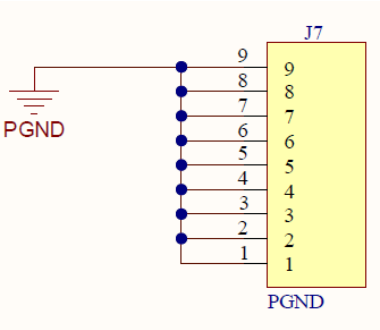
The schematics for this design can be downloaded from CRD-25BDA6512N-K 25kW T-type Inverter Product Page > Download Design files.

Figure 7 (a) shows the top-sheet labelled Power Stage 1.SchDoc. The schematic is set up using multi-sheet feature on Altium where each “repeat” sub-sheet is for similar circuitry for each phase. PGND is the midpoint of the DC-bus voltage. The control GND can be left floating or can be connected to the DC- or midpoint depending on the control strategy employed by the user. For testing this board, the control GND is left floating as shown in Figure 7 (b), i.e., no jumper is placed across P13 or P14. PGND terminal shown in figure 7 (c) is used to interface with an external EMI filter.



(a)





(b) *(c)*

Figure 7: Power Stage 1.SchDoc (a) Repeat Sub-sheets (b) Control Power GND connection (c) Terminal for PGND Mid-point DC

Subsheet PowerStage.SchDoc is the schematic for the MOSFETs, some of their gate drive components, and the LC filter for each phase as shown in figure 8. Each sheet in the .pdf version is sheet numbered x.1, x.2 and x.3 for phase A, B and C respectively where x is the main sheet number for the repeat sheets. The heatsink shown on this sheet is also per-phase. The board comes populated with the jumper to tie to heatsink PGND (DC Mid-point).

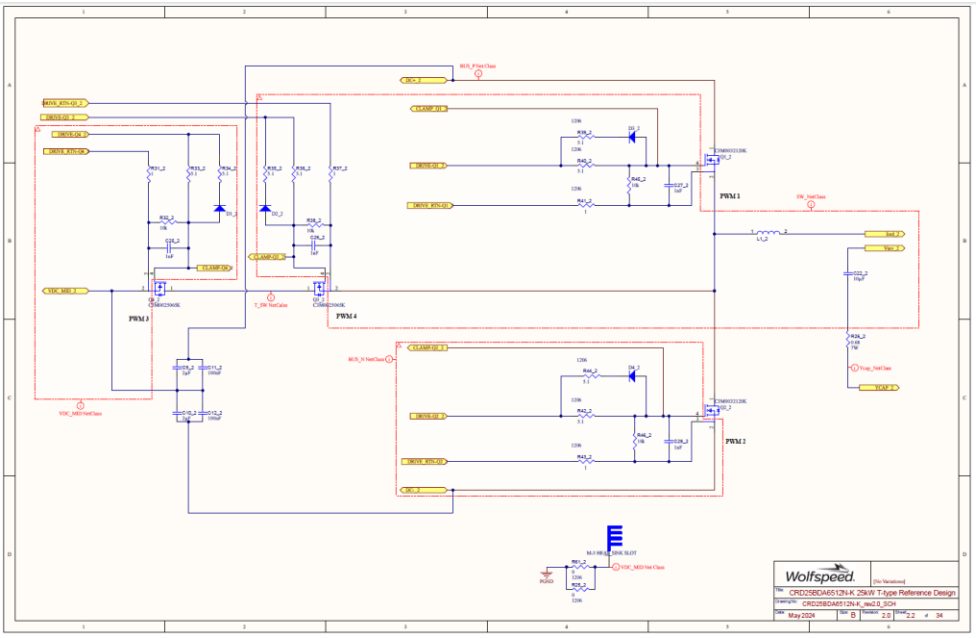


Figure 8: PowerStage.SchDoc

Figure 9 shows subsheet PWM Buffer.SchDoc which is the PWM buffer for all the 4 gate signals per phase.

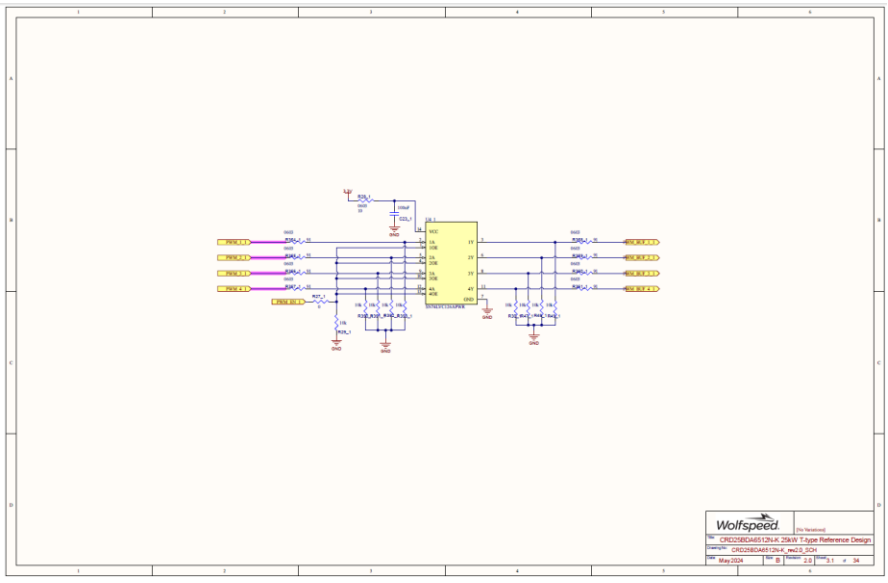


Figure 9: PWM Buffer.SchDoc

The Gate Drive_High-Side_Switching Node.SchDoc shown in figure 10 is also a repeat sheet which shows that gate drive bias supply of +15/-3V for the gate source voltage of the MOSFET is generated using a push-pull circuit with TI's SN6507 push-pull transformer driver IC and 750320528 transformer from Würth Elektronik that offers a low profile. This is a low-cost discrete implementation for generating the gate drive voltage. Using a common-drain design for the 650V side MOSFETs allows the design to use the same supply for the high-side switch (Q1) and one of the side MOSFETs (Q3) that are referenced to the same switching node for each phase.

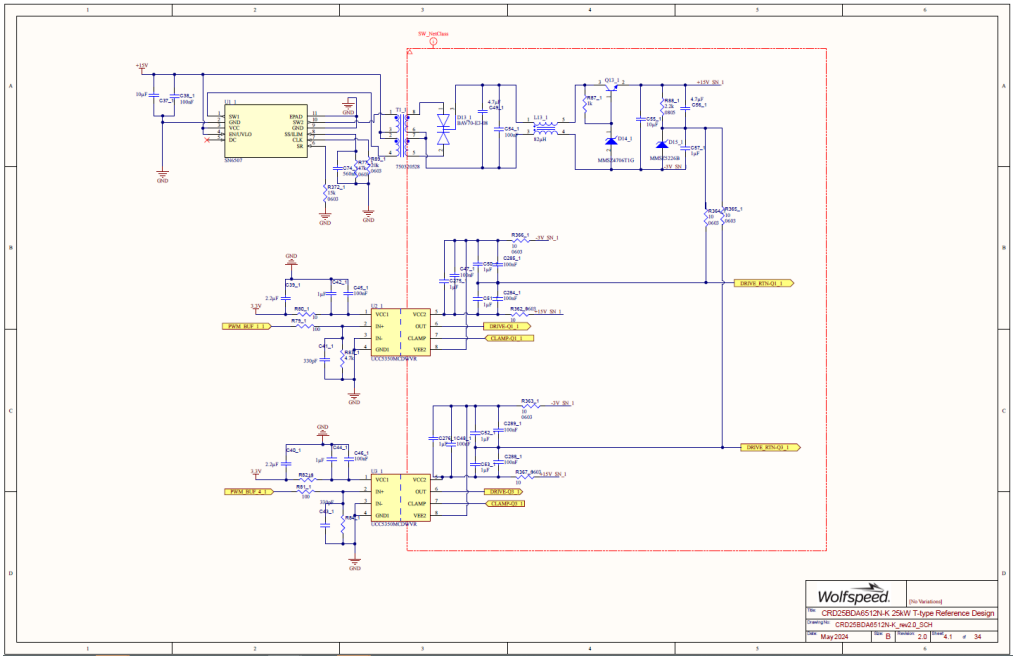


Figure 10: Gate Drive_High-Side_Switching Node.SchDoc

The interwinding capacitance of this transformer for push-pull is ~9pF, which is high and can result in more EMI. For new designs, customers can also consider using LLC topology for bias power supply generation instead of push-pull for a low-cost discrete supply.

Figure 11 and figure 12 show the implementation of gate drive bias power supply and gate driver for all low-side switches (Q2). Gate Drive_Low-Side_Power supply.SchDoc is not a repeat sheet, as the low-side switches of all the phases A, B and C share the same power supply and are referenced to the same DC- node. Gate Drive_Low-Side.SchDoc is a repeat sheet as each low-side switch has its own gate driver IC.

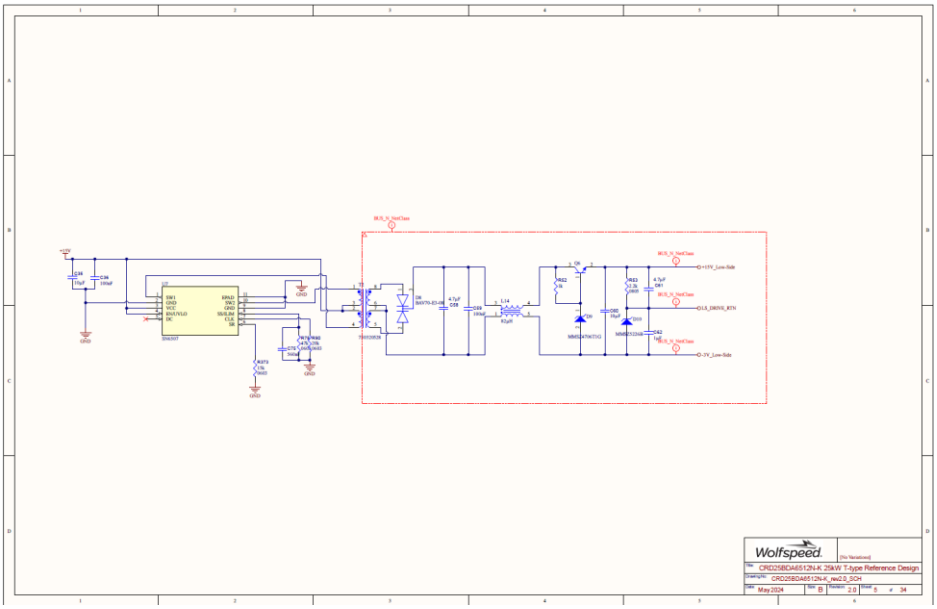


Figure 11: Gate Drive_Low-Side_Power supply.SchDoc

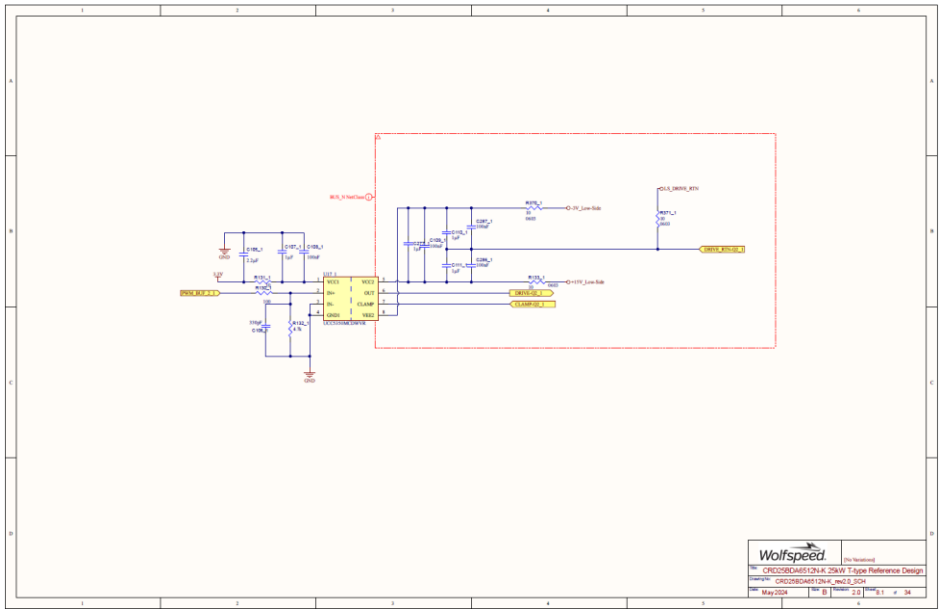


Figure 12: Gate Drive_Low-Side.SchDoc

Figure 13 and figure 14 show the implementation of gate drive bias power supply and gate driver for all the 650V side switches at are referenced to the mid-point (Q4). Gate Drive_Mid-point_Power supply.SchDoc is not a repeat sheet as the 650V side switches of all the phases share the same power supply and are referenced to the same PGND node. Gate Drive_Low-Side.SchDoc is a repeat sheet as each middle-side switch has its own gate driver IC.

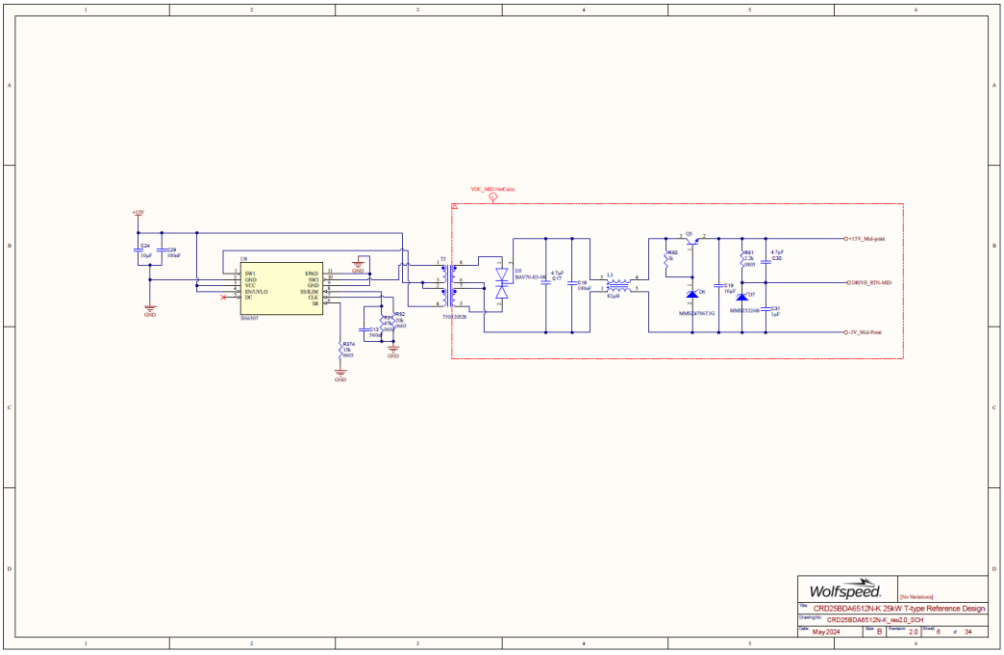


Figure 13: Gate Drive_Mid-point_Power supply.SchDoc

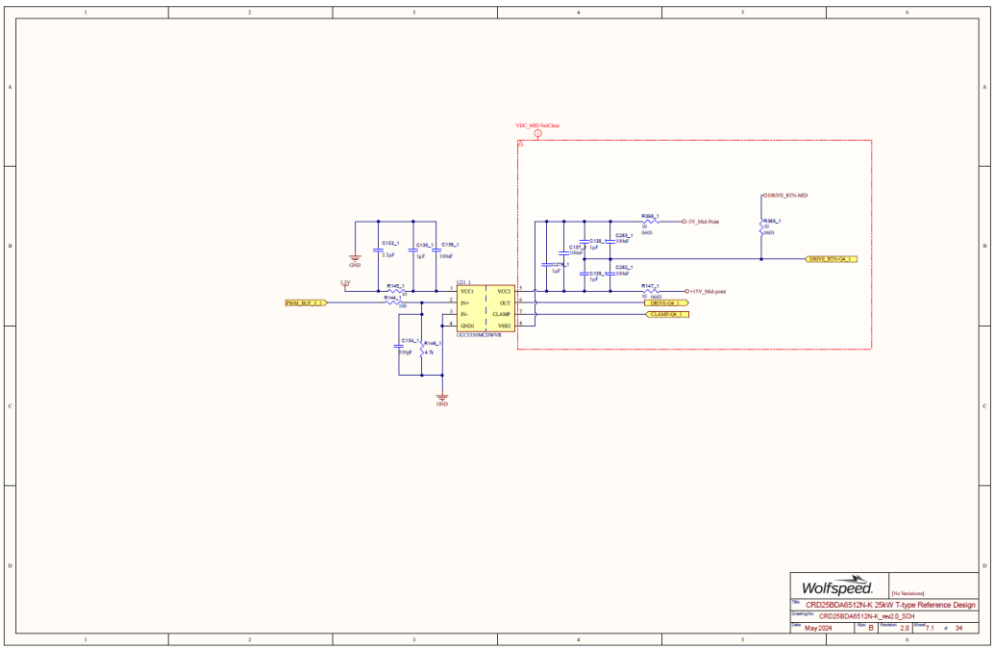


Figure 14: Gate Drive_Mid-point.SchDoc

This approach of common-drain topology for 650V side switches allows the design to use five discrete gate voltage bias power supplies instead of seven, which would be required for a common-source 650V side-switch topology, saving cost and space on the board.

Power Supplies.SchDoc is shown in figure 15. The user has an option to use an external 15V supply to power the control/auxiliary components on the board or use a Wolfspeed auxiliary flyback board that can be provided with the main board on request to generate the isolated 15V.

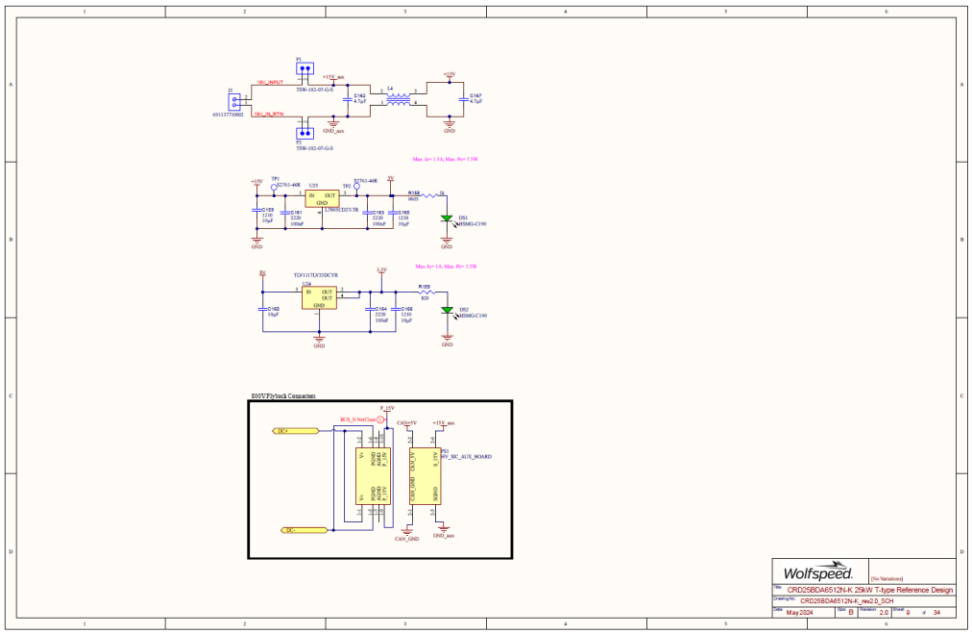


Figure 15: Power Supplies.SchDoc

Voltage Sensing.SchDoc in figure 16 shows the DC input voltage sensing, U5 IC, which is a 4-channel op-amp IC OPA4340UA used for feedback of the output inverter phase voltage sensing, and connector J6, which is used to interface with an external EMI filter in case external VGrid needs to be sensed.

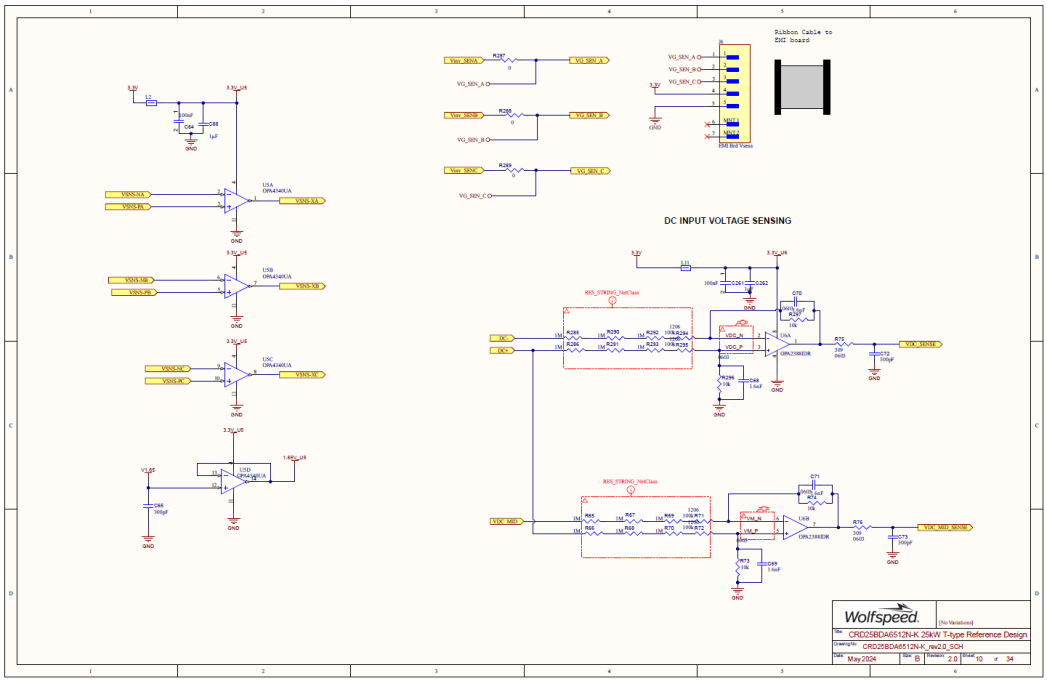


Figure 16: Voltage Sensing.SchDoc

Figure 17 shows Phase Protection.SchDoc is a repeat sheet with the AC line facing relay circuitry and inrush current limiters for each phase.

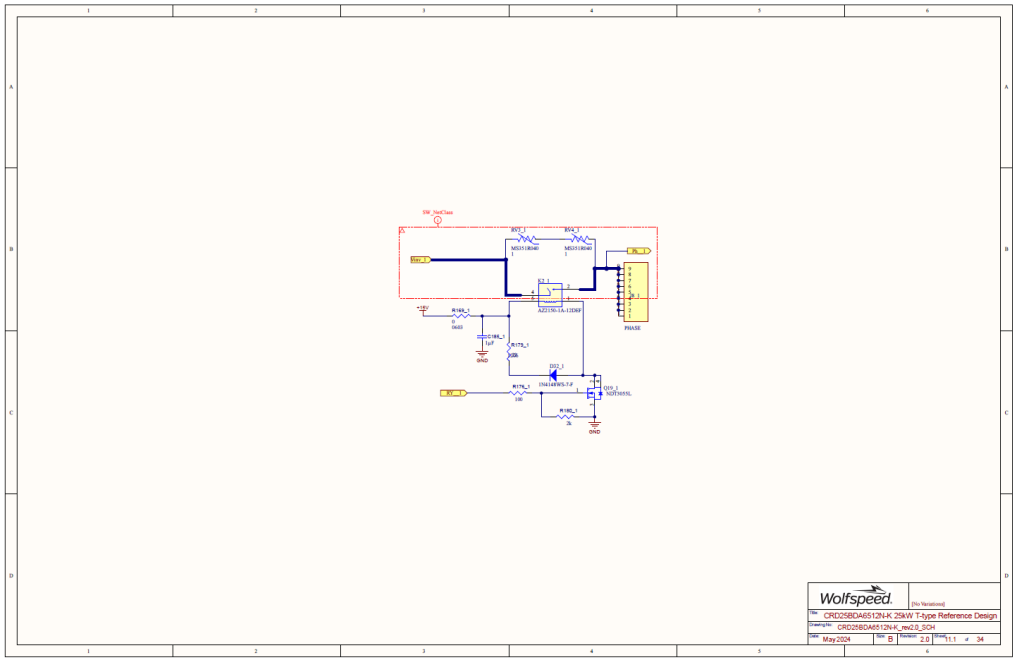


Figure 17: Phase Protection.SchDoc

The Phase Sensing.SchDoc in figure 18 contains the current, phase voltage and temperature sensing for each phase. The current is sensed using a Hall-effect-current-sensing IC ACS733KLATR-65AB-T by Allegro. This IC is capable of sensing AC current where 0A corresponds to 1.65V. Since the current in the Hall IC flows from IP- to IP+ in inverter mode and IP+ to IP- in PFC mode, the current direction is calibrated accordingly in the firmware.

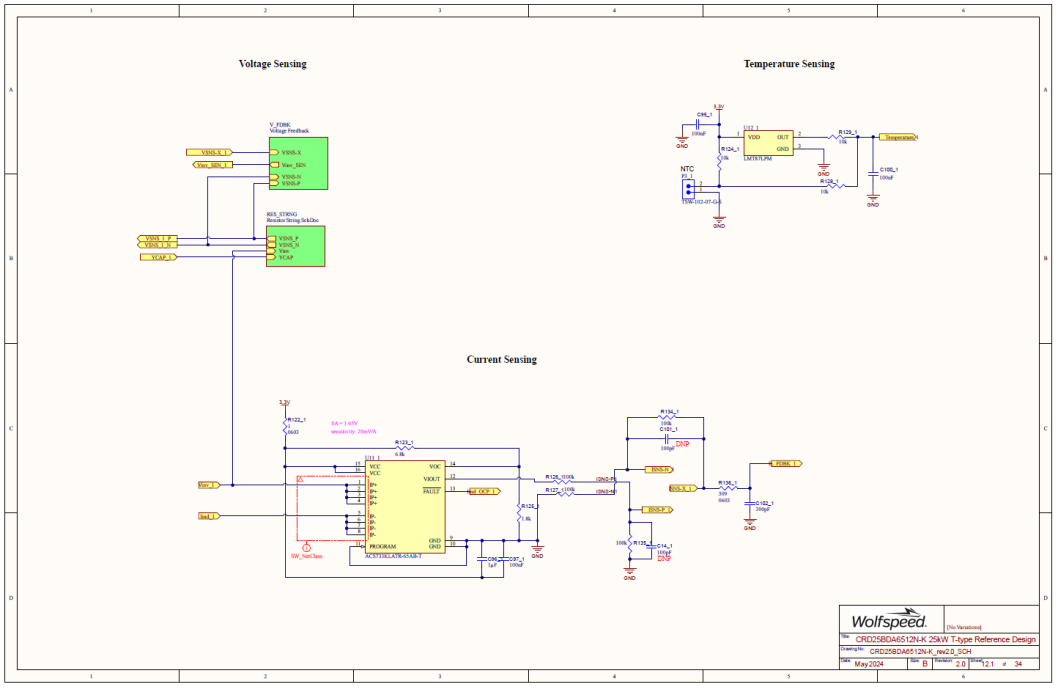
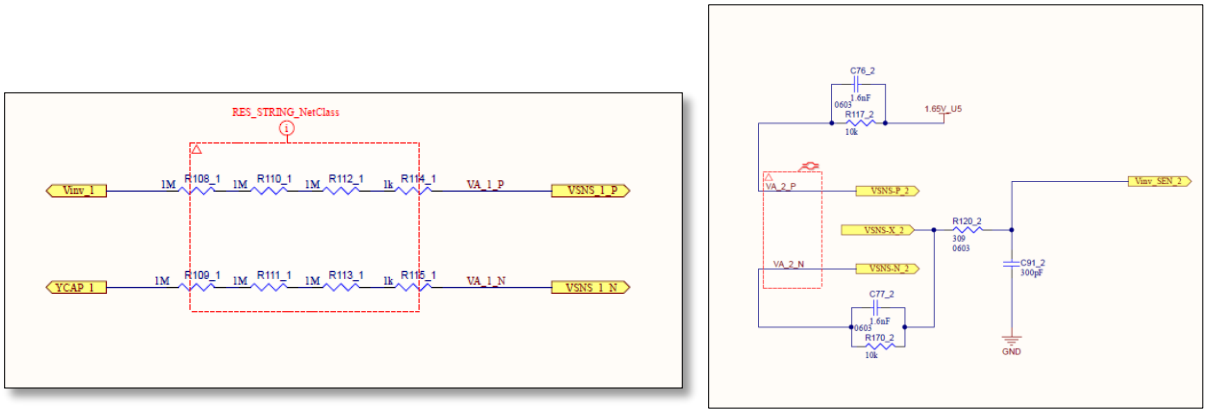


Figure 18: Phase Sensing.SchDoc

The Resistor String.SchDoc and Voltage Feedback.SchDoc make up the circuit that sense AC phase voltage shown in figure 19. They feed into U5 op-amps that are part of the Voltage sensing.SchDoc. Since the op-amp IC has four channels that are used individually for each phase, that IC couldn't be part of the "repeat" sheets as it is the same IC for all phases.



(a) (b)

Figure 19: (a) Resistor String.SchDoc (b) Voltage Feedback.SchDoc

Similarly, Current Sense.SchDoc in figure 20 has U13 which is a 4-channel op-amp IC OPA4340UA and is not a "repeat" sheet as it's the same IC for all the phases and the output from U11 (Phase Sensing.SchDoc) feeds into these op-amp channels.

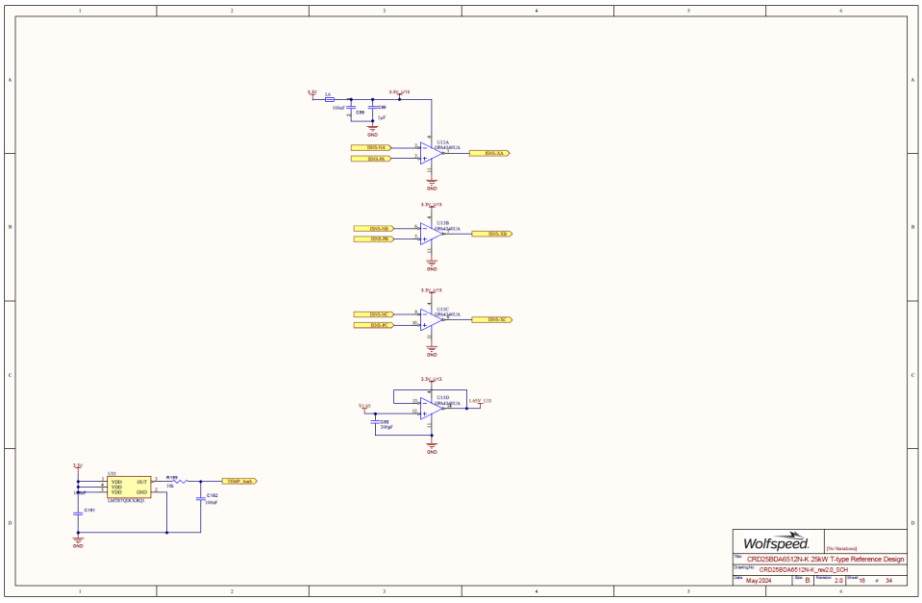


Figure 20: Current Sense.SchDoc

Figure 21 shows the Control Card Connector Up.SchDoc with the connections to control card TMDSCND28039C, the 1.65V generation circuit and CAN communication pins. The CAN communication pins have not been tested but are still placed on the schematic for future improvements to the design.

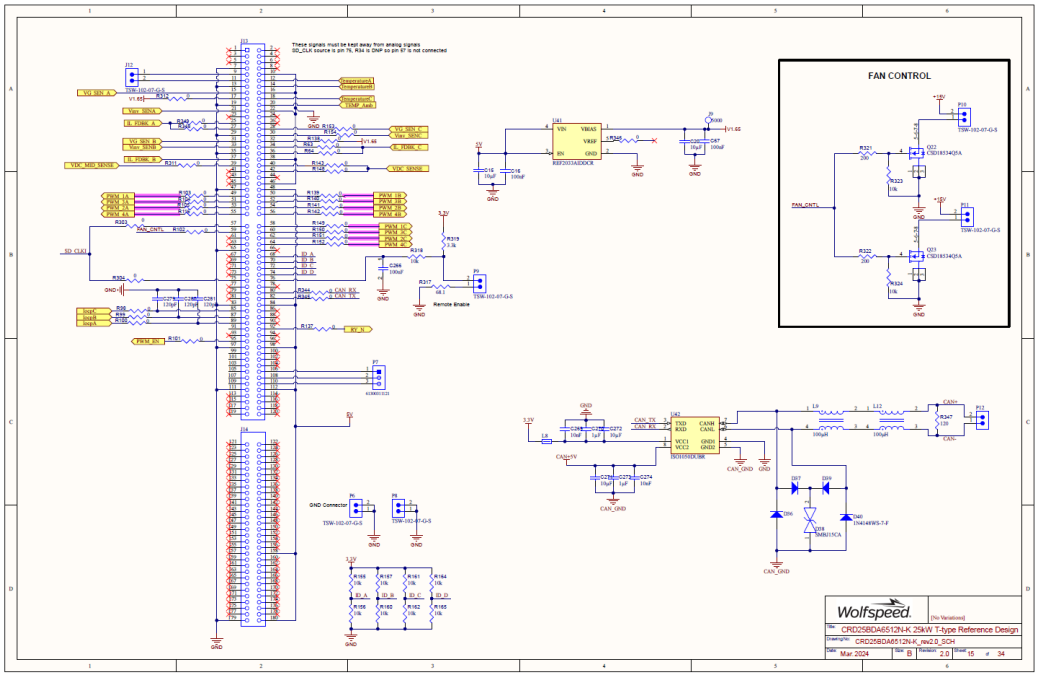


Figure 21: Control Card Connector Up.SchDoc

5. Hardware Set-up & Testing

CAUTION

IT IS NOT NECESSARY FOR YOU TO TOUCH THE BOARD WHILE IT IS ENERGIZED. WHEN DEVICES ARE BEING ATTACHED FOR TESTING, THE BOARD MUST BE DISCONNECTED FROM THE ELECTRICAL SOURCE AND ALL BULK CAPACITORS MUCH BE FULLY DISCHARGED.

SOME COMPONENTS ON THE BOARD REACH TEMPERATURES ABOVE 50^{O} CELSIUS. THESE CONDITIONS WILL CONTINUE AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED. DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE BOARD.

PLEASE ENSURE THAT APPROPRIATE SAFETY PROCEDURES ARE FOLLOWED WHEN OPERATING THIS BOARD AS SERIOUS INJURY, INCLUDING DEATH BY ELECTROCUTION OR SERIOUS INJURY BY ELECTRICAL SHOCK OR ELECTRICAL BURNS, CAN OCCUR IF YOU DO NOT FOLLOW PROPER SAFETY PRECAUTIONS.

警告

通电时不必接触板子。连接器件进行测试时，必须切断板子电源，且大容量电容器必须释放完所有电荷。

板子上一些组件的温度可能超过 50 摄氏度。移除电源后，上述情况可能会短暂持续，直至大容量电容器完全释放电荷。通电时禁止触摸板子，应在大容量电容器完全释放电荷后，再操作电路板。

请确保在操作电路板时已经遵守了正确的安全规程，否则可能会造成严重伤害，包括触电死亡、电击伤害、或电灼伤。

警告

通電している時にボードに接触する必要がありません。設備をつないで試験する時、必ずボードの電源を切ってください。また、大容量のコンデンサーで電力を完全に釈放してください。

ボードのモジュールの温度は 50 度以上になるかもしれません。電源を切った後、上記の状況がしばらく持続する可能性がありますので、大容量のコンデンサーで電力を完全に釈放するまで待ってください。通電している時にボードに接触するのは禁止です。大容量のコンデンサーで電力をまだ完全に釈放していない時、ボードを操作しないでください。

ボードを操作している時、正確な安全ルールを守っているのを確保してください。さもなければ、感電、電撃、厳しい火傷などの死傷が出る可能性があります。

Figure 22 shows the CRD-25BDA6512N-K power board. The input DC power supply is connected to terminals "DC+" and "DC-". The DC-Bus E-caps between DC+ to mid-point (PGND) and DC- to mid-point (PGND) are equally divided across the 2 edges of the board to minimize the commutation loop for all switches. These, along with the high-frequency film capacitors, form the DC Bulk Capacitors.

Each phase is placed linearly in front of the fan. Closest to the airflow is the heatsink and the MOSFET, then the LC filter, then inrush current limiters and relays finally connected to the output terminal for that phase. The four MOSFETs for each phase are positioned in a way that minimizes the switching node trace on the PCB.

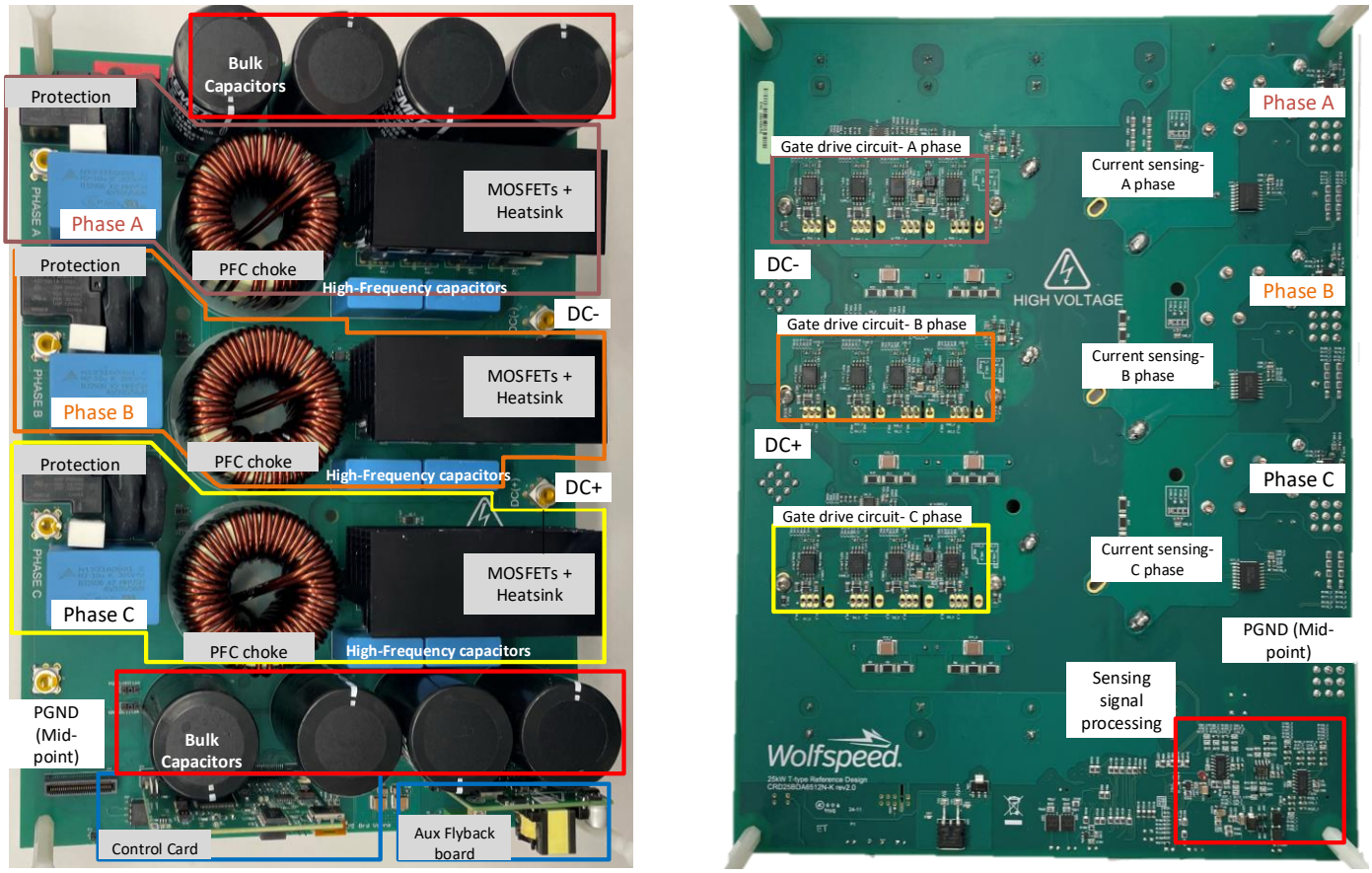


Figure 22: CRD-25BDA6512N-K reference design hardware

5.1 Importing Firmware

To start testing this design, please request the firmware of this design from the CRD-25BDA6512N-K 25kW T-type Inverter Product Page > Request separately > Request Firmware. Save the file to a local directory. To open the project:

1. Install Code Composer Studio (CCS version 10.1 or above)
2. Install C2000Ware DigitalPower SDK package Version 4.04 from Texas Instruments tool page.

3. Open CCS, and create a new workspace

4. Inside CCS, go to File > Open Projects from File System > Import source > Directory and navigate to the firmware folder that you received and saved on your PC > finish. Your CCS window should now look like figure 23.

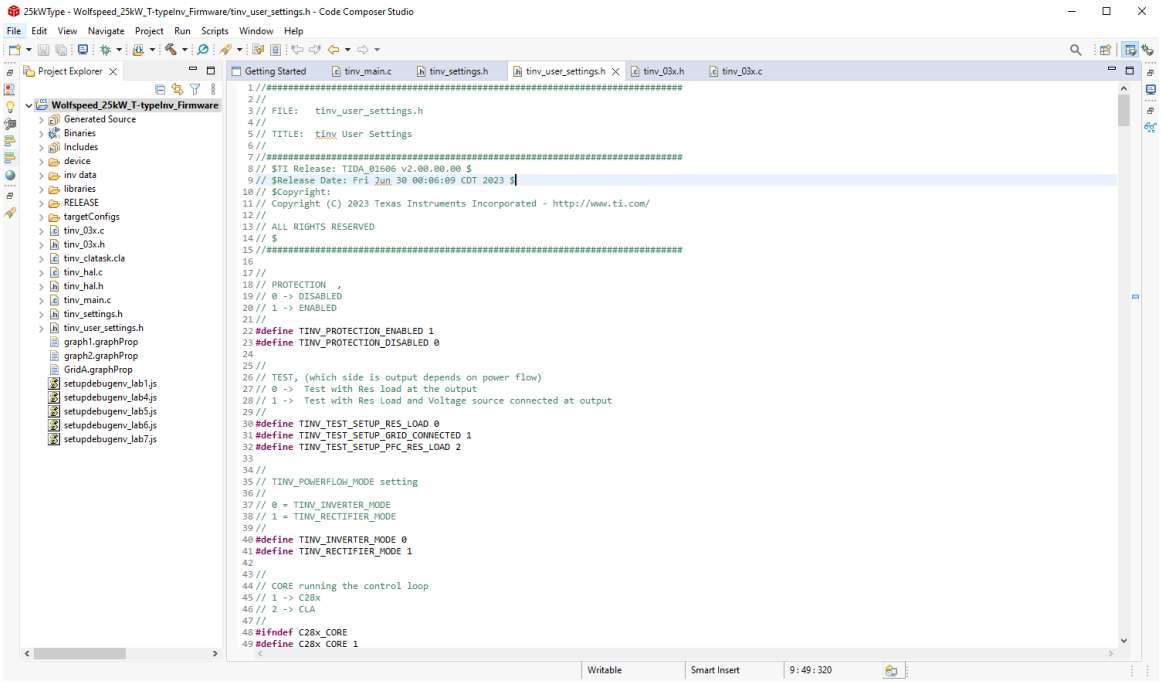


Figure 23: CCS window after importing firmware

5.2 Building, Loading and Debugging the Firmware

To build the project, right-click on the project name and click 'Build Project'. To load the project, first make sure in the Project Explorer the correct target configuration file is set as Active under targetConfigs (*.ccxml file). Then, click Run → Debug to launch a debugging session.

To debug the system one would monitor the variables in the watch/expressions window. To populate this window with the correct variables, click View → Scripting Console to open the scripting console dialog box. On the upper right corner of this console, click on Open and then browse to the "setupdebugenv_lab#X.js" script file located inside the project folder. This will populate the watch window with the appropriate variables needed to debug the system. Enable Continuous Refresh button on the watch window to enable continuous update of values from the controller.

Real-time emulation is a special emulation feature that allows windows within Code Composer Studio to be updated while the MCU is running. This allows graphs and watch views to updated, but also allows the user to change values in watch or memory windows and see the effect of these changes in the system without halting the processor. To enable real-time mode, click  on the top bar of CCS. A message box may appear. If so, select YES to enable debug events.

In different labs, sometimes the measured currents and voltages or control variables need to be verified by viewing the data in the graph window. For this Graph window can be used which in conjunction with a piece of code that runs on the controller can show a snapshot of how the values are being sensed by the controller. The values are logged by the datalogger typically in the slower ISRs. To import the graph into the CCS view, select Tools > Graph > DualTime, and click Import and point to the graph1.GraphProp file inside the project folder. Two graphs will appear in CCS. Click Continuous Refresh on these graphs. A second set of graphs can also be added by importing the graph2.GraphProp file.

You can also refer to TIDA-01606 10-kW, bidirectional three-phase three-level (T-type) inverter and PFC reference design's user guide for more details on each file, ISRs, ADC loading, CPU loading and information on control variables.

5.3 Protections

Table 3 describes over/under voltage protection (OVP/UVP) and over current protection (OCP) functions in the reference design. OCP protection is a one-shot protection that requires a system reset to clear the fault and restart.

A user should not overload the converter out of the SOA (Safe Operation Area). This may damage the unit.

Table 3: Protection Details

Power Signal	Protection	Trip Point	Control Variable
Input/Output DC Voltage	OVP	>900V	TINV_VBUS_OVERVOLT_LIMIT
DC mid-point Voltage	OVP	>450V	TINV_VMID_OVERVOLT_LIMIT
AC Voltage	UVP	<50VAC	TINV_UNIVERSAL_GRID_MIN_VRMS
Phase Current	OCP	40A (rms)	TINV_IINV_TRIP_LIMIT_AMPS

The user is required to set appropriate limits on the supply and load equipment that is used for testing in order to remain within the SOA of the board.

5.4 Hardware Equipment

DC Input Source: The input source must be an adjustable DC source whose output can be adjusted up to the maximum bus voltage desired for testing up to 900V. It must be capable of supplying at least the rated power of the intended load with 10-20% margin.

AC Input Source: The input source must be an adjustable AC source whose output can be adjusted between 220VAC to 277VAC. It must be capable of supplying at least the rated power of the intended load with 10-20% margin.

Output AC Load: A high-voltage 3-phase resistor load bank can be used for PFC mode testing. Each phase must be capable of sinking 38A of load current supplied from the evaluation board whose output can be 220VAC-277VAC at 25kW.

Output DC Load: A programmable high-voltage electronic load or a high-voltage resistor bank may be used. Each must be capable of sinking 39A of load current supplied from the evaluation board whose output can be 650-900VDC/25kW.

Power Meter: A power analyzer from Yokogawa Test and Measurement Corporation (P/N: WT 5000) or any other equivalent power analyzer should be used. An external Hall effect sensor can be used when the output current exceeds the rating of the internal shunt resistor.

Oscilloscope: A 300 MHz or greater digital or analog oscilloscope with 100 MHz or greater isolated differential voltage probes and isolated current probes (i.e., Hall effect) should be used.

Power Supplies: The following power supplies with isolated grounds should be used and must be obtained separately:

1. 15 V @ 1.5 A capability is required to supply the auxiliary power to the board.
2. 12 VDC @ 6 A capability in total is required to power the cooling fans.

To use an external supply to power the auxiliary circuit, the user can connect the 15V to terminal J3 shown in figure 24 and place jumper cap connectors (Ex: Wurth Elektronik PN: 60900213421) on P1 and P2 separately. Alternatively, the user can use a Wolfspeed auxiliary flyback board that can be provided with the main board on request.

Figure 24: Auxiliary Power Supply Connector

External Fans: Cooling fans should be used and must be obtained separately. As shown in Figure 25, at least 3 cooling fans (1 per phase), such as the Delta Electronics Inc. DC12 V/3.30 A fan (P/N: PFR0612XHE) or an equivalent fan, must be used to cool the heatsink for each phase. The air flows through the heatsink to the PFC choke and is enough for cooling the devices and the magnetics. The board is tested placing the MOSFETs and choke side as the bottom as shown Figure 25 so that it creates an air chamber to provide a direction for airflow.

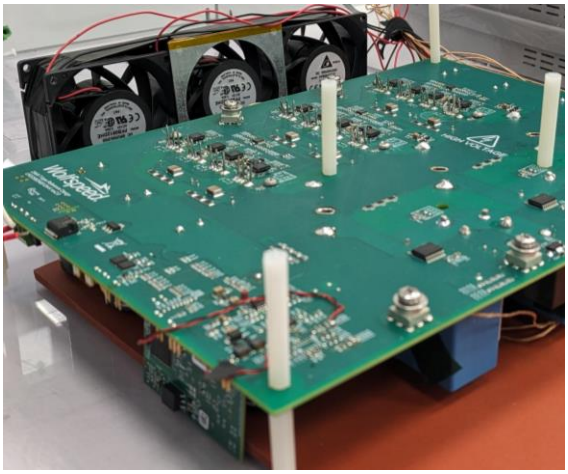


Figure 25: Cooling fan setup for testing

Recommended Wire Gauge: Cable with a minimum AWG #8 wire gauge is recommended to carry the DC input and output currents.

5.5 Testing the Unit in inverter Mode

5.5.1 Recommended Test Setup

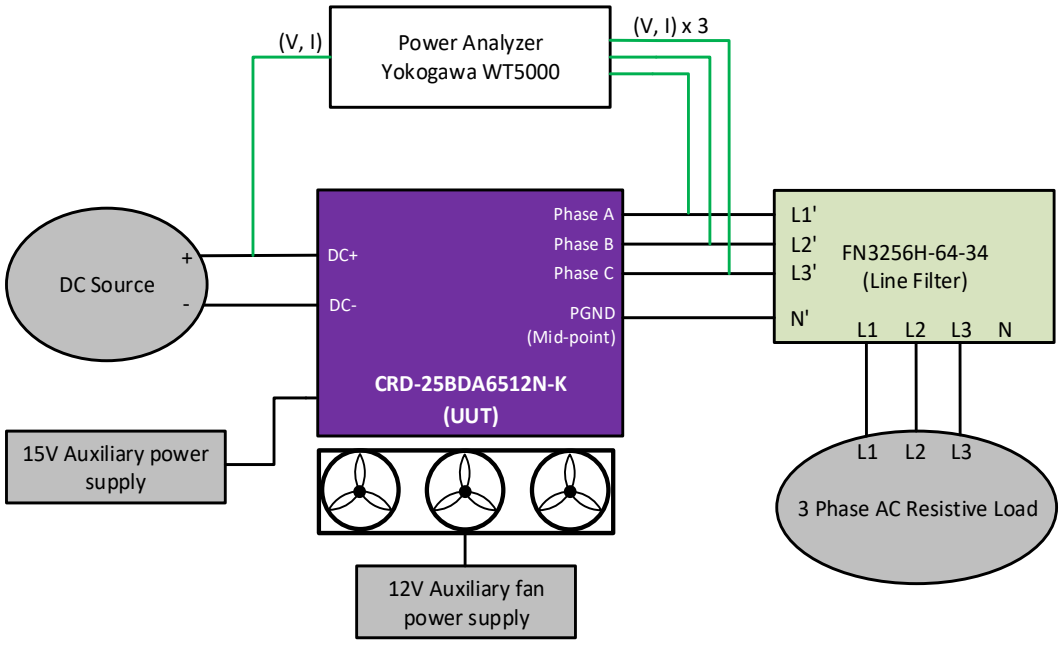


Figure 26: Recommended test setup for inverter testing

5.5.2 Testing the Unit

The user can test the unit in inverter mode with open-loop and closed-loop control. The two labs that the user can test for inverter mode are summarized in Table 4.

Table 4: Inverter testing lab numbers summary

Lab Number	Description	Comments
2	Inverter: Open-Loop	PWM Check, ADC check, Protection Check, Inverter mode DC bus connected and 3-phase resistive load
3	Inverter: Closed Current Loop	Output Current control with DC bus connected and 3-phase resistive load

Important Note: The firmware also has Lab 4 which can be used to test the inverter as a grid-connected system, but this lab not been tested, and the gains have not been optimized on this board. The user is advised not to test the inverter as a grid-connection system.

Lab 2

To check the open-loop inverter operation of the board follow the steps listed below in order:

1. Connect the hardware as shown in figure 26 and turn on the auxiliary supplies
2. In the tinv_settings.h file change the lab number to 2 in line 91

```
#define TINV_LAB 2
```

3. Build, load and debug the code, use the lab2.js file to populate the watch variables in the CCS window
4. In the expressions window, turn on the relay by writing a 1 to TINV_allRelaySet. The auxiliary power supply should draw close to 550 mA
5. Set the TINV_clearPWMTrip = 1, to clear the PWM trip signal. Now the switching action begins. ~~a~~And the user can verify the open-loop PWM on the scope. At this point the auxiliary power supply should draw close to 570 mA
6. Set up an appropriate resistive load around 1 kΩ for the 3-phase load although the inverter mode can be started at no load as well
7. The DC input voltage can now be ramped up to 800V. The sinusoidal output should also be appearing and increasing as the DC voltage is increased
8. TINV_vdInvRef_pu (default value is 0.845) is the modulation index that can be used to vary the AC output of the inverter in open-loop fashion
9. Verify the sensed voltage and current measurement data in the graph window before proceeding to close the current loop in Lab 3.

Only four signals can be viewed in Graph during one debug session. You can change these variables, build the code, and start a debug session again to view different variables.

```
#ifndef __TMS320C28XX_CLA__
        TINV_dVal1 = TINV_iInv_A_sensed_Amps;
```

```
            TINV_dVal2 = TINV_iInv_B_sensed_Amps;
            TINV_dVal3 = TINV_iInv_C_sensed_Amps;
            TINV_dVal4 = TINV_vGrid_C_sensed_Volts;
            DLOG_4CH_run(&TINV_dLog1);
#endif
```

Figure 27 shows a typical waveform from Lab 2, open loop inverter where Channels 2, 3 and 4 are phase A, B and C output phase voltages respectively and Channels 1, 6 and 8 and are phase A, B and C output line currents respectively at 25kW output power.

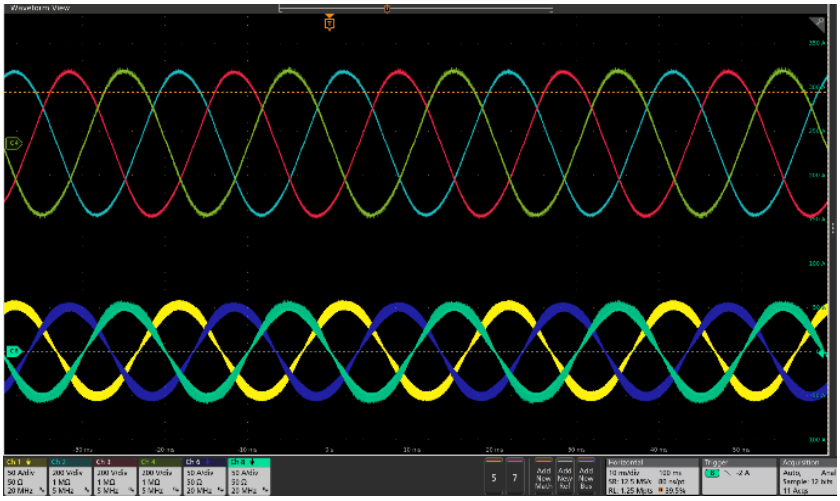


Figure 27: Lab 2 Output phase voltages and line currents

To shut down the system:

1. Reduce the load gradually to no load
2. Turn OFF the DC source, wait until the DC source has fully discharged its output.
3. Turn OFF load after the bus capacitors are fully discharged.
4. Capacitors may remain charged for up to 30 minutes after the circuit is turned OFF if steps 3 or 4 are skipped or compromised**.** They must be allowed to fully discharge before handling the board. Please check the terminal voltages with the power analyzer or a digital multimeter to ensure that the board has fully discharged and is therefore safe to handle.
5. Turn-off the auxiliary power supplies

Lab 3

To check the closed current loop inverter operation of the board, follow the steps listed below in order:

1. Connect the hardware as shown in figure 26 and turn-on the auxiliary supplies
2. In the tinv_settings.h file change the lab number to 3 on line 91

```
#define TINV_LAB 3
```

3. The current compensator coefficients used for running the control loop are shown in the following code. The user does not need to modify these gains, these gains are optimized to work with CRD-25BDA6512N-K

```
#define TINV_GI_PI_KP (((float32_t)0.250000)
#define TINV_GI_PI_KI ((float32_t)0.0075683544)
```

4. Build, load and debug the code, use the lab3.js file to populate the watch variables in the CCS window
5. In the expressions window, turn on the relay by writing a 1 to TINV_allRelaySet. The auxiliary power supply should draw close to 550 mA
6. Set up an appropriate resistive load around 250 Ω to start with although the inverter mode can be started at no load as well
7. It is safe to start the inverter at low voltage first so slowly ramp the DC bus voltage to 400V
8. Set the TINV_clearPWMTrip = 1, to clear the PWM trip signal. Now the switching action begins, and sinusoidal voltages start appearing at the output. At this point the auxiliary power supply should draw close to 570 mA
9. As soon as TINV_clearPWMTrip is set, the TINV_closeGiLoop variable is enabled and closed current loop action begins
10. TINV_idRef_pu is the current command reference and by default it is populated to a value of 0.01 pu at start-up. Slowly vary this to increase the output AC voltage and observe measured current tracks the commanded value.
11. Slowly ramp up the DC voltage to 800V now
12. Slowly increase id_ref_pu to 0.078 pu at 800-V input voltage to improve output power to 3.9kW

Figure 28 shows a typical waveform from Lab 3, closed current loop inverter where Channels 2, 3 and 4 are phase A, B and C output phase voltages respectively and Channels 1, 5 and 6 and are phase A, B and C output line currents respectively at 25kW output power.

Figure 28: Lab 3 Output line-line voltages and line currents

To shut down the system:

1. Decrease id_ref_pu to reduce the current and output voltage while slowly decreasing the DC voltage
2. Turn OFF the DC source, wait until the DC source has fully discharged its output.
3. Turn OFF load after the bus capacitors are fully discharged.
4. Capacitors may remain charged for up to 30 minutes after the circuit is turned OFF if steps 2 or 3 are skipped or compromised. They must be allowed to fully discharge before handling the board. Please

check the terminal voltages with the power analyzer or a digital multimeter to ensure that the board has fully discharged and is therefore safe to handle.

5. Turn off the auxiliary power supplies.

5.6 Test the unit in PFC mode

5.6.1 Recommended Test Setup

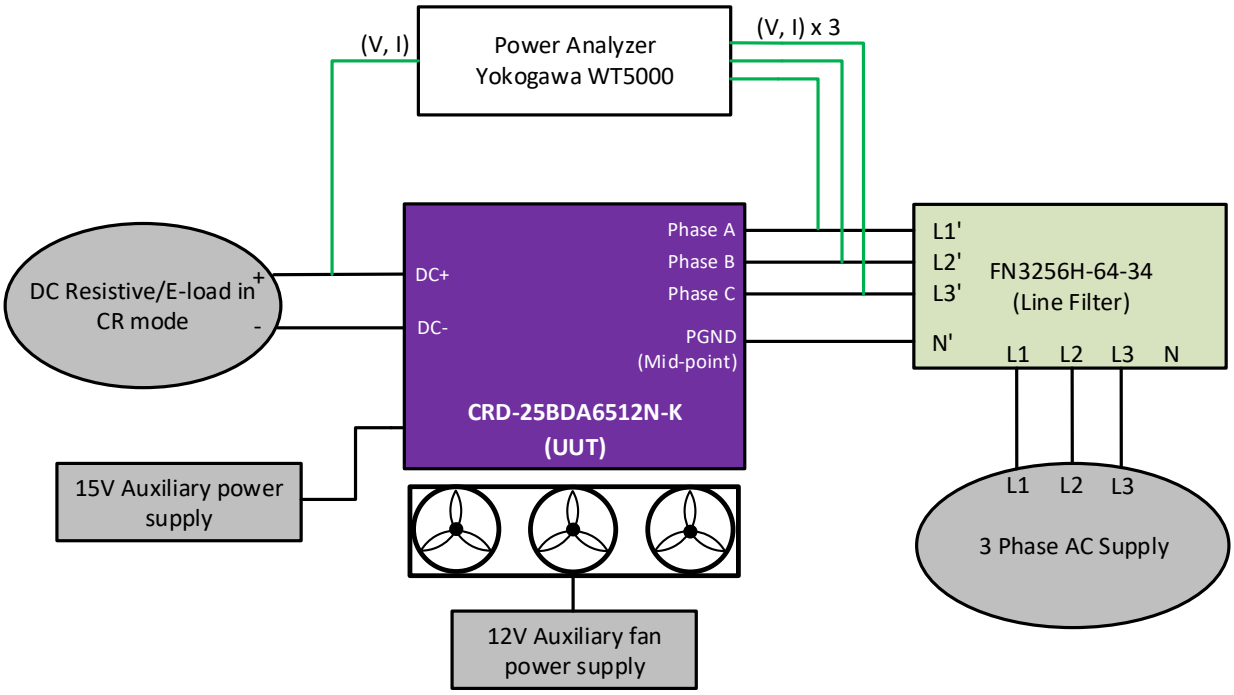


Figure 29: Recommended test set-up for PFC testing

5.6.2 Testing the unit

The user can test the unit in PFC mode with open-loop and closed-loop control. The three labs that the user can test for inverter mode are summarized in Table 5.

Table 5: PFC testing lab numbers summary

Lab Number	Description	Comments
5	PFC: Open-Loop	Check if phase sequence from AC source is correct and PLL is locking
6	PFC: Closed current loop	Output Current control with AC source connected and DC Electronic load in CR mode

7	PFC: Closed voltage and current loop	Output voltage control with AC source connected and DC Electronic load in CR mode

Lab 5

To check the PLL locking in open-loop PFC, follow the steps listed below in order:

1. Connect the hardware as shown in figure 29 and turn on the auxiliary supplies
2. In the tinv_settings.h file change the lab number to 5 on line 91

```
#define TINV_LAB 5
```

3. Make sure the variables for datalogger/graph for lab 5 are:

```
#ifndef __TMS320C28XX_CLA__
   TINV_dVal1 = TINV_vGrid_A_sensed_pu;
   TINV_dVal2 = TINV_angleSPLL_radians / (float32_t)(2.0f * TINV_PI);
   TINV_dVal3 = TINV_iGrid_A_sensed_pu;
   TINV_dVal4 = TINV_iGrid_B_sensed_pu;
   DLOG_4CH_run(&TINV_dLog1);
#endif
```

4. Make sure the grid frequency is specified correctly, the default F_{ac} specified is 60Hz. It can be changed in tinv_settings.h file:

```
#define TINV_AC_FREQ_HZ ((float32_t)60)
```

5. Build, load and debug the code, use the lab5.js file to populate the watch variables in the CCS window
6. Connect suitable E-load in CR mode of about 2kΩ. Make sure to use a high load resistance otherwise can lead to high inrush currents triggering the overcurrent flag
7. Apply 50 V_{RMS} AC voltage to the three phase terminals
8. Immediately turn on the relay by writing a 1 to TINV_allRelaySet. Rectified voltage should now start to appear across the DC terminals
9. In the graph window, verify if the PLL locking as shown in figure 30. Cosine transforms are used hence the angle will be 0 when the V_{inv} is at its peak.

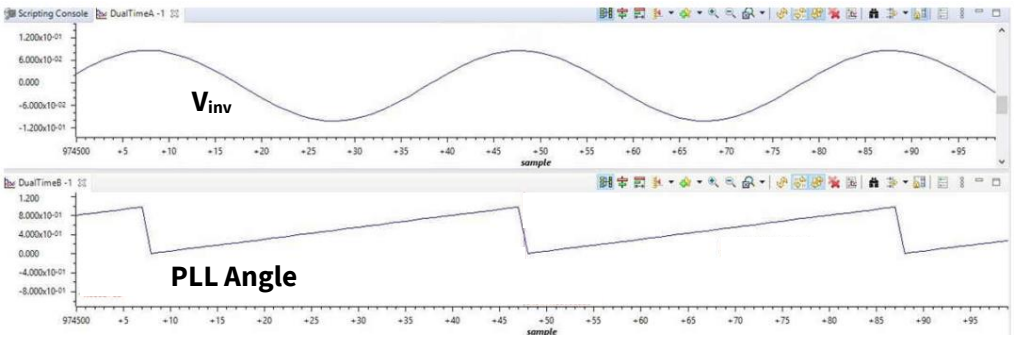


Figure 30: PLL locking in PFC mode

If PLL is not locking it could be for the following 2 reasons:

- The phase sequence for the AC supply is incorrect and needs to be reversed
- The AC line frequency is different from the specified line frequency in firmware

If both of these are correct and the PLL still doesn't lock, the user can try to reset the PLL by setting a tinv_reset_PLL to 1.

10. Verify the rectified current being drawn due to the load on DC side
11. Clear the PWM trip by setting TINV_clearPWMTrip to 1 to see a slight boost in DC voltage

To turn off the board:

1. Turn of the AC source, wait until the AC source has fully discharged its output
2. Turn Off load after the bus capacitors are fully discharged.
3. Capacitors may remain charged for up to 30 minutes after the circuit is turned OFF if steps 2 or 3 are skipped or compromised. They must be allowed to fully discharge before handling the board. Please check the terminal voltages with the power analyzer or a digital multimeter to ensure that the board has fully discharged and is therefore safe to handle.
4. Turn off the auxiliary power supplies

Important Note:
In Labs 5, 6 and 7, in case PWMs do not turn on when the user sets TINV_clearPWMTrip to 1, it could be due to an overcurrent fault flag which is set in one of the three phases and this happens under three circumstances:

1. On closing the relays, there is an inrush current which creates an overcurrent trip in one of the three phases
2. When TINV_clearPWMTrip to 1, the switching action causes one of the flags to be set
3. Setting TINV_StartpowerStage to 1 for closing the current and voltage loop

The EPWM TZFLG is set to 0X000C and under this condition no switching occurs. The load resistance must be increased so that the inrush currents will not cause a trip condition and the EPWM TZFLG changes from 0x0004 to 0x0000 and switching occurs.

Once the FLG is set to 0x000C, even if a TINV_reset_fault_status is performed to reset the faults, PWM action will not be observed even though the faults may be cleared. The user will need to stop and debug the code again to reset that fault status.

Lab 6

This lab is to check the closed current loop operation in PFC mode. It is always safe to start Lab 6 at low voltage and low power as starting at higher power without a supervisory voltage loop can boost the voltage due to overcurrent events and can blow away the switches. Hence, it is very important to carefully set the TINV_idRef_pu variable to avoid overcurrent trips and high voltages at the DC terminals. Also, the

TINV_idRef_pu is defined with a negative sign for PFC mode of operation and with a positive sign for inverter mode of operation.

1. Connect the hardware as shown in figure 29 and turn on the auxiliary supplies
2. In the tinv_settings.h file change the lab number to 6 on line 91

```
#define TINV_LAB 6
```

3. Make sure the variables for datalogger/graph for lab 5 are:

```
#ifndef __TMS320C28XX_CLA__
   TINV_dVal1 = TINV_vGrid_A_sensed_pu;
   TINV_dVal2 = TINV_angleSPLL_radians / (float32_t)(2.0f * TINV_PI);
   TINV_dVal3 = TINV_iGrid_A_sensed_pu;
   TINV_dVal4 = TINV_iGrid_B_sensed_pu;
   DLOG_4CH_run(&TINV_dLog1);
#endif
```

4. Make sure the grid frequency is specified correctly, the default F_{ac} specified is 60Hz. It can be changed in tinv_settings.h file:

```
#define TINV_AC_FREQ_HZ ((float32_t)60)
```

5. The current compensator coefficients used for running the control loop for PFC are shown in the following code. The user does not need to modify these gains, these gains are optimized to work with CRD-25BDA6512N-K

```
#define TINV_GI_PI_KP (((float32_t)0.33000001)
#define TINV_GI_PI_KI ((float32_t)0.0075683544)
```

6. Build, load and debug the code, use the lab6.js file to populate the watch variables in the CCS window
7. Connect suitable E-load in CR mode of about 2kΩ. Make sure to use a high load resistance otherwise can lead to high inrush currents triggering the overcurrent flag
8. Apply 50 V_{RMS} AC voltage to the three-phase terminals
9. Immediately turn on the relay by writing a 1 to TINV_allRelaySet. Rectified voltage should now start to appear across the DC terminals
10. Set TINV_idRef_pu to –0.015 pu
11. To start the PFC mode, enter "1" on TINV_startPowerStage variable, the current should now be drawn from the grid as a sinusoidal signal (with some harmonics as it is at low power) and boost action seen on the vBus. The output voltage boosts from 86 V to around 180 V.
12. The current becomes sinusoidal as the load is increased. This verifies start-up of PFC at 50 VRMS.
13. The user can now increase the input AC voltage slowly while increasing the TINV_idRef_pu to improve the output voltage
14. Once the user is at 230V AC input and 800V DC output, the resistance is decreased to increase the load. As there is no voltage loop in this lab, as the user decreases the resistance, the output voltage will drop too. TINV_idRef_pu can be increased to maintain the output voltage

To turn off the board:

1. Turn of the AC source, wait until the AC source has fully discharged its output
2. Turn Off load after the bus capacitors are fully discharged.
3. Capacitors may remain charged for up to 30 minutes after the circuit is turned OFF if steps 2 or 3 are skipped or compromised. They must be allowed to fully discharge before handling the board. Please check the terminal voltages with the power analyzer or a digital multimeter to ensure that the board has fully discharged and is therefore safe to handle.
4. Turn off the auxiliary power supplies

Lab 7

To check the closed current and closed voltage loop operation in PFC mode, follow the steps below:

1. Connect the hardware as shown in figure 29 and turn-on the auxiliary supplies
2. In the tinv_settings.h file change the lab number to 7 on line 91

```
#define TINV_LAB 7
```

3. Make sure the variables for datalogger/graph for lab 5 are:

```
#ifndef __TMS320C28XX_CLA__
   TINV_dVal1 = TINV_vGrid_A_sensed_pu;
   TINV_dVal2 = TINV_angleSPLL_radians / (float32_t)(2.0f * TINV_PI);
   TINV_dVal3 = TINV_iGrid_A_sensed_pu;
   TINV_dVal4 = TINV_iGrid_B_sensed_pu;
   DLOG_4CH_run(&TINV_dLog1);
#endif
```

4. Make sure the grid frequency is specified correctly, the default F_{ac} specified is 60Hz. It can be changed in tinv_settings.h file:

```
#define TINV_AC_FREQ_HZ ((float32_t)60)
```

5. The current compensator coefficients used for running the control loop for PFC are shown in the following code. The user does not need to modify these gains, these gains are optimized to work with CRD-25BDA6512N-K

```
#define TINV_GI_PI_KP (((float32_t)0.33000001)
#define TINV_GI_PI_KI ((float32_t)0.0075683544)
```

6. The voltage compensator coefficients used for running the voltage control loop for PFC are shown in the following code. The user does not need to modify these gains, these gains are optimized to work with CRD-25BDA6512N-K

```
#define TINV_GV_PI_KP ((float32_t) 4)
#define TINV_GV_PI_KI ((float32_t) 0.008)
```

7. Build, load and debug the code, use the lab7.js file to populate the watch variables in the CCS window
8. Connect suitable E-load in CR mode of about 2kΩ. Make sure to use a high load resistance otherwise can lead to high inrush currents triggering the overcurrent flag

9. Apply 50 VRMS AC voltage to the three-phase terminals
10. Immediately turn on the relay by writing a 1 to TINV_allRelaySet. Rectified voltage should now start to appear across the DC terminals
11. Set TINV_vBusRef_pu to 0.202 pu which corresponds to approximately 200V
12. To start the PFC mode, enter "1" on TINV_startPowerStage variable, the current should now be drawn from the grid as a sinusoidal signal (with some harmonics as it is at low power) and boost action seen on the vBus. The output voltage boosts from 86 V to around 200 V.
13. Now to verify start-up at 230Vac input, stop the code and debug the firmware again
14. Apply 230 V_{RMS} AC voltage to the three phase terminals
15. Immediately turn on the relay by writing a 1 to TINV_allRelaySet. Rectified voltage should now start to appear across the DC terminals
16. Set TINV_vBusRef_pu to 0.775 pu which corresponds to approximately 800V
17. To start the PFC mode, enter "1" on TINV_startPowerStage variable, the current should now be drawn from the grid as a sinusoidal signal (with some harmonics as it is at low power) and boost action seen on the Vbus. The output voltage boosts from 650 V to around 800 V. Start-up at 230 Vrms is shown in figure 31.

    Ch 1, 5 & 6 are phase A, B and C line currents respectively, Ch 2 is output Vbus voltage, Ch 3 is phase A Vrms, Ch 4 is drain-source voltage across Q2 phase A and Ch 7 and 8 are gate-to-source voltages of the Q1 and Q2 switches of Phase A respectively.

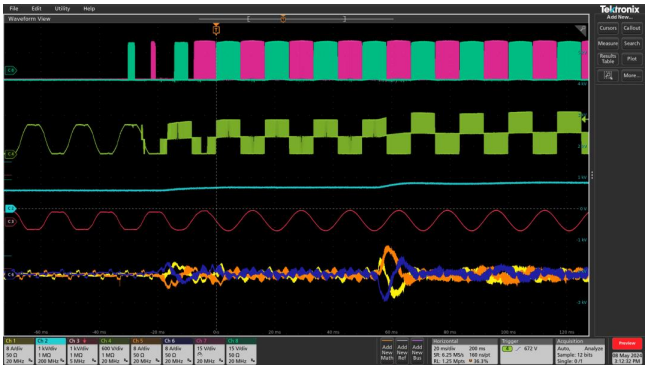


Figure 31: 230Vac PFC start-up

18. In case any overcurrent trip is observed which causes the PWMs to switch off, please refer the note in Lab 5 to debug this condition.
19. Load can now be increased to 25kW by lowering the resistance

To turn off the board:

1. Bring the load down by increasing the resistance
2. Turn of the AC source, wait until the AC source has fully discharged its output
3. Turn Off load after the bus capacitors are fully discharged.
4. Capacitors may remain charged for up to 30 minutes after the circuit is turned OFF if steps 2 or 3 are skipped or compromised. They must be allowed to fully discharge before handling the board. Please

check the terminal voltages with the power analyzer or a digital multimeter to ensure that the board has fully discharged and is therefore safe to handle.

5. Turn off the auxiliary power supplies

6. Test Results

6.1 Inverter Mode Test Results (DC-AC)

Table 6 shows the efficiency data for CRD-25BDA6512N-K in inverter mode switching at 60kHz switching frequency. The efficiency curves are shown in figure 32.

Table 6: Inverter Mode Efficiency at 60kHz switching frequency and varied input and output voltages

Input Voltage (Vdc)	Input Power (kW)	Output Voltage (VAC)	Output Power (kW)	Efficiency (%)
670	3.69	400	3.66	99.20
670	7.02	400	6.97	99.27
670	10.76	400	10.68	99.25
670	14.47	400	14.34	99.13
670	18.07	400	17.89	98.99
670	21.38	400	21.13	98.82
670	24.92	400	24.56	98.57
800	3.32	380	3.28	98.71
800	6.37	380	6.31	98.98
800	9.69	380	9.60	98.98
800	13.07	380	12.93	98.90
800	16.43	380	16.23	98.79
800	19.57	380	19.31	98.65
800	22.97	380	22.60	98.47
800	26.47	380	25.98	98.35
800	3.70	400	3.65	98.68
800	7.09	400	7.02	99.00
800	10.74	400	10.63	99.00
800	14.56	400	14.41	98.94
800	18.20	400	17.98	98.79

800	21.45	400	21.16	98.63
800	25.27	400	24.85	98.45
800	5.22	480	5.18	99.18
800	10.05	480	9.98	99.28
800	15.27	480	15.16	99.25
800	20.37	480	20.20	99.12
800	25.46	480	25.19	98.93
900	3.70	400	3.63	98.31
900	7.10	400	7.01	98.75
900	10.74	400	10.62	98.85
900	14.49	400	14.31	98.77
900	17.72*	400	17.48	98.64
900	5.21	480	5.16	98.90
900	10.04	480	9.95	99.10
900	15.22*	480	15.08	99.09
***Input Power at V_{in}= 900V is limited by maximum current of the DC input supply used for testing**				

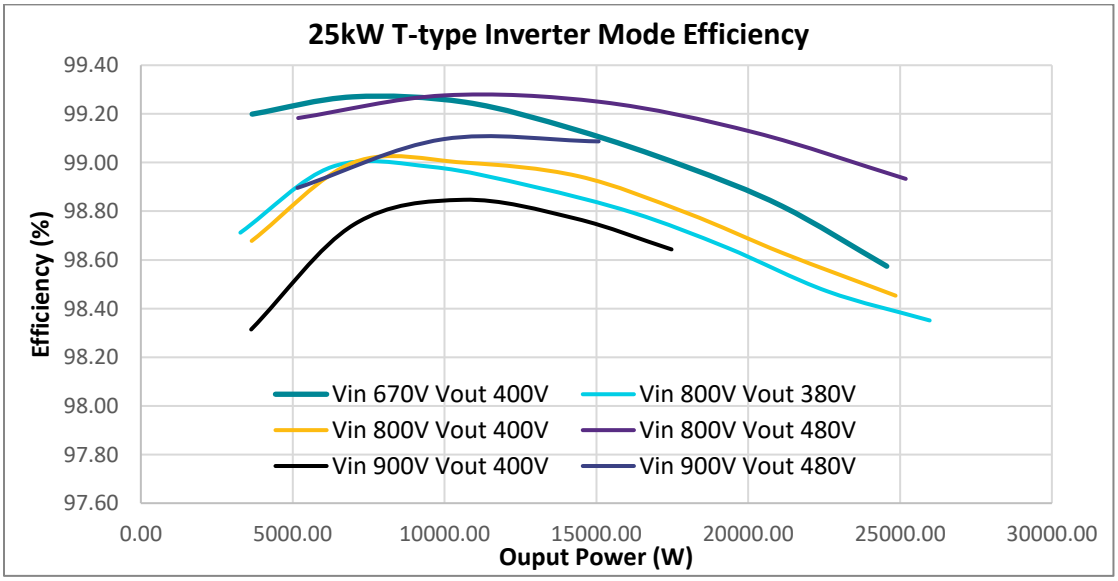
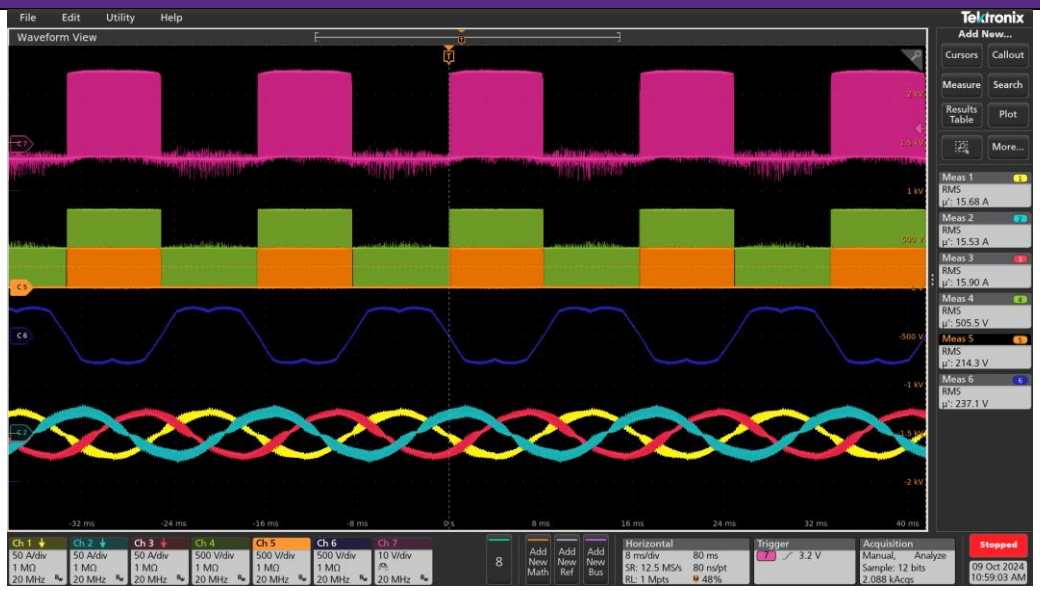
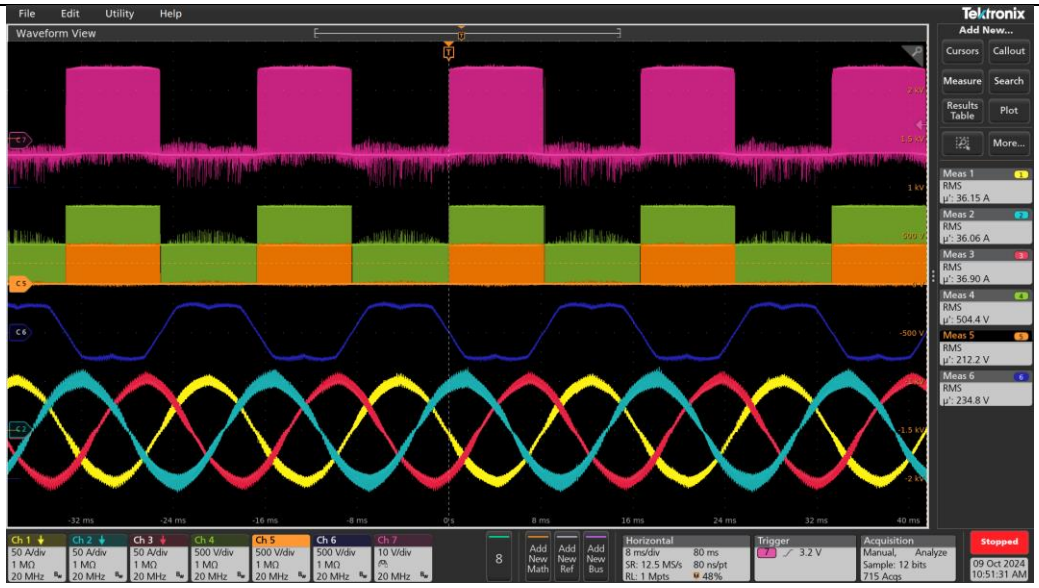
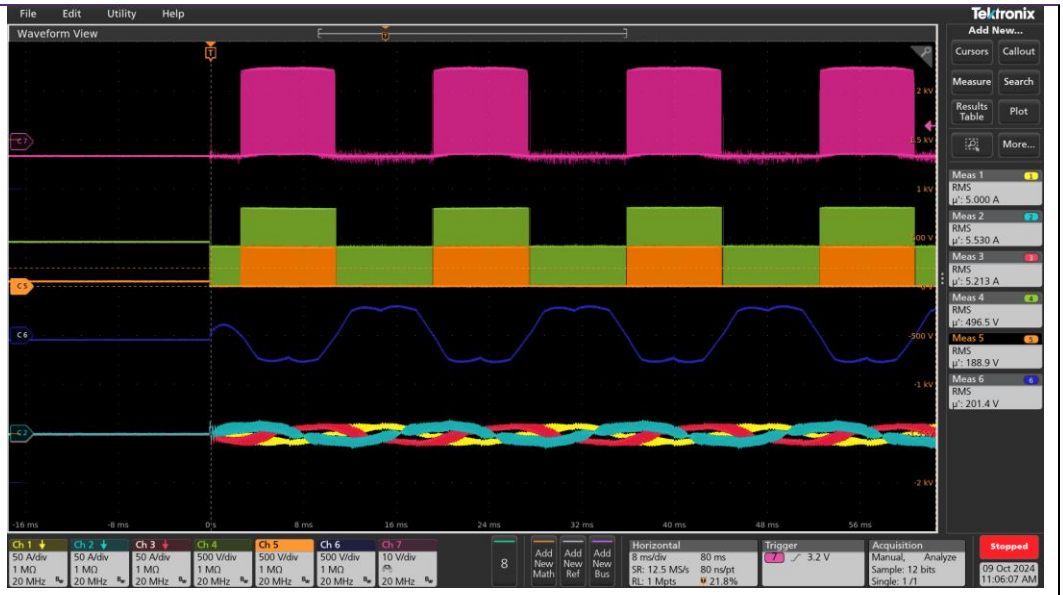


Figure 32: Inverter Mode Efficiency curve

Typical waveforms for the inverter mode are summarized in table 7.

Table 7: Typical waveforms for CRD-25BDA6512N-K Inverter Mode

Description	Waveform
Lab 3: Half-load **(V_{in}=800V, V_{out}= 400V_{l-l}, Fsw= 60kHz)** Ch 1,2 and 3- Phase A,B,C line currents respectively Ch 4 and 5- V_{ds} Q1 and Q3 respectively Ch 6: Output V_{rms} phase A Ch 7 : V_{gs} Q2	
Lab 3: Full-load **(V_{in}=800V, V_{out}= 400V_{l-l}, Fsw= 60kHz)** Ch 1,2 and 3- Phase A,B,C line currents respectively Ch 4 and 5- V_{ds} Q1 and Q3 respectively Ch 6: Output V_{rms} phase A Ch 7 : V_{gs} Q2	

Inverter Start-up at 800V, 3.9kW Ch 1,2 and 3- Phase A,B,C line currents respectively Ch 4 and 5- V_{ds} Q1 and Q3 respectively Ch 6: Output V_{rms} phase A Ch 7 : V_{gs} Q2	

6.2 PFC Mode Test Results (AC-DC)

Table 8 and 9 show the efficiency data for CRD-25BDA6512N-K in PFC switching at 60kHz. The efficiency curves are shown in figure 33 and 34.

Table 8: PFC Mode Efficiency at 60kHz switching frequency for varied input voltages

Input Voltage (Vline-line)	Input Power (W)	Load (%)	Output Voltage (VDC)	Output Power (W)	Efficiency (%)
400	1285	5%	800	1253	97.251
400	2567	10%	800	2526	98.32
400	5088	20%	800	5033	98.88
400	7588	30%	800	7512	98.98
400	10332	40%	800	10231	99.02
400	12640	50%	800	12510	98.985
400	14298	60%	800	15088	98.93
400	16195	70%	800	17525	98.86
400	18973	75%	800	18745	98.8
400	20318	80%	800	20055	98.728
400	22374	90%	800	22574	98.64
400	25427	100%	800	25048	98.51

380	1287	5%	800	1250	97.12
380	2565	10%	800	2522	98.31
380	5090	20%	800	5029	98.8
380	7588	30%	800	7507	98.93
380	10339	40%	800	10229	98.94
380	12651	50%	800	12509	98.88
380	15267	60%	800	15087	98.82
380	17754	70%	800	17527	98.72
380	18998	75%	800	18745	98.67
380	20324	80%	800	20037	98.59
380	22920	90%	800	22569	98.47
380	25462	100%	800	25044	98.36
480	1283	5%	800	1253	97.66
480	2560	10%	800	2526	98.68
480	5080	20%	800	5033	99.08
480	7571	30%	800	7512	99.22
480	10305	40%	800	10231	99.28
480	12605	50%	800	12510	99.25
480	15204	60%	800	15088	99.24
480	17668	70%	800	17525	99.19
480	18902	75%	800	18745	99.17
480	20231	80%	800	20055	99.13
480	22784	90%	800	22574	99.08
480	25296	100%	800	25048	99.02

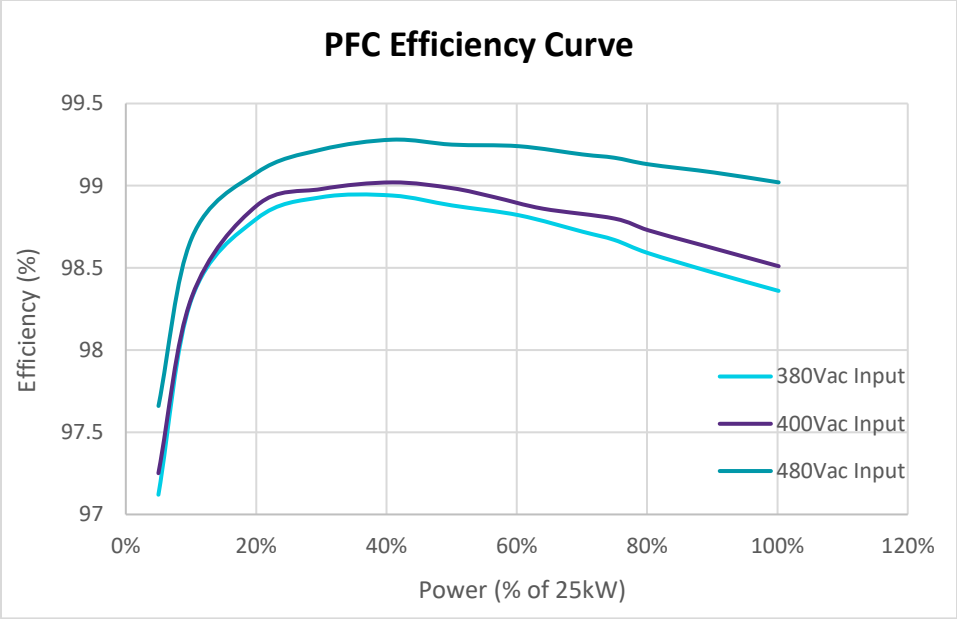


Figure 33: PFC Efficiency Curve with Varying Input Voltages

Table 9: PFC Mode Efficiency at 60kHz switching frequency for varied output voltages

Input Voltage (V_{l-l})	Input Power (W)	Load (%)	Output Voltage (VDC)	Output Power (W)	Efficiency (%)
400	1285	5%	800	1253	97.251
400	2567	10%	800	2526	98.32
400	5088	20%	800	5033	98.88
400	7588	30%	800	7512	98.98
400	10332	40%	800	10231	99.02
400	12640	50%	800	12510	98.985
400	14298	60%	800	15088	98.93
400	16195	70%	800	17525	98.86
400	18973	75%	800	18745	98.8
400	20318	80%	800	20055	98.728
400	22374	90%	800	22574	98.64
400	25427	100%	800	25048	98.51
400	1283	5%	700	1256	97.89

400	2598	10%	700	2567	98.81
400	5079	20%	700	5035	99.14
400	7572	30%	700	7513	99.22
400	10171	40%	700	10090	99.2
400	12631	50%	700	12525	99.16
400	15159	60%	700	15020	99.08
400	17729	70%	700	17552	99
400	18920	75%	700	18721	98.95
400	20785	80%	700	20550	98.87
400	22856	90%	700	22577	98.78
400	25361	100%	700	25024	98.67
400	1295	5%	850	1254	96.84
400	2634	10%	850	2589	98.29
400	5109	20%	850	5045	98.74
400	7593	30%	850	7508	98.88
400	10184	40%	850	10071	98.89
400	12725	50%	850	12585	98.9
400	15204	60%	850	15026	98.83
400	17778	70%	850	17556	98.75
400	18991	75%	850	18744	98.7
400	20295	80%	850	20023	98.66
400	22849	90%	850	22518	98.55
400	25423	100%	850	25024	98.43

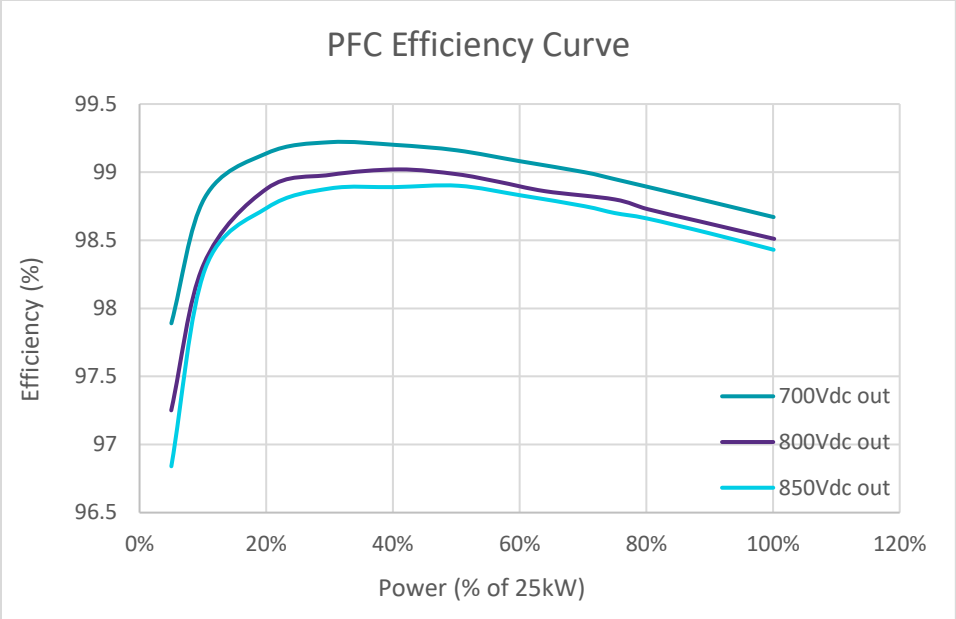


Figure 34: PFC Efficiency Curve with Varying output Voltages

The total harmonic distortion (THD) data for the current in each phase and the power factor data, both at 60kHz switching frequency are summarized in table 10. The graph is shown in figure 35 and figure 36 for the THD and power factor respectively.

Table 10: PFC Mode Current Distortion and Power Factor Data

Input Voltage (V_{l-l})	Output Voltage (VDC)	Output Power (W)	Phase A Current THD (%)	Phase B Current THD (%)	Phase C Current THD (%)	Power Factor
400	800	1270	20.03	17.20	19.30	0.8960
400	800	1587	17.80	15.10	17.20	0.9490
400	800	3173	8.60	8.30	9.80	0.9844
400	800	5300	6.45	7.31	7.80	0.9919
400	800	7059	5.80	6.30	6.60	0.9952
400	800	9082	5.26	5.36	5.74	0.9965
400	800	12710	4.19	4.25	4.70	0.9975
400	800	15890	3.74	3.69	3.91	0.9982
400	800	17176	3.56	3.50	3.72	0.9985
400	800	19265	3.14	3.13	3.21	0.9988

400	800	21178	3.16	3.01	3.10	0.9990
400	800	23012	2.88	2.90	2.87	0.9992
400	800	25002	2.69	2.71	2.71	0.9993

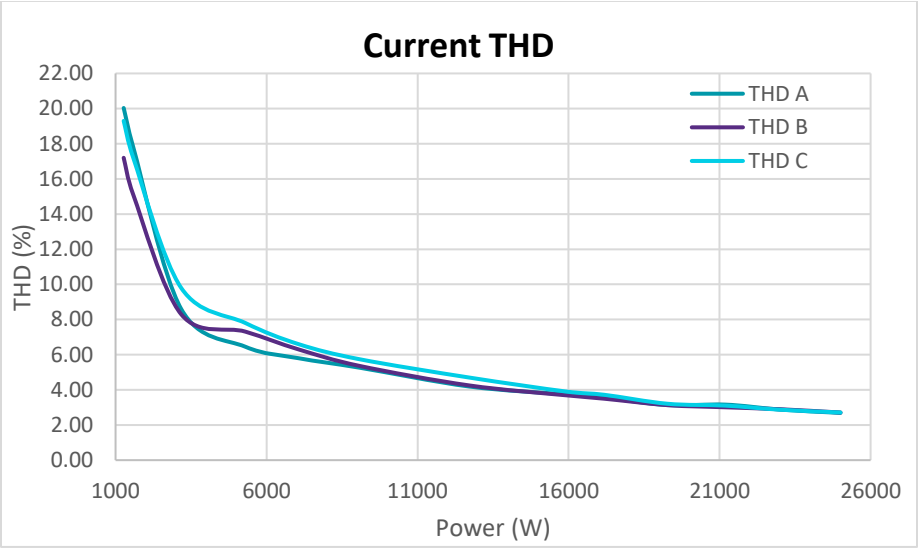


Figure 35: Current THD in PFC Mode

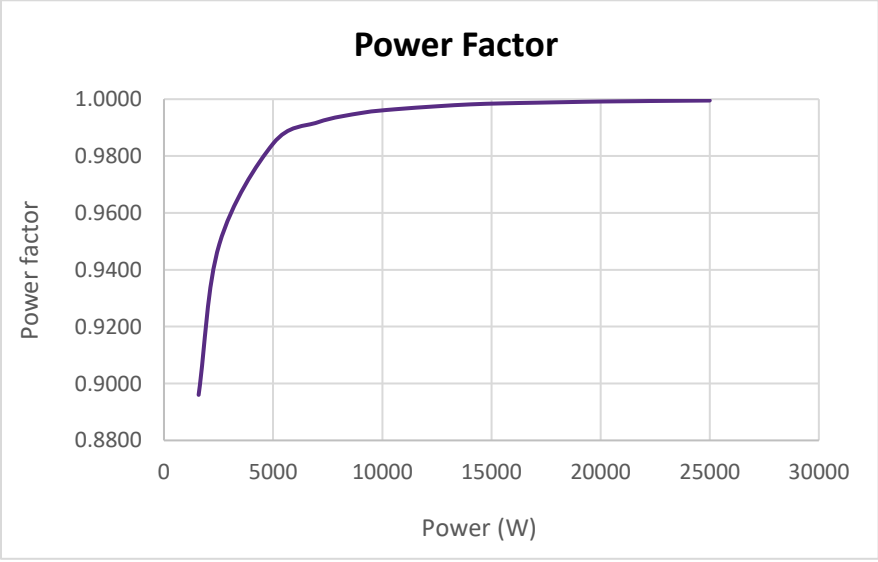
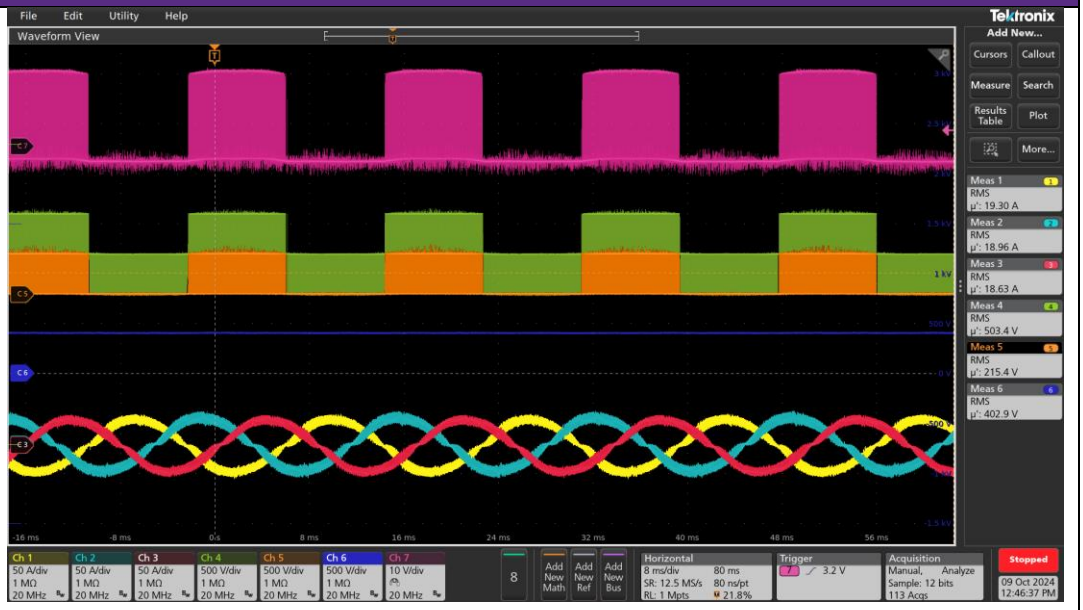
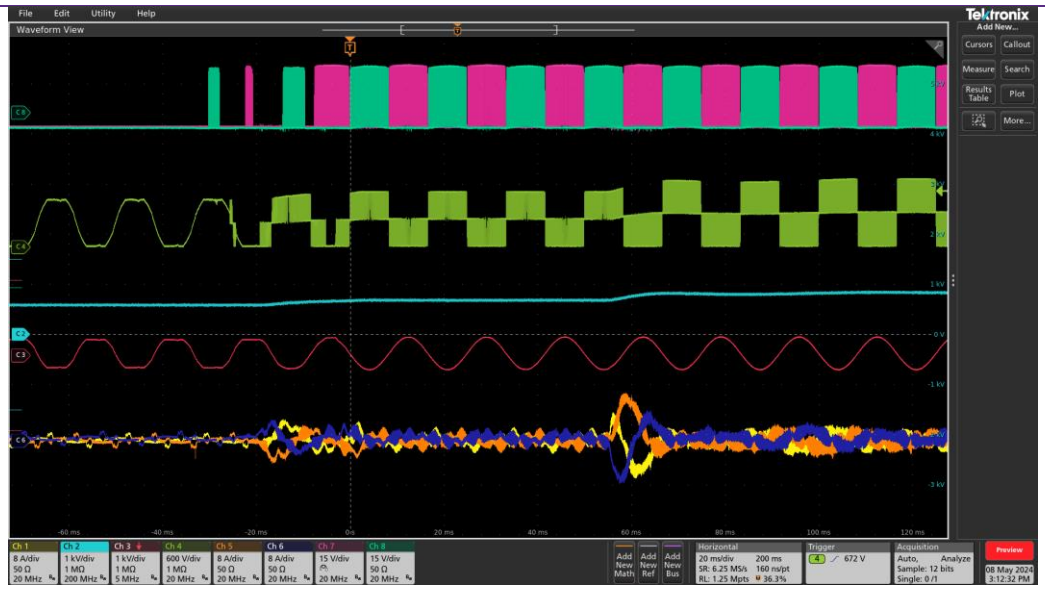
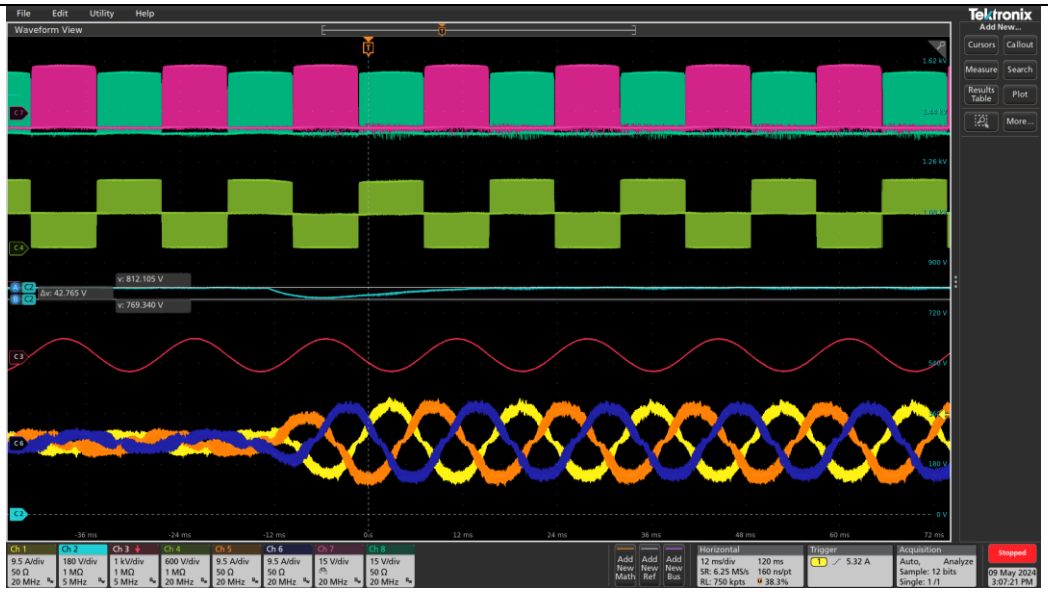


Figure 36: Power Factor results in PFC Mode

Typical waveforms for the PFC mode are summarized in table 11.

Table 11: Typical waveforms for CRD-25BDA6512N-K PFC Mode

Description	Waveform
Lab 7: Half-load **(V_{in}=400V_{l-l}, V_{out}= 800V, Fsw= 60kHz)** Ch 1,2 and 3- Phase A,B,C line currents respectively Ch 4 and 5- V_{ds} Q1 and Q3 respectively Ch 6: Output Vdc mid-point voltage Ch 7 : V_{gs} Q2	
Lab 7: Full-load **(V_{in}=400V_{l-l}, V_{out}= 800V, Fsw= 60kHz)** Ch 1,2 and 3- Phase A,B,C line currents respectively Ch 4 and 5- V_{ds} Q1 and Q3 respectively Ch 6: Output Vdc mid-point voltage Ch 7 : V_{gs} Q2	

Lab 7: PFC Start-up at V_{in}=400V_{l-l}, V_{out}= 800V, P= 3.9kW Ch 1,5 and 6- Phase A,B,C line currents respectively Ch 2 and 4- V_{ds} Q2 and Q1 respectively Ch 2: Output Vrms phase A Ch 7 and 8: Vgs Q1 and Q2 respectively	
Lab 7: PFC Load transient at V_{in}=400V_{l-l}, V_{out}= 800V, from 10% to 50% load Ch 1,5 and 6- Phase A,B,C line currents respectively Ch 2 and 4- V_{ds} Q2 and Q1 respectively Ch 2: Output Vrms phase A Ch 7 and 8: Vgs Q1 and Q2 respectively	

6.3 Thermal Test Results

This design is tested with forced air cooling with direct flow of air on the MOSFETs and heatsink by placing the cooling fans and the board as shown in figure 25. The fan for each phase is a 12V fan operating at approximately 8W power. The case temperature reading of each switch was taken using a K-type thermocouple and an Agilent 34970A Data logger unit.

The test results under these conditions are shown in Table 12. The highest case temperature among all three phases of a 1200V switch and a 650V switch is noted for both Inverter and PFC modes. The junction temperature is calculated based on the measured case temperature, the thermal resistance of the MOSFET from junction to case, and the calculated power loss.

The maximum junction temperature for C3M0032120K and C3M0025065K is 175^0C and the derating requirement for T_j is 135^0C. The results below show that the SiC MOSFETs meet the derating requirements in all test conditions and therefore pass the thermal tests.

Table 12: Thermal test results of SiC power MOSFETs in CRD-25BDA6512N-K

Description	R_{th} (j-c) (^{0}C/W)	Calculated Power loss (W)	Measured Case Temp. (°C)	Calculated Junction Temp. (°C)	Max. Operating junction temp (°C)	Derating Requirement (°C)	Result
Inverter Mode: 800Vdc 400Vac 25kW 60kHz							
C3M0032120K Q1_A	0.44	28.5	58.2	70.5	175 °C	135°C	Pass
C3M0025065K Q3_A	0.46	11	55.5	60.6	175 °C	135°C	Pass
PFC mode: 380Vac 800Vdc 25kW 60kHz							
C3M0032120K Q1_C	0.44	18.2	57.9	65.9	175 °C	135°C	Pass
C3M0025065K Q3_C	0.46	15.5	65.3	72.4	175 °C	135°C	Pass
PFC mode: 400Vac 850Vdc 25kW 60kHz							
C3M0032120K Q1_C	0.44	17	55.1	62.6	175 °C	135°C	Pass
C3M0025065K Q3_C	0.46	13.8	62.5	68.9	175 °C	135°C	Pass

Revision History

Date	Revision	Changes
May 2024	1	Initial Release
October 2024	2	Updated Table 1, 6, 7, 11 Updated Section 5.5.2 current loop gains in Lab 3 Updated Figure 28 Updated Section 5.6.2 current and voltage loop gains in Lab 6 and Lab 7 Updated Table Numbers Updated figure 32

References

[1] Texas Instruments Design Guide: TIDA-01606, 10-kW, Bidirectional Three-Phase Three-Level (T-type) Inverter and PFC Reference Design (Web Link)

[2] M. Schweizer, I. Lizama, T. Friedli, and J. W. Kolar, “Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies,” in IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society, 2010, pp. 391–396

[3] M. Schweizer, J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications", IEEE Transactions on Power Electronics, Vol. 28, No. s2, pp. 899-907, February 2013

[4] M. Dursun and M. K. DÖŞOĞLU, “LCL Filter Design for Grid Connected Three-Phase Inverter,” in 2018 2nd International Symposium on Multidisciplinary Studies and Innovative Technologies (ISMSIT), Oct. 2018, pp. 1–4. doi: 10.1109/ISMSIT.2018.8567054.

[5] S. Jayalath and M. Hanif, “Generalized LCL-Filter Design Algorithm for Grid-Connected Voltage-Source Inverter,” IEEE Transactions on Industrial Electronics, vol. 64, no. 3, pp. 1905–1915, Mar. 2017, doi: 10.1109/TIE.2016.2619660.

[6] G. R. Wehmuth, T. D. Curi Busarello, and A. Péres, “Step-by-Step Design Procedure for LCL-Type Single-Phase Grid Connected Inverter Using Digital Proportional-Resonant Controller With Capacitor-Current Feedback,” in 2021 IEEE Green Technologies Conference (GreenTech), Apr. 2021, pp. 448–454. doi: 10.1109/GreenTech48523.2021.00076.

[7] Y. Han et al., “Modeling and Stability Analysis of LCL -Type Grid-Connected Inverters: A Comprehensive Overview,” IEEE Access, vol. 7, pp. 114975–115001, 2019, doi: 10.1109/ACCESS.2019.2935806.

[8] “Magnetics - Inductor Design with Magnetics Powder Cores.” https://www.mag-inc.com/Inductor-Design-with-Magnetics-Powder-Cores (accessed Feb. 15, 2023).

[9] KDM inductor design

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