

# C3M0021120J2

Silicon Carbide Power MOSFET  
N-Channel Enhancement Mode

## Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- Larger drain tab for better thermal performance
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ( $Q_{rr}$ )
- Halogen free, RoHS compliant

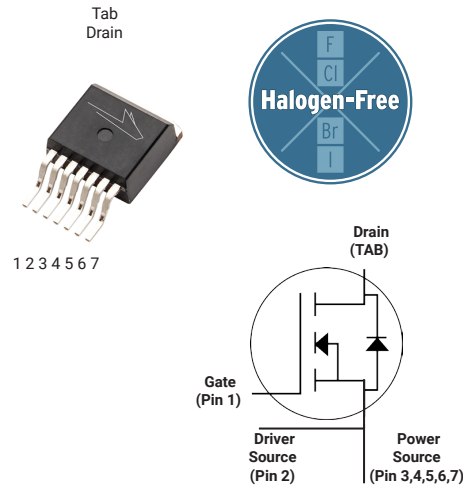
## Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

## Typical Applications

- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters

## Package



Part Number	Package	Marking
C3M0021120J2	TO-263-7XL	C3M0021120J2

## Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	$V_{DS}$			1200	V	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	$I_D$			114	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Fig. 19
				83		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Note 2
Pulsed Drain Current	$I_{DM}$			248		$t_{Pmax}$ limited by $T_{Jmax}$ $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	$P_D$			500	W	$T_c = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	$T_J, T_{stg}$			-40 to +175	$^\circ\text{C}$		
Solder Temperature	$T_L$			260		According to JEDEC J-STD-020	

Note (1): Recommended turn-on gate voltage is 15V with  $\pm 5\%$  regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design


**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.9	3.8	V	$V_{DS} = V_{GS}, I_D = 17.10\text{ mA}$	Fig. 11
			2.3		V	$V_{DS} = V_{GS}, I_D = 17.10\text{ mA}, T_J = 175^\circ\text{C}$	
$I_{DSS}$	Zero Gate Voltage Drain Current		1	50	$\mu\text{A}$	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$	
$I_{GSS}$	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance		21	29	m $\Omega$	$V_{GS} = 15\text{ V}, I_D = 62.12\text{ A}$	Fig. 4, 5, 6
			35			$V_{GS} = 15\text{ V}, I_D = 62.12\text{ A}, T_J = 175^\circ\text{C}$	
$g_{fs}$	Transconductance		38		S	$V_{DS} = 20\text{ V}, I_{DS} = 62.12\text{ A}$	Fig. 7
			35			$V_{DS} = 20\text{ V}, I_{DS} = 62.12\text{ A}, T_J = 175^\circ\text{C}$	
$C_{iss}$	Input Capacitance		5100		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V to }1000\text{ V}$ $f = 100\text{ kHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
$C_{oss}$	Output Capacitance		174				
$C_{rss}$	Reverse Transfer Capacitance		11				
$E_{oss}$	$C_{oss}$ Stored Energy		98		$\mu\text{J}$	$V_{DS} = 1000\text{ V}, f = 100\text{ kHz}$	Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		210		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }800\text{ V}$	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		323		pF		
$E_{ON}$	Turn-On Switching Energy (Body Diode FWD)		1.7		mJ	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 62.12\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega, L = 59\text{ }\mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode	Fig. 26, 28
$E_{OFF}$	Turn-Off Switching Energy (Body Diode FWD)		0.3				
$t_{d(on)}$	Turn-On Delay Time		15		ns	$V_{DD} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 62.12\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega, L = 59\text{ }\mu\text{H}, T_J = 25^\circ\text{C}$ Timing relative to $V_{DS}$ Inductive load	Fig. 27, 28
$t_r$	Rise Time		34				
$t_{d(off)}$	Turn-Off Delay Time		54				
$t_f$	Fall Time		13				
$R_{G(int)}$	Internal Gate Resistance		2.9		$\Omega$	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$	
$Q_{gs}$	Gate to Source Charge		60		nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 62.12\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
$Q_{gd}$	Gate to Drain Charge		45				
$Q_g$	Total Gate Charge		169				

Note (3):  $C_{o(er)}$ , a lumped capacitance that gives same stored energy as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 800V  
 $C_{o(tr)}$ , a lumped capacitance that gives same charging time as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 800V

Reverse Diode Characteristics (T<sub>c</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V <sub>SD</sub>	Diode Forward Voltage	4.9		V	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 31.1 A, T <sub>J</sub> = 25 °C	Fig. 8, 9, 10
		4.4		V	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 31.1 A, T <sub>J</sub> = 175 °C	
I <sub>S</sub>	Continuous Diode Forward Current		85	A	V <sub>GS</sub> = -4 V, T <sub>c</sub> = 25°C	
I <sub>SM</sub>	Diode pulse Current		248	A	V <sub>GS</sub> = -4 V, pulse width t <sub>p</sub> limited by T <sub>Jmax</sub>	
t <sub>rr</sub>	Reverse Recover time	16		ns	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 62.12 A, V <sub>R</sub> = 800 V di <sub>F</sub> /dt = 5300 A/μs, T <sub>J</sub> = 25 °C	
Q <sub>rr</sub>	Reverse Recovery Charge	416		nC		
I <sub>rrm</sub>	Peak Reverse Recovery Current	44		A		
t <sub>rr</sub>	Reverse Recover time	22		ns	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 62.12 A, V <sub>R</sub> = 800 V di <sub>F</sub> /dt = 2240 A/μs, T <sub>J</sub> = 25 °C	
Q <sub>rr</sub>	Reverse Recovery Charge	268		nC		
I <sub>rrm</sub>	Peak Reverse Recovery Current	21		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
R <sub>θJC</sub>	Thermal Resistance from Junction to Case	0.23	°C/W		Fig. 21



## Typical Performance

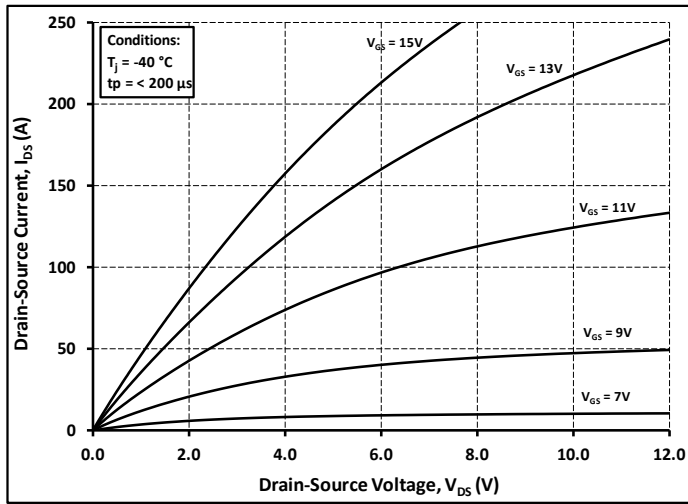


Figure 1. Output Characteristics  $T_J = -40\text{ }^{\circ}\text{C}$

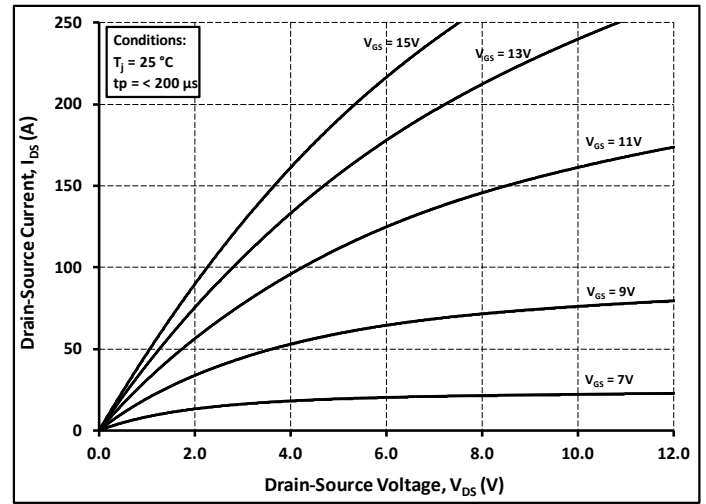


Figure 2. Output Characteristics  $T_J = 25\text{ }^{\circ}\text{C}$

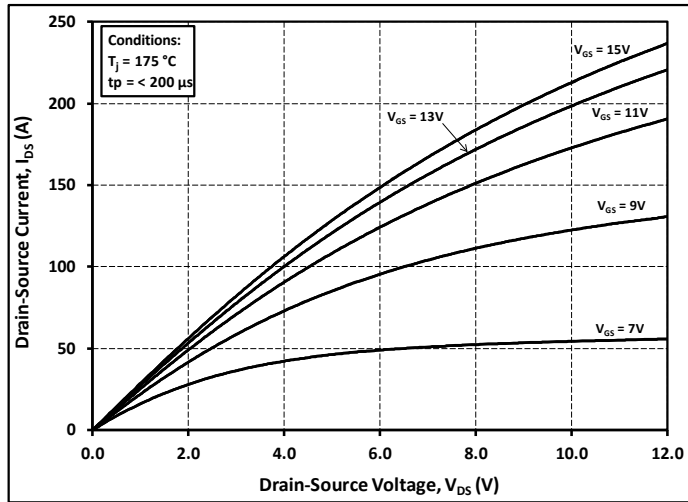


Figure 3. Output Characteristics  $T_J = 175\text{ }^{\circ}\text{C}$

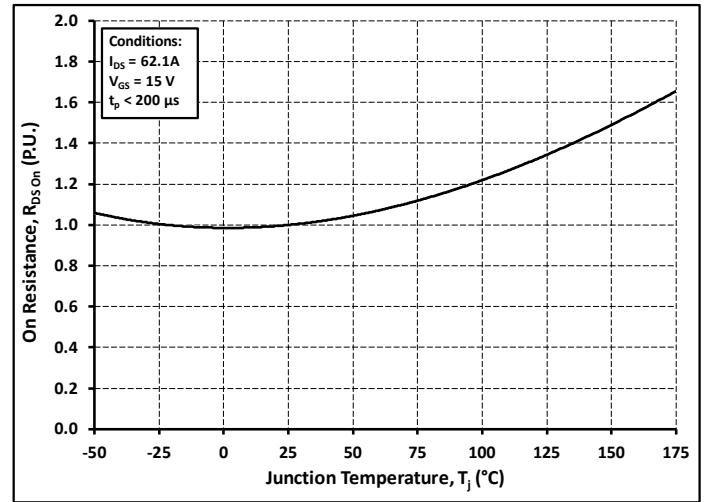


Figure 4. Normalized On-Resistance vs. Temperature

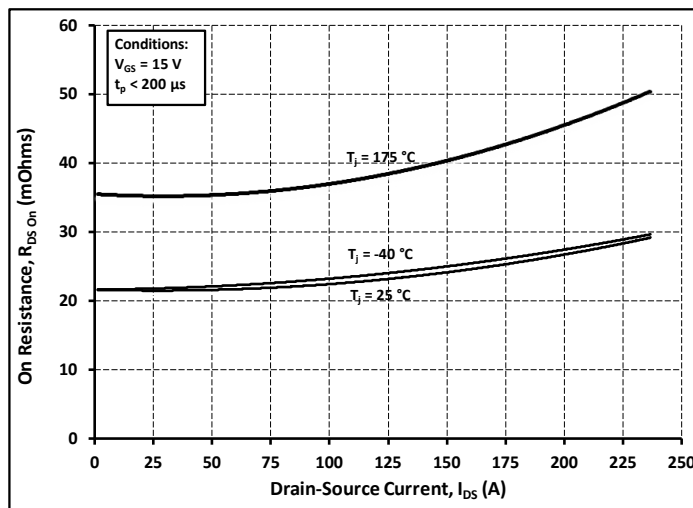


Figure 5. On-Resistance vs. Drain Current  
For Various Temperatures

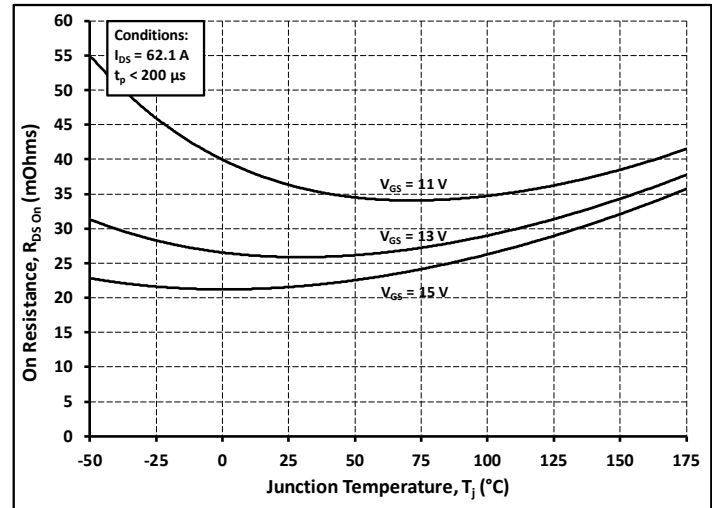


Figure 6. On-Resistance vs. Temperature  
For Various Gate Voltage

## Typical Performance

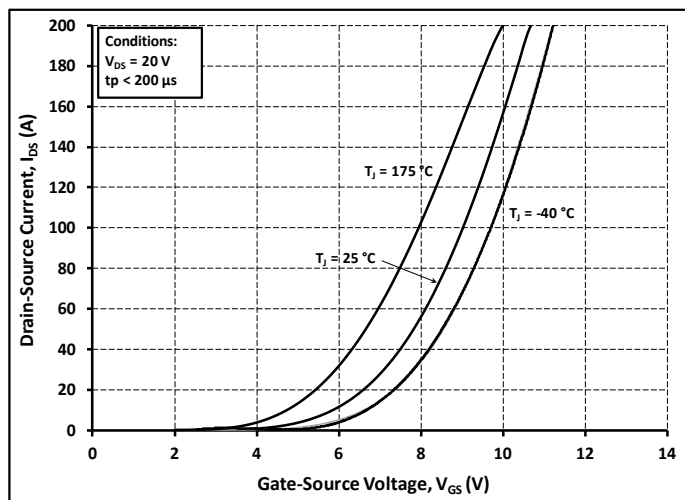


Figure 7. Transfer Characteristic for Various Junction Temperatures

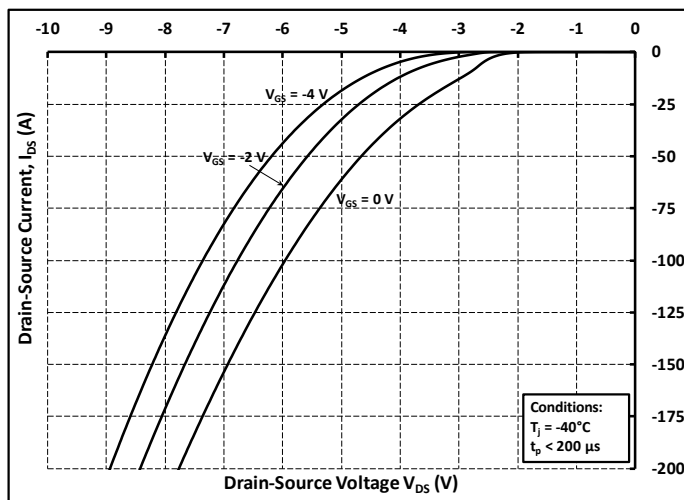


Figure 8. Body Diode Characteristic at  $-40\text{ }^{\circ}\text{C}$

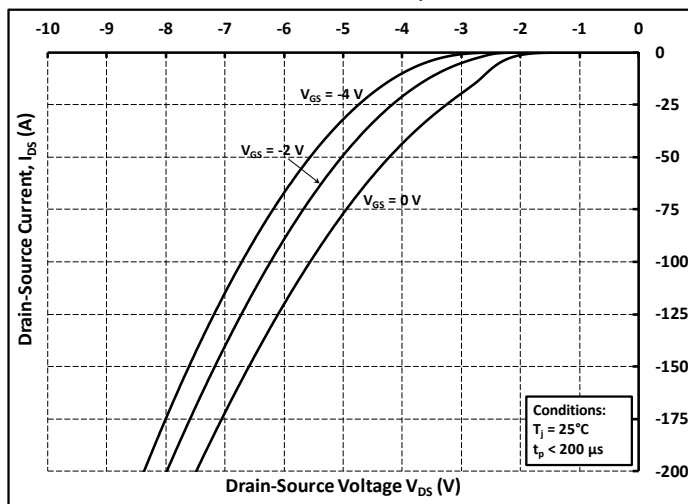


Figure 9. Body Diode Characteristic at  $25\text{ }^{\circ}\text{C}$

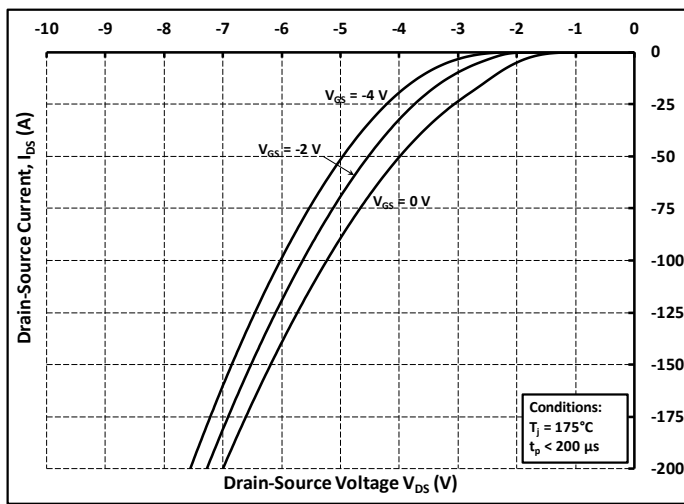


Figure 10. Body Diode Characteristic at  $175\text{ }^{\circ}\text{C}$

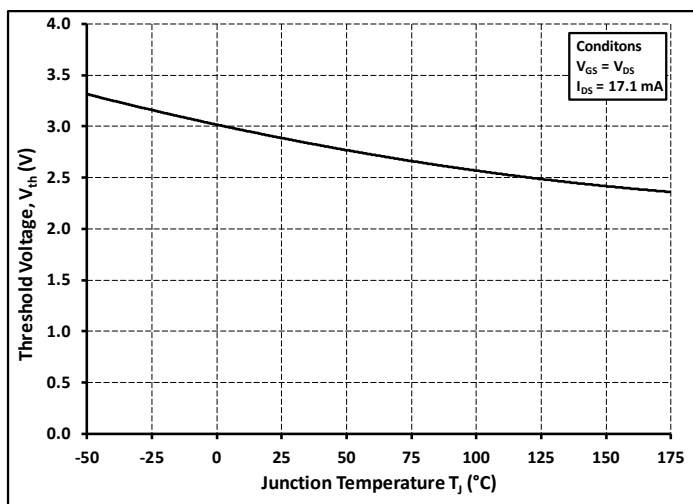


Figure 11. Threshold Voltage vs. Temperature

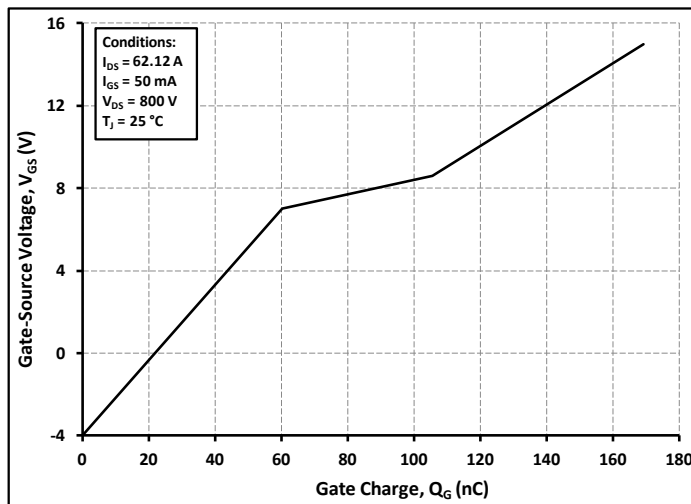


Figure 12. Gate Charge Characteristics

## Typical Performance

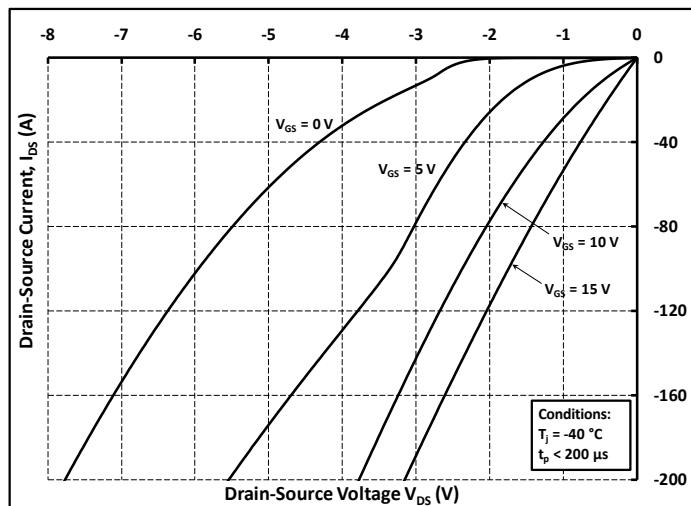
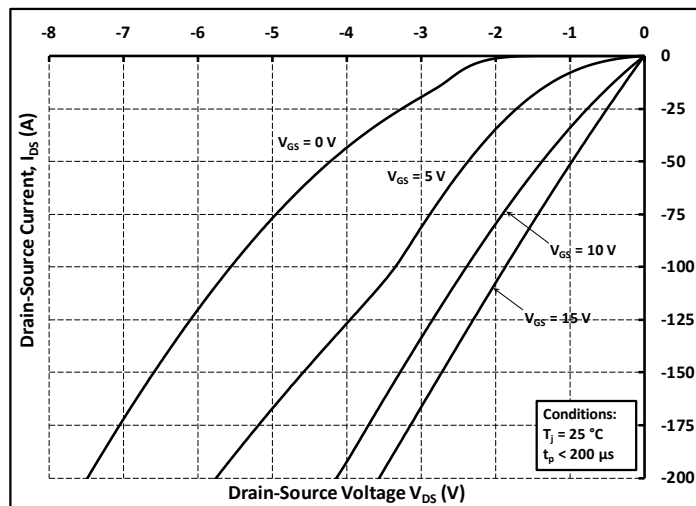
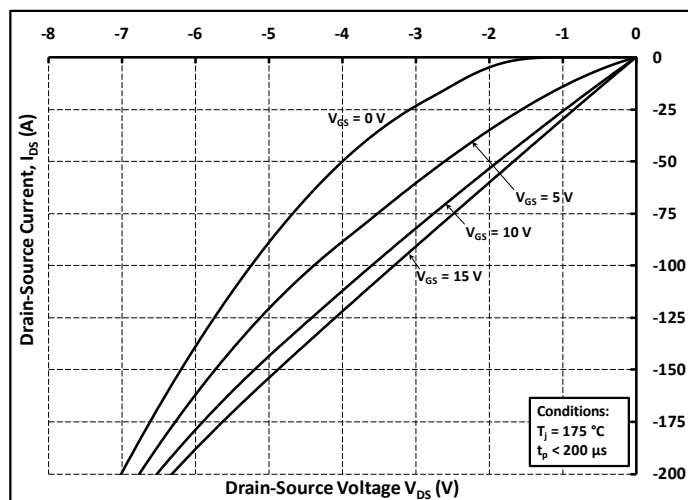
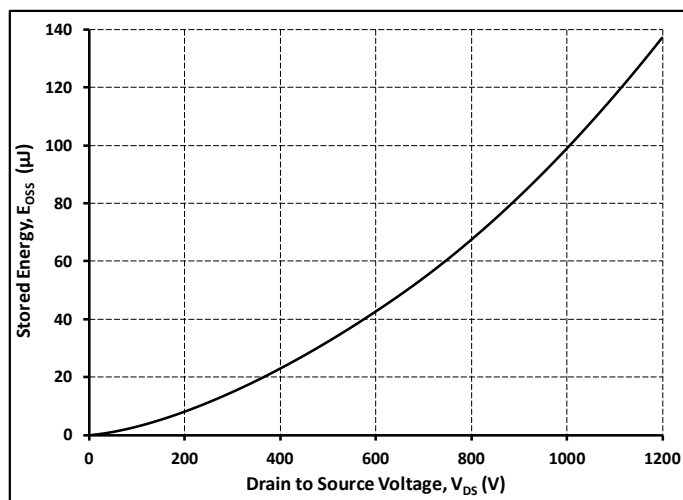
Figure 13. 3rd Quadrant Characteristic at  $-40\text{ }^{\circ}\text{C}$ Figure 14. 3rd Quadrant Characteristic at  $25\text{ }^{\circ}\text{C}$ Figure 15. 3rd Quadrant Characteristic at  $175\text{ }^{\circ}\text{C}$ 

Figure 16. Output Capacitor Stored Energy

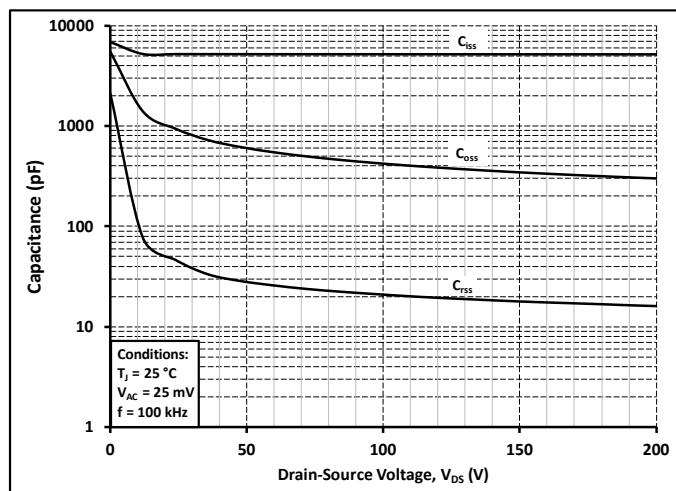


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

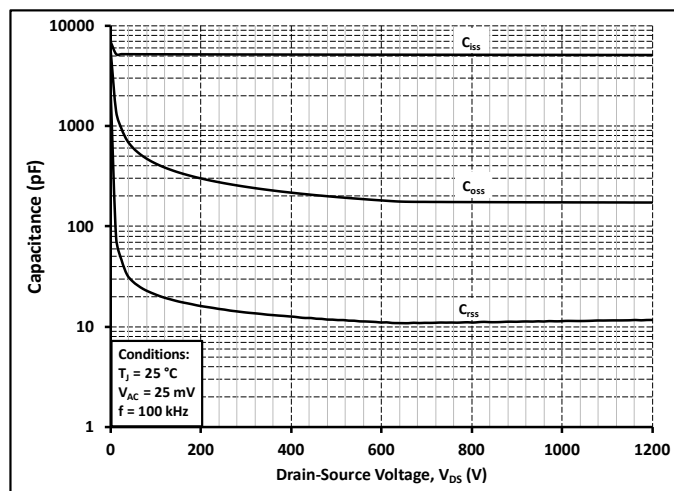


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)

## Typical Performance

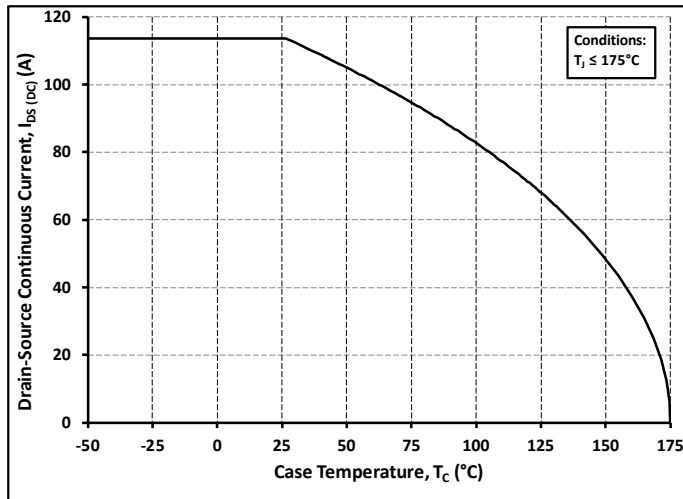


Figure 19. Continuous Drain Current Derating vs. Case Temperature

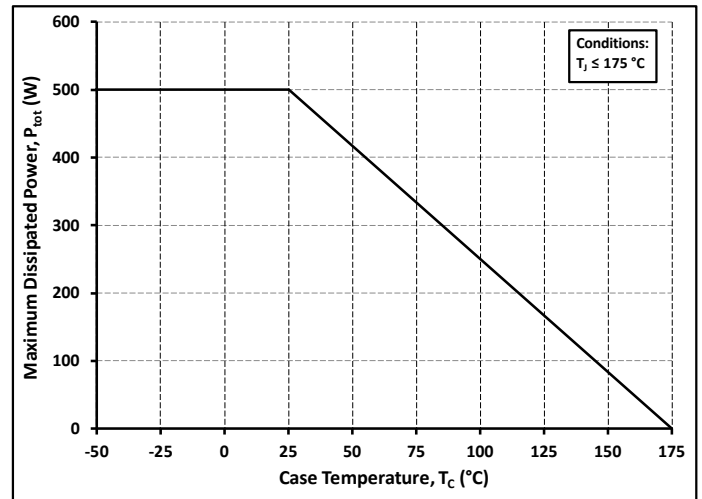


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

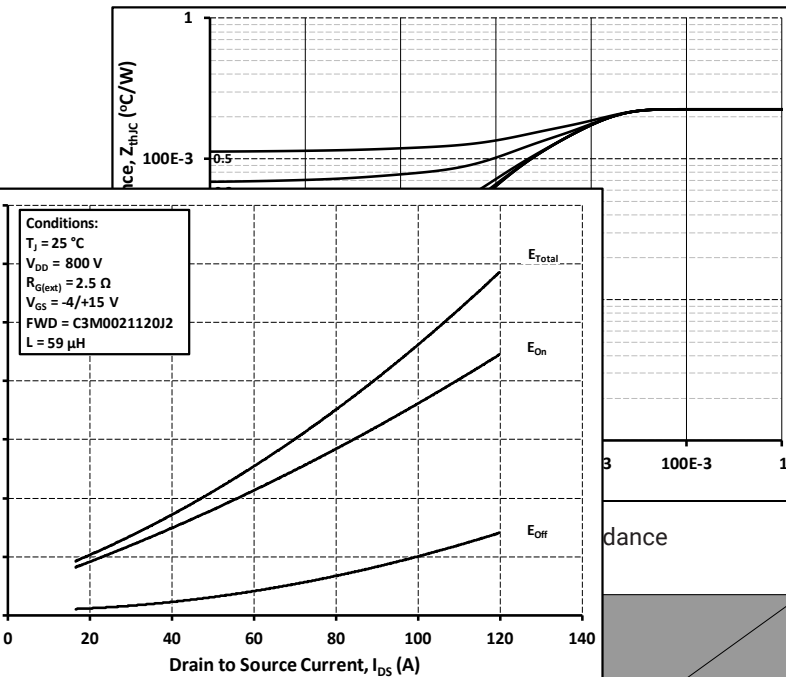
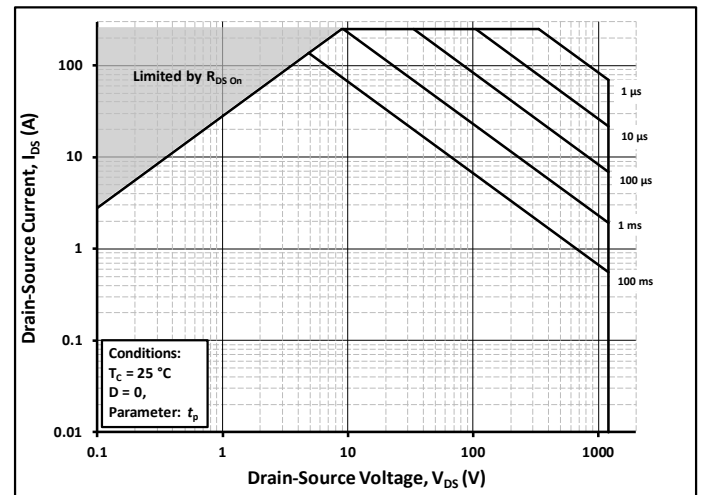
Figure 23. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 600V$ )

Figure 22. Safe Operating Area

Figure 24. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 800V$ )

## Typical Performance

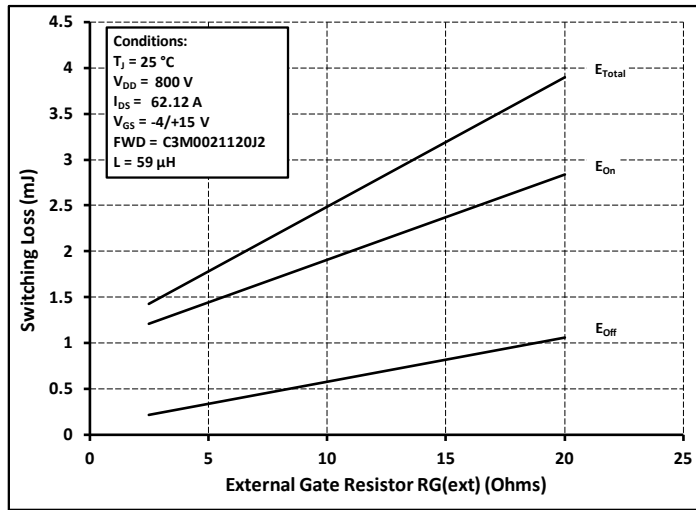
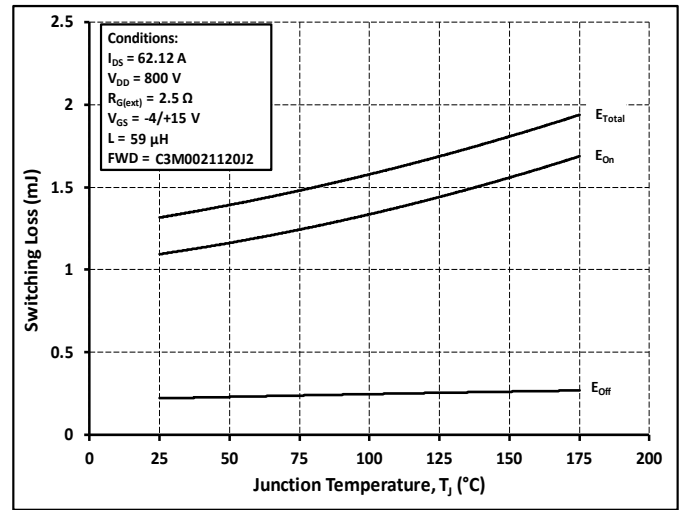
Figure 25. Clamped Inductive Switching Energy vs.  $R_{G(ext)}$ 

Figure 26. Clamped Inductive Switching Energy vs. Temperature

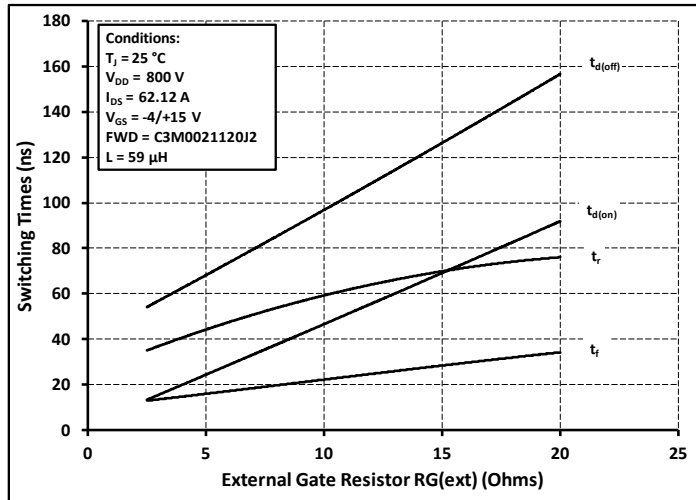
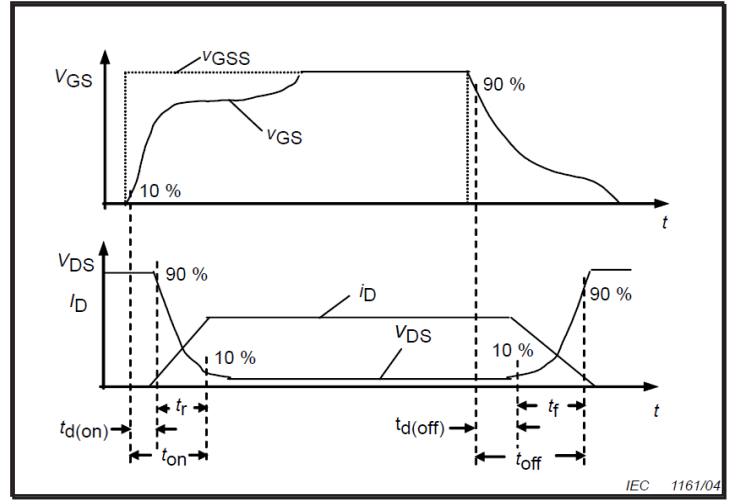
Figure 27. Switching Times vs.  $R_{G(ext)}$ 

Figure 28. Switching Times Definition

## Test Circuit Schematic

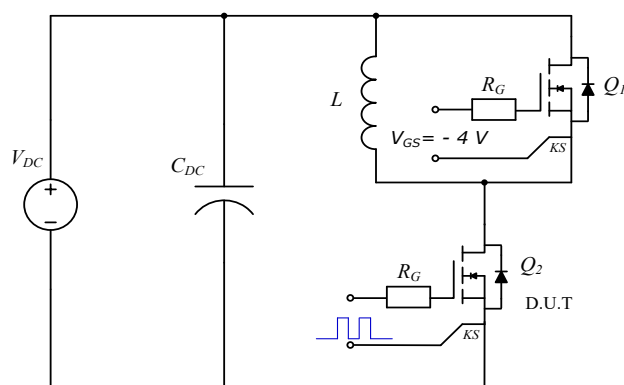
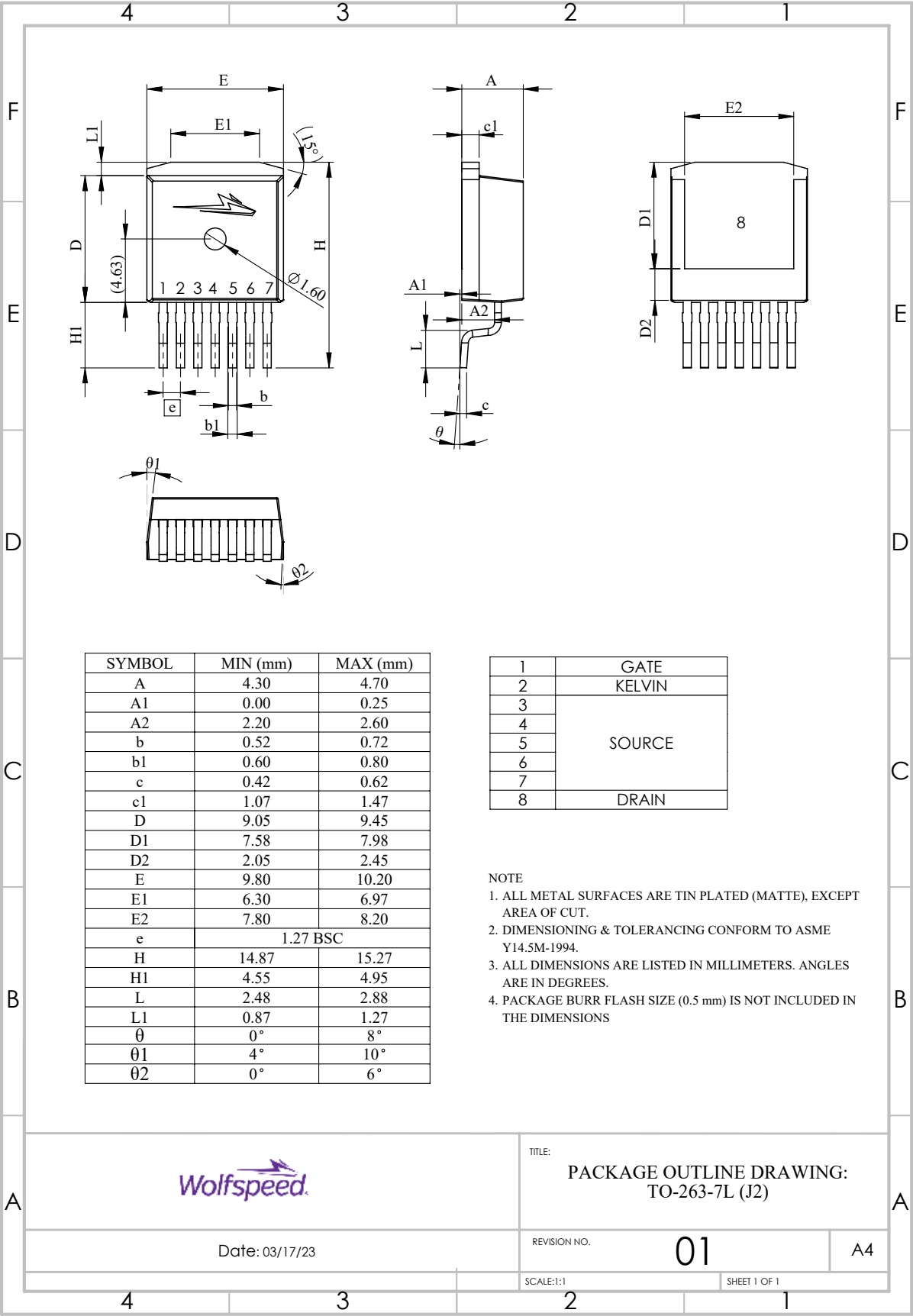


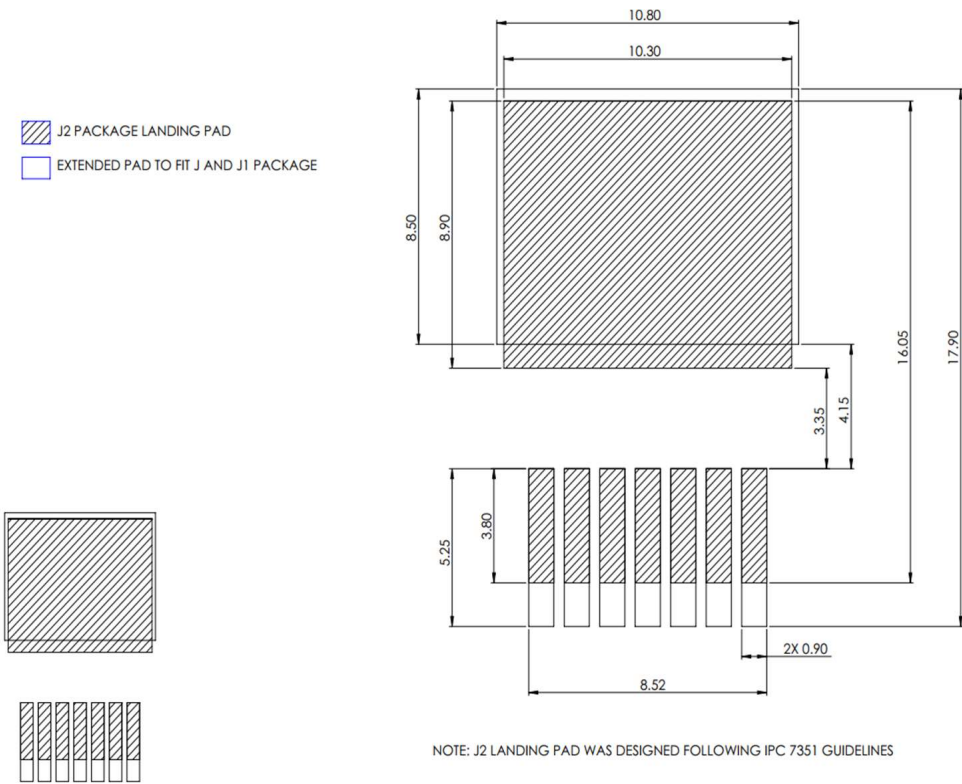
Figure 29. Clamped Inductive Switching  
Waveform Test Circuit

Package Dimensions



**Recommended Solder Pad Layout**

All dimensions in mm



**Revision history**

Document Version	Date of release	Descriptiion of changes
1	March 2024	Initial release
2	December 2024	Legal Disclaimer Updated



## Notes & Disclaimer

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