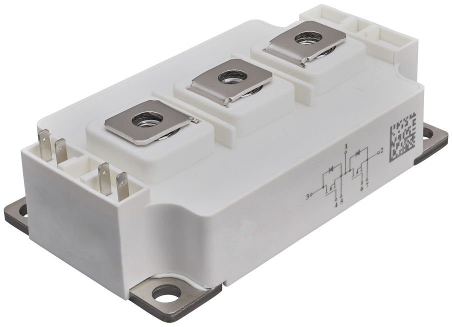
WAS110M12BM2

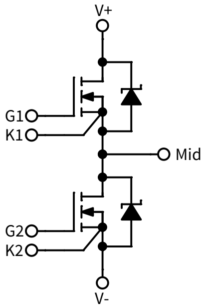
1200 V, 110 A, Silicon Carbide, Half-Bridge Module

V_{DS}	**1200 V**
I_{DS}	**110 A**

Technical Features

- Industry Standard 62 mm Footprint
- High Humidity Operation THB-80 (HV-H3TRB)
- Ultra Low Loss, High-Frequency Operation
- Zero Reverse Recovery from Diodes
- Zero Turn-off Tail Current from MOSFET
- Normally-off, Fail-safe Device Operation
- Copper Baseplate and Aluminum Nitride Insulator





Typical Applications

- Induction Heating
- Motor Drives
- Renewables
- Railway Auxiliary & Traction
- EV Fast Charging
- UPS and SMPS

System Benefits

- 62 mm Form Factor Enables System Retrofit
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Voltage	V_{DS}			1200	V	T_C = 25 °C	
Gate-Source Voltage, Maximum Value	$V_{GS(max)}$	-10		+25	V	Transient	Note 1 Fig. 33
Gate-Source Voltage, Recommended	$V_{GS(op)}$	-5		+20	V	Static	Note 1 Fig. 33
DC Continuous Drain Current	I_D		183		A	V_{GS} = 20 V, T_C = 25 °C, T_{VJ} ≤ 150 °C	Notes 2, 3 Fig. 21
			127		A	V_{GS} = 20 V, T_C = 90 °C, T_{VJ} ≤ 150 °C	Notes 2, 3 Fig. 21
DC Source-Drain Current (Schottky Diode)	$I_{SD(SD)}$		185		A	V_{GS} = -5 V, T_C = 25 °C, T_{VJ} ≤ 150 °C	Notes 2, 3 Fig. 21
Pulsed Drain-Source Current	I_{DM}		220		A	t_{Pmax} limited by T_{VJmax} V_{GS} = 20 V, T_C = 25 °C	Notes 2, 3 Fig. 21
Power Dissipation	P_D		723		W	T_C = 25 °C, T_{VJ} ≤ 150 °C	Note 4 Fig. 21
Virtual Junction Temperature	$T_{VJ(op)}$	-40		150	°C	Operation	
				175	°C	Intermittent with Reduced Life	

Note (1): Recommended turn-on gate voltage is 20 V with ±5 % regulation tolerance
Note (2): Current limit calculated by $I_{D(max)} = \sqrt{(P_D/R_{DS(typ)}(T_{VJ(max)},I_{D(max)}))}$
Note (3): Verified by design
Note (4): $P_D = (T_{VJ} - T_C)/R_{TH(JC,typ)}$

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MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
Gate Threshold Voltage	$V_{GS(th)}$	2.0	2.9	4.0		V_{DS} = V_{GS}, I_D = 30 mA	
Zero Gate Voltage Drain Current	I_{DSS}		4	1200	µA	V_{GS} = 0 V, V_{DS} = 1200 V	
Gate-Source Leakage Current	I_{GSS}			1200	nA	V_{GS} = 20 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		12.5	17.0	mΩ	V_{GS} = 20 V, I_D = 100 A	Fig. 2 Fig. 3
			21.5			V_{GS} = 20 V, I_D = 110 A, T_{VJ} = 150 °C	
Transconductance	g_{fs}		57.2		S	V_{DS} = 20 V, I_D = 110 A	Fig. 4
			56.7			V_{DS} = 20 V, I_D = 110 A, T_{VJ} = 150 °C	
Turn-On Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C	E_{ON}		1.47 1.34 1.29		mJ	V_{DD} = 600 V, I_D = 110 A, V_{GS} = -5 V/20 V, $R_{G(ext)}$ = 0.0 Ω, L = 22.2 µH	Fig. 11 Fig. 13
Turn-Off Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C	E_{OFF}		1.02 1.08 1.10				
Internal Gate Resistance	$R_{G(int)}$		8.1		Ω	f = 100 kHz	
Input Capacitance	C_{iss}		6.2		nF	V_{GS} = 0 V, V_{DS} = 800 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		0.9				
Reverse Transfer Capacitance	C_{rss}		42		pF		
Gate to Source Charge	Q_{GS}		92		nC	V_{DS} = 800 V, V_{GS} = -5 V/20 V, I_D = 100 A, Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		100				
Total Gate Charge	Q_G		322				
FET Thermal Resistance, Junction to Case	$R_{th\ JC}$		0.173		°C/W		Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Diode Forward Voltage	V_F		1.62		V	V_{GS} = -5 V, I_F = 110 A, T_{VJ} = 25 °C	Fig. 7
			2.23			V_{GS} = -5 V, I_F = 110 A, T_{VJ} = 150 °C	
Reverse Recovery Time	t_{RR}		20.2		ns	V_{GS} = -5 V, I_{SD} = 110 A, V_R = 600 V di/dt = 22 A/ns, T_{VJ} = 150 °C	Fig. 32
Reverse Recovery Charge	Q_{RR}		1.56		µC		
Peak Reverse Recovery Current	I_{RRM}		127		A		
Reverse Recovery Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C	E_{RR}		0.41 0.48 0.48		mJ	V_{DS} = 600 V, I_D = 110 A, V_{GS} = -5 V/20 V, $R_{G(ext)}$ = 0.0 Ω, L = 22.2 µH	Fig. 14 Note 5
Diode Thermal Resistance, JCT. to Case	$R_{th\ JC}$		0.213		°C/W		Fig. 18

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Package Resistance, M1 (High-Side)	R_{3-1}		0.60		µΩ	T_C = 25 °C, I_{SD} = 110 A, Note 6
Package Resistance, M2 (Low-Side)	R_{1-2}		0.51			T_C = 125 °C, I_{SD} = 110 A, Note 6
Stray Inductance	L_{Stray}		13.5		nH	Between DC- and DC+, f = 10 MHz
Case Temperature	T_C	-40		125	°C	
Mounting Torque	M_S	4	5	5.5	N-m	Baseplate, M6-1.0 Bolts
		4	5	5.5		Power Terminals, M6-1.0 Bolts
Weight	W		300		g	
Case Isolation Voltage	V_{isol}	5			kV	AC, 50 Hz, 1 minute
Clearance Distance		9			mm	Terminal to Terminal
		30				Terminal to Baseplate
Creepage Distance		30				Terminal to Terminal
		40				Terminal to Baseplate

Note (6): Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance

Typical Performance

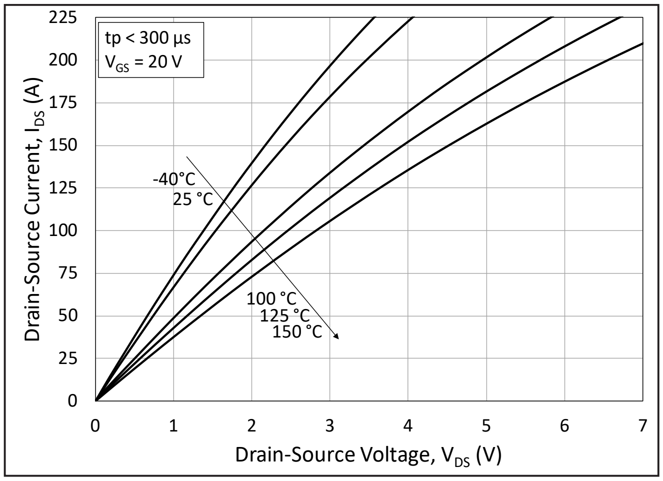


Figure 1. Output Characteristics for Various Junction Temperatures

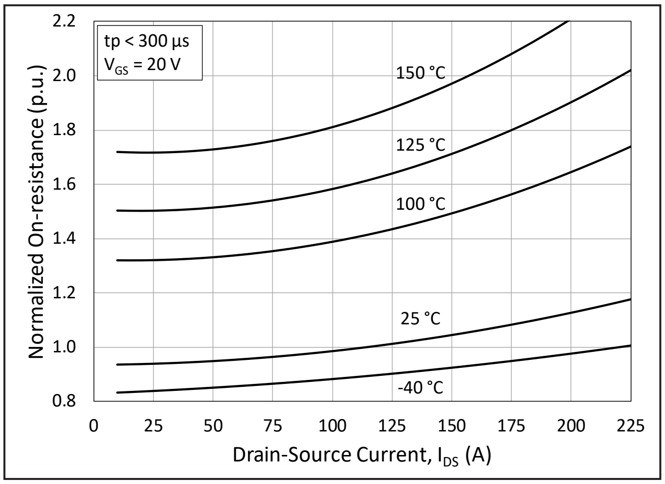


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

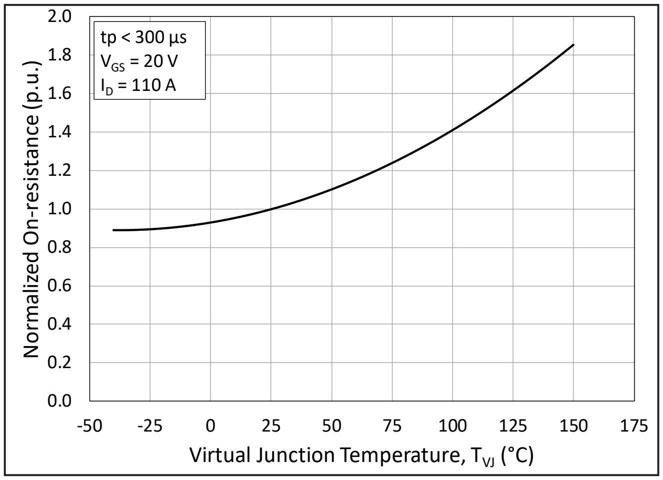


Figure 3. Normalized On-State Resistance vs. Junction Temperature

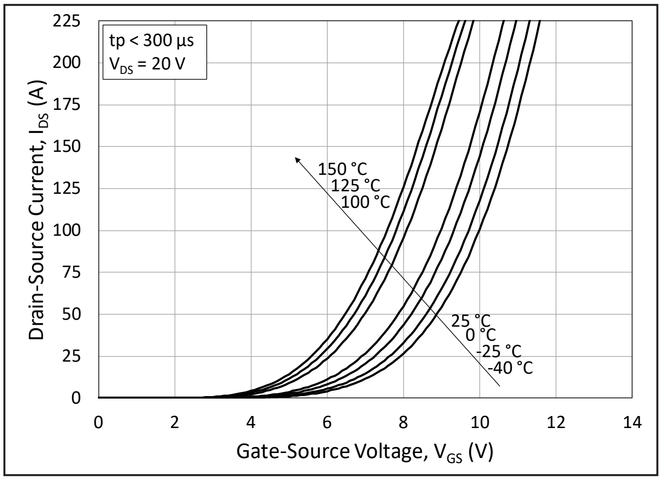


Figure 4. Transfer Characteristic for Various Junction Temperatures

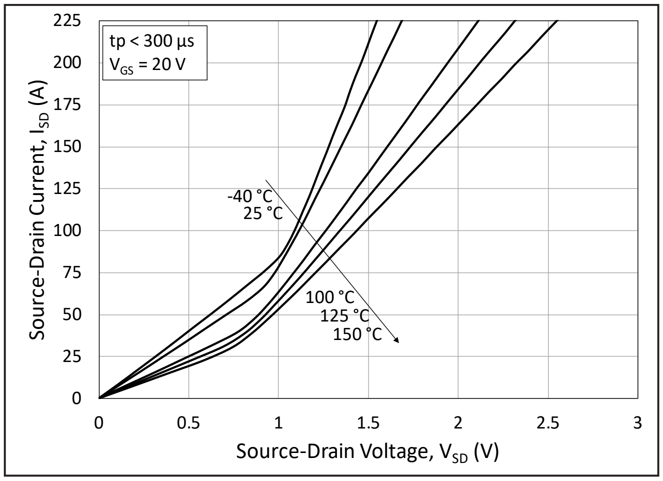


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 20 V

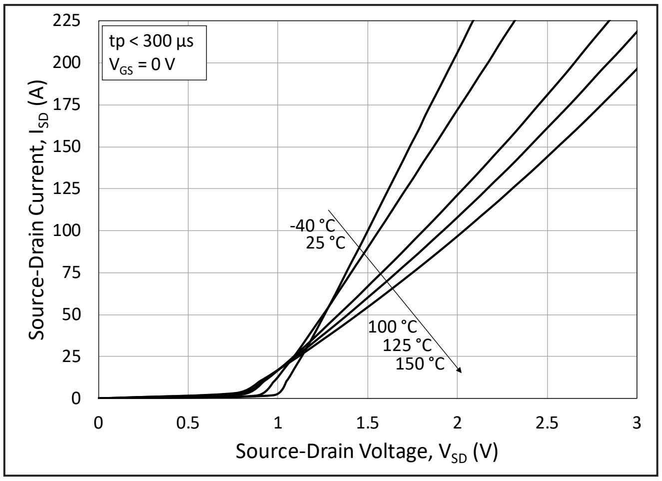


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Diode)

Typical Performance

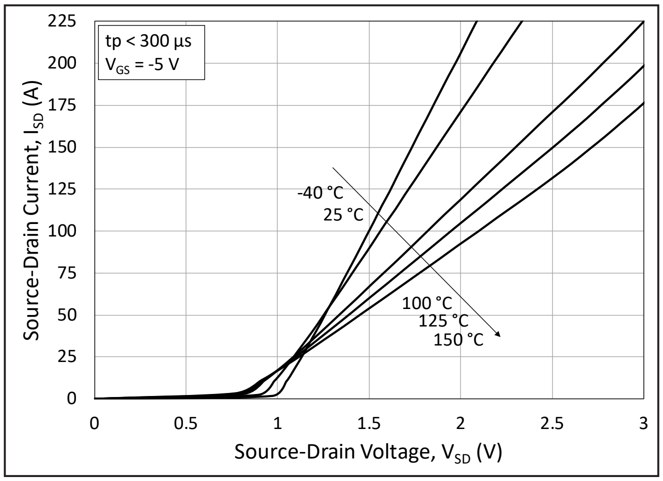


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = -5 V (Diode)

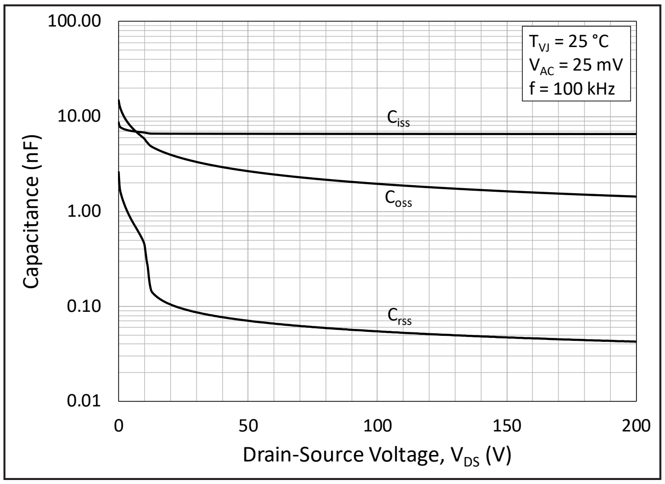


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200 V)

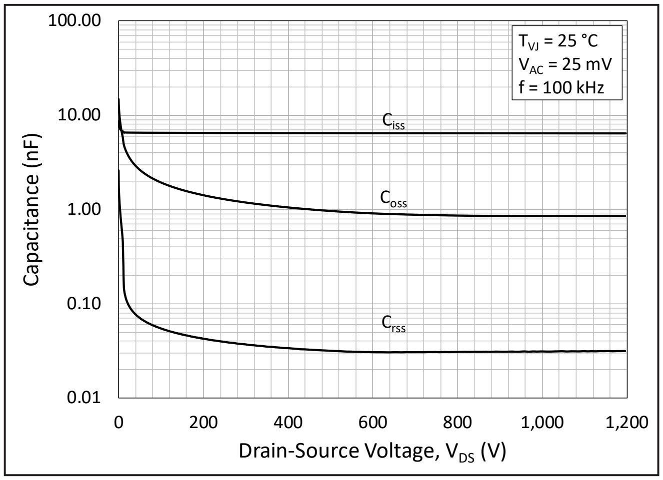


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200 V)

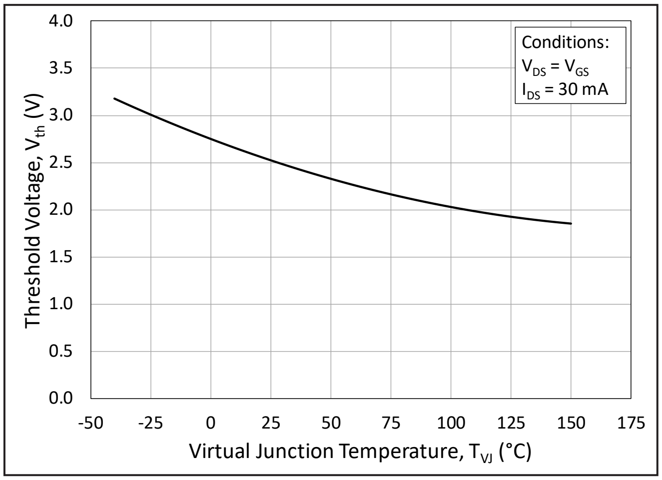


Figure 10. Threshold Voltage vs. Junction Temperature

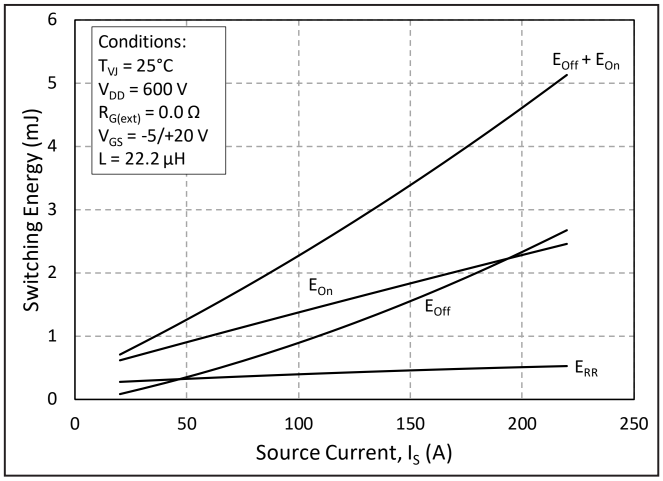


Figure 11. Switching Energy vs. Drain Current (V_{DS} = 600 V)

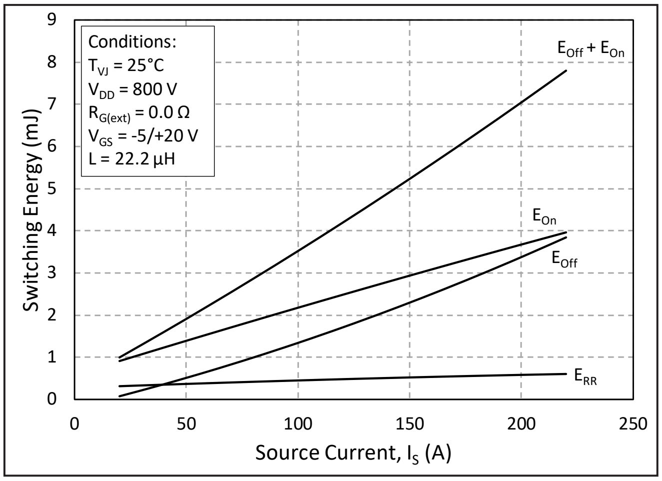


Figure 12. Switching Energy vs. Drain Current (V_{DS} = 800 V)

Typical Performance

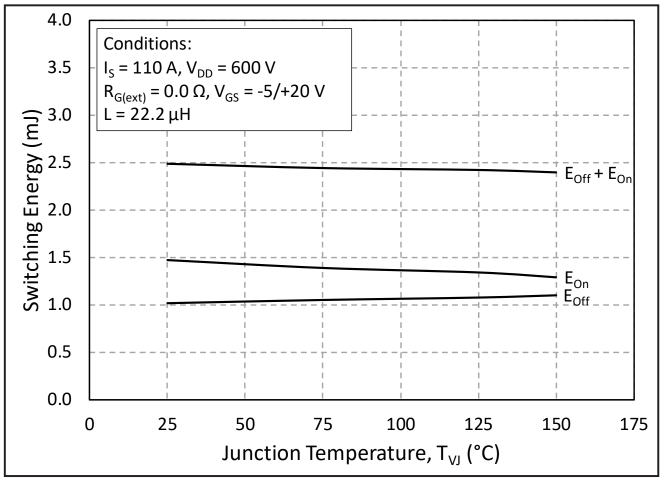


Figure 13. MOSFET Switching Energy vs. Junction Temperature

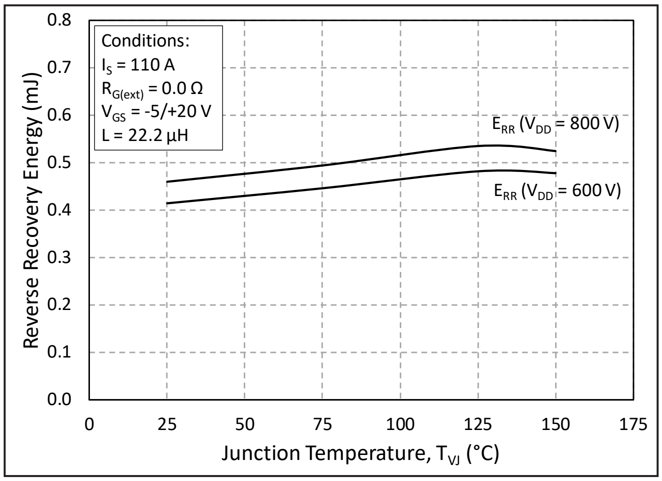


Figure 14. Reverse Recovery Energy vs. Junction Temperature

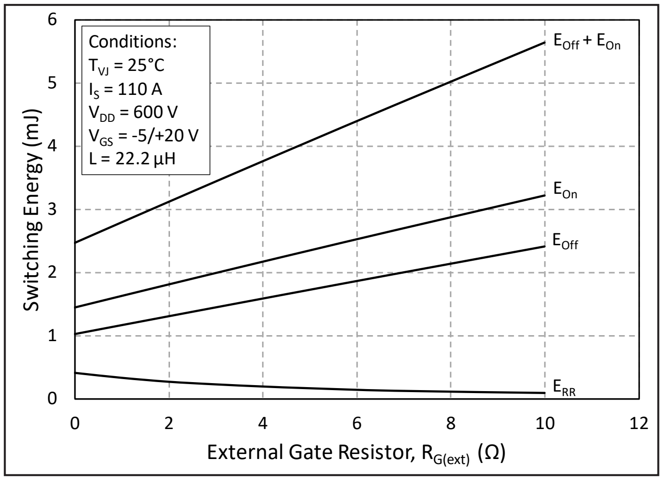


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

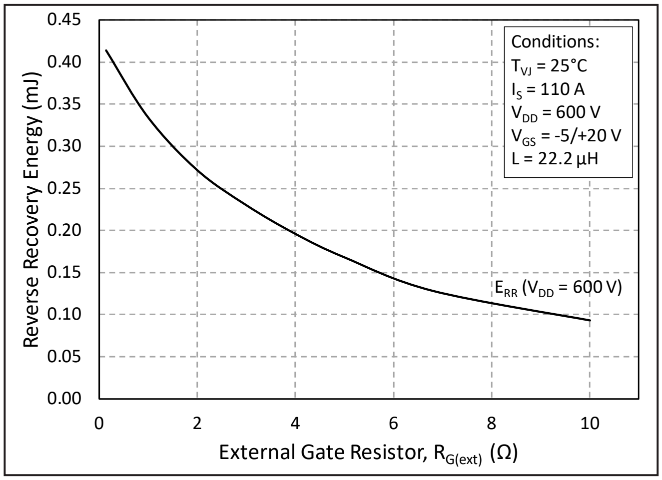


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

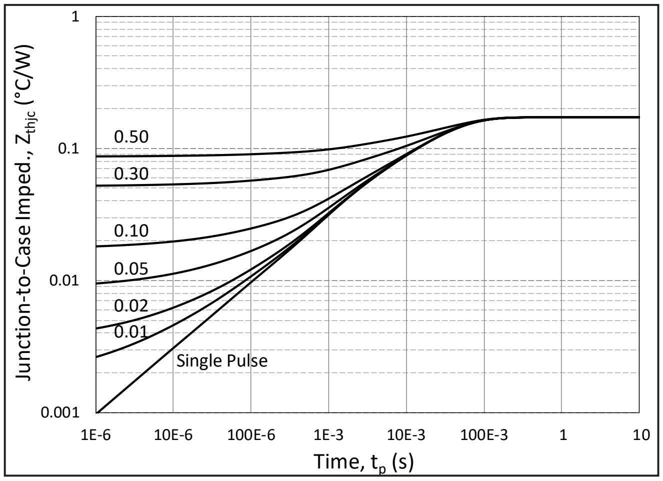


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, $Z_{th,jc}$ (°C/W)

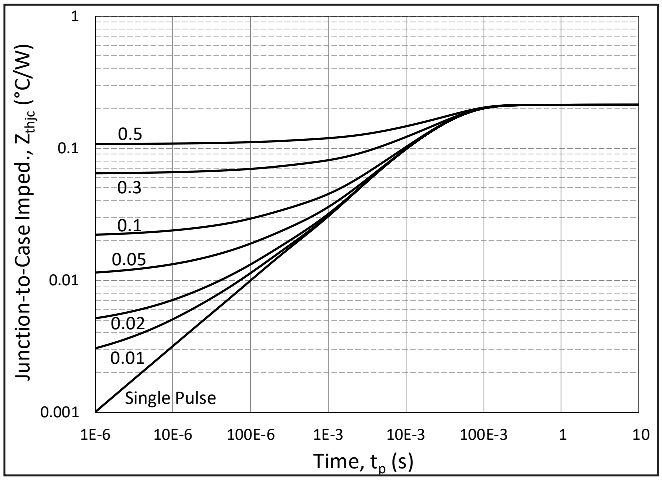


Figure 18. Diode Junction to Case Transient Thermal Impedance, $Z_{th,jc}$ (°C/W)

Typical Performance

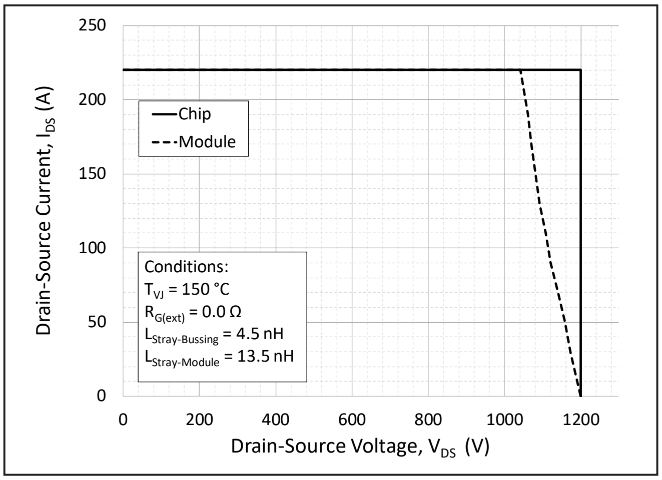


Figure 19. Switching Safe Operating Area

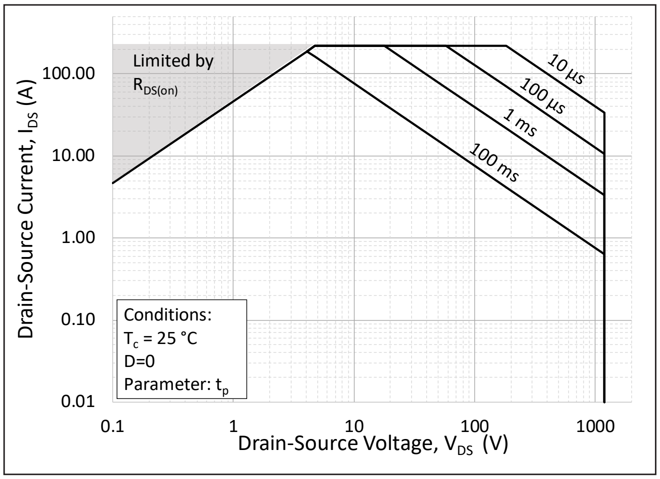


Figure 20. Forward Bias Safe Operating Area (FBSOA)

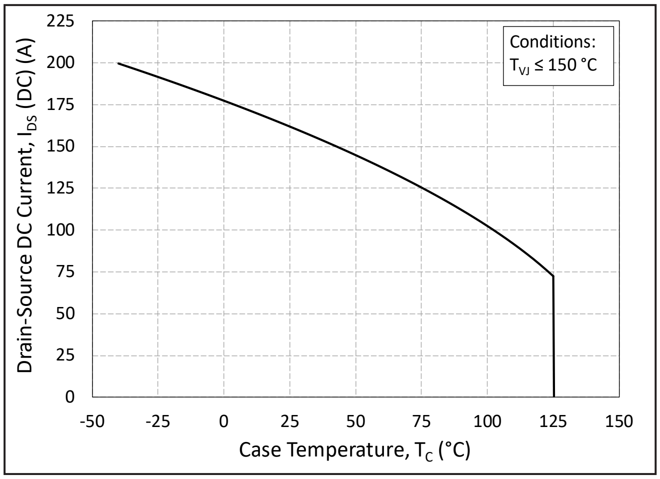


Figure 21. Continuous Drain Current Derating vs. Case Temperature

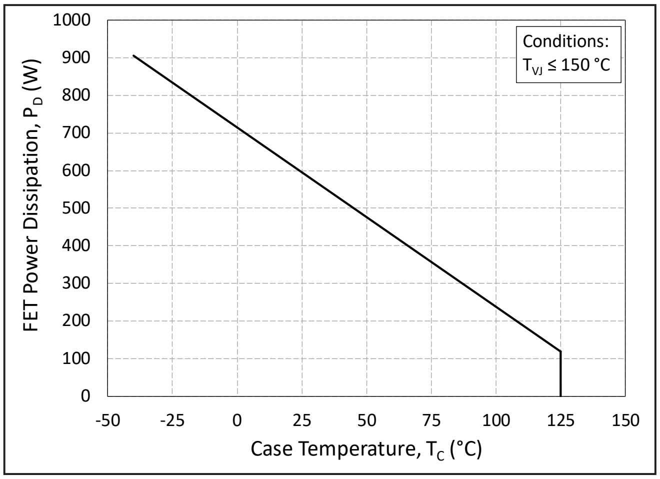


Figure 22. Maximum Power Dissipation Derating vs Case Temperature

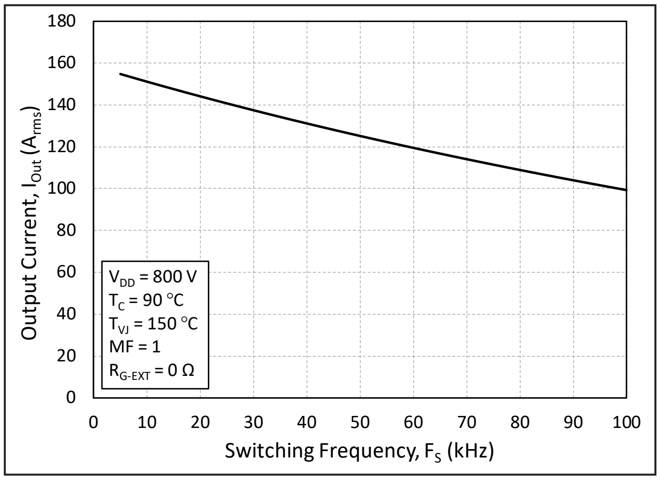


Figure 23. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

Timing Characteristics

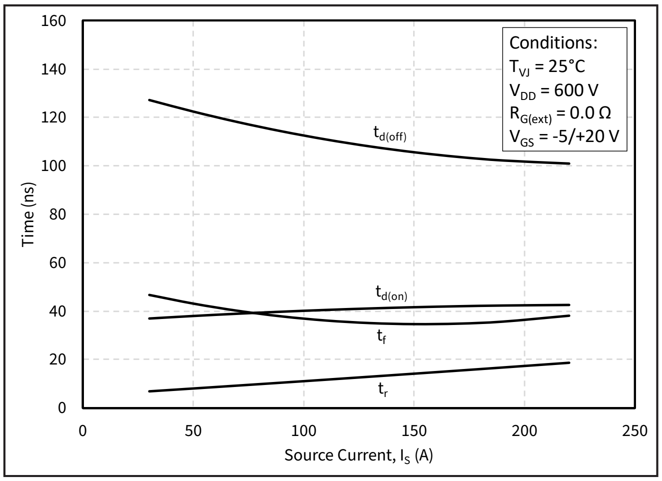


Figure 24. Timing vs. Source Current

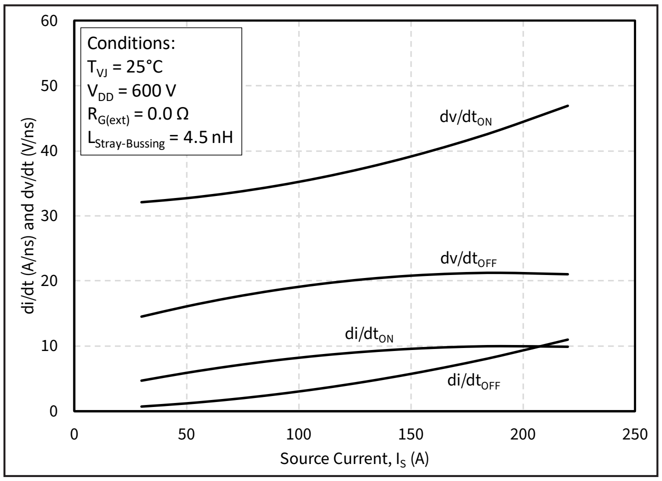


Figure 27. dv/dt and di/dt vs. Source Current

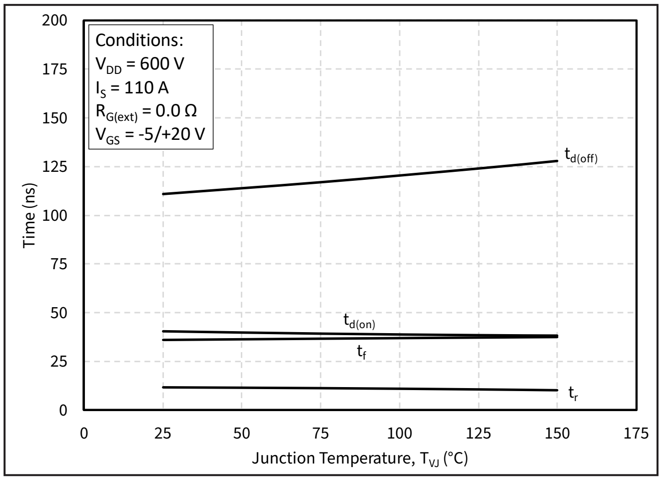


Figure 26. Timing vs. Junction Temperature

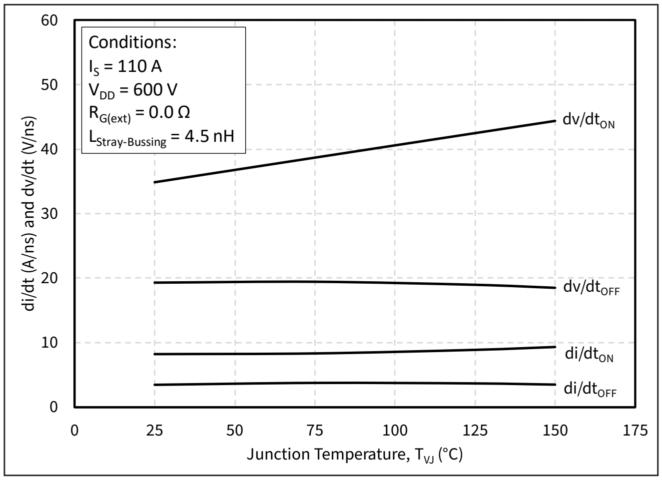


Figure 27. dv/dt and di/dt vs. Junction Temperature

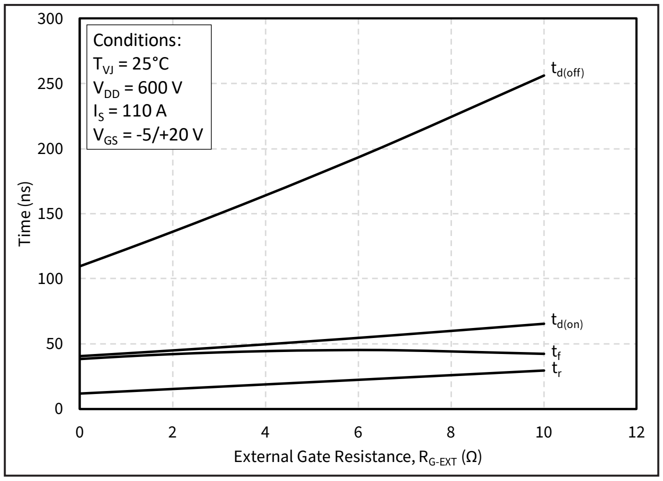


Figure 28. Timing vs. External Gate Resistance

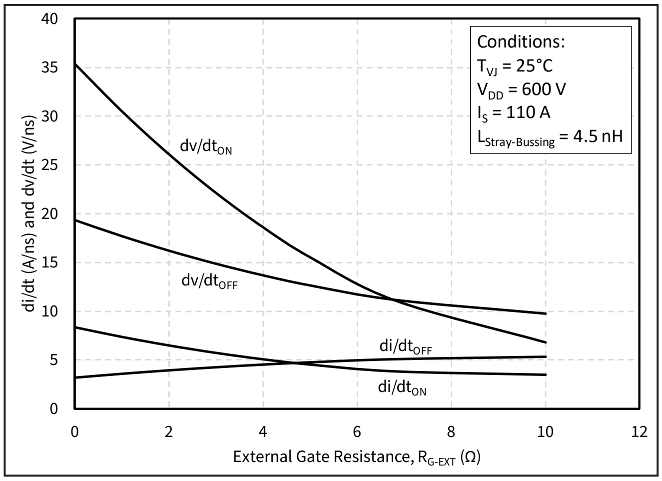


Figure 29. dv/dt and di/dt vs. External Gate Resistance

Definitions

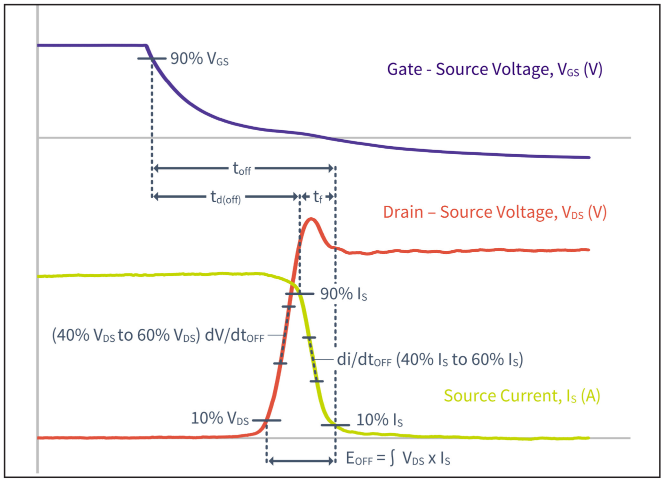


Figure 30. Turn-Off Transient Definitions

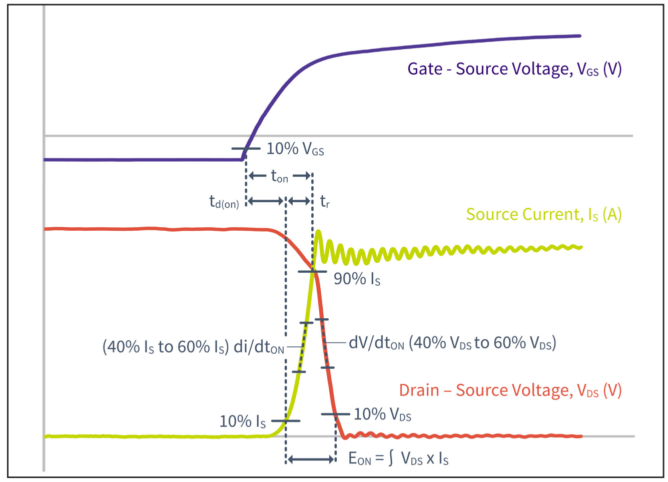


Figure 31. Turn-On Transient Definitions

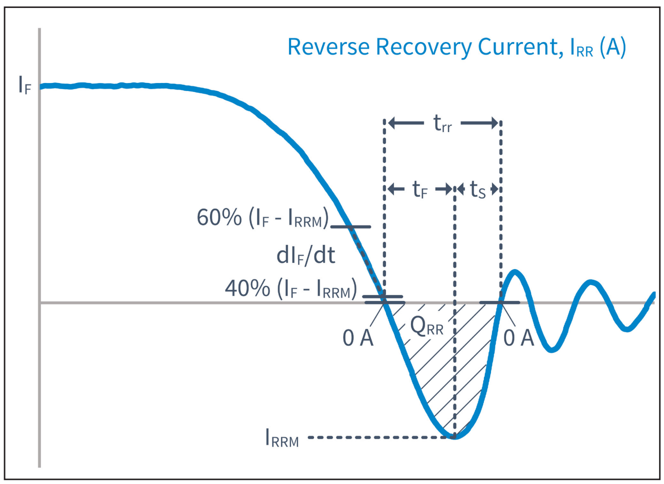


Figure 32. Reverse Recovery Definitions

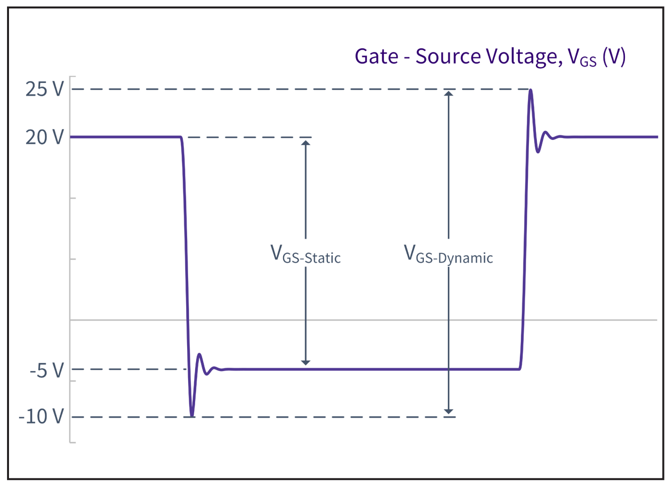
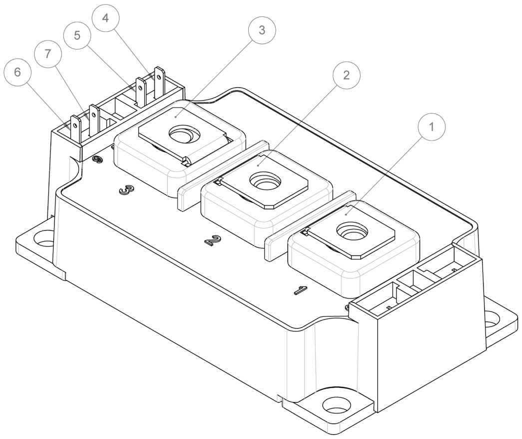
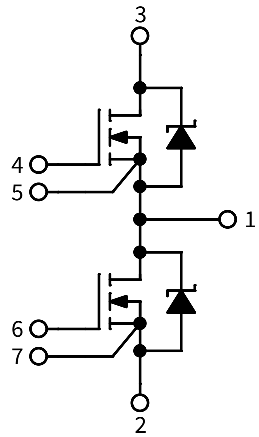


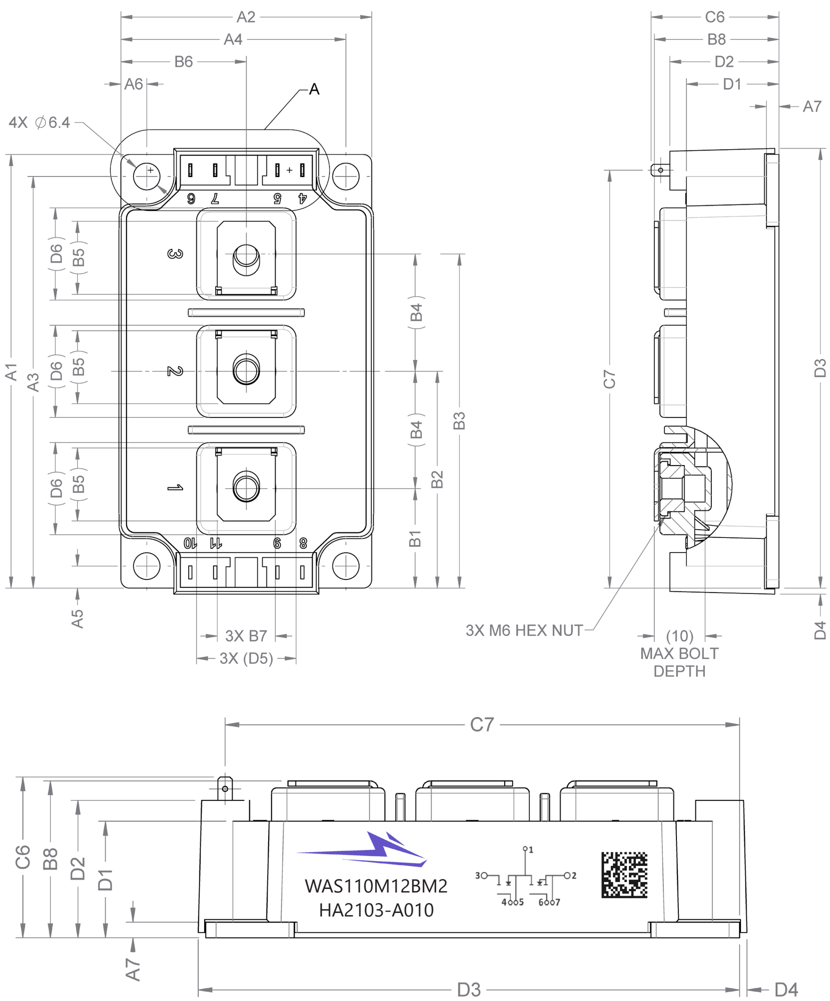
Figure 33. V_{GS} Transient Definitions

Schematic and Pin Out

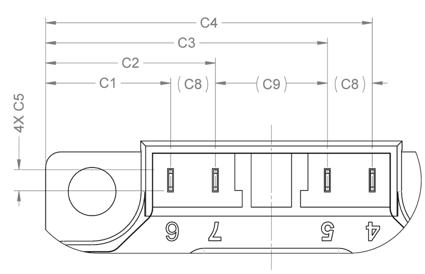




Package Dimension (mm)



DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	103.5	±0.30
A2	60.44	±0.30
A3	98.25	±0.30
A4	54.22	±0.30
A5	5.25	±0.30
A6	6.22	±0.30
A7	3	±0.30
B1	23.75	±0.40
B2	51.75	±0.40
B3	79.75	±0.40
B4	(28)	REF.
B5	(17.43)	REF.
B6	30.23	±0.40
B7	(14)	REF.
B8	30.03	±0.40
C1	16.73	±0.40
C2	22.73	±0.40
C3	37.73	±0.40
C4	43.73	±0.40
C5	2.8	±0.40
C6	30.8	±0.50
C7	99.75	±0.40
C8	(6)	REF.
C9	(15)	REF.
D1	22.3	±0.30
D2	26.3	±0.30
D3	104.95	±0.30
D4	1.45	±0.40
D5	(24)	REF.
D6	(22)	REF.



DETAIL A
SCALE 3 : 1

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Supporting Links & Tools

Simulation Tools & Support

- PLECS Models
- LTSpice Models
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum

Compatable Evaluation Hardware

- CGD1200HB2P-BM2: Dual Channel Differential Isolated Half Bridge Gate Driver Board
- KIT-CRD-CIL12N-BM: Dynamic Performance Evaluation Board for the BM2 and BM3 Module
- CGD1700HB2P-BM2: Evaluation Gate Driver Tool Optimized for the 1700 V BM2 Power Modules
- KIT-CRD-CIL17N-BM: Dynamic Characterization Evaluation Tool Optimized for 1700 V BM Power Modules
- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

Application Notes

- PRD-07933: Wolfspeed Power Module Thermal Interface Material Application User Guide
- PRD-06379: Environmental Considerations for Power Electronics
- PRD-08710: Measuring Stray Inductance in Power Electronic Systems
- PRD-07845: Power Module Baseplate Capacitance and Electromagnetic Compatibility
- PRD-08376: Thermal Characterization Methods and Applications
- PRD-06933: Capacitance Ratio and Parasitic Turn-On

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