Application Note **PRD-06701**

Thermal Management of Bottom-Side Cooled Surface-Mount Devices and Design Considerations

Introduction

Thermal design is an important consideration for power devices. With a trend to push power levels, power density, and efficiency higher in power converters, surface-mount power switches are gaining popularity due to their small form factor and ease of manufacturing. This application note discusses important design considerations for the thermal design of Wolfspeed's discrete bottom-side cooled device portfolio to extract the best performance out of these devices. It will discuss the importance of selecting the right device package and following the recommended soldering profile, Printed Circuit Board (PCB) design, thermal interface material, and heatsink mounting. The PCB thermal impedance plays a critical role in bottom-side cooled devices, so it is important to consider the thermal impedance when optimizing footprint and the number of vias required, which also impact the cost.

Contents

1. Bottom-Side Cooled Surface Mount Discrete Device

Wolfspeed has a wide bottom-side cooled Surface-Mount Discrete Device portfolio including SiC MOSFETs and SiC Schottky diodes. Figure 1 shows the available SiC MOSFET packages and portfolios.

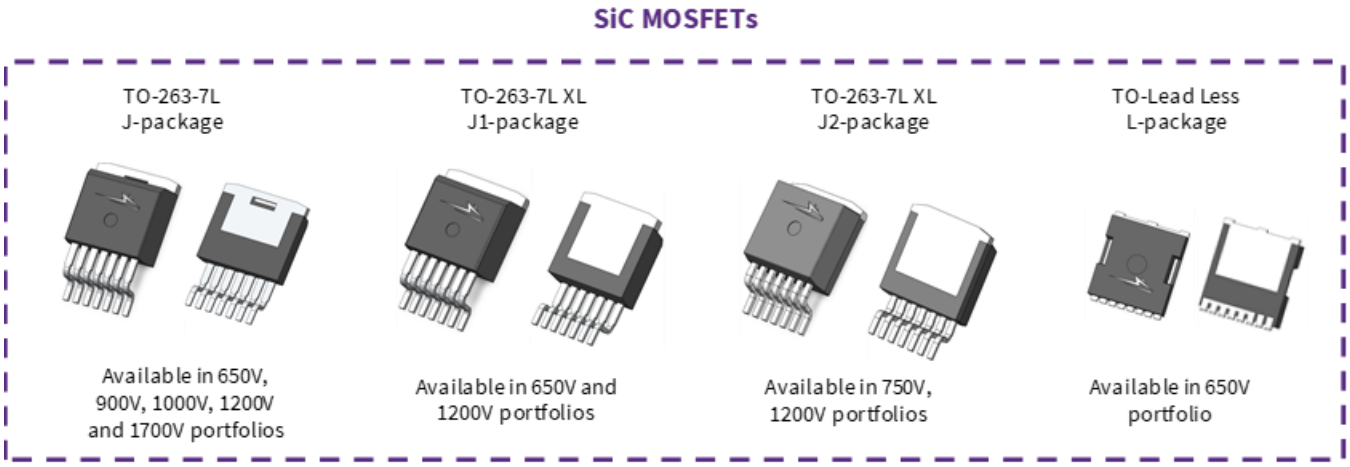


Figure 1: Wolfspeed Bottom-Side Cooled SiC Discrete MOSFET Portfolio

Along with the maximum junction temperature rating of the device (T_{jmax}), thermal management of MOSFETs is crucial; as seen in Figure 2, two of the critical parameters that define the performance of the power MOSFET in a power converter increase with junction temperature (T_j). The $R_{DS(ON)}$ of the device dictates the device's conduction losses, which is the dominant source of power loss at higher power levels. Thankfully, Wolfspeed SiC devices have a low $R_{DS(ON)}$ temperature coefficient which means the $R_{DS(ON)}$ does not increase significantly with T_j.

The total switching loss also increases slightly with T_j, but since the total power losses at higher power levels are dominated by conduction losses, the increase in switching loss becomes less significant. To extract the best performance out of SiC devices and keep power losses at a minimum, it becomes very important to have a good thermal management system that will keep the junction temperature as low as possible.

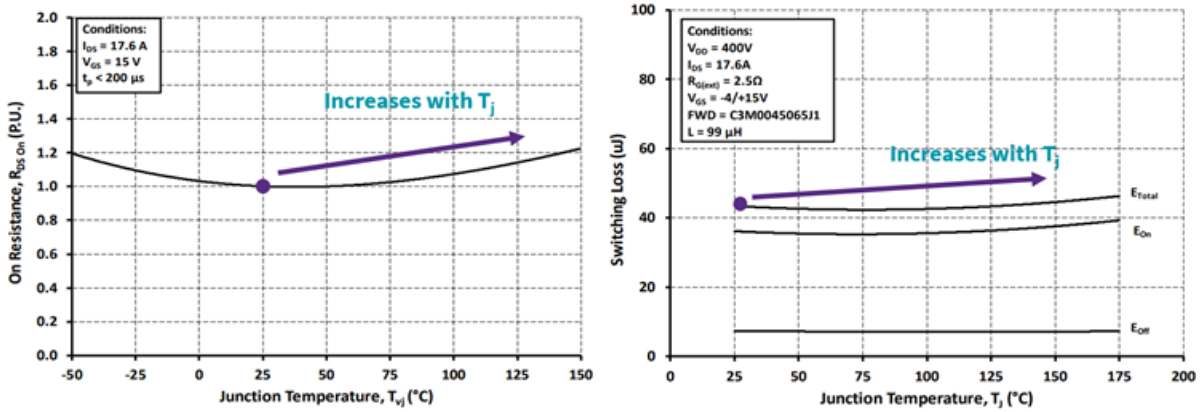


Figure 2: Wolfspeed 650V SiC MOSFET $R_{ds(on)}$ vs T_j and Switching Loss vs T_j

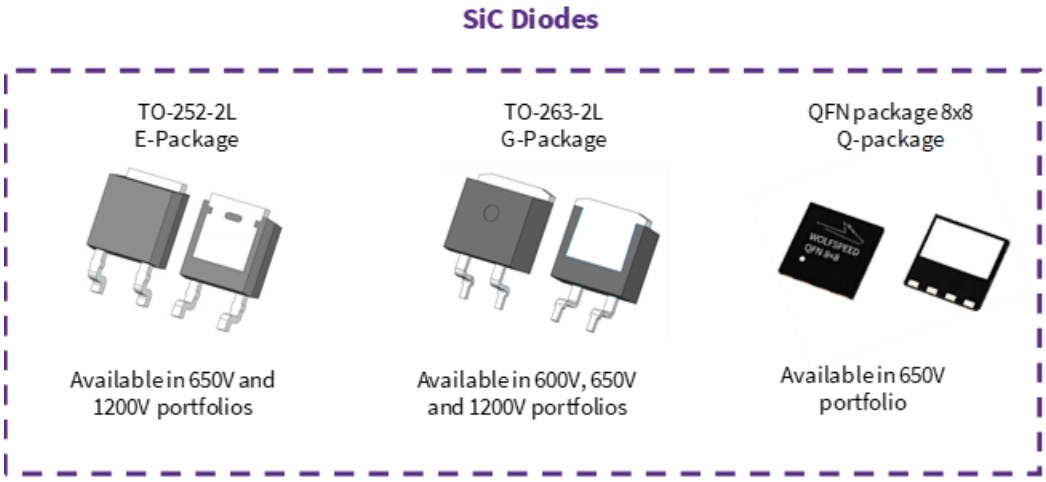


Figure 3: Wolfspeed Bottom-Side Cooled Discrete SiC Schottky Diode Portfolio

The reverse leakage current I_R in diodes increases with increasing junction temperature T_j as seen in Figure 4. The reverse losses given by,

$$P_{rev} = \frac{1}{T_{sw}} \int_0^{T_{sw}} V_R(t).\, I_R(V_R.T_j)\,.\,\mathrm{dt}$$

Where, T_{sw} is the switching period and V_R is the reverse voltage, also increase with the increasing T_j. Therefore, to keep the reverse losses at a minimum and the efficiency as high as possible, devices should be operated at lower temperatures.

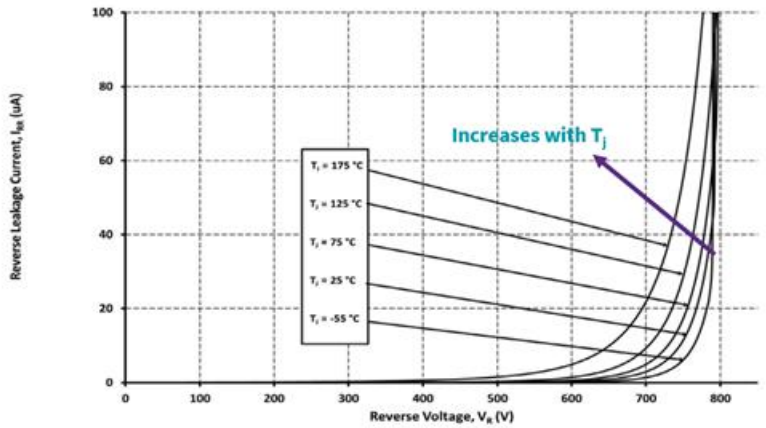


Figure 4: Wolfspeed SiC Schottky Diode Reverse Leakage Current vs Reverse Voltage at various T_j

The maximum junction temperatures T_{jmax} of all Wolfspeed surface-mount discrete packages are 150-175°C (refer to the datasheet for the exact value). Customers are advised to take their application's thermal cycling profile into account and consider a T_{jmax} derating depending on that profile and the system in general.

Thermal management is transferring the heat produced in the die of the power device to the ambient atmosphere. Ideally, this transfer should be done with good thermal conductivity and minimal thermal resistance ($R_{\theta, JA}$) in the heat flow path shown in Figure 5. For Wolfspeed bottom-side cooled SMDs the drain pad is also a thermal pad (case) directly connected to the die, which is used for heat transfer. The devices are packaged to provide a low $R_{\theta, JC}$,

$R_{\theta, JC}$= Thermal resistance from Junction to Case (°C/W)

The drain (case) is soldered onto the top copper layer of the PCB,

$R_{\theta, solder}$= Thermal resistance of the solder (°C/W)

The thermal vias in the PCB transfer the heat from the case to the heatsink through the PCB,

$R_{\theta, PCB}$ = Thermal resistance of the PCB (°C/W)

A Thermal Interface Material (TIM) that provides electrical isolation and good thermal conductivity from the board to the heatsink is used between the PCB and heatsink,

$R_{\theta, TIM}$ = Thermal resistance of the TIM (°C/W)

Finally, the heatsink transfers the heat to the ambient atmosphere,

$R_{\theta, HA}$= Thermal resistance from Heatsink to Ambient (°C/W)

The Junction Temperature of the device can be estimated as:

$$R_{\theta, JA} = R_{\theta, JC} + R_{\theta, solder} + R_{\theta, PCB} + R_{\theta, TIM} + R_{\theta, HA}$$

$$T_j = P_{LOSS} \times R_{\theta, JA} + T_{AMB}$$

where,

- $R_{\theta, JA}$ is the total thermal resistance from Junction to Ambient
- P_{LOSS} is the total power dissipation of the device
- T_{AMB} is the ambient temperature
- The total heat dissipated from the top side of the package is very low

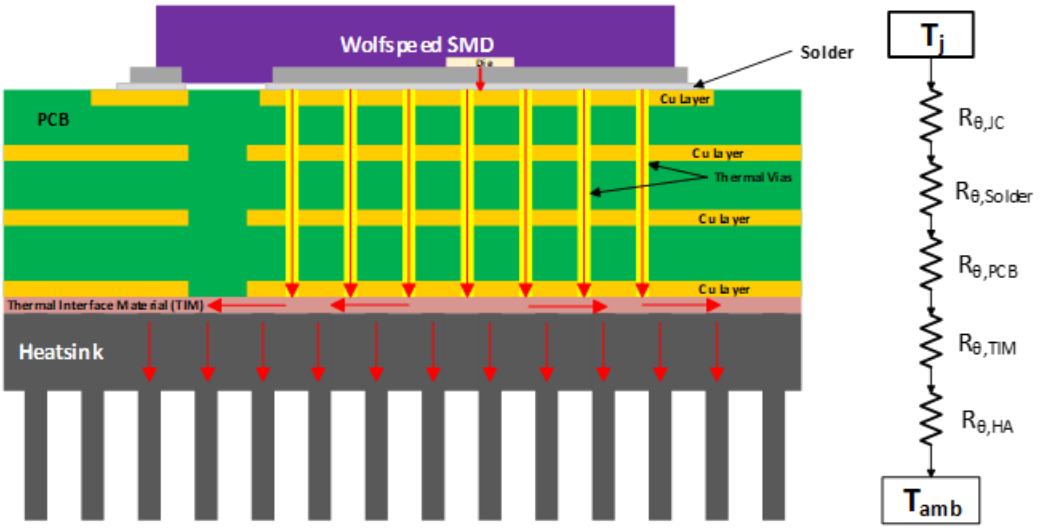


Figure 5: Bottom-Side Cooled Surface Mount Device Heat Flow Path

2. Design Considerations

2.1 Device Package ($R_{\Theta, JC}$)

Wolfspeed SMDs have low thermal impedance with large thermal pad areas for effective heat transfer. Typical thermal resistances from Junction to Case $R_{\theta, JC}$ for the following MOSFET packages for a 650V and 750V, similar $R_{DS(ON)}$ device are:

- J-package ($R_{DS(ON)}$= 60mΩ): 1.1°C/W
- J1-package ($R_{DS(ON)}$= 45mΩ): 0.85°C/W
- J2-package ($R_{DS(ON)}$= 45mΩ): 0.83°C/W
- TOLL- package ($R_{DS(ON)}$= 45mΩ): 0.64°C/W

Figure 6 shows the thermal pad areas of these MOSFETs.

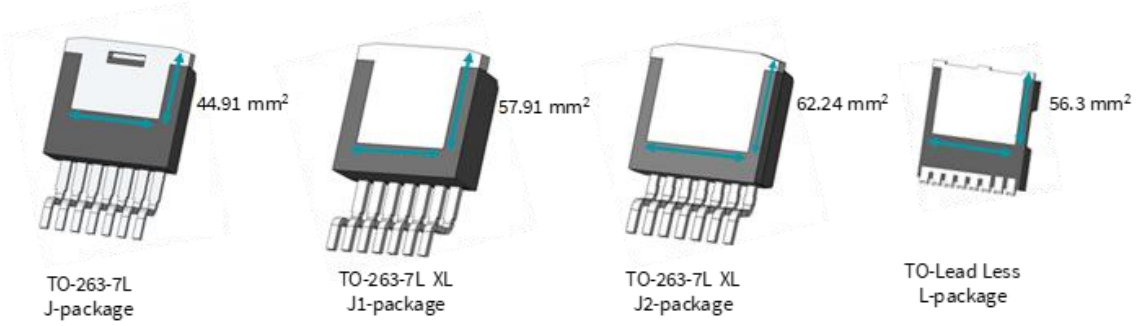


Figure 6: Thermal Pad Area of Wolfspeed's SMD MOSFETs

Wolfspeed's 7-lead MOSFET packages product line evolves with performance, efficiency and the market need. J-package is the original TO-263-7L package offered by Wolfspeed. Followed by the introduction of the J1-package with the larger drain pad area than J and could provide lower $R_{DS(ON)}$ devices, Wolfspeed is coming up

with a new J2-package that offers even larger drain pad area and lower $R_{DS(ON)}$ (15mOhm) devices to be more compatible with competitors part numbers.

Along with Wolfspeed's bottom-side cooled 7-lead packages, competitors' parts in TO-263-7 package are studied and compared depending on their footprints and landing areas. This comparison for the TO-263-7 packages is given as follows in Table 1.

Landing pads for Wolfspeed's SMD and competitor's 7 lead package is given in Figure 7.

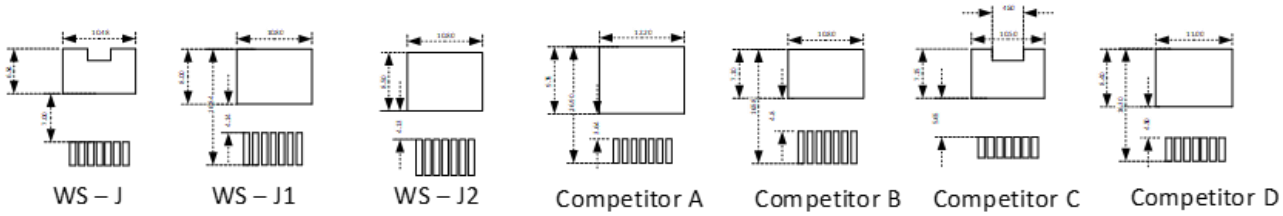


Figure 7: Landing pad Information for Wolfspeed's SMD MOSFETs and Competitor's 7-lead Packages

Table 1: Comparison of TO-263-7 Packages

Item All dimensions in mm	WS-J	WS-J1	WS-J2	Competitor A	Competitor B	Competitor C	Competitor D
Device Length	16.178	16.178	15.07	15	15	15.4	15.4
Device Width	10.18	10.18	10	10.2	10	9.90	10.2
Device Height	4.435	4.435	4.5	4.55	4.4	4.5	4.5
Drain Pad Length - Device	6.218	8.018	7.78	7.05	6	6.8	7.8
Contact Pin Length - Device	2.512	2.7	2.7	2.2	2.7	2.64	2.3
Creepage on Device	6.87	4.83	4.65	5.7*	6.65	6	5.4
Creepage on Board (Based on Recommended Landing Pad)	6.99	4.15	4.15	3.65	4.8	5.65	4.5
Drain Solder Pad Length - PCB	6.538	8.0	8.5	9.75	7.1	7.15	8.4
Drain Solder Pad Width - PCB	10.480	10.8	10.8	12.20	10.8	10.50	11.0
Contact Pin Solder Pad Length - PCB	3.4	4.7	5.25	3.5	4.7	3	3.4
Contact Pin Solder Pad Width - PCB	0.9	0.8	0.9	0.8	0.8	0.95	0.9
$R_{th(j-c)}$ (Typical) in K/W	1.1	0.85	0.83	0.72	0.8	0.88	0.73

Voiding may create mechanical weaknesses which lead to cracks in the solder joint. There are several factors which cause voiding. One of these causes includes gases generated from the solder paste and it can be solved by using good solder paste to minimize voiding effect. Modification of the stencil design is also one of the possible solutions to voiding. The stencil area should be less than landing pad area of surface mount device to avoid solder defects known as solder balling [1]. According to the industry standard, the stencil aperture size should be designed approximately 95% of the landing pad area.

For Wolfspeed's J2 package, the recommended landing pad is given in Figure 8 (a). This landing pad is designed by following the guideline IPC 7351 and can be modified according to system design requirements. The extended landing pad is recommended in Figure 8 (b) so that the same landing pad can be used for all the Wolfspeed's 7-lead packages J, J1 and J2 and it is mostly compatible with competitor's part numbers. However, slots can be added in the PCB to attain more creepage for higher voltage applications. For more information regarding PCB design, please refer to Wolfspeed's application note "PCB LAYOUT TECHNIQUES FOR DISCRETE SIC MOSFETS" [2].

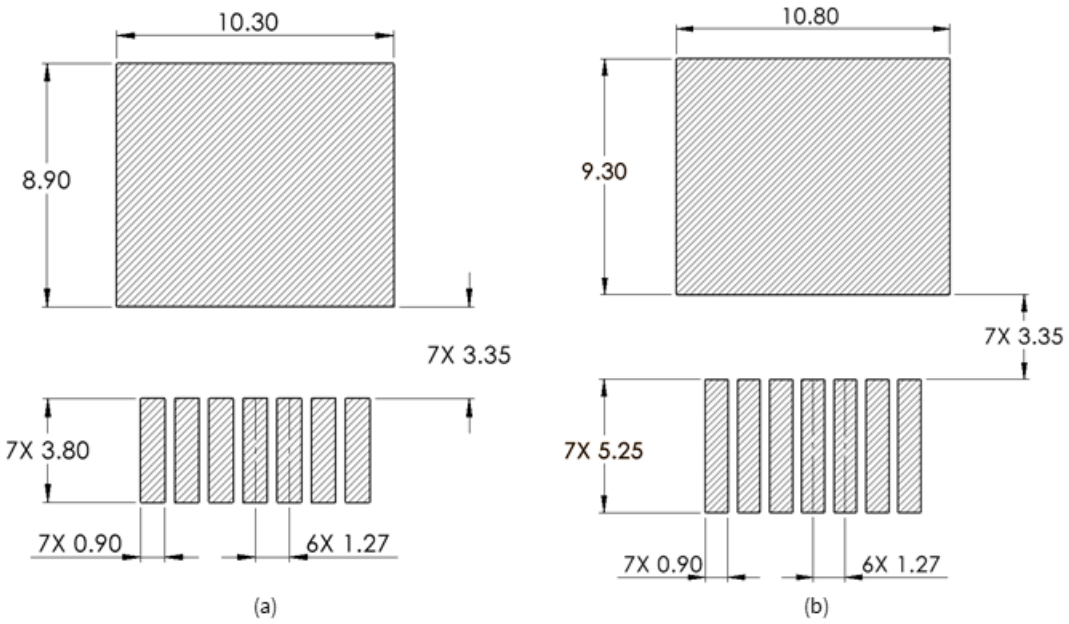


Figure 8: (a) Recommended landing pad for Wolfspeed's J2 package
(b) Recommended landing pad compatible for all J, J1 and J2 packages

Typical thermal resistances from Junction to Case $R_{\theta, JC}$ for diodes with I_F= 10A current rating are:

- E-package is 1.5 °C/W
- G-Package is 1.38 °C/W
- QFN package is 1.4 °C/W

Figure 9 shows the thermal pad areas of these diodes.

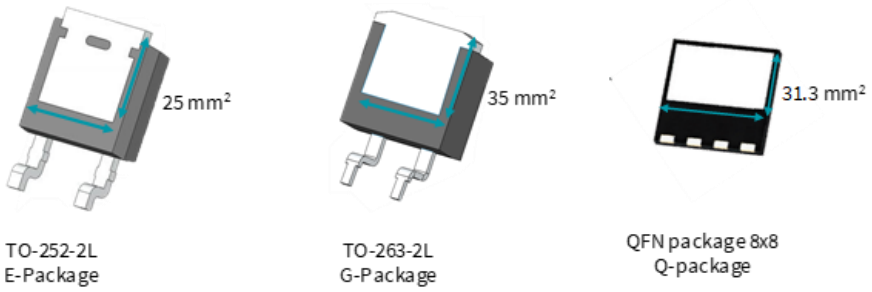


Figure 9: Thermal Pad Area of Wolfspeed's SMD Diodes

2.2 Device Soldering ($R_{\Theta, SOLDER}$)

A good solder joint between the thermal pad and the PCB is required, with a proper re-flow of solder between the pad and the PCB layered as thin as possible. Please refer to the "SOLDERING RECOMMENDATIONS FOR WOLFSPEED® POWER DEVICES" Application Note for the soldering procedures of Wolfspeed devices [3]. A good solder with less than 10% voids can decrease the $R_{\theta, solder}$ by about 30% over a bad solder job with 50% voids. The $R_{\theta, solder}$ is the smallest contributor to the stack-up but is the first contact of the device with the PCB and will therefore decide the contributions of the other thermal impedances of the heat-flow path. Figure 10 shows a poor solder joint.

Figure 10: Solder Joint with Voids for SMDs

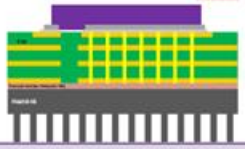
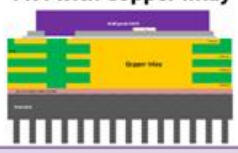
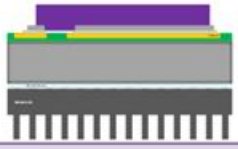
2.3 PCB Design ($R_{\Theta, PCB}$)

The most important design consideration for thermal management of SMDs is PCB. The thermal resistance of the PCB $R_{\theta, PCB}$ is the one of the largest contributors to the total thermal resistance $R_{\theta, JA}$. There are 4 types of PCB design commonly used for thermal management:

- FR4 with thermal vias
- FR4 with Cu inlay
- Insulated metal substrate (IMS)
- FR4 with ceramic inserts

A comparison of these four designs is discussed in Table 2.

Table 2: Comparison of PCB Designs for Thermal Management

	FR4 with Thermal Vias	FR4 with Copper Inlay	Insulated Metal Substrate	FR4 with ALN inserts
				
Thermal Conductivity	Good	Better	Better	Best
Cost	Low	High	High	Highest
Electrical Isolation	No (Requires Isolating TIM)	No (Requires Isolating TIM)	Yes	Yes
Advantages	• Standard Manufacturing process • Layout Flexibility	• Layout Flexibility • Better thermal performance	• Better thermal performance • No additional TIM cost and thermal resistance	• Best thermal performance • No additional TIM cost and thermal resistance
Disadvantages	• High overall thermal resistance	• High manufacturing complexity • High TIM thermal resistance	• Higher manufacturing complexity • Layout only on 1 layer • High parasitic inductance and coupling capacitances in metal	• Higher manufacturing complexity • Longer lead times depending on availability of Ceramics

FR4 with thermal vias is the most common PCB design for thermal management of surface-mount devices. The thermal impedance of the via can be calculated as:

$$R_{\theta,via} = \frac{h}{\lambda \pi t (D + t)}$$

Where,

h= height of the via (or the board thickness if the via is a see-through via) (m)

D= the inner Diameter (m)

t= thickness of plated copper (m)

λ= Thermal conductivity of copper (W/mK)

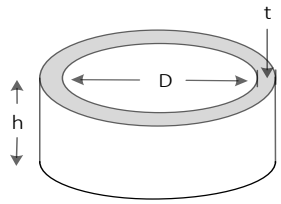


Figure 11: Single Thermal Via Dimensions

The impedance of each via divided by the total number of vias gives us a theoretical estimation of the thermal impedance of the PCB. However, the heat through the device does not spread indefinitely away from the source of the heat. The most crucial vias are the ones directly below the thermal pad (case) of the device. Increasing the number of vias to achieve better thermal performance becomes redundant as the heat is not spreading through all the vias used. This study is an attempt to find the optimum number of vias for the Wolfspeed SMD packages, which varies with the $R_{\theta, JC}$ of the device and the size of the thermal (case/drain pad) to find a balance between the $R_{\theta, PCB}$ and the size (footprint) with a selected via specification.

The selection of the thermal via pattern and number of vias is critical for the cost and footprint (power density) of the system, but care should be taken not to compromise the performance of the device [4]. For the J and J1 package surface-mount device, the following thermal via pattern is selected for the simulations:

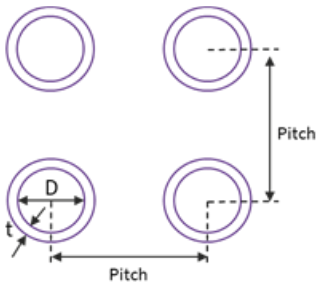


Figure 12: Single Thermal Via Dimensions

PCB Details:

- FR-4 PCB with four Cu layers
- Each Cu layer has a thickness of 2.8mil
- Thickness of the PCB is 1.6mm

Thermal Vias details:

- D= 12mil
- t= 2mil
- Pitch (distance between vias) = 32mil
- Height of the vias= 1.6mm (See-through vias)
- Non-conductive epoxy filling- FR4
- The number of thermal vias is increased from 43 to 221 vias

The thermal impedance of the PCB is calculated using,

$$R_{\theta,\ PCB} = \frac{T_{top(maximum)} - T_{bottom(maximum)}}{P_{loss}}$$

Where,

$T_{top(maximum)}$ = Maximum temperature on the top side of the PCB (device side)

$T_{bottom(maximum)}$ = Maximum temperature on the bottom side of the PCB

P_{loss} = Power loss of the device

The epoxy filling in the vias does very little in the way of heat conduction. It prevents solder from wicking through the vias from the top to the bottom side of the PCB. This is critical as it prevents solder from accumulating in the bottom-side pad and making the surface uneven, which can result in poor heat flow through the TIM. Figure 13 shows the placement of the device on the PCB on seven layouts, each with a different number of thermal vias.

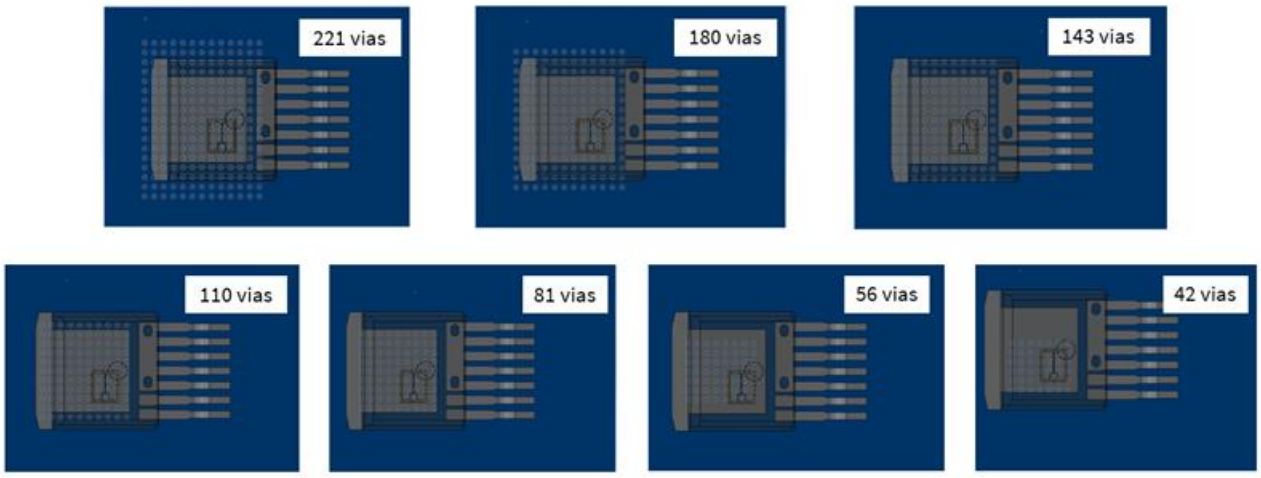


Figure 13: PCB Thermal Via Layouts

Each of these cases with the J and J1-package have been simulated with an input power loss to find the maximum temperature on top of the PCB (device side) and bottom of the PCB (TIM side). The simulated images for the J1-package are shown in Table 3, showing the $R_{\theta, PCB}$ calculated using the formula discussed above. Table 3 shows that as the number of vias is increased, the $R_{\theta, PCB}$ decreases. For the case with 221 vias, the heat does not spread throughout all the vias, making the vias on the edges redundant.

Similar simulations have been carried out for the J-package. The results of these simulations for the J- and J1-package are summarized in Table 4 (a) and (b) respectively. The case with the optimum number of vias is selected by observing less than or equal to 5% difference between $R_{\theta, PCB}$ from the maximum number of vias (221 vias). For the J-pack, the 81-vias case has less than 5% higher $R_{\theta, PCB}$ from the maximum number of 221 vias; for the J1-pack, the case with 180 vias has about 5% higher $R_{\theta, PCB}$ from the maximum number of 221 vias. These are the optimum number of vias for these packages.

Table 3: Simulated PCB Images for Three Layouts with Calculated $R_{\theta, PCB}$

	221 vias	110 vias	42 vias
PCB Top (Device Side)	T_{top_max} = 64.39°C	T_{top_max} = 66.82°C	T_{top_max} = 77.38°C
PCB Bottom	T_{bottom_max} = 58.96°C	T_{bottom_max} = 60.63°C	T_{bottom_max} = 65.22°C
Calculated $R_{\theta, PCB}$	0.584°C/W	0.666°C/W	1.308°C/W

Table 4: (a) *Summary of Results: J-Pack* (b) *Summary of Results: J1-Pack*

No. of vias	T_{top_max} (°C)	T_{bottom_max} (°C)	P_{loss} (W)	$R_{\theta,PCB}$ (°C/W)	% Difference from least $R_{\theta,PCB}$
221	73.13	60.5	9.22	1.37	-
180	73.32	60.6	9.22	1.38	0.73
143	74.2	61.42	9.22	1.386	1.17
110	75.1	62.29	9.22	1.389	1.39
81	76.4	63.4	9.22	1.41	2.92
56	78.84	65.17	9.22	1.483	8.25
42	84.68	67.46	9.22	1.868	36.35

No. of vias	T_{top_max} (°C)	T_{bottom_max} (°C)	P_{loss} (W)	$R_{\theta,PCB}$ (°C/W)	% Difference from least $R_{\theta,PCB}$
221	64.391	58.963	9.3	0.584	
180	65.03	59.31	9.3	0.615	5.38
143	65.56	59.66	9.3	0.634	8.7
110	66.82	60.63	9.3	0.666	14.04
81	68.76	62.01	9.3	0.726	24.36
56	72.52	63.79	9.3	0.939	60.83
42	77.38	65.22	9.3	1.308	124.02

These results can be observed from the graph in Figure 14. There is initially a steep decrease in thermal impedance of the PCB, but as the number of vias is increased the decrease in thermal impedance saturates and eventually there is a point where there is no advantage to having more vias.

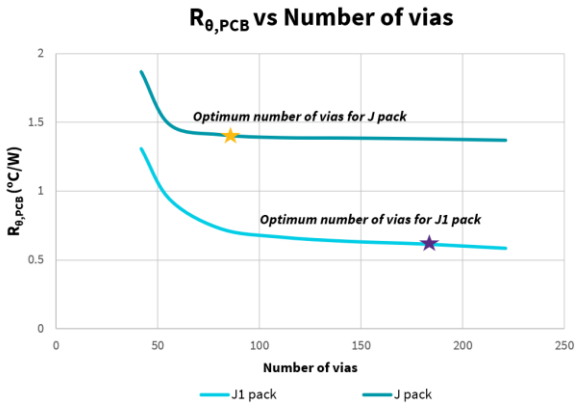


Figure 14: Optimum Number of Vias

The simulation results forJ1 pack is valid for J2 package as both package geometries are almost similar and hence PCB via optimization is valid from J1. The G-pack diode is packaged similarly to the J-pack MOSFET, with the only difference being the number of leads. The drain pad area (thermal pad) of the J-pack MOSFET is same as the G-pack diode's cathode pad (thermal pad). From this, we deduce that the thermal performance of these packages will be similar and 81 vias is also the optimum number of vias for the G-pack.

2.4 Thermal Interface Material ($R_{\Theta, TIM}$)

Thermal interface material (TIM) also plays a crucial role in the assembly, as $R_{\theta, TIM}$ contributes to around 20-30% of the total $R_{\theta, JA}$. There are a few types of thermal interface materials, discussed below and summarized in Table 5:

- **Gap-Filling Pads:** These materials generally have the highest thermal conductivity. They must be mounted in a way to keep constant pressure between the heatsink and the PCB. Soft pads reduce in thickness when mounted with constant pressure. Hard ceramic pads have a constant thickness but

are very high in thermal conductivity. These pads also provide electrical isolation, which is required if thermal via inserts are used in the PCB.
When using aluminum nitride (AlN) inserts in the PCB, electrical isolation is not required as AlN is an electrical insulator. In this use case, any good quality thermal grease or graphite pads can be used which are highly thermally conductive.

- **Adhesives:** Solid adhesives may have lower thermal conductivity than the gap-filling pads, but liquid-bond adhesives have comparable conductivity. The liquid-bond adhesives (discussed in Table 5) do not require a constant pressure mounting for the entire operation but do require pressure and temperature cure for some time during assembly. Adhesives are a good option for smaller heatsinks (typically less than 40mm x 40mm).

- **Phase-Change Materials:** Most phase-change materials have thermal conductivity lower than the other options discussed in Table 5. These also require constant pressure mounting of the heatsink. Their thermal resistance does not significantly change with pressure; hence this option provides the most consistent performance.

To compare different TIM thermal resistances, $R_{\theta, TIM}$ can be estimated using the following equation,

$$R_{\theta,TIM} = \frac{L}{A \times k}$$

Where,
L= Thickness of the TIM (m)
A= Assumed thermal transfer area (m^2)
k= Thermal conductivity of the TIM (W/mK)

This equation can be used to estimate thermal resistances and give a good idea about choosing a TIM, but accurate measurements and thermal simulation are required for calculating the actual $R_{\theta, TIM}$.

The thermal transfer area used to populate the calculated $R_{\theta, TIM}$ column of the table is A= 56 mm^2, which is the thermal pad area of the TOLL package. This thermal transfer area changes with PCB properties such as the number of copper layers, number of vias, PCB thickness, etc., which are discussed in the previous section. The selection of TIM is based on cost, availability, assembly complexity, and various other factors. For some applications, the use of TIM can be eliminated altogether and the heatsink can be soldered onto the PCB directly. This reduces the size of the heatsink as there is no electrical isolation and an individual heatsink must be used for every device. Furthermore, copper heatsinks, or electro-plated aluminum heatsinks must be used. This might cause EMI issues as the heatsink is directly soldered to high dv/dt nodes. A larger heatsink can be used for multiple devices if AlN inserts are used in the PCB, as AlN provides electrical isolation and can be used without a TIM.

Table 5: Comparing Different TIM Options

Type	Part No.	Thermal Conductivity	Thickness	Breakdown Voltage	Calculated $R_{\theta, TIM}$
Gap filling pad	TGARD210	5 W/mK	0.25mm	6 kV	0.89 K/W
	AlN Ceramic	170 W/mK	0.25mm	17kV/mm	0.03 K/W
Adhesive	SA3500	3.5 W/mK	Custom (0.15mm)	10kV/mm	0.77 K/W
	TIA520R	5.2 W/mK	Custom (0.15mm)	20kV/mm	0.52 K/W
Phase Change Materials	HI-FLOW 300P	1.6W/mK	0.1mm	5kV	1.12 K/W

2.5 Heatsinks and Mounting ($R_{\theta, HA}$)

Heatsinks are very important for the entire thermal management assembly as their size is normally constrained by the overall power density of system. They are widely available in aluminum and copper material, with copper being slightly more expensive due to better thermal properties (higher thermal conductivity/ lower thermal resistance).

- **Smaller heatsinks** (<15x15mm) used for individual devices can be mounted directly by soldering them onto the board as discussed in previous sections. This can be used for low-power applications (P <1kW). As mentioned previously, this might cause EMI issues as the heatsink has no electrical isolation from the drain.

- **Medium size heatsinks** (> 15x15mm and <40x40mm) can be used with adhesive liquid bonds or push-pin attachments.
  - The adhesive liquid bonds will provide consistent performance throughout the heatsink area if applied uniformly.
  - The push-pin attachment is used to easily modify the compressional force, but the force is not consistent throughout the area, having higher force at the points where pushpin is attached.

- **Larger heatsinks** (>40x40mm) are generally used on the main board with several devices for higher power levels. They must provide uniform pressure across the heatsink and therefore use QSZ clips with anchor pins or pressure bars across the heatsink.

Table 6: Comparing Different Heatsink Sizes

Heatsink Dimensions	Heatsink Material	Mounting Mechanism	Recommended Use
<15x15mm	Cu/Electro-plated Al	Soldering/Adhesives	On Daughter Card
>15x15mm & <40x40mm	Cu/Al	Adhesives/Push-Pins	On Daughter Card
>40x40mm	Cu/Al	QSZ clips with anchor pins/ Pressure bars	On main board

3. Design Examples

3.1 Speedfit Design Example – 2kW Asynchronous Boost Converter

Speedfit 2.0 is Wolfspeed's online design simulator that can be used to run all Wolfspeed devices in various topologies with different system specifications [5]. For this design example, a 2kW asynchronous boost converter is considered in Figure 15.

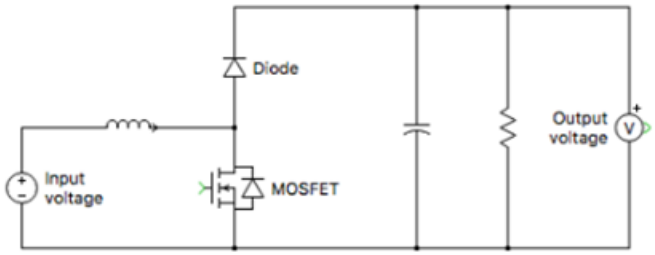


Figure 15: Asynchronous Boost Converter

Calculating the junction temperature assuming both the devices are mounted on the same heatsink (Refer to Figure 16):

$$T_h = (P_{Loss1} + P_{Loss2}) \times R_{\theta,HA} + T_{amb} \quad \text{Eq. 1}$$

$$T_{j1} = \left(R_{\theta,JC} + R_{\theta,solder} + R_{\theta,PCB} + R_{\theta,TIM}\right) \times P_{Loss1} + T_h \quad \text{Eq. 2}$$

$$T_{j2} = \left(R_{\theta,JC} + R_{\theta,solder} + R_{\theta,PCB} + R_{\theta,TIM}\right) \times P_{Loss2} + T_h \quad \text{Eq. 3}$$

Where,

T_{j1} and T_{j2} = Junction temperatures of MOSFET and diode respectively

T_h = Heatsink temperature

P_{Loss1} and P_{Loss2} = Power loss of MOSFET and diode respectively

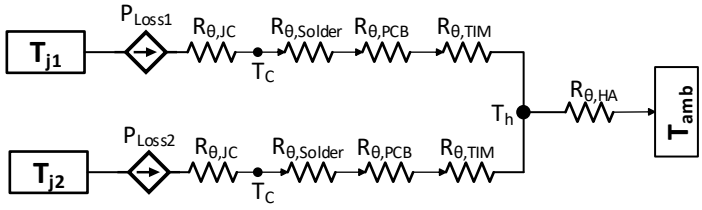


Figure 16: Junction Temperature Calculation

The system specifications chosen for this analysis are shown in Table 7.

Table 7: System Specifications

Specification	Value
Input Voltage (V_{in})	200V
Output Voltage (V_{out})	400V
Switching Frequency (F_{sw})	60kHz
Output Power (P_{out})	2kW
MOSFET	C3M0060065J
Diode	C6D10065G

Consider a thermal impedance breakdown as shown in Table 8, which is extracted from the previously discussed design considerations. This thermal impedance is then input into the Speedfit thermal details as shown in Figure 17(a). The $R_{th,\,ch}$ is the case-to-heatsink thermal impedance, calculated as:

$$R_{th,\,ch} = R_{\theta,solder} + R_{\theta,PCB} + R_{\theta,TIM} = 0.015 + 1.39 + 0.52 = 1.925\ ^{o}\text{C/W}$$

The junction temperature of the devices can then be estimated using equations 1, 2 and 3:

$$T_h = (P_{Loss1} + P_{Loss2}) \times R_{\theta,HA} + T_{amb}$$

$$T_h = (6.23 + 6.45) \times 2 + 50 = \mathbf{75.36^{o}C}$$

$$T_{j1} = \left(R_{\theta,JC} + R_{\theta,solder} + R_{\theta,PCB} + R_{\theta,TIM}\right) \times P_{Loss1} + T_h$$

$$T_{j1} = (1.1 + 0.015 + 1.41 + 0.52) \times 6.23 + 75.36 = \mathbf{94.33\ ^{o}C}$$

$$T_{j2} = \left(R_{\theta,JC} + R_{\theta,solder} + R_{\theta,PCB} + R_{\theta,TIM}\right) \times P_{Loss2} + T_h$$

$$T_{j2} = (1.38 + 0.015 + 1.41 + 0.52) \times 6.45 + 75.36 = \mathbf{96.81\ ^{o}C}$$

These calculated results are in line with the Speedfit results shown in Figure 17(b).

Table 8: Thermal Impedance Breakdown

Thermal Impedance	C3M0060065J	C6D10065G	Units	Comments
$R_{\theta,JC}$	1.1	1.38	°C/W	Typ. Junction to case thermal impedance of each device
$R_{\theta,solder}$	0.015	0.015	°C/W	Thermal impedance of 0.06mm thick Tin-Silver Solder
$R_{\theta,PCB}$	1.41	1.41	°C/W	For 81 vias with specifications • D= 12mil • t= 2mil • Pitch= 32mil • Height of vias= 1.6mm (See-through vias)
$R_{\theta,TIM}$	0.52	0.52	°C/W	Adhesive TIA520R
$R_{\theta,HA}$	2	2	°C/W	Al heatsink: 28x28x11mm (pin fin) (1000 LFM airflow)
$R_{\theta,\,total}$	5.045	5.045	°C/W	Total thermal impedance
T_{amb}	50	50	°C	Ambient Temperature
P_{loss}	6.23	6.45	W	Power loss of one device
Calculated T_j	94.33	96.8	°C	Calculated junction temperature

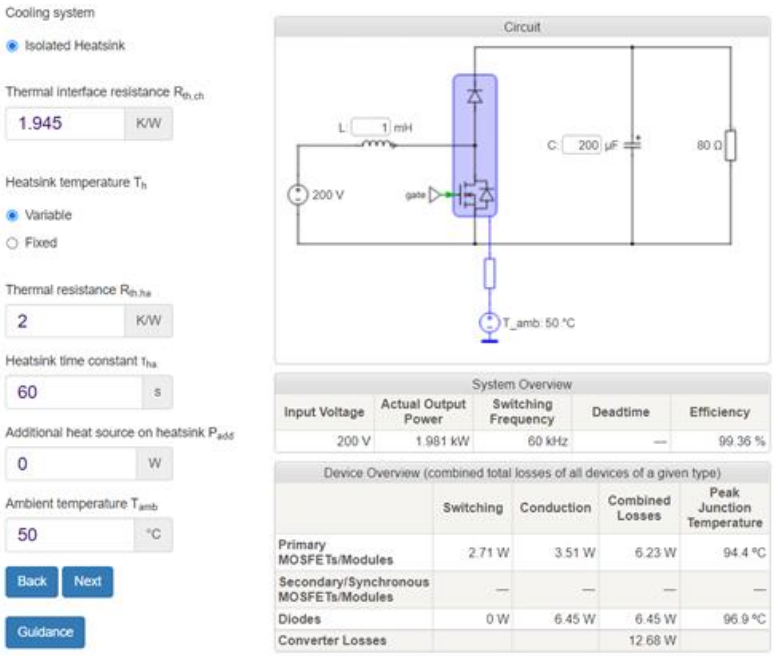


Figure 17(a): Speedfit Thermal Details (b): Speedfit Results

3.2 6.6 kW Bi-directional EV OBC with AlN Ceramic Inserts

Wolfspeed's CRD-06600FF0917N 6.6kW bi-directional EV OBC design is considered for this example. Figure 18 shows the reference design and the device mounting over AlN inserts used in the PCB for the thermal management of the Wolfspeed C3M0065090J device. A pressure bar is used on top of the device to ensure good contact between the device and the PCB.

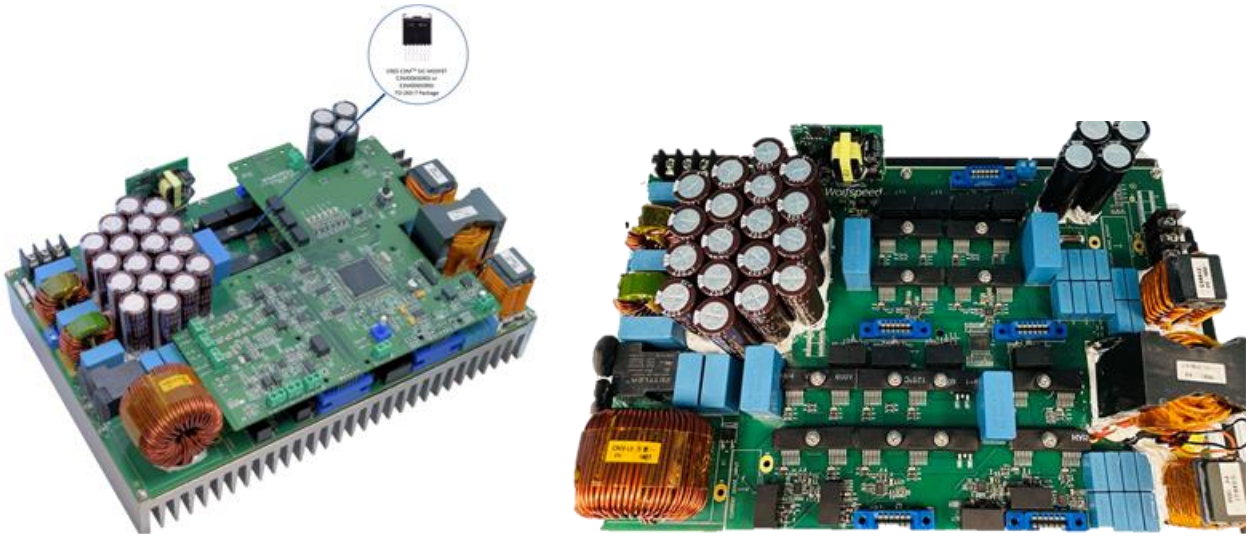


Figure 18: CRD-06600FF0917N 6.6kW Bi-directional On-Board Charger Design

The block diagram of the reference design is shown in Figure 19. The design has two sections, an AC-DC section using a totem-pole PFC converter and a DC-DC section using a CLLC resonant converter. The specifications of these converters are discussed in Table 9(a) and 8(b) respectively. The overall power density of the design is 36W/in^3.

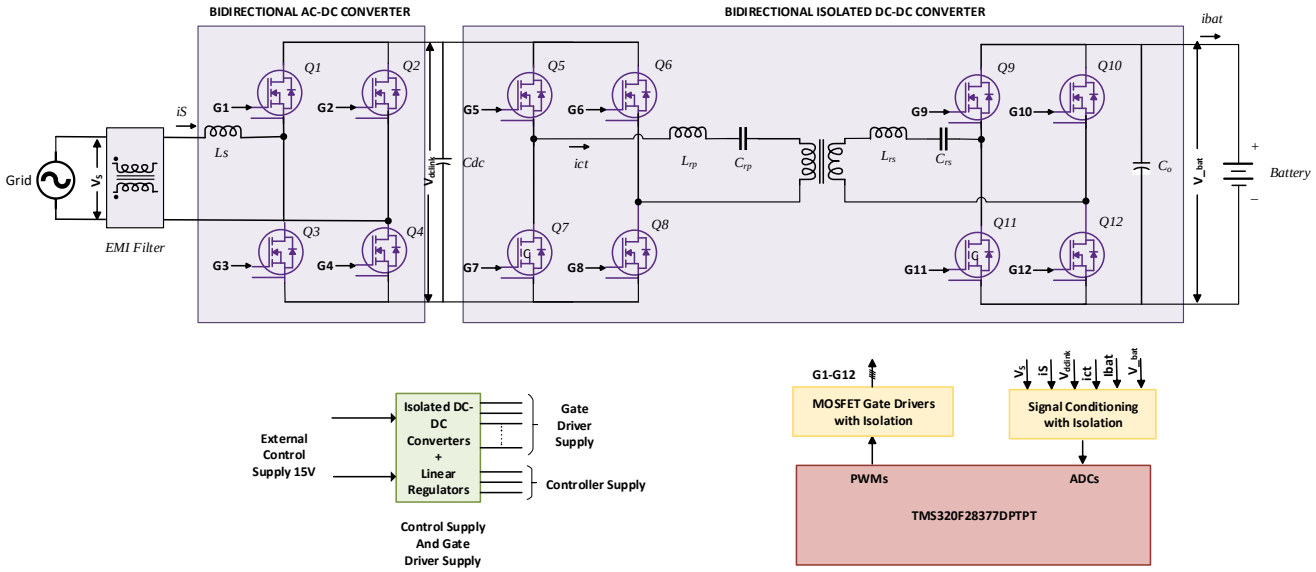


Figure 19: Block Diagram of CRD-06600FF0917N

Table 9 (a) Totem-pole PFC System Specifications, (b) CLLC System Specifications

Specification	Value
Input Voltage (V_{in})	90-265Vac
Output Voltage (V_{out})	250-450Vdc
Switching Frequency (F_{sw})	67kHz
Deadtime (T_{dead})	200ns
Output Power (P_{out})	6.6kW
Peak Efficiency (η_{peak})	97.2%

Specification	Value
Input Voltage (V_{in})	250-450Vdc
Output Voltage (V_{out})	250-450Vdc
Switching Frequency (F_{sw})	195kHz
Deadtime (T_{dead})	100ns
Output Power (P_{out})	6.6kW
Peak Efficiency (η_{peak})	97.2%

Thermal management of these devices is extremely critical at higher power levels, which is the reason AlN ceramics are used in the PCB to provide the least thermal-resistant path. The thermal design for a single device is shown in Figure 20.

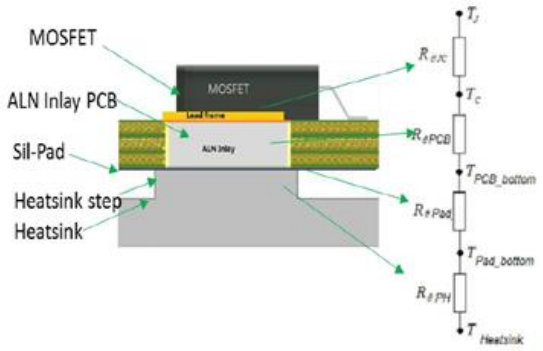


Figure 20: Thermal Design and Thermal Resistance Analysis

The device is soldered onto the AlN insert in the PCB. A Sil-Pad LI-98C is used between the PCB and the heatsink. This Sil-pad can be eliminated if there are no copper traces in the 4mm radius of the AlN insert at the bottom of the PCB, which is a clearance requirement. AlN itself provides electrical insulation, so in that case thermal grease or a TIM material with a much higher thermal conductivity could be used. Since this design does not have greater than 4mm clearance of copper traces on the bottom side of the PCB, an electrically isolating pad is required. An aluminum heatsink is used with a heatsink step for each device connecting to the main heatsink for the board. The temperature at the bottom of the heatsink step is maintained at 65°C by adjusting the temperature of the cold plate at the bottom of the heatsink to simulate the thermal condition in an OBC. The thermal impedance breakdown of all the components is shown in Table 10. The junction temperatures are calculated based on Eq. 1, 2 and 3 from Section 3.1.

Table 10: Thermal Impedance Breakdown of Each Device

Thermal Impedance	High- Frequency PFC MOSFET	CLLC Primary MOSFET	Units	Comments
$R_{\theta,JC}$	1.1	1.1	°C/W	Typ. Junction to case thermal impedance of C3M0065090J
$R_{\theta,solder}$	0.015	0.015	°C/W	Thermal impedance of 0.06mm thick Tin-Silver Solder
$R_{\theta,PCB}$	0.12	0.12	°C/W	Thermal impedance of 8mm*10mm*1.6mm AlN insert
$R_{\theta,TIM}$	0.9	0.9	°C/W	Thermal impedance of sil-pad LI-98C
$R_{\theta,HA}$	0.132	0.132	°C/W	Thermal impedance of Al heatsink step
$R_{\theta,total}$	2.267	2.267	°C/W	Total thermal impedance
T_{amb}	65	65	°C	Temperature at the bottom of Heatsink step
P_{loss}	23.5	9.9	W	Power loss of one device
Calculated T_j	118.27	87.44	°C	Calculated junction temperature

4. Summary

Thermal management can greatly affect the efficiency, power density, and reliability of power converters. This document goes over the important design considerations when designing a thermal management system. Each component in the thermal stack impacts the overall performance of the device. For surface-mount

devices, the PCB thermal impedance and the heatsink mounting play a huge role and should be designed taking power level, power density, and cost into consideration.

5. References

[1] Solder Voiding

[2] Application Note – PCB Layout Techniques for Discrete SiC MOSFETs

[3] Application Note – Soldering Recommendations for Wolfspeed Power Devices

[4] Deepak Gautam, Dale Wager, Fariborz Musavi, Murray Edington, Wilson Eberle, William G. Dunford "*A Review of Thermal Management in Power Converters with Thermal Vias*"

[5] Wolfspeed Design Simulator – Speedfit