Application Note PRD-08296

SiC MOSFET Short Circuit Application Note

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Implementing protection against short-circuit events is critical for designing safe and reliable power electronic systems. In both automotive and industrial applications, it is necessary for the power semiconductor component to be able to withstand a certain amount of short-circuit energy. This application note provides guidance on how to minimize the risk of system failure due to short-circuit events. It will also discuss the importance of DESAT protection for minimizing the energy dissipated in short-circuit events.

Contents

1. Introduction

The recent shift towards electrification calls for increasingly challenging operating conditions for power semiconductors. In particular, the push for higher energy efficiency in power systems is steering the power industry away from traditional silicon (Si) IGBTs and towards silicon carbide (SiC) MOSFETs. SiC-based devices have higher thermal conductivity and lower switching losses than their Si counterparts [1], [2]. SiC MOSFETs are also capable of higher current and voltage ratings with reduced die areas. However, trade-offs do exist between the two modern-day power switches. During a short-circuit (SC) event, the semiconductor device will need to withstand currents tens to hundreds of times higher than the device-rated current. Due to differences in saturation behavior between Si IGBTs and SiC MOSFETs, the peak energy during a SC event will be much higher for the SiC MOSFET than Si IGBT for similarly rated devices [3]. In addition, SiC devices have a smaller die size and therefore must withstand a much higher energy density and rapid temperature rise. These effects lead to a shorter SC withstand time for SiC MOSFETs. This application note will demonstrate that SiC MOSFETs can be safely turned off well before failure with proper circuit protection. In addition, this application note will discuss SC theory, test setup and analysis, and common failure mechanisms.

2. Short-Circuit Theory

Historically, SC behavior in power applications has been studied using Si IGBTs [4], [5]. Three common SC types have been defined using Si IGBTs in a 2-phase inverter [6]. Further studies of these SC types have been performed using SiC MOSFETs [7], [8]. For either device, various faults can occur during the forward and reverse operation of the semiconductor. These faults cause various SC types which have different paths within the circuit. Each path will have different parasitic inductance L_{par} and thus apply a different amount of stress on the device. SC type I, seen in Figure 1, is also known as the hard switching fault, which occurs when the device under test (DUT) is turned on into an existing short. SC type II, fault under load, occurs when a short-circuit event happens during the on time of the MOSFET and while the MOSFET is operating in forward conduction. SC type III is described as a short circuit occurring while the MOSFET is functioning in reverse conduction mode and current is flowing through the freewheeling body diode (FWD) of the device. Common faults that cause this SC type are mainly seen in railway applications.

2.1 Short Circuit Type I (SC I) – Hard Switching Fault (HSF)

The most common short-circuit type is the hard-switching fault that occurs when the device under test (DUT) is turned on into an existing short. In Figure 1, the schematic illustrates the short-circuit path for SC type I in a half-bridge module. The pulse pattern begins with both devices in the off state over time period t_0. S_1 is then switched into the on state over period t_1. S_2 is falsely switched to the on state and into the short circuit during t_{SC}.

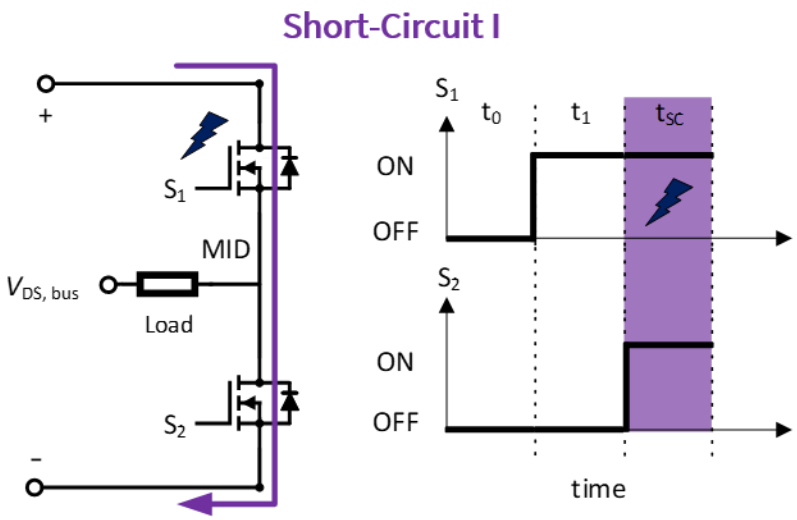

Figure 1: SC path and pulse pattern for hard switching fault

Schematic trajectories of V_{DS}, I_D and V_{GS} are depicted in Figure 2. Before the short-circuit event, when the MOSFET S_2 is still turned off, a voltage bias $V_{DS,bus}$ exists across the DUT. When MOSFET S_2 is turned on by a false signal or by parasitic turn-on of the complementary device (S_1), which is dependent on the capacitance ratio of the devices [9], its V_{GS} surpasses the gate source threshold voltage $V_{GS,th}$, and the drain current starts to increase. Due to the steep increase in I_D, the voltage across the switch is decreased, as per equation (1) [10].

$$V_{\mathrm{DS}} = V_{\mathrm{bus}} - L_{\mathrm{par}} * \frac{\mathrm{d}i_{\mathrm{D}}}{\mathrm{d}t} \qquad (1)$$

V_{DS} is dependent on the parasitic inductance L_{par}, which is the unwanted inductance effect present in any system and is meant to be kept low. The slope of the current rise is dependent on the external gate resistance $R_{G,on/off}$. $I_{D,peak}$ is reached for the saturation drain current $I_{D,sat}$ at a given gate source voltage and temperature. Furthermore, the voltage drop from drain to source depends on the applied bus voltage $V_{DS,bus}$.

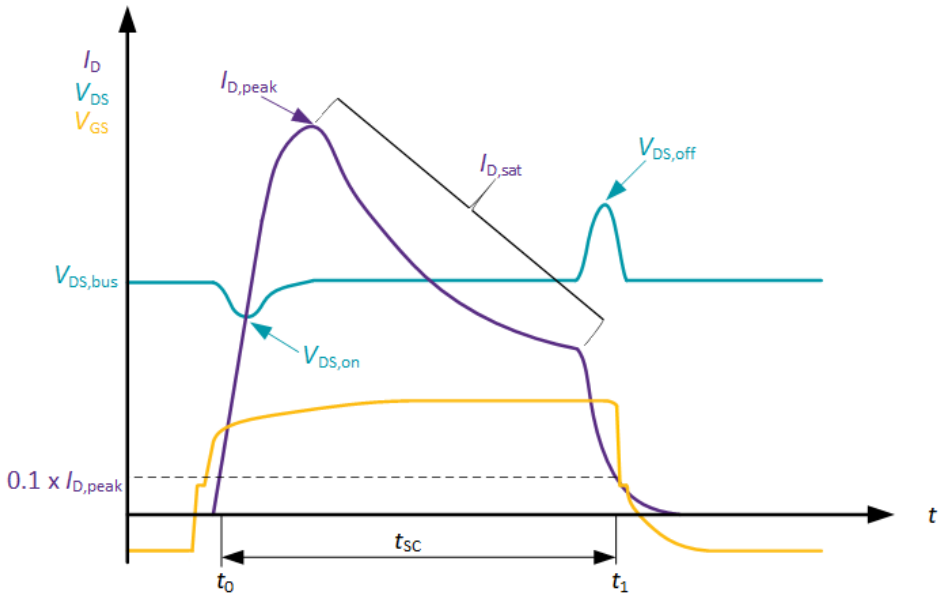

Figure 2: Ideal waveforms for SC type I

The saturation drain current, $I_{D,sat}$, is dependent on the physical dimensions and material properties of the MOSFET unit cell, the applied V_{GS}, and $V_{GS,th}$ of the device [10]. After reaching $I_{D,peak}$, the saturation current begins to decrease over time as a result of the DUT heating from energy losses. Before any damage to the device occurs, the MOSFET should be turned off safely. If the device is turned off too quickly, the drain voltage overshoot might exceed the rated blocking voltage of the device. Therefore, a relatively higher $R_{G,off}$ helps with a soft shutdown to minimize the voltage overshoot due to a steep negative $\frac{di_D}{dt}$. The short circuit energy, E_{SC}, the device is subjected to during a short circuit event is defined in equation (2) [10].

$$E_{SC} = \int_{t_0}^{t_1} P_{SC}\, dt = \int_{t_0}^{t_1} v_{DS} \cdot i_D\, dt \qquad (2)$$

E_{SC} is the integral over the product of v_{DS} and i_D, which is the short circuit power, P_{SC}, for the short-circuit period from t_0 to t_1. If the short-circuit energy exceeds the critical short-circuit energy, then destruction of the device occurs. This failure is caused by thermal runaway which occurs when the energy the device sees cannot be dissipated fast enough. Subsequently, the device temperature increases to the point of device failure.

2.2 Short-Circuit Type II (SC II) – Fault Under Load (FUL)

The short-circuit type II, fault under load, occurs when a short-circuit event happens during the on time of the MOSFET and while the MOSFET is operating in forward conduction. In Figure 3 the short occurs across the load, from the MID point of the half bridge to the negative terminal, during the on time of S_1. S_2 is not turned on but could be damaged form the short-circuit event.

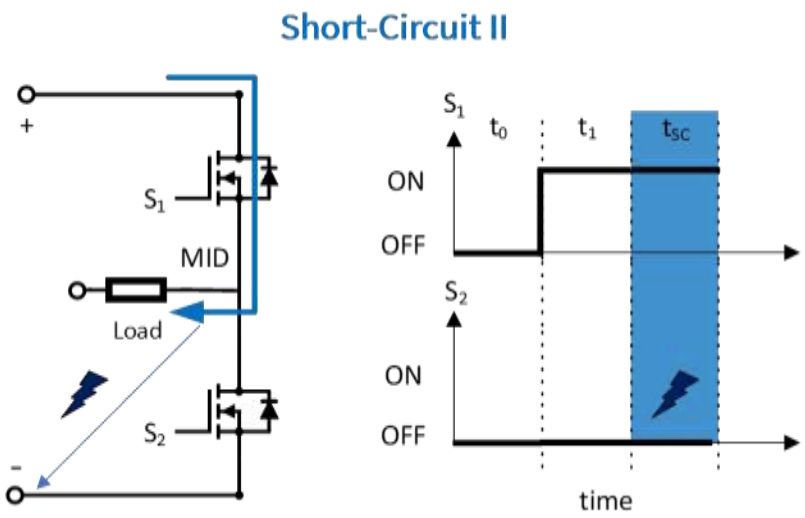

Figure 3: SC path and pulse pattern for fault under load

For this short-circuit type I_D, V_{DS} and V_{GS} trajectories behave as depicted in Figure 4. Prior to the short-circuit event, V_{GS} is positive and the MOSFET S_1 is in the on-state. The DUT is carrying the on-state current $I_{D,on}$ and the on-state voltage V_{DS} is set by the current $I_{D,on}$ and the $R_{DS(on)}$ of the device. When the short-circuit event occurs across the load, the current in S_1 rises sharply and the drain voltage across the device desaturates and rises steeply from $V_{DS,load}$ to $V_{DS,bus}$. $I_{D,peak}$ keeps increasing due to the continuing rise of V_{DS} leading to drain-induced barrier-lowering (DIBL) effect.

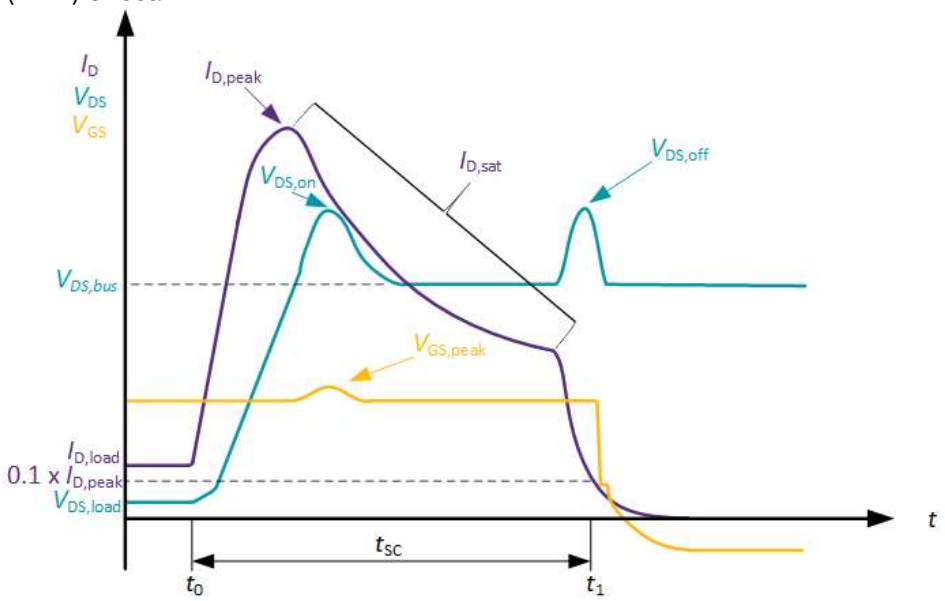

Figure 4: Ideal waveforms for short circuit type II

As a result of the DIBL effect, $V_{GS,th}$ of the DUT is decreased leading to further increase of $I_{D,sat}$. Once the peak current is reached, the short-circuit behavior becomes similar to that of SC I. The device heats up due to energy losses leading to a decrease in $I_{D,sat}$. The negative $\frac{di_D}{dt}$ during the device's turn-off leads to an elevation of V_{DS}. Once again, special caution must be taken to avoid any voltage overshoot during turn-off by suitably tuning the $R_{G,off}$.

2.3 Short-Circuit Type III (SC III) – Fault in Freewheeling Mode (FWM)

SC III is described as a short circuit occurring across the load while the MOSFET is functioning in freewheeling body diode conduction mode. If a fault occurs that causes a short across the load, S_3 will see the short-circuit current from the load and the reverse-recovery current from the diodes.

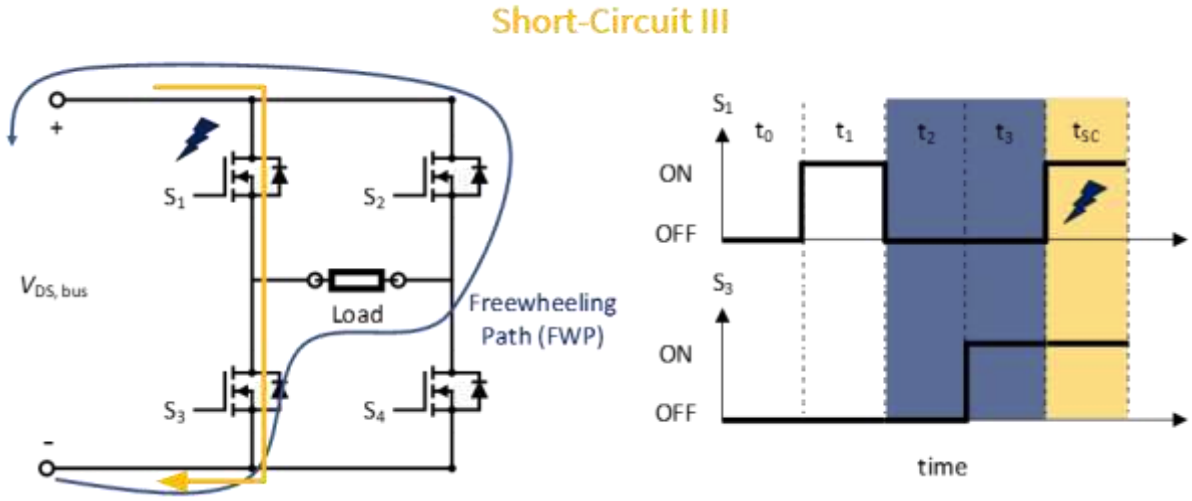

Figure 5: SC path and pulse pattern for fault during freewheeling mode

Figure 5 shows the freewheeling path of the commutating current in a single phase 2-level converter. From the pulse pattern, S_1 and S_4 are initially turned on during t_1 and back off during t_2. During this time the current remains flowing through the body diodes of S_3 and S_2 following the freewheeling path depicted in the schematic. S_2 and S_3 are turned back on for t_3. At t_{sc} a fault occurs and S_1 is turned back on prompting SC III through S_1 and S_3.

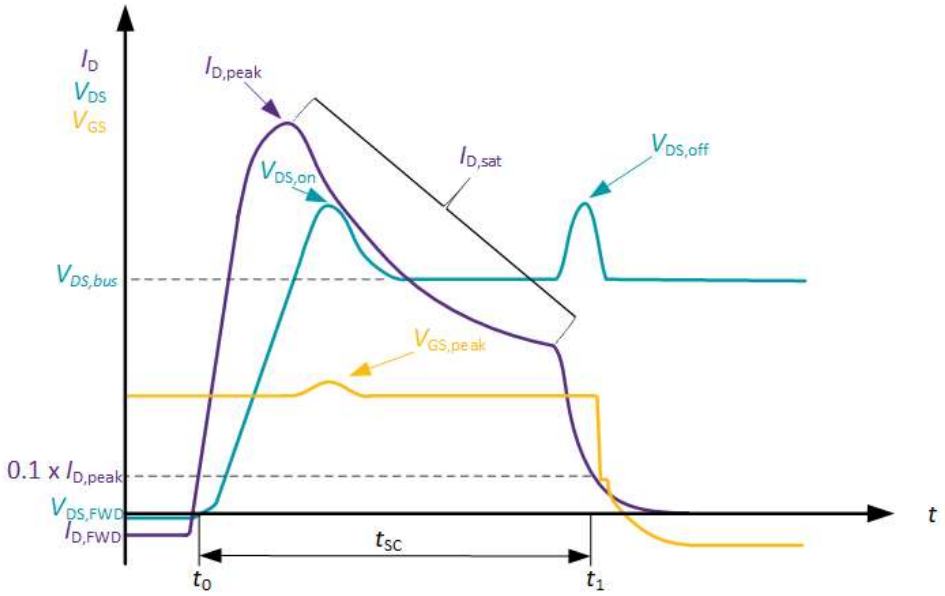

Figure 6: Ideal waveforms for short circuit type III

Figure 6 displays the respective I_D, V_{DS} and V_{GS} waveforms for SC III. Prior to the short-circuit event, the current and voltage are negative because the MOSFET S_3 is in reverse-conduction mode. Once the SC event occurs, the current starts rising steeply. After the current peak, the short-circuit behavior is the same as SC I & II as in Figure 6.

3. Short Circuit Testing with Discrete Packaging

SC testing is one of the most rigorous tests performed on power semiconductor devices. Often, a SC test can result in a package rupture producing shrapnel, arcing events, and a gunshot-like sound. **Prior to performing any SC tests, ensure that the test station is properly enclosed and equipped with the proper personal protective equipment (PPE), and that standard test procedures are followed**.

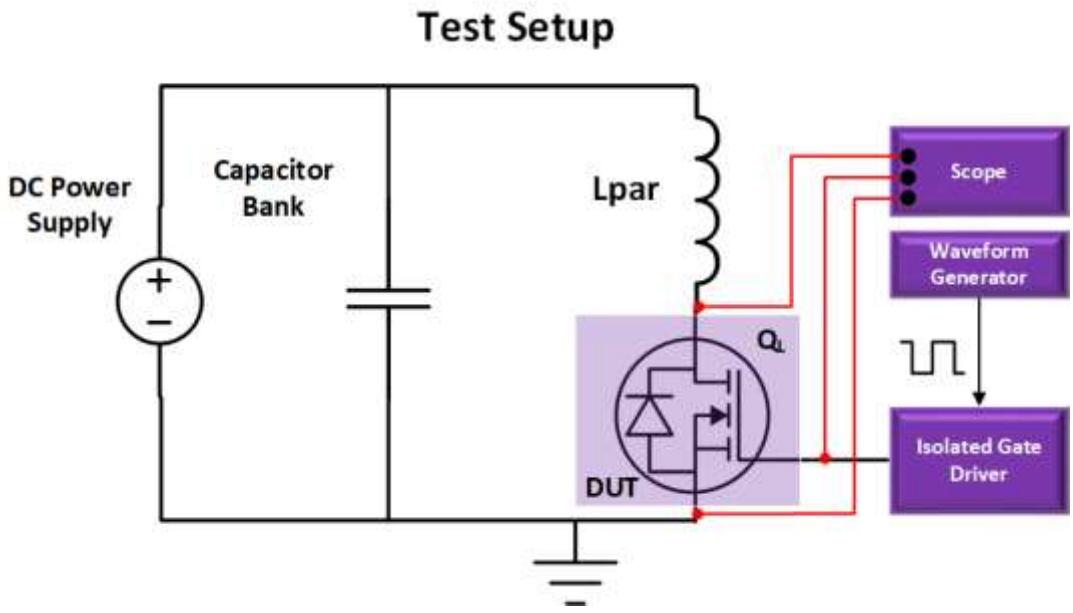

Figure 7: Example of a short-circuit test circuit.

Figure 7 illustrates a typical SC test circuit and setup. The test bench consists of a waveform generator and low-voltage power source to bias the gate of the DUT, a high-voltage power source, a multimeter to supply and measure the BUS voltage across the DUT, and an oscilloscope to record the resulting current and voltage waveforms. The test circuit is designed to replicate SC type I. A high-voltage probe for V_{DS}, a low-voltage probe for $V_{GS,}$ and a Rogowski coil used to measure I_D are connected to the test circuit in a high-voltage enclosure. Although higher accuracy current measurement methods exist, a Rogowski coil offers a robust current probe method when properly shrouded (as otherwise it could be damaged from the destructive nature of the SC event).

3.1 Short Circuit Failure Modes

To determine the maximum short-circuit withstand time, the device is tested until failure. There are two types of failure modes that can result from the failure mechanisms later discussed in Section 6. The first type is a catastrophic failure, which is when the SC event damages the DUT beyond being able to safely test. Physical package limitations include missing leads, missing wire bonds, and exposed die as seen in Figure 19. The second type of failure mode is a parametric failure, which occurs when a DUT no longer maintains its electrical

characteristics within the range of the specification limits defined in the applicable product data sheet. A user must pre-test and post-test devices during SC testing to screen for this failure mode. When testing until failure, typically the step size of the short-circuit time t_{SC} is 0.2 µs or 0.1 µs for fine resolution. The destructive or failure pulse is the pulse after which the device sees a catastrophic or parametric failure, whereas the last pass pulse (LPP) is the very last pulse in which the MOSFET could be turned off safely without loss of electrical functionality. How often each failure mode occurs can vary between products with different voltage ratings.

3.2 Waveform Analysis

Figure 8 shows the resulting waveforms from a standard SC test performed on Wolfspeed's EPM3-1200D-0017D-R01 die product. The bus voltage is set to 2/3 the rated voltage of the device (here, 800 V for a 1200V rated device). Industry standards require the V_{DS} undershoot and overshoot during turn-on and turn-off to be less than ±5%, which is achieved here through proper design of a test board with ultra-low parasitics. The waveform shape and duration is set through the waveform generator. An external gate resistance of 10 Ω is used here to limit the $\frac{dv_{GS}}{dt}$ and minimize V_{DS} undershoot and overshoot during gate turn-on and turn-off, respectively. The short-circuit time t_{SC} is set in the waveform generator and is measured from 50% of V_{GS} for t_0 during turn-on to 50% of V_{GS} for t_1 during turn-off. The inrush current can reach up to 20 times the rated device current and decays with time until V_{GS} is finally fully shut-off. The E_{SC} can be calculated using equation (3).

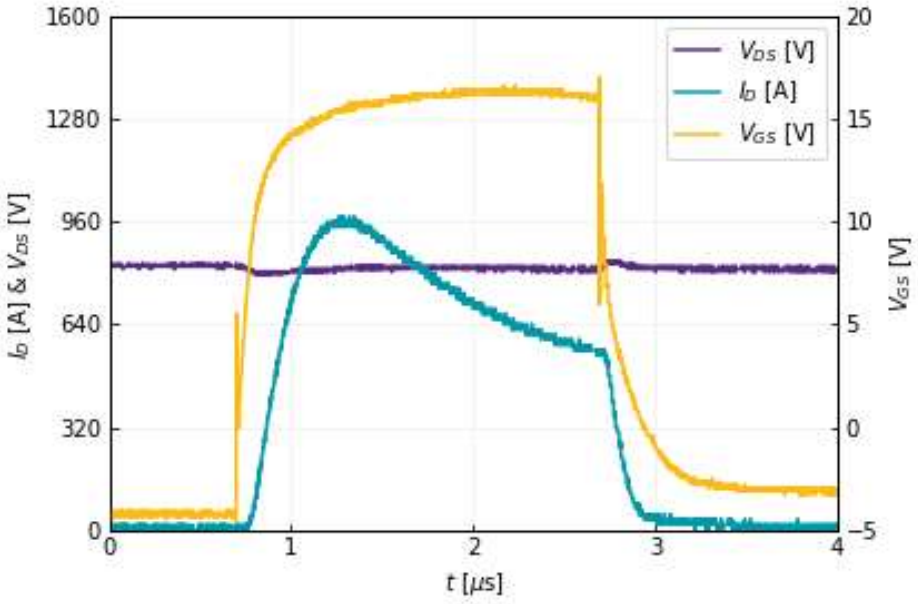

Figure 8: Typical short-circuit waveform at V_{bus} = 800 V, t_{SC} = 2 µs, T_J = 25 °C and $R_{G,ext}$ = 10 Ω

4. Short-Circuit Testing with a Wolfspeed FM3 Module

The test setup for short-circuit testing with power modules differs from the test method performed on packaged parts and will be discussed in this section. The results described in this section are from short-circuit testing performed on a Wolfspeed CAB016M12FM3 half-bridge power module.

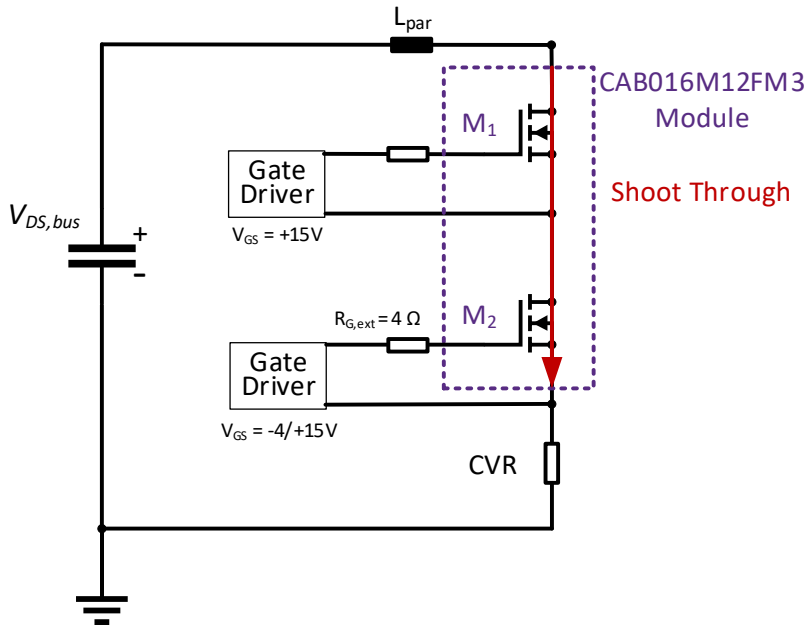

Figure 9: Short-circuit test setup for CAB016M12FM3 module in half-bridge configuration

Figure 9 shows the test circuit using a Dynamic Performance Evaluation Board for the Wolfspeed WolfPACK™ Half-Bridge Module Platform. The FM3 module, in a half-bridge configuration, is used as the DUT. In this set up, the short-circuit current is monitored with a 5 mΩ current viewing resistor (CVR) and an external $R_{G,ext}$ of 4 Ω. Figure 10 shows the trajectories of I_D, V_{DS} and V_{GS}. This module is in half-bridge configuration, and therefore voltage and current across the highside (HS) and lowside (LS) MOSFETs are displayed. The HS, represented by turquoise dashed lines, is always turned on at V_{GS} = -15 V, whereas before the short-circuit pulse, the LS MOSFET (solid purple line) is kept turned off at V_{GS} = -4 V. For this reason, to perform a SC type 1 test in this case, the LS must initially block the complete bus voltage of 800 V. As long as the LS MOSFET is in blocking mode, no current will flow through the circuit. Once the LS is turned on, the current shoots through both of the MOSFETs of the CAB016M12FM3, rising rapidly once the LS MOSFET gate voltage surpasses the gate-source threshold voltage $V_{GS,th}$. The current stops rising once it reaches $I_{D,sat}$ for the LS MOSFET.

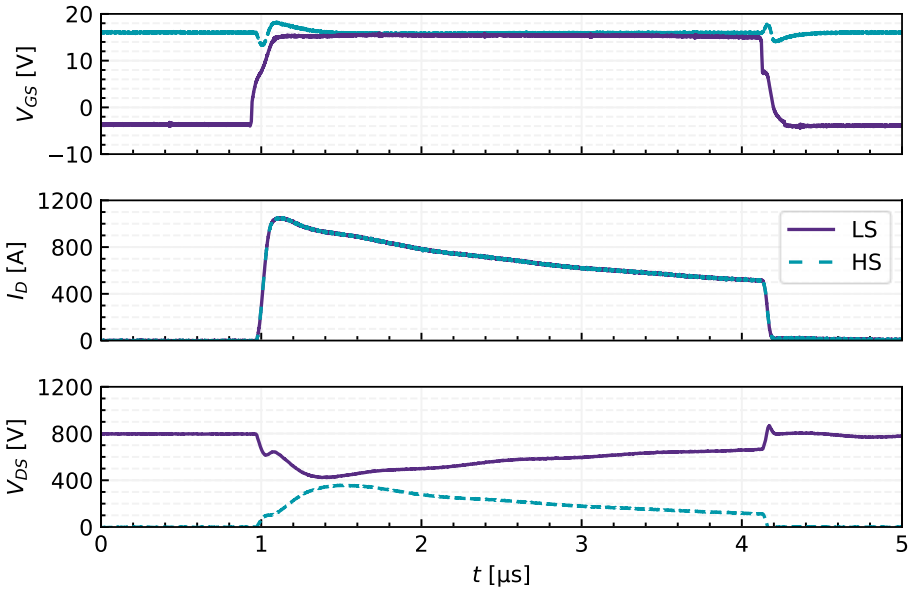

Figure 10: V_{GS}, I_D and V_{DS} for LS and HS during SC type I at V_{bus} = 800 V, T_j = 175°C, V_{GS} = 15 V and $R_{G,ext}$ = 4 Ω

The quick current rise leads to a decrease in the drain source voltage of the LS MOSFET, as per equation (1). Therefore, the voltage across the HS MOSFET rises and leads to a drop and then rise in gate voltage for the HS, as a result of a displacement current between the internal gate capacitances, from C_{GS} to C_{GD} first and then from C_{GD} to C_{GS}. However, this does not influence the short-circuit current, as the gate voltage of the LS MOSFET is still lower and therefore $I_{D,sat}$ of the LS device is limiting the short-circuit current. Once $I_{D,sat}$ is reached, V_{DS} reaches a local maximum, because of $\frac{di}{dt}$ being zero. The LS MOSFET channel continues opening further with increasing V_{GS}, and V_{DS} across the LS starts to rise again once the $\frac{di}{dt}$ decreases. Due to the high energy losses resulting out of a high V_{DS} and high I_D, the LS MOSFET heats up more than the HS device. Therefore, the short-circuit current starts decreasing as a result of negative current temperature feedback. With increasing temperature, $R_{DS,on}$ increases and $I_{D,sat}$ decreases further. During this time the bus voltage is being shared by HS and LS devices, but the LS must dissipate more energy at that point, leading to a stronger increase in temperature and therefore a higher voltage drop compared to the HS. For this reason, the junction temperature Tj of the LS is higher and the voltage across the LS starts increasing again, putting more stress on the LS device. When turning the LS MOSFET gate voltage off, the current starts to decrease until V_{GS} is smaller than $V_{GS,th}$ and no current can flow through the devices. Depending on the bus voltage and the maximum breakdown voltage of the MOSFET, $R_{G,off}$ must be modified to avoid device failure.

4.1 Bus Voltage Influence on Short Circuit

Figure 11 displays I_D, V_{DS} and V_{GS} for the last-pass pulse of the LS MOSFET of a CAB016M12FM3 module at three different bus voltages. The purple, turquoise, and yellow waveforms represent results from tests performed with a V_{DS} of 800 V, 600 V, and 400 V, respectively. This is done to emphasize the influence of the applied bus voltage on the short-circuit withstand time of the device. The theory behind the behavior of the trajectories, such as voltages spikes or breakdowns, are the same as explained in the previous sections. Once the gate of the LS is turned on, the current starts rising and V_{DS} drops. Each test is performed with the same $R_{G,on}$, and therefore

$I_{D,peak}$ is similar for all tests. Yet, at 400 V $I_{D,sat}$ is slightly higher due to the lower energy losses and therefore slightly lower T_j. $I_{D,sat}$ is approximately 1050 A for each test, which is more than 11 times the rated current for the device.

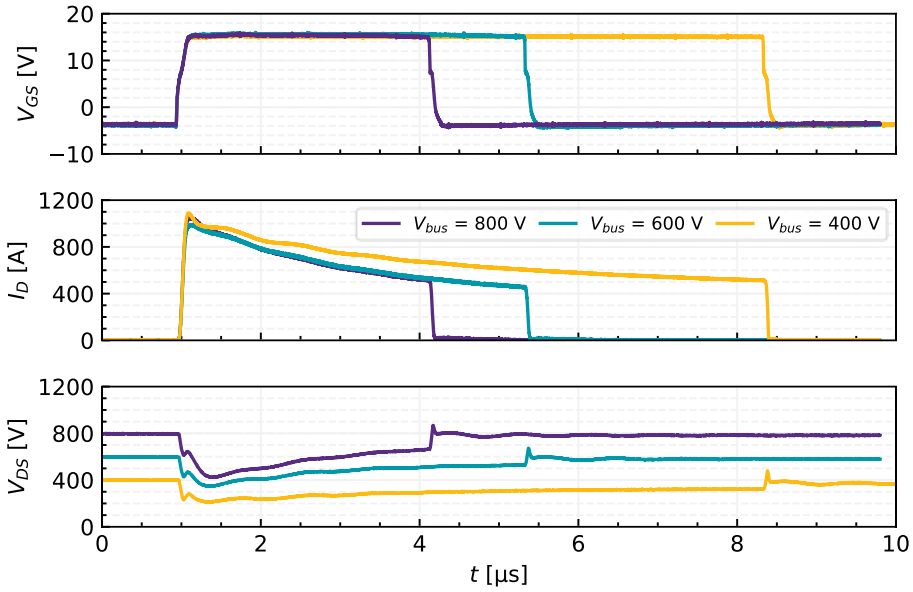

Figure 11: V_{GS}, I_D and V_{DS} for LS and HS during SC type I at T_j = 175°C, V_{GS} = 15 V and $R_{G,ext}$ = 4 Ω

Furthermore, the decrease in current over the short-circuit pulse, as a result of the heating of the device, is much more pronounced for 600 V and 800 V compared to 400 V. Most importantly, the short-circuit withstand time decreases with increase in bus voltage, before the critical short circuit energy is exceeded.

4.2 Short-Circuit Withstand Time and Energy

Figure 12 shows the short-circuit withstand time as a function of the bus voltage. The three colors indicate the maximum, minimum, and average measured short-circuit withstand time for the different voltages. These are displayed for the last-pass pulse (dashed line) and the destructive pulse (solid line). It can be seen that the t_{SC} decreases with increasing bus voltage because the device reaches the critical E_{SC} in a shorter amount of time. The critical short-circuit energy depends on the device design and therefore stays constant with different bus voltages applied. This trend can be seen in Figure 13.

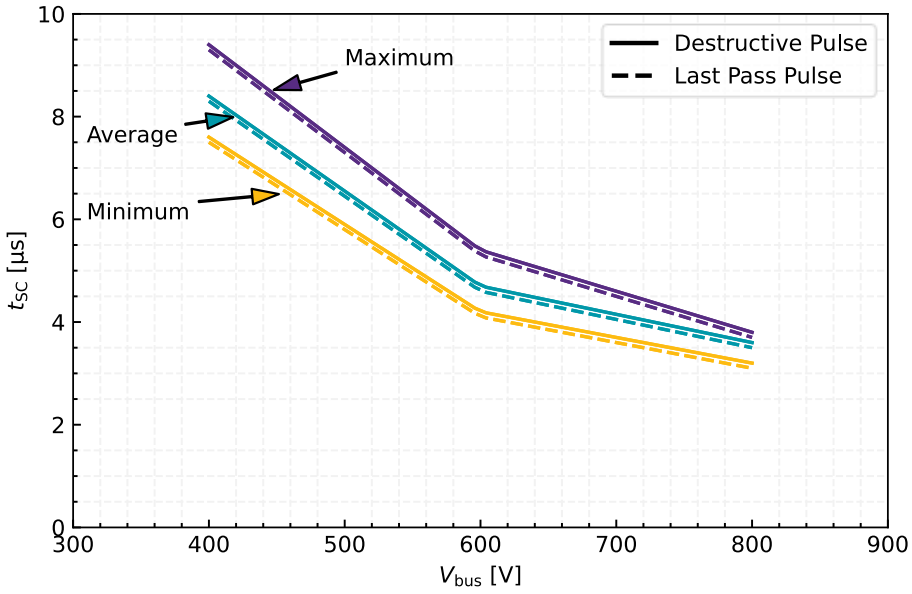

Figure 12: Short-circuit withstand time over bus voltage at T_j = 175°C, V_{GS} = 15 V and $R_{G,ext}$ = 4 Ω

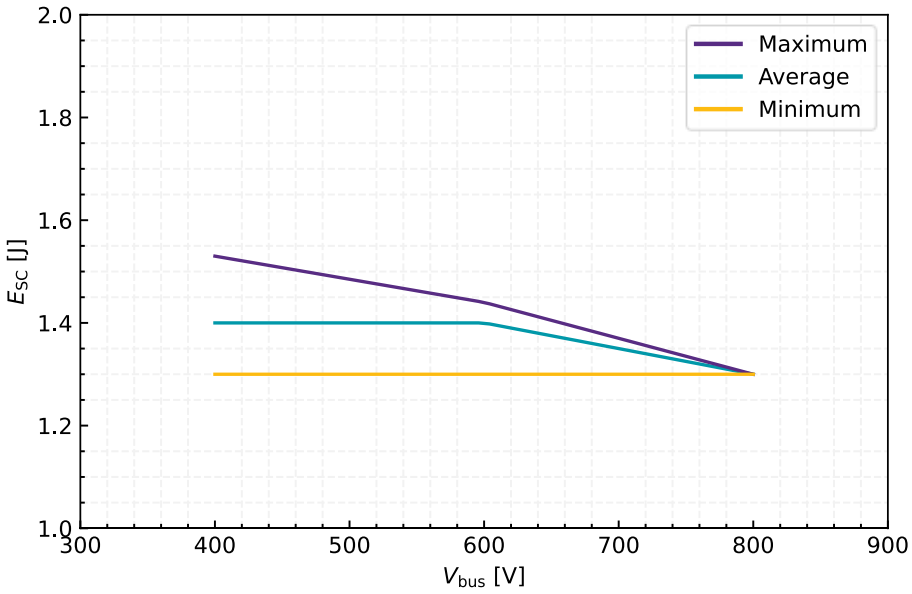

Figure 13: Short-circuit energy of last passed pulse as a function of bus voltage at T_j = 175°C, V_{GS} = 15 V and $R_{G,ext}$ = 4 Ω

Figure 13 displays the E_{SC} dissipated in the last-pass pulse for different bus voltages across the LS device that is turned on into the short. The E_{SC} for the maximum value (purple), average value (turquoise), and minimum value (yellow) is plotted. Once these critical energies are exceeded, the device may be destroyed. One solution to prevent device destruction due to short-circuit events is to use desaturation (DESAT) protection, which is discussed in the next section.

5. DESAT Protection

DESAT protection is used to achieve fast protection for the module in case of a short-circuit event. Here, the goal is to turn off the module quickly and safely before the device's critical short-circuit energy is reached. During the short-circuit event, the MOSFET reaches current saturation, which ultimately leads to desaturation of V_{DS}. Using a desaturation detection circuit, such as in Figure 14, the change in V_{DS} can be detected within a few hundred nano-seconds. For the regular turn-on of a SiC MOSFET, a blanking switch B_{BLK} is used to determine a time when the DESAT protection is not triggered during possible voltage overshoots during a normal turn-on of the device. After this blanking time, V_{DS} monitoring uses a comparator to determine when a certain threshold voltage, $V_{th,DESAT}$, is surpassed. Once $V_{th,DESAT}$ and a delay time caused by C_{BLK} are exceeded, the module is turned off. The additional delay time is applied to avoid false triggering of the turn-off during the subsequent turn-on of the device. This delay time can be tuned by changing the capacitance, C_{BLK}.

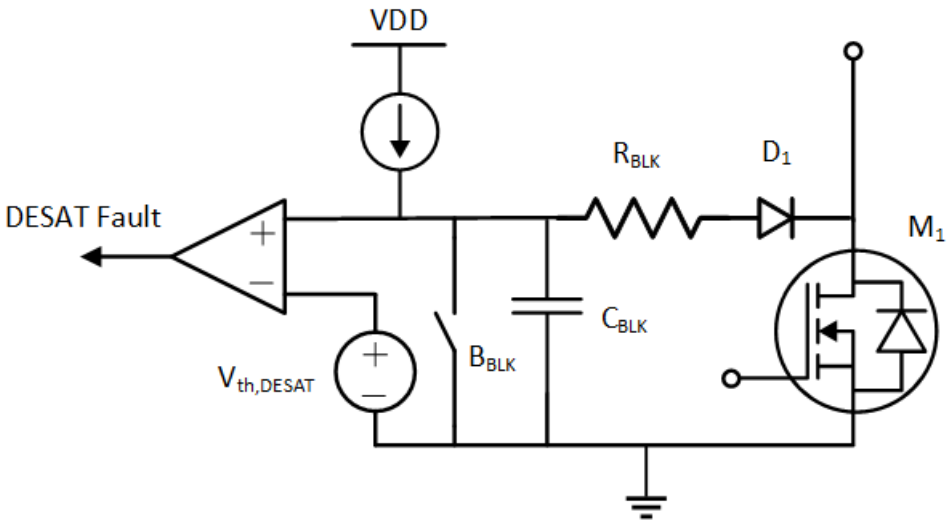

Figure 14: DESAT detection and comparator circuit

Starting from fault initiation to fault detection, a detailed comparison between the SC behavior of a fault under load and a hard switching fault with DESAT protection is discussed. Figure 15 shows the drain source voltage after a SC has been initiated and includes critical times such as the blanking and delay times.

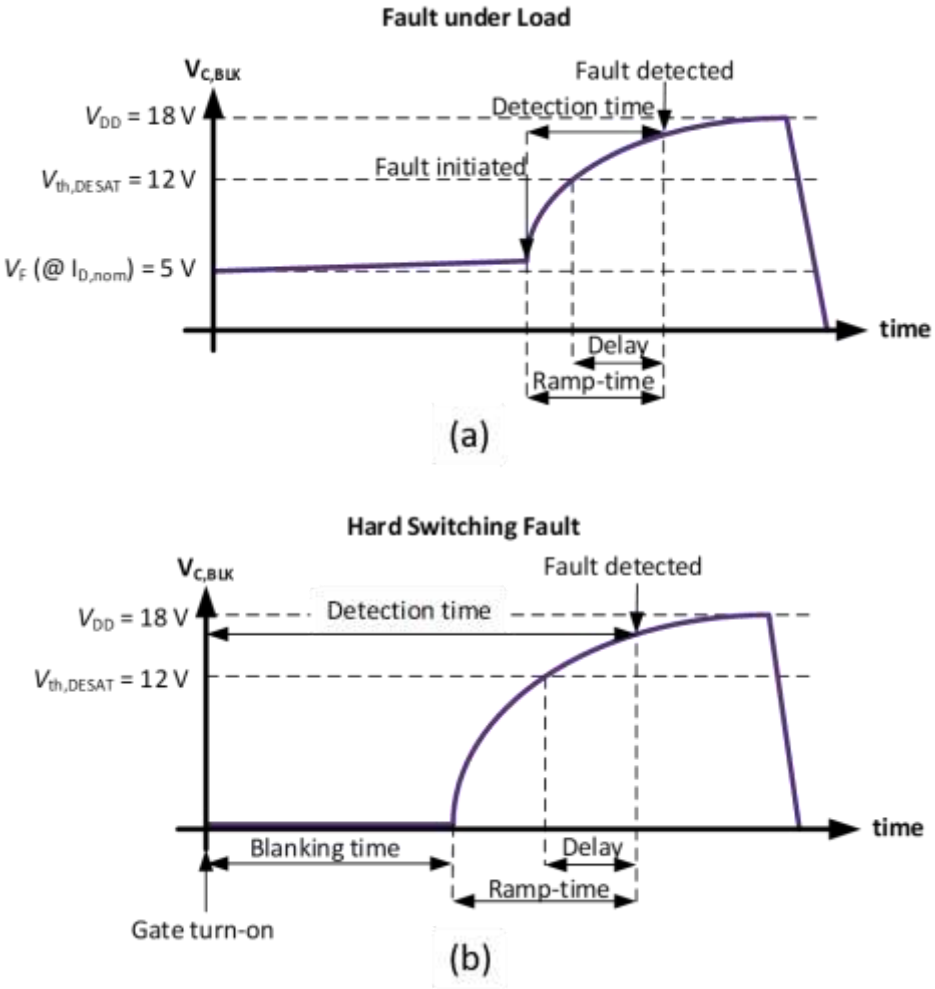

Figure 15: DESAT short circuit detection over time for (a) FUL and (b) HSF

First, the V_{DS} over time for a SC type II is shown in Figure 15 (a). Here, the MOSFET is already conducting when the short occurs and therefore there is a voltage drop during the normal operation. Once the fault occurs, the voltage will start to desaturate with increasing current. If this V_{DS} crosses the preset threshold voltage the protection is triggered, and the device is shut off after the delay time set by the blanking capacitor. In summary, after a short ramp time, the drain source voltage of the device is turned off safely. Similar behavior is seen for a SC type I fault event (see Figure 15 (b)). Differences are the banking time and longer ramp time and therefore the larger detection time when compared to a FUL event. The reason is the inclusion of a long initial blanking time set through a blanking switch B_{BL} (see Figure 14) that is used to prevent false fault detections during turn-on of the SiC MOSFET. This adds to the complete DESAT detection time in case of a HSF. Nevertheless, the time is sufficiently short enough to safely turn off the devices, as displayed by the waveforms in Figure 16.

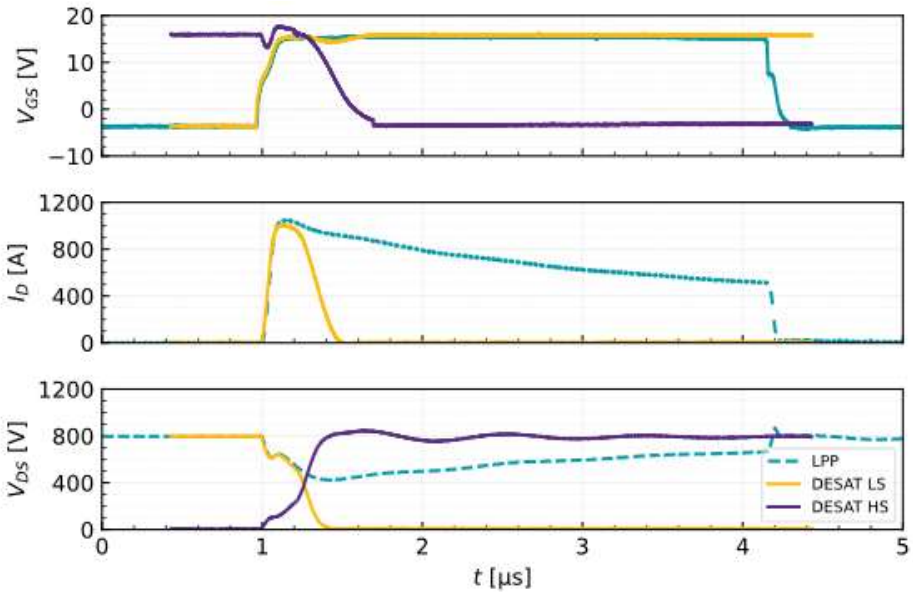

Figure 16: V_{GS}, I_D and V_{DS} showing short-circuit withstand time DESAT protection vs. last pass pulse at V_{bus} = 800 V, T_j = 175°C, V_{GS} = 15 V and $R_{G,ext}$ = 4 Ω

In Figure 16, V_{GS}, I_D, and V_{DS} are displayed for two scenarios. The dashed turquoise line represents the last-pass pulse at given conditions and displays a short-circuit withstand time of 2.9 µs. In purple, a short-circuit event under the same conditions is initiated and turned off through DESAT protection. Here, the short-circuit time is slightly above 300 ns. Additionally, gate and drain voltages are displayed for the HS and LS MOSFETs with DESAT protection. Initially, the HS is turned on, which is indicated by the 15 V gate voltage of the HS. Once the SC type I is initiated, V_{GS} of the LS starts to rise. About 200 ns later the HS gate voltage is turned off and decreases to the off-state voltage. This breaks the short and leads to a reduction in current until the device is fully turned off. Lastly, the HS switch blocks the complete bus voltage when it is fully turned off. This reduces harmful levels of the short-circuit energy that could damage other MOSFETs. Ultimately, each MOSFET must withstand much lower levels of short-circuit energy thanks to DESAT protection. Just how much energy DESAT protection can potentially reduce is shown in Figure 17. The purple curves represent the E_{SC} for different bus voltages. The energies represented by the maximum, average, and minimum purple curves are calculated from the last-past pulse and therefore define the critical energy of the DUT. Here, the device can withstand energies around 1.4 J on average. When using DESAT protection, which is represented by the turquoise curve, the device is turned off before the short-circuit energy reaches 0.2 J. Therefore, the devices can be safely turned off even at high bus voltages.

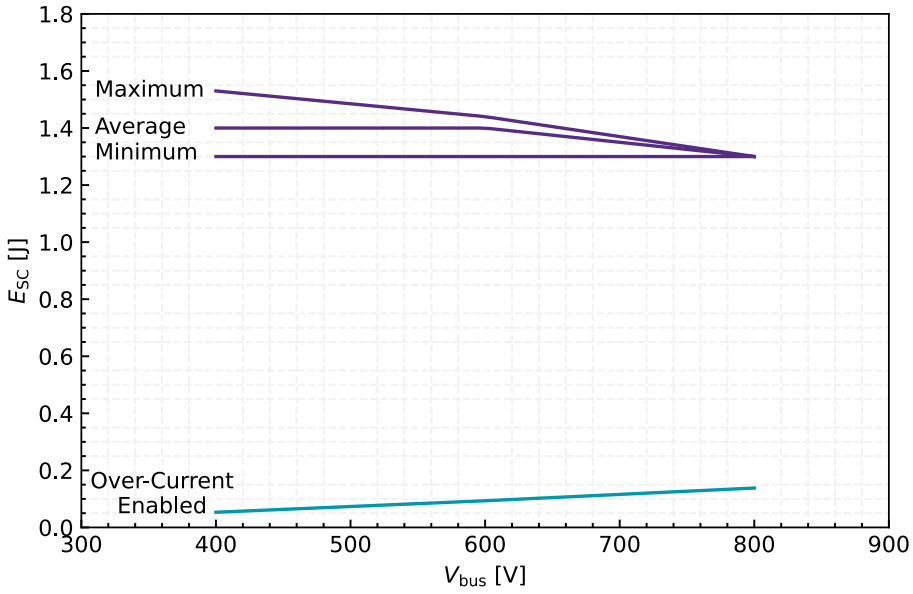

Figure 17: E_{SC} for last pass pulse vs. E_{SC} with DESAT protection over bus voltage at T_j = 175°C, V_{GS} = 15 V and $R_{G,ext}$ = 4 Ω

6. Failure Mechanisms

SiC MOSFETs experience failure through different mechanisms. Under SC fault conditions, a tremendous amount of energy is dissipated by the SiC MOSFET, leading to rapid heating of the internal structure of the device. This kind of heating is typically adiabatic, and the resulting temperatures can trigger a failure within a few microseconds. This section discusses the most common SC failure mechanisms.

6.1 Thermal Runaway

The most common cause of SC failure in SiC MOSFETs is thermal runaway [8]. High current conduction in the simultaneous presence of high voltage results in catastrophic heating near the upper structure of the chip. This extreme heating is intense enough to reflow the top-side metal layer, as shown in Figure 18. In liquid state, the top metal can flow into surface irregularities and cracks, percolating into the SiC, and creating a physical short between source and drain [8] [11]. SiC devices failing in this manner have their terminals shorted.

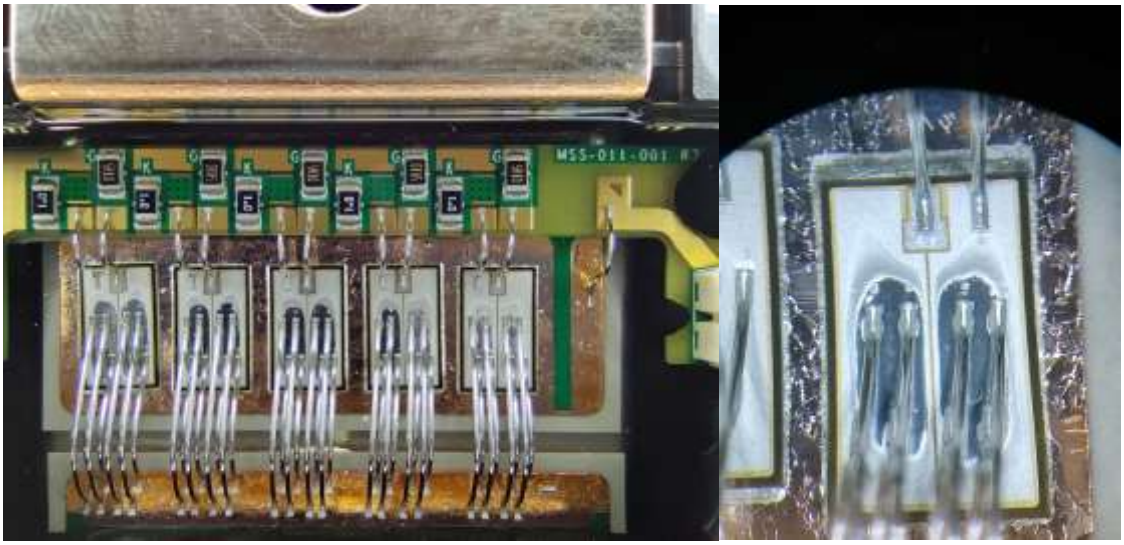

Figure 18: (a) Open XM module after SC with melted topside metallization below bond feet and (b) melted metallization below bond feet for one die.

Depending on the currents and bus voltage, the heat generated by a thermal-runaway-induced short-circuit could be intense enough to burn out the wire bonds and die attach, which could result in the physical destruction of the discrete package or module. It is worth pointing out that although the chip might fail short, it is possible that the discrete package or module terminals fail open due to wire-bond burnout as shown in Figure 19. A thermal-runaway-induced failure can be identified by the lack of anomalous features in the waveforms, i.e., no gate voltage degradation or no current leakage after turning off the SiC MOSFET [12]. Due to the nature of this failure mechanism, if the top-side metal percolation continues after device turn-off, the internal shorting could occur with a delay.

6.2 Gate Oxide Failure

If $V_{DS,bus}$ is low compared to the rated voltage, a longer pulse width is required for the critical energy of the device to be reached. In this case, the energy will have more time to dissipate into other regions of the MOSFET. As a result, the mismatching coefficients of thermal expansion (CTE) between silicon dioxide SiO_2 and SiC can cause cracks on the edges of the gate oxide. Then, the melted aluminum can flow into these cracks leading to a shorted gate and source [13] [11]. Consequently, it is no longer possible to turn on the gate despite the device's ability to remain blocking.

6.3 Activation of Parasitic BJT Inside SiC MOSFET

Under short-circuit fault conditions, most of the current flow occurs from drain to source through the channel. A small portion of current can create leakage path through the P-base. If the amount of leakage current is sufficient to activate the parasitic n-p-n bipolar transistor, this could result in additional heating of the top structure and burn out the MOSFET due to extreme thermal stress over a short time. This mechanism of failure can be identified by anomalies in the device current profile during MOSFET turn-off [12].

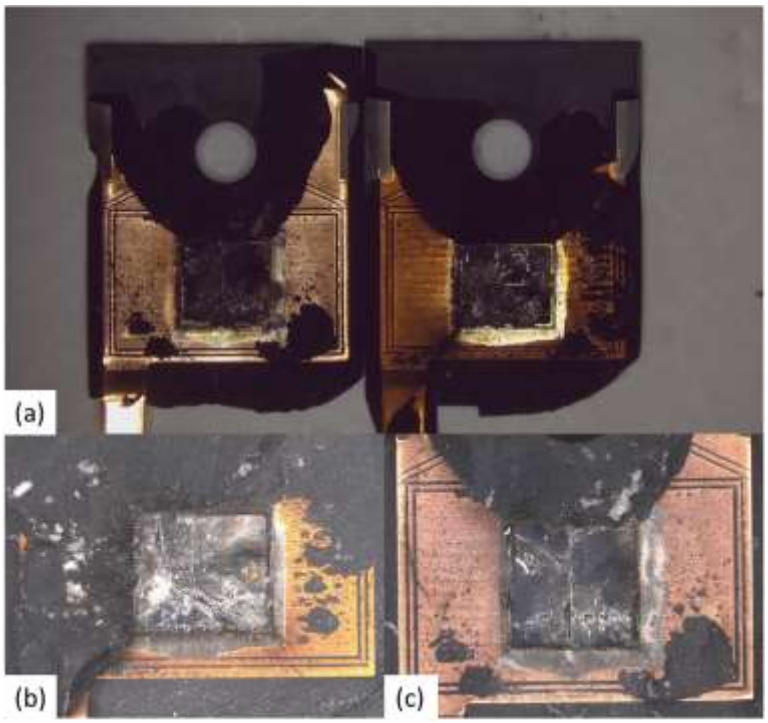

Figure 19: Device destroyed destructively from SC event in TO-247 package

7. Conclusion

In conclusion, a SiC MOSFET's unique saturation characteristics will result in a very high energy density during a SC event. Integrating DESAT protection into the gate driver circuit can greatly reduce the energy seen by the MOSFET in such events. For optimal results, tuning then timing of the blanking switch is required to avoid accidental turn-on complimentary switches. In addition, theory, test methods, and failure mechanisms related to short circuit were discussed. Individual SiC MOSFETs with a higher voltage rating will usually fail catastrophically while SiC MOSFETs with a lower voltage rating will typically fail parametrically. Ultimately, SC performance between devices should be compared using SC withstand energy rather than the SC withstand time. In the future, Wolfspeed looks forward to publishing further investigations with a focus on short-circuit behavior. For any product-specific SC questions please reach out to your Wolfspeed point of contact.

Revision history

Date	Revision	Changes	Authors
December 2023	1	Initial Release	Nicolas Lozada / Felix Fraas

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