Test Report **PRD-00409**

Driving Wolfspeed® C3M™ SiC MOSFETs with Analog Devices® ADuM4121

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Contents

1. Introduction

The purpose of the test report is to document the results of testing performed to characterize the switching characteristics (double pulse), efficiency and thermal performance of Wolfspeed® C3M™ 650V 7-pin D2PAK MOSFETs (C3M0060065J) when driven in a synchronous boost configuration with an Analog Devices® ADuM4121 gate driver.

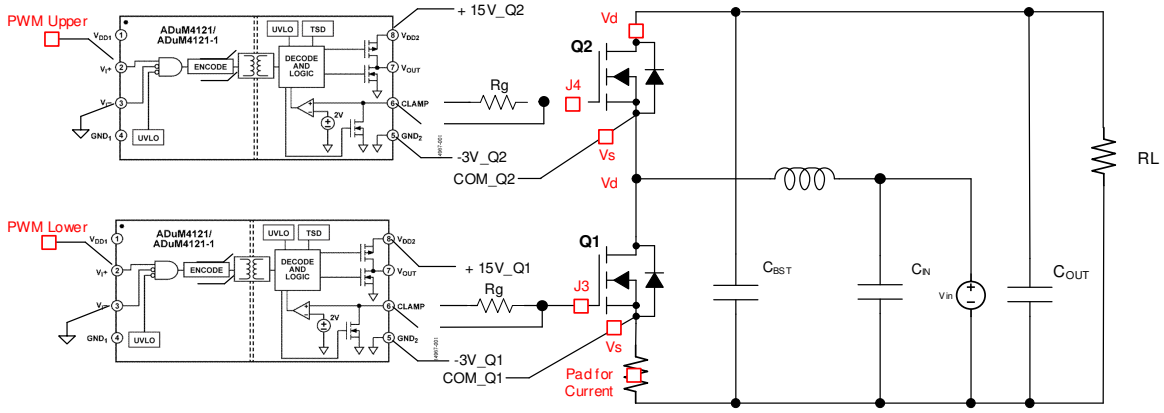
This document along with the user guide for Evaluation kit KIT-CRD-8FF65P may be used to assess the feasibility of new designs using Wolfspeed C3M 650V 7-pin D2PAK MOSFETs with ADuM4121 gate drivers.

2. Background

Non-isolated DC-DC synchronous buck and synchronous boost converters are a popular choice for energy storage systems, industrial power supply and DC-DC converters for electric vehicles. Synchronous boost topologies eliminate the diode loss seen in asynchronous variants, especially at high output currents. SiC MOSFETs offer the benefits of a low diode Q_{rr}, reduced switching losses, low C_{oss} and low $R_{ds(on)}$ which can increase the efficiency of the converters. The use of 7-pin D2PAK packages further reduces parasitic inductances and improves thermal spreading, enabling higher power designs. The ADuM4121 gate driver's low $R_{ds(on)}$ (<2 Ω) provides enough gate drive current to allow the MOSFETs to be driven as fast as 55kV/µs in this test setup. The high common mode transient immunity (CMTI) of >150KV/µs supports data integrity during these fast transitions while an internal Miller clamp prevents any Miller capacitance induced turn on.

3. Test Setup

This section describes the set up for Wolfspeed's KIT-CRD-8FF65P Evaluation Kit in a Synchronous Boost Converter topology (Fig. 1 and Table 1). The electrical parameters for the test setup are shown below in Figure 1 and Figure 2. The KIT-CRD-8FF65P has been modified thermally for this experiment to enable higher power testing but the electrical circuits were unchanged.



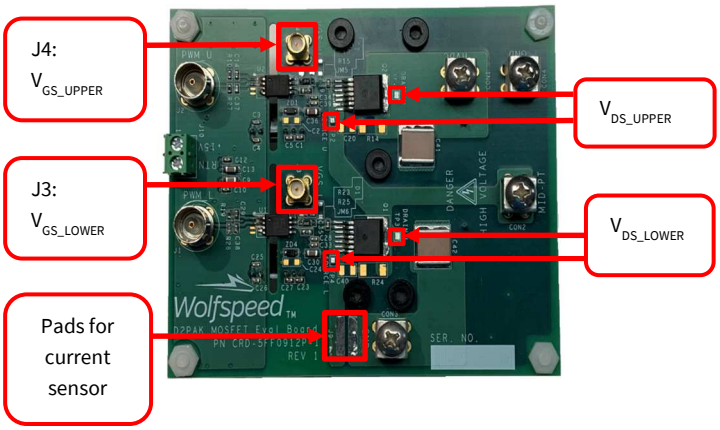


Figure 1: Measurement points on the evaluation board

Table 1: Test setup parameters

Item	Parameters
Input Voltage	200 V
Input Current	6 A-25 A
Output Voltage	≈385 V
Output Current	3 A-15 A
Output Power	1kW-4.5kW
Switching Frequency	100 kHz
Duty Cycle	48.5%
Deadtime	200 ns
Inductor	400 µH
Output Capacitor	40 µF
Input Capacitor	40 µF
Gate Resistor (R_g)	6 Ohms/12 Ohms
C_{gs} Capacitor	1 nF

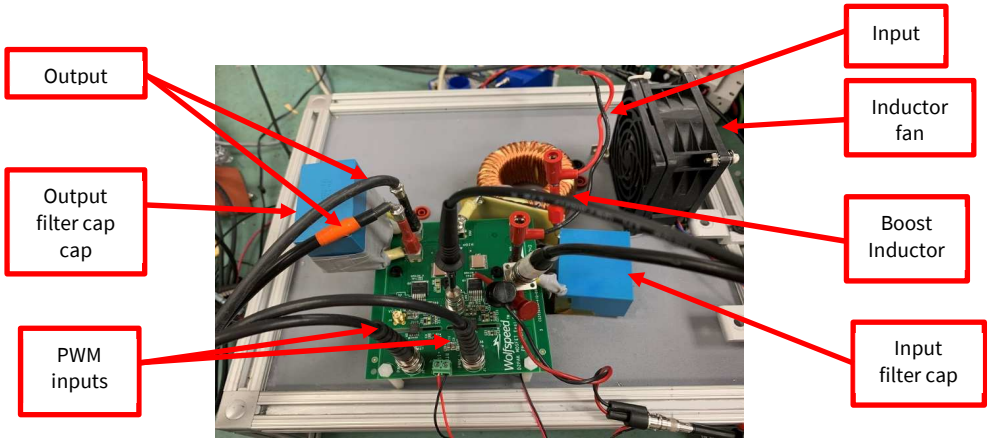


Figure 2: Board setup

3.1 Test Procedure

An SMA to BNC adapter should be connected to J3 (V_{GS} lower MOSFET). A 10X compensated passive oscilloscope probe with a BNC connector is then attached with J3 to monitor the V_{GS} on the lower MOSFET (Fig. 18). A 10mΩ current viewing resistor from T&M Research (P/N: SDN-414-01) is populated at J9 to get current measurements through the lower MOSFET. Since the lower MOSFET is referenced to the -DC link along with the V_{GS} probe, a 100X high-voltage passive probe is attached to the drain and power source of the lower MOSFET to capture V_{DS}. The current shunt is installed backwards so that its common is connected to the same node as V_{DS} and V_{GS} (all three probes are referenced to the same point or the MOSFET source).

The bridge was operated with a fixed duty-cycle and the operating points were obtained by varying R_{load}. The measurements for efficiency, switching energy and temperature were taken at two different values of the gate resistor R_g.

Efficiency Measurements

Efficiency measurements are taken with Yokogawa® WT1600 digital power meter.

Voltages are taken directly from the input and output terminals of the CRD8FF6590P evaluation board. Input and output currents are measured using LEM current sensor

(IT 200-S Ultrastab) and IST ULTRASTAB power supply.

Figure 3: Equipment used for efficiency measurements

Switching Energy Measurements

The switching energy measurements are taken by multiplying V_{DS} and I_{DS} during the turn-on and turn-off event. The product of V_{DS} and I_{DS} yields the switching power waveform (purple). To get the energy, you simply take the area underneath the power curve (purple) during turn-off or turn-on. The two channels being multiplied must be de-skewed to yield accurate measurements.

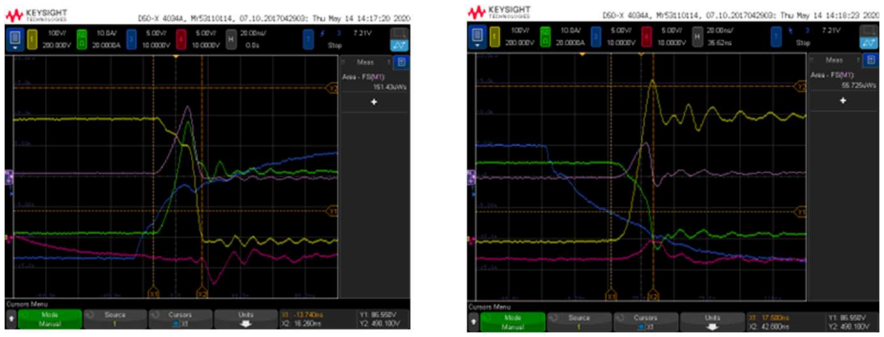


Figure 4: Examples of Turn On (L) and Turn Off (R) signals used for efficiency calculations

Thermal Measurements

All thermal measurements are taken with a FLIR® T420 IR camera like the one shown below

Figure 5: Thermal camera used for measurements

4. Test Results

4.1 Summary of Results

The test results for efficiency, switching energy and MOSFET temperature are summarized for the two values of the gate resistor, R_g.

Efficiency Measurements

Table 2: Measured efficiency

Rg Ohms	Input Voltage (VDC)	Input Current (A)	Input Power (W)	Output Voltage (VDC)	Output Current (A)	Output Power (W)	Overall Efficiency (%)
6	199	6.2	1237	387	3.2	1224	98.97
	199	9.2	1840	385	4.7	1821	98.96
	199	12.3	2448	384	6.3	2420	98.85
	199	15.3	3048	384	7.8	3008	98.69
	199	18.3	3643	383	9.4	3587	98.45
	199	21.3	4237	381	10.9	4162	98.22
	198	24.2	4811	379	12.4	4710	97.90
12	201	6.3	1257	390	3.2	1242	98.83
	201	9.3	1868	389	4.7	1847	98.84
	201	12.4	2489	388	6.3	2457	98.72
	200	15.4	3094	387	7.9	3049	98.55
	200	18.4	3696	385	9.4	3633	98.29
	199	21.4	4264	382	10.9	4181	98.04

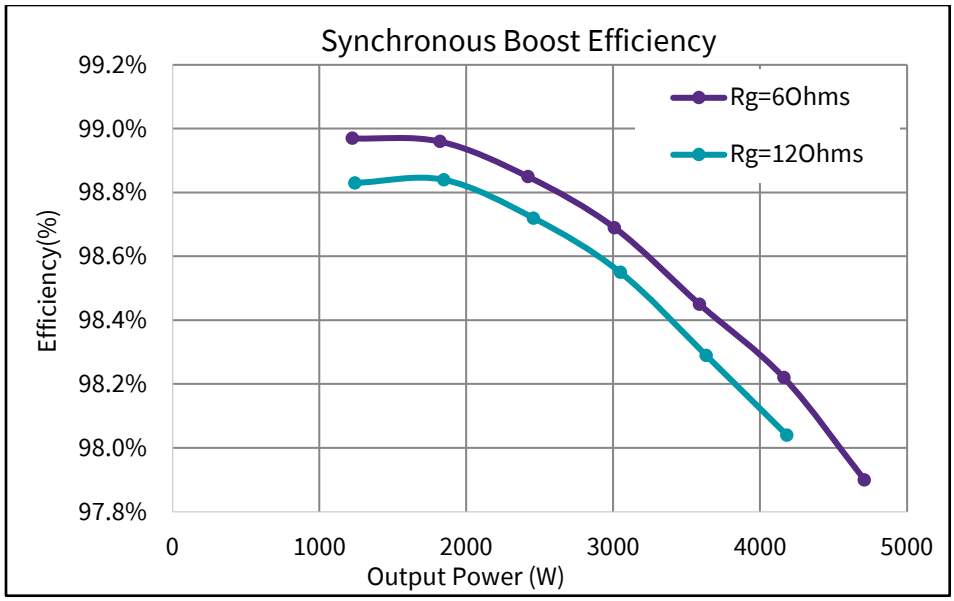


Figure 6: Measured efficiency

Switching Energy and dv/dt Measurements

Table 3: Measured dv/dt and switching energy

Rg	dv/dt (turn-on)	dv/dt (turn-off)	Eon	Eoff
Ohms	V/ns	V/ns	µJ	µJ
6	54.9	49.8	100.4	20.0
	51.6	51.8	114.8	27.2
	47.7	52.9	129.6	34.8
12	42.2	33.4	130.7	44.8
	43.7	34.5	151.4	55.7

Temperature Measurements

Table 4. Measured dv/dt, switching energy and temperature measurements

Rg	Output Power	Ambient Temp	Lower MOSFET Q1 Case Temp	Upper MOSFET Q2 Case Temp	Upper Gate Driver GD1 Case Temp	Lower Gate Driver GD2 Case Temp
Ohms	(W)	(C)	(C)	(C)	(C)	(C)
6	1224	23	34.4	31.6	-	-
	1821	23.1	39.7	36.5	-	-
	2420	24	50.3	46.7	-	-
	3008	24	62.4	58.5	-	-
	3587	24	76.2	72	-	-
	4162	24.4	94.8	89	-	-

Rg	Output Power	Ambient Temp	Lower MOSFET Q1 Case Temp	Upper MOSFET Q2 Case Temp	Upper Gate Driver GD1 Case Temp	Lower Gate Driver GD2 Case Temp
	4710	25.2	120.0	111.2	-	-
12	1242	22.7	37.8	33.0	30.6	28.5
	1847	23.3	46.4	40.3	-	-
	2457	23.7	57.3	48.9	-	-
	3049	24.3	72.2	62.2	-	-
	3633	25	89.6	77.1	37.5	32.7
	4181	25.6	112.8	96.0		

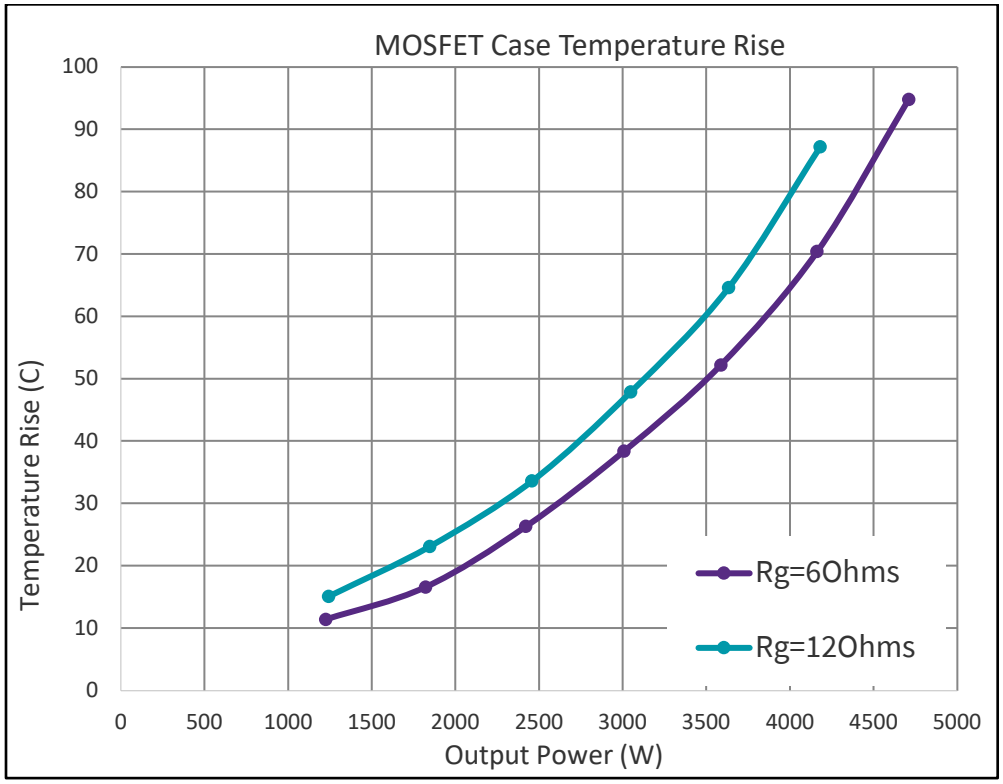


Figure 7: MOSFET Q1 temperature rise

5. Observations

High efficiencies of close to 99% along with well managed MOSFET and gate driver temperature rise can be achieved even at power levels of 4.5kW. High switching slew rates of 55kV/µs have been demonstrated for high efficiencies without disturbances in the gate driver propagation delay or the possibility of Miller induced turn-on. The internal Miller clamp on the AduM4121 provides the driven gate with a lower impedance path to reduce the chance of Miller capacitance induced turn on.

6. Test Data

Oscilloscope plots of relevant signals are summarized in this section. The key for the plots is consistent for all plots in this set:

Green = MOSFET Q1 IDS

Blue = MOSFET Q1 V_{gs}

Pink = MOSFET Q2 V_{gs} (diff probe)

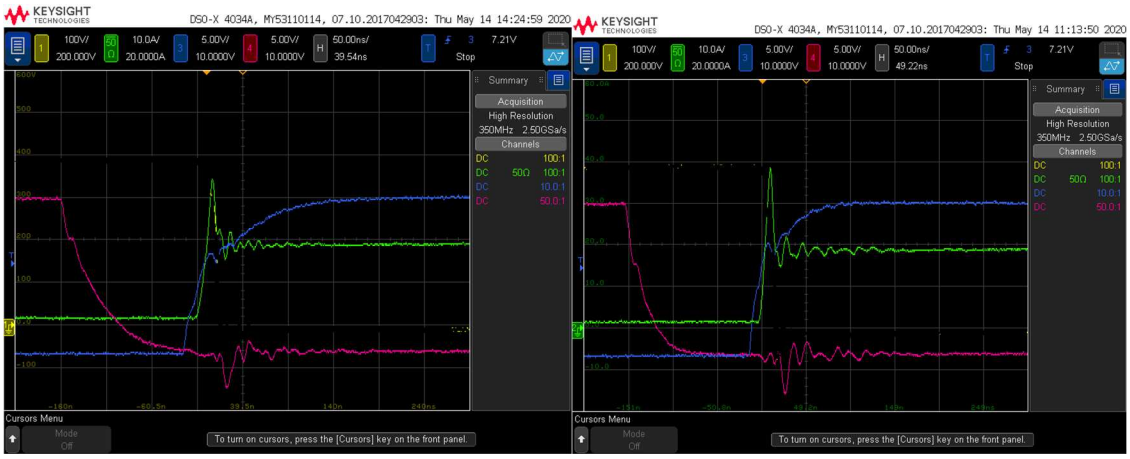


Figure 8: Turn-on switching transition at 3.5kW for R_g=12 (left) and R_g=6 (right). Note that the negative voltage seen on the Q2 V_{gs} is a measurement artifact

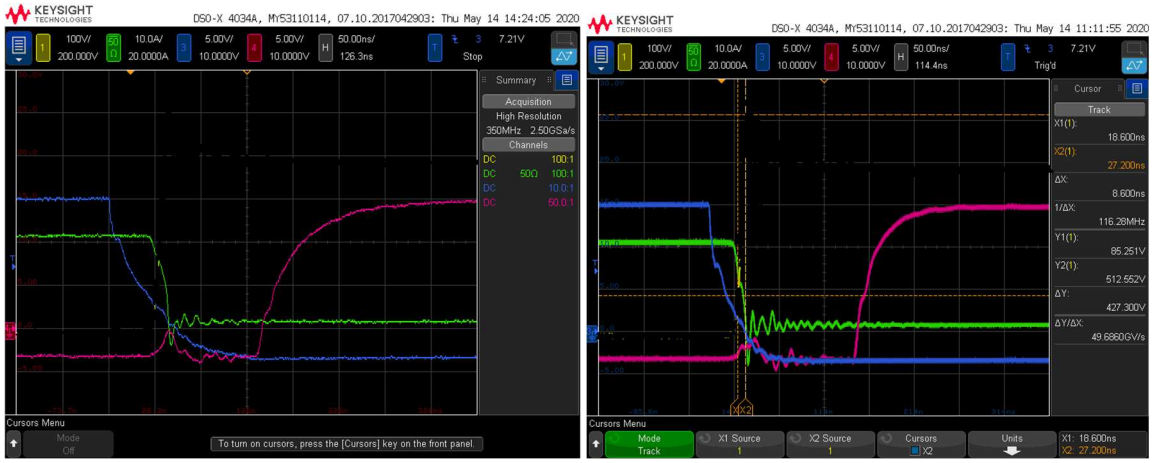


Figure 9: Turn-off switching transition at 3.5kW for R_g=12 (left) and R_g=6 (right)