

# E3M0075120K

Silicon Carbide Power MOSFET  
E-Series Automotive  
N-Channel Enhancement Mode



## Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ( $Q_{rr}$ )
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

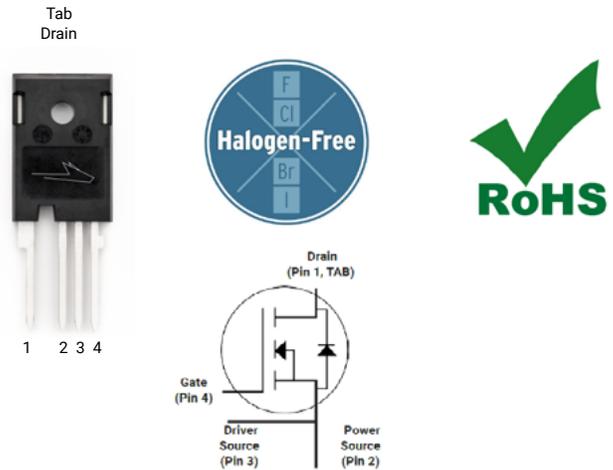
## Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

## Typical Applications

- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters

## Package



Part Number	Package	Marking
E3M0075120K	TO-247-4L	E3M0075120K

## Maximum Ratings ( $T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Note	
$V_{DSmax}$	Drain - Source Voltage	1200	V		
$V_{GSmax}$	Gate - Source Voltage	-8/+19	V	Note: 1	
$I_D$	Continuous Drain Current, $V_{GS} = 15\text{ V}$	$T_c = 25^\circ\text{C}$	32	A	Fig. 19 Note: 2
		$T_c = 100^\circ\text{C}$	23		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width $t_p$ limited by $T_{jmax}$	80	A	Fig. 22	
$P_D$	Power Dissipation, $T_c=25^\circ\text{C}$ , $T_j = 175^\circ\text{C}$	145	W	Fig. 20 Note: 2	
$T_j, T_{stg}$	Operating Junction and Storage Temperature	-55 to +175	$^\circ\text{C}$		
$T_L$	Solder Temperature, 1.6mm (0.063") from case for 10s	260	$^\circ\text{C}$		
$M_d$	Mounting Torque , M3 or 6-32 screw	1	Nm lbf-in		
		8.8			

Note (1): Recommended turn off / turn on gate voltage  $V_{GS} = -4V...0V / +15V$

Note (2): Verified by design

**Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.6	3.6	V	$V_{DS} = V_{GS}, I_D = 5\text{ mA}$	Fig. 11
			2.1		V	$V_{DS} = V_{GS}, I_D = 5\text{ mA}, T_J = 175^\circ\text{C}$	
$I_{DSS}$	Zero Gate Voltage Drain Current		1	50	$\mu\text{A}$	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$	
$I_{GSS}$	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance		75	97.5	m $\Omega$	$V_{GS} = 15\text{ V}, I_D = 17.9\text{ A}$	Fig. 4, 5, 6
			135			$V_{GS} = 15\text{ V}, I_D = 17.9\text{ A}, T_J = 175^\circ\text{C}$	
$g_{fs}$	Transconductance		11		S	$V_{DS} = 20\text{ V}, I_{DS} = 17.9\text{ A}$	Fig. 7
			10.5			$V_{DS} = 20\text{ V}, I_{DS} = 17.9\text{ A}, T_J = 175^\circ\text{C}$	
$C_{iss}$	Input Capacitance		1480		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{V to }1000\text{ V}$ $F = 1\text{ MHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
$C_{oss}$	Output Capacitance		58				
$C_{rss}$	Reverse Transfer Capacitance		2.7				
$E_{oss}$	$C_{oss}$ Stored Energy		32		$\mu\text{J}$		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		67		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0\dots 800\text{V}$	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		96				
$E_{oN}$	Turn-On Switching Energy (External Diode)		257		$\mu\text{J}$	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 20\text{ A},$ $R_{G(ext)} = 2.5\ \Omega, L = 135\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = External SiC DIODE	Fig. 26, 28
$E_{oOFF}$	Turn Off Switching Energy (External Diode)		71				
$E_{oN}$	Turn-On Switching Energy (Body Diode FWD)		467		$\mu\text{J}$	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 20\text{ A},$ $R_{G(ext)} = 2.5\ \Omega, L = 135\ \mu\text{H}, T_J = 175^\circ\text{C}$ FWD = Internal Body Diode	Fig. 26, 28
$E_{oOFF}$	Turn-Off Switching Energy (Body Diode FWD)		77				
$t_{d(on)}$	Turn-On Delay Time		8		ns	$V_{DD} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 20\text{ A}, R_{G(ext)} = 2.5\ \Omega,$ Timing relative to $V_{DS}$ Inductive load	Fig. 27, 28
$t_r$	Rise Time		22				
$t_{d(off)}$	Turn-Off Delay Time		29				
$t_f$	Fall Time		11				
$R_{G(int)}$	Internal Gate Resistance		9.0		$\Omega$	$f = 1\text{ MHz}$	
$Q_{gs}$	Gate to Source Charge		17		nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 17.9\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
$Q_{gd}$	Gate to Drain Charge		18				
$Q_g$	Total Gate Charge		55				

Note (3):  $C_{o(er)}$ , a lumped capacitance that gives same stored energy as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 800V  
 $C_{o(tr)}$ , a lumped capacitance that gives same charging time as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 800V


**Reverse Diode Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$V_{SD}$	Diode Forward Voltage	4.8		V	$V_{GS} = -4\text{ V}, I_{SD} = 9\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.2		V	$V_{GS} = -4\text{ V}, I_{SD} = 9\text{ A}, T_J = 175^\circ\text{C}$	
$I_S$	Continuous Diode Forward Current		27	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
$I_{S, pulse}$	Diode pulse Current		80	A	$V_{GS} = -4\text{ V}$ , pulse width $t_p$ limited by $T_{Jmax}$	
$t_{rr}$	Reverse Recover time	20		ns	$V_{GS} = -4\text{ V}, I_{SD} = 20\text{ A}, V_R = 800\text{ V}$ $dif/dt = 5280\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
$Q_{rr}$	Reverse Recovery Charge	376		nC		
$I_{rrm}$	Peak Reverse Recovery Current	25		A		
$t_{rr}$	Reverse Recover time	28		ns	$V_{GS} = -4\text{ V}, I_{SD} = 20\text{ A}, V_R = 800\text{ V}$ $dif/dt = 1305\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
$Q_{rr}$	Reverse Recovery Charge	338		nC		
$I_{rrm}$	Peak Reverse Recovery Current	16		A		

**Thermal Characteristics**

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.88	1.03	$^\circ\text{C}/\text{W}$		Fig. 21

### Typical Performance

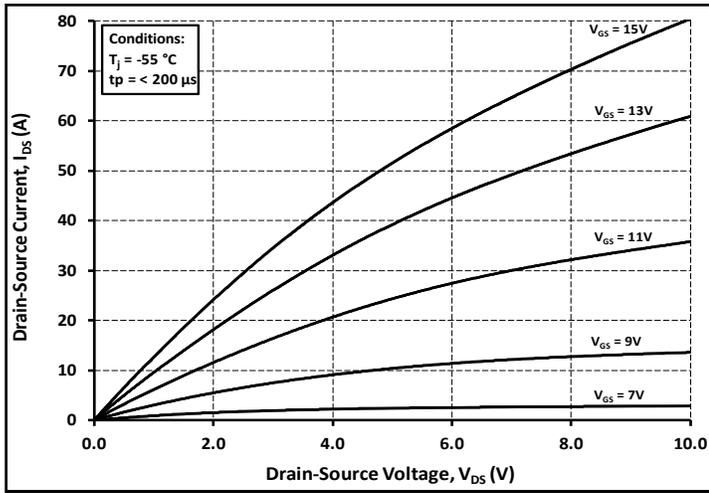


Figure 1. Output Characteristics  $T_J = -55\text{ }^\circ\text{C}$

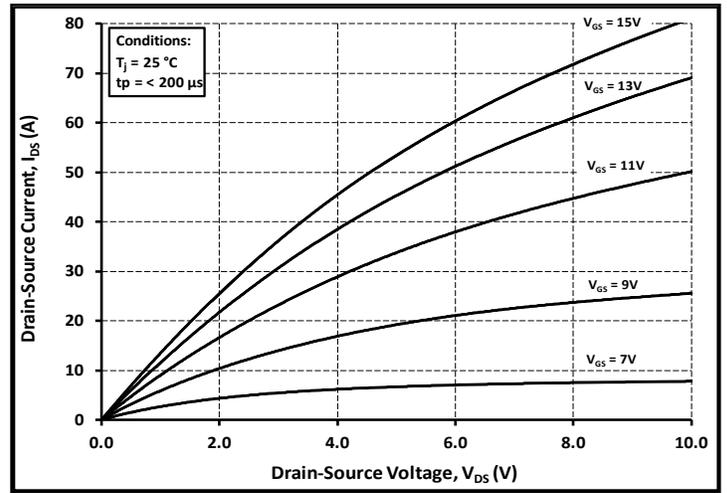


Figure 2. Output Characteristics  $T_J = 25\text{ }^\circ\text{C}$

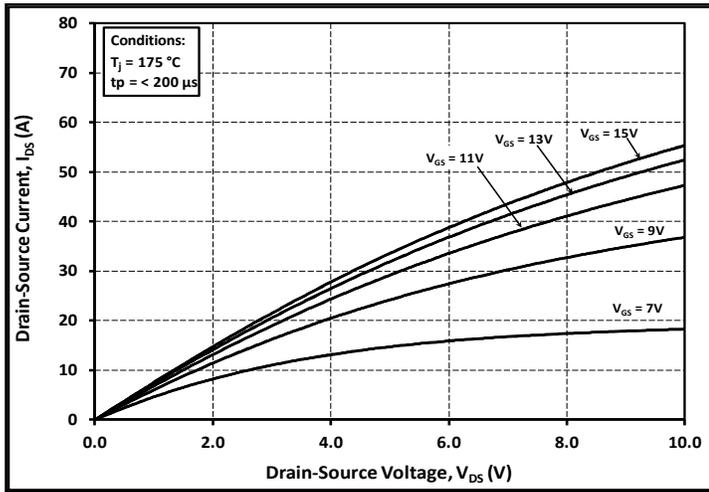


Figure 3. Output Characteristics  $T_J = 175\text{ }^\circ\text{C}$

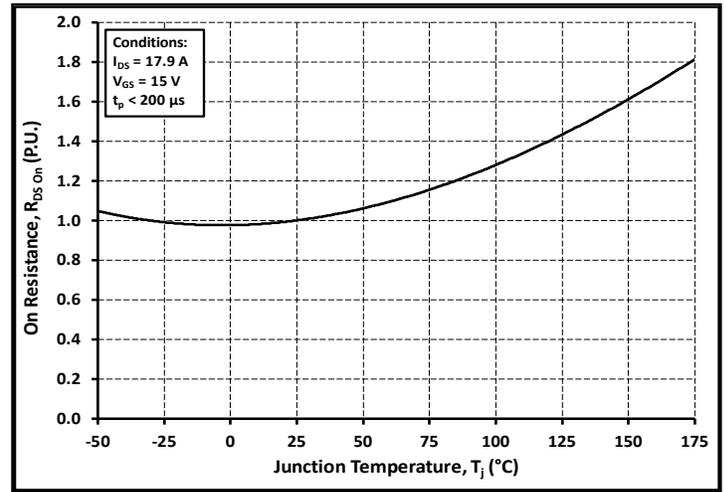


Figure 4. Normalized On-Resistance vs. Temperature

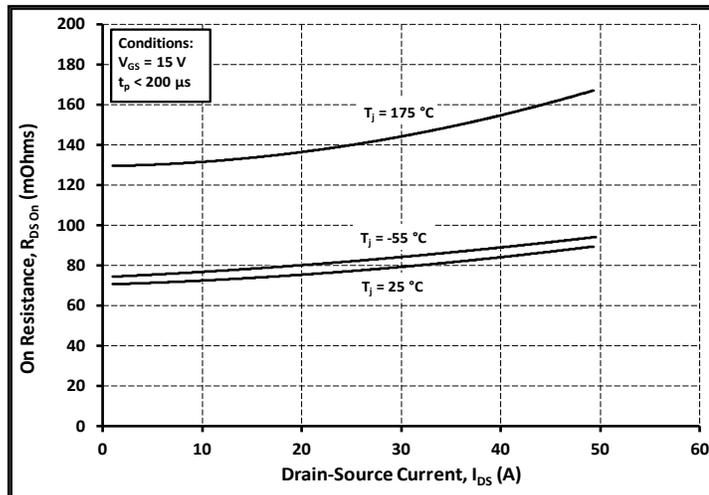


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

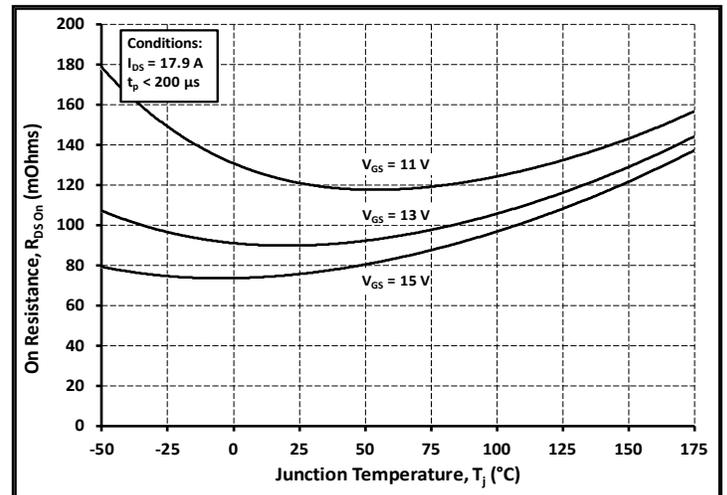


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

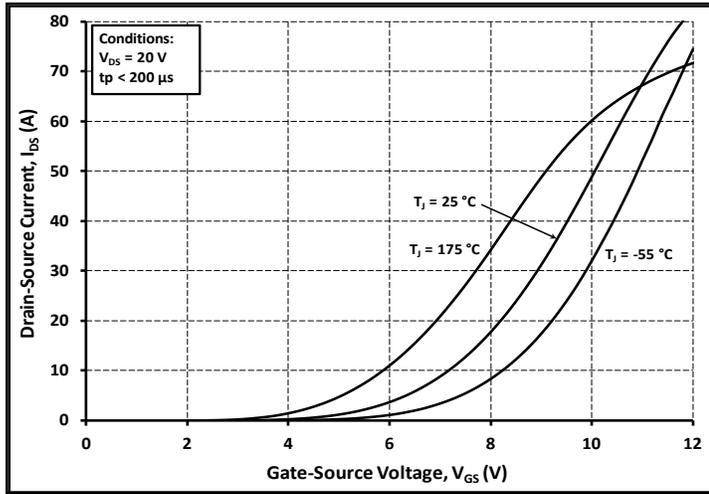


Figure 7. Transfer Characteristic for Various Junction Temperatures

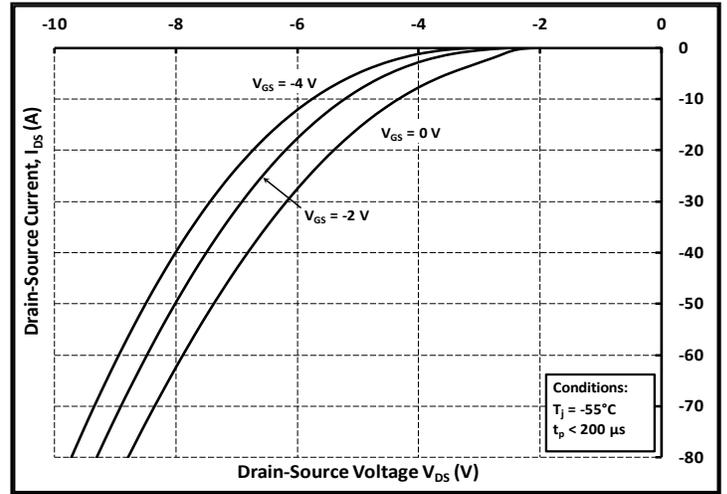


Figure 8. Body Diode Characteristic at -55 °C

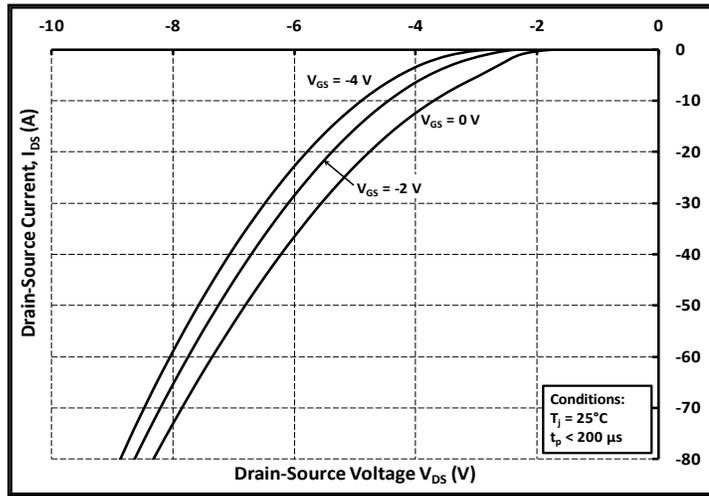


Figure 9. Body Diode Characteristic at 25 °C

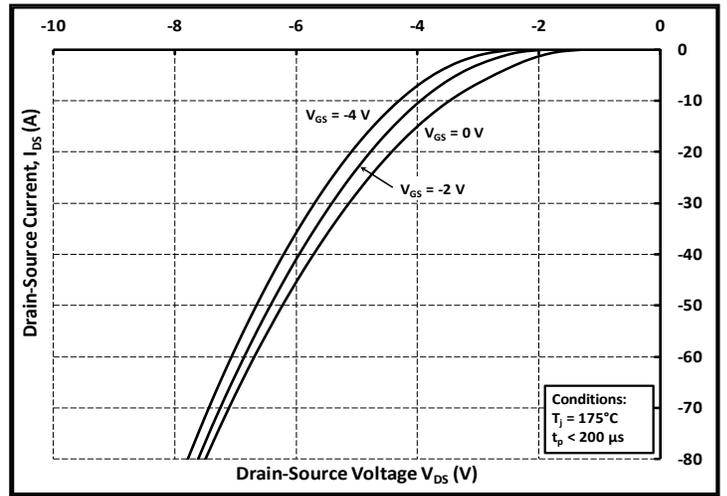


Figure 10. Body Diode Characteristic at 175 °C

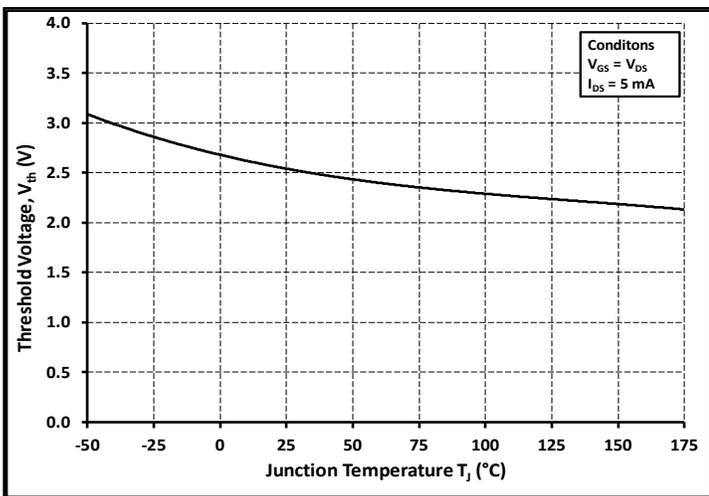


Figure 11. Threshold Voltage vs. Temperature

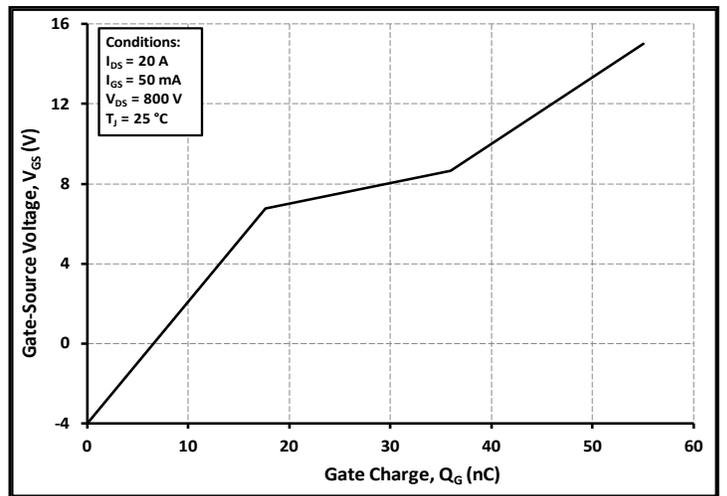


Figure 12. Gate Charge Characteristics



Typical Performance

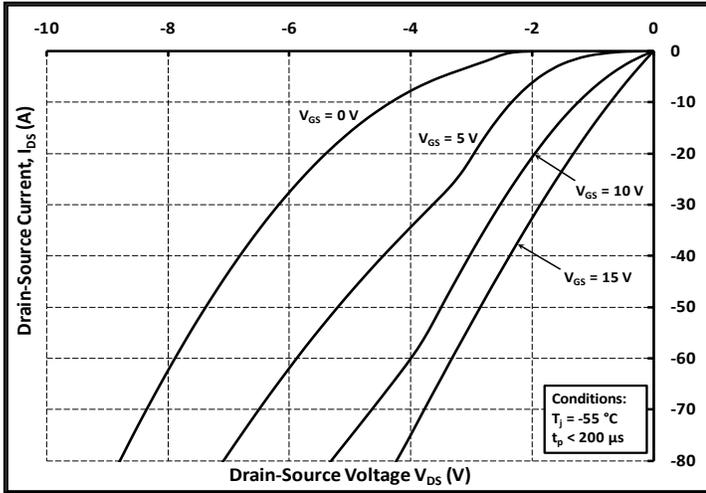


Figure 13. 3rd Quadrant Characteristic at -55 °C

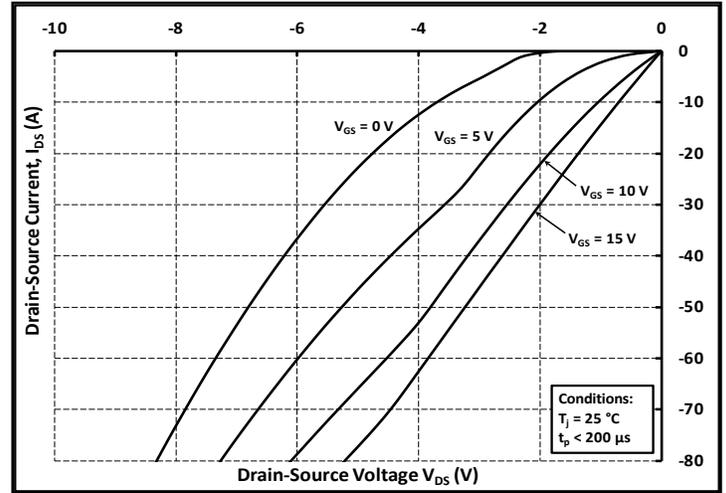


Figure 14. 3rd Quadrant Characteristic at 25 °C

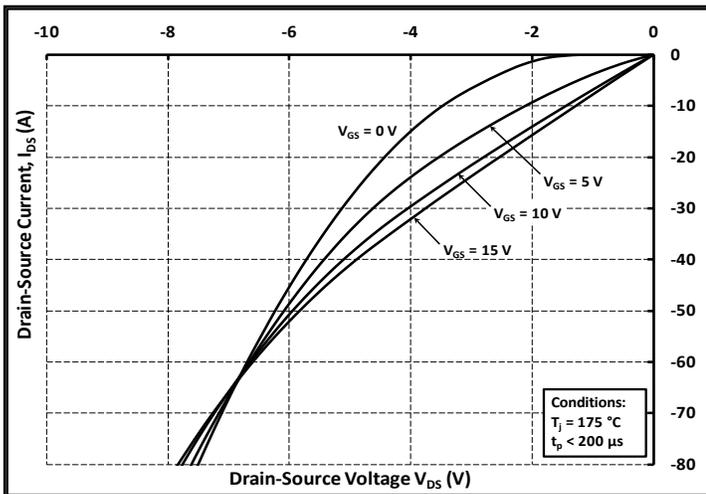


Figure 15. 3rd Quadrant Characteristic at 175 °C

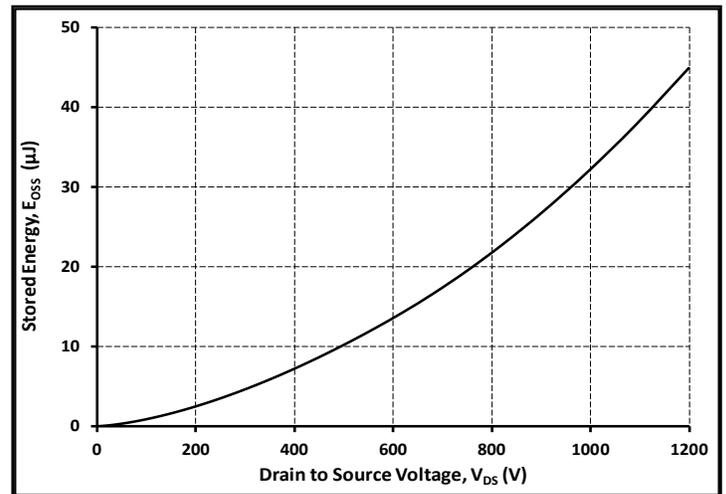


Figure 16. Output Capacitor Stored Energy

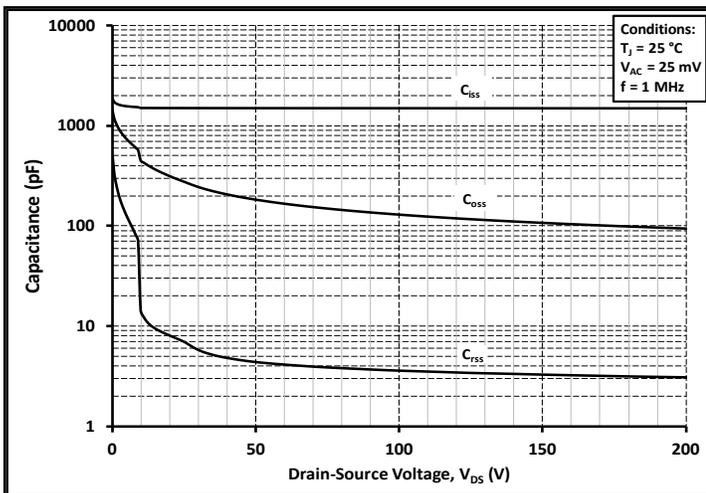


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

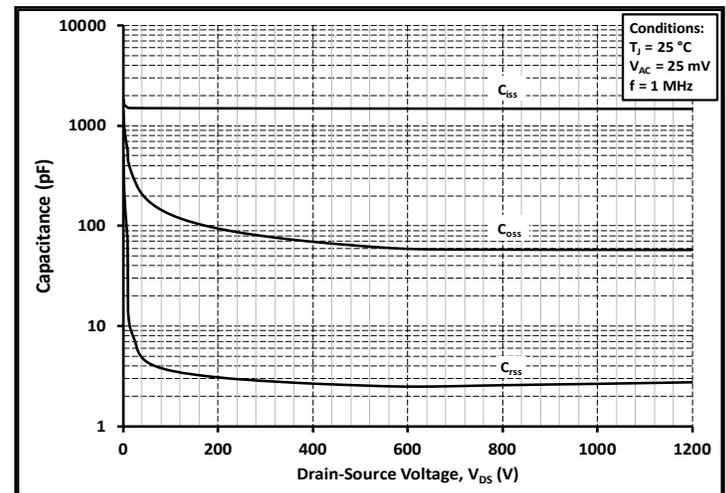


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)



Typical Performance

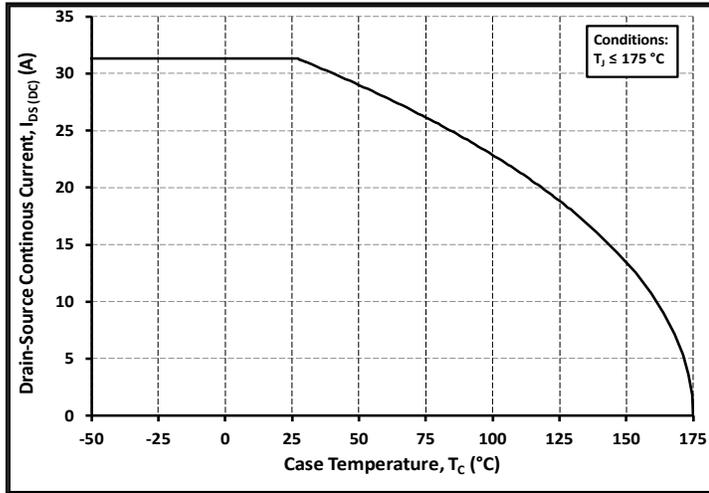


Figure 19. Continuous Drain Current Derating vs. Case Temperature

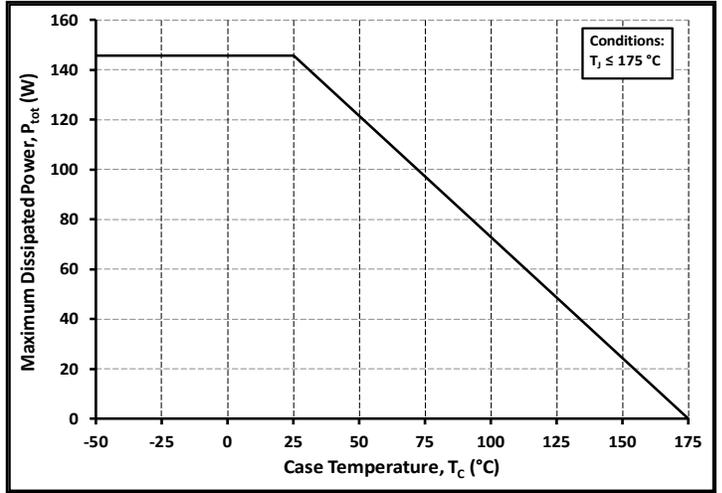


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

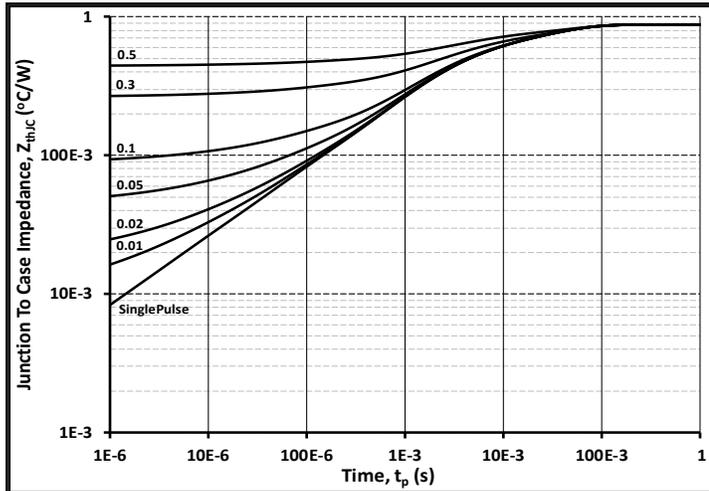


Figure 21. Transient Thermal Impedance (Junction - Case)

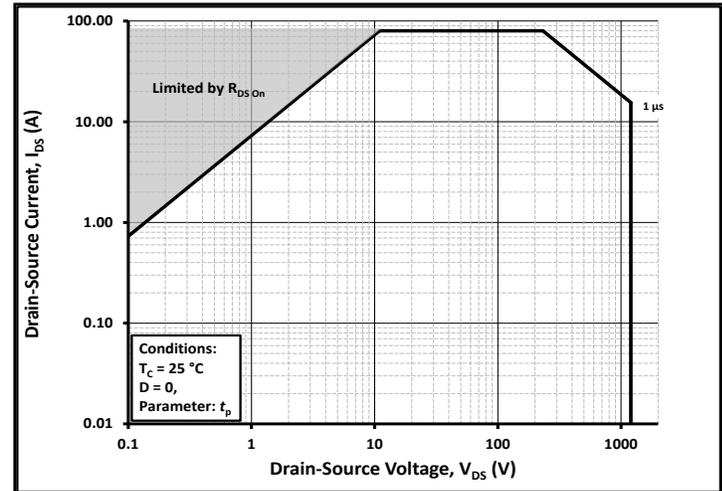


Figure 22. Safe Operating Area

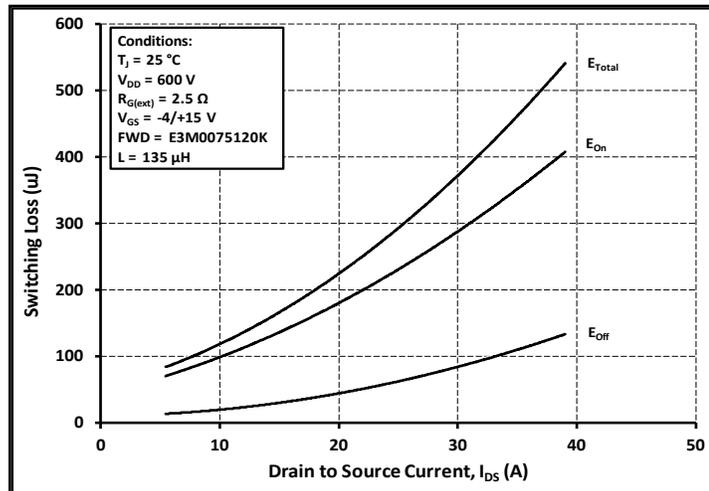


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 600V$ )

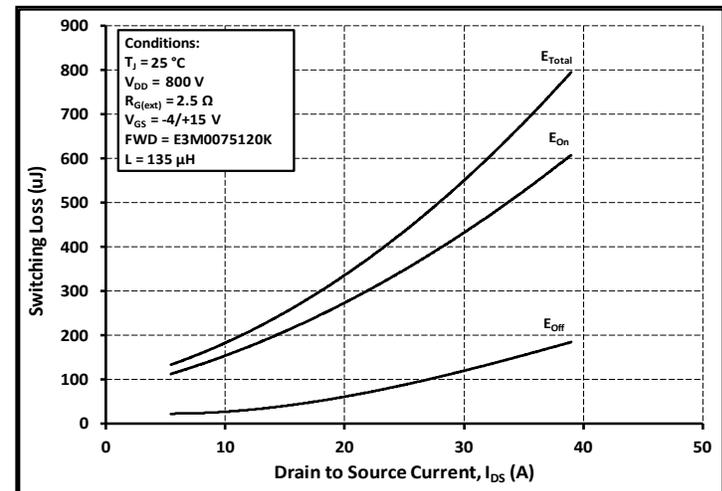


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 800V$ )



Typical Performance

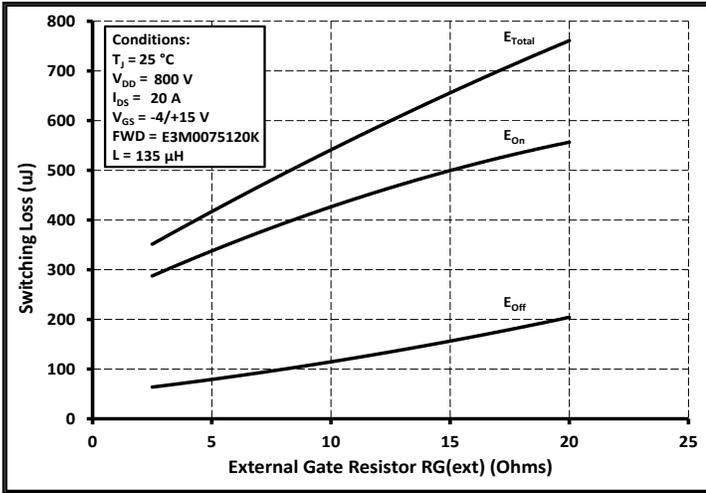


Figure 25. Clamped Inductive Switching Energy vs.  $R_{G(ext)}$

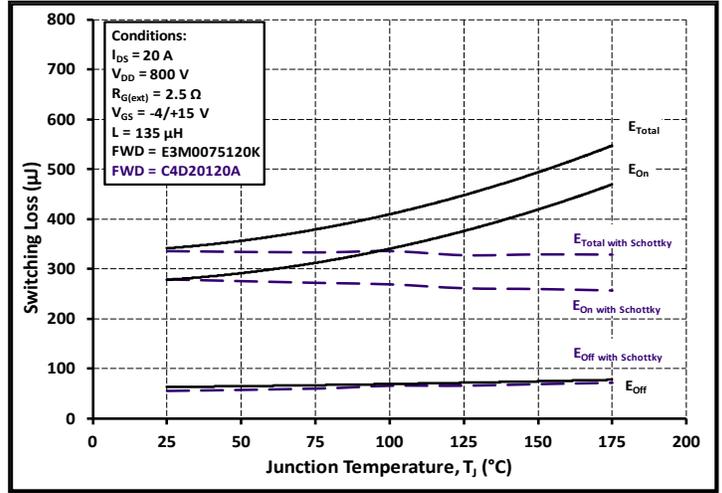


Figure 26. Clamped Inductive Switching Energy vs. Temperature

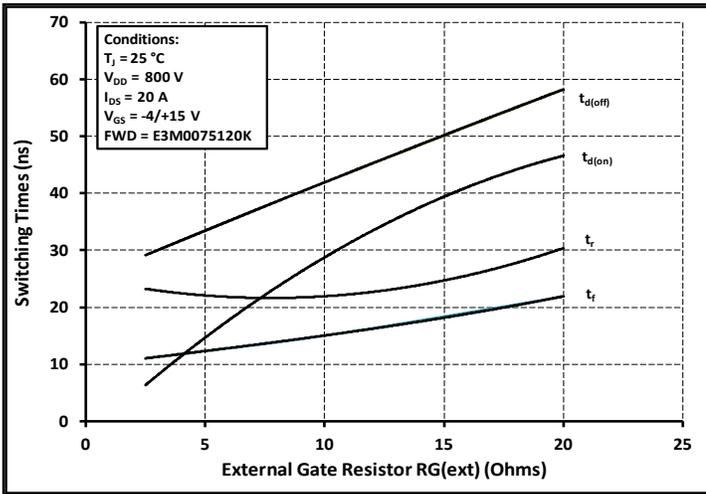


Figure 27. Switching Times vs.  $R_{G(ext)}$

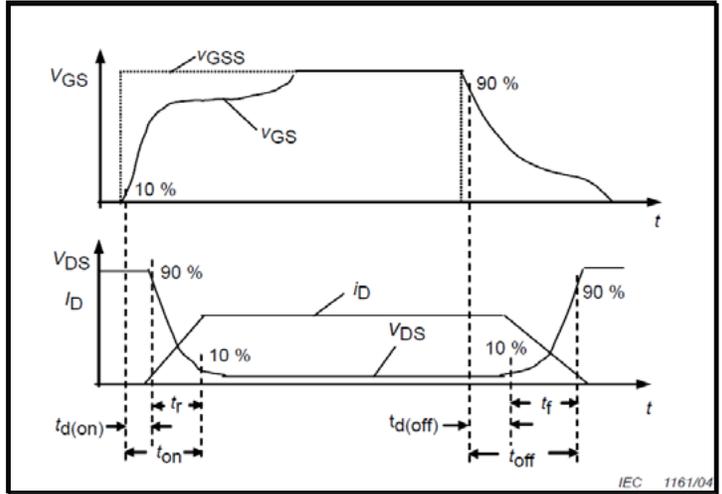


Figure 28. Switching Times Definition

## Test Circuit Schematic

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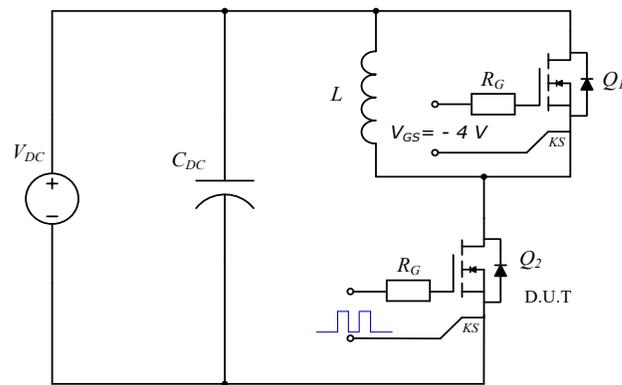
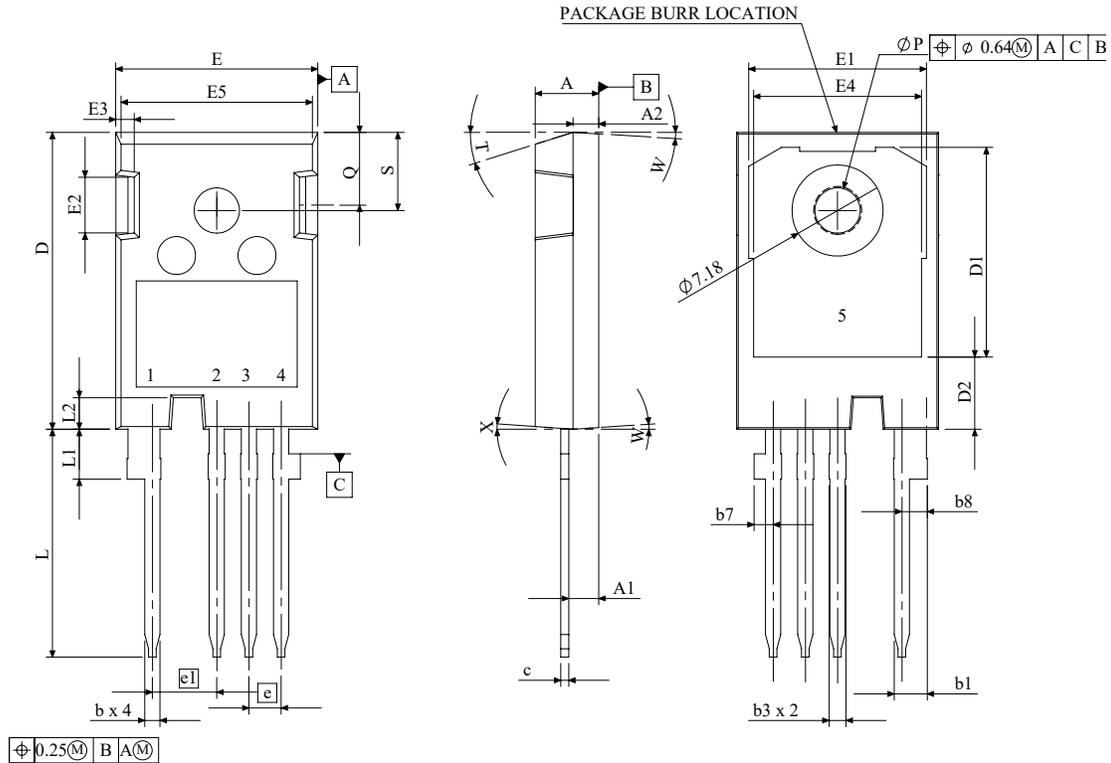


Figure 29. Clamped Inductive Switching Waveform Test Circuit

Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.23	2.54
A2	1.91	2.16
b	1.07	1.33
b1	2.39	2.94
b3	1.07	1.60
b7	1.30	1.70
b8	1.80	2.20
c	0.55	0.68
D	23.30	23.63
D1	16.25	17.65
D2	5.55	5.95
E	15.75	16.13
E1	13.1	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
E5	14.65	15.05
e1	5.08 BSC	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
$\phi P$	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	DRAIN
2	SOURCE
3	DRIVER SOURCE
4	GATE
5	DRAIN

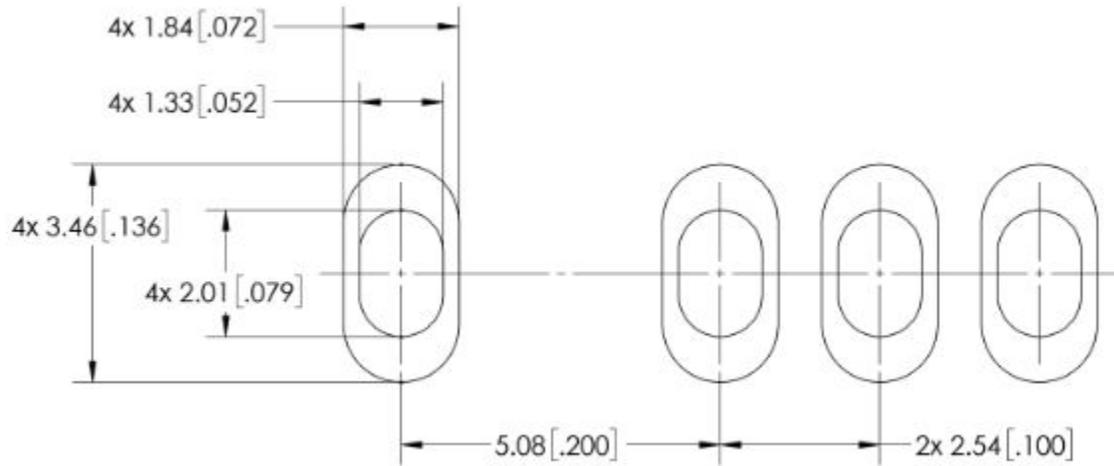
NOTE:

1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS



## Recommended Solder Pad Layout

All dimensions in mm





## Revision history

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Document Version	Date of release	Description of changes
2.0	March-2021	Initial datasheet
3.0	November-2023	Updated format and logo to Wolfspeed
4	January - 2025	Legal Disclaimer Updated
5	March - 2025	Removed $V_{AC}$ from $R_{G(int)}$ test condition Updated Fig 22 $E_{ON}$ and $E_{OFF}$ table values and conditions corrected Fig 25 updated



## Notes & Disclaimer

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