# E3M0040120J2

## Silicon Carbide Power MOSFET
## E-Series Automotive
## N-Channel Enhancement Mode

## Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- 4.7mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ($Q_{rr}$)
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

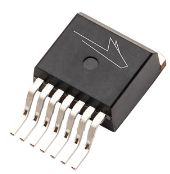
## Benefits

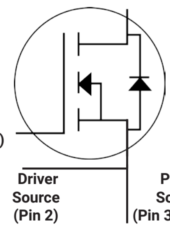
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

## Applications

- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters

## Package




| Part Number | Package | Marking |
|---|---|---|
| E3M0040120J2 | TO-263-7XL | E3M0040120J2 |

## Maximum Ratings ($T_C$ = 25 ˚C unless otherwise specified)

| Symbol | Parameter | | Value | Unit | Note |
|---|---|---|---|---|---|
| $V_{DSmax}$ | Drain - Source Voltage | | 1200 | V | |
| $V_{GSmax}$ | Gate - Source Voltage | | -8/+19 | V | Note: 1 |
| $I_D$ | Continuous Drain Current, $V_{GS}$ = 15 V | $T_C$ = 25˚C | 63 | A | Fig. 19<br>Note: 2 |
| | | $T_C$ = 100˚C | 46 | | |
| $I_{D(pulse)}$ | Pulsed Drain Current, Pulse width $t_P$ limited by $T_{jmax}$ | | 127 | A | Fig. 22 |
| $P_D$ | Power Dissipation, $T_C$=25˚C, $T_J$ = 175 ˚C | | 294 | W | Fig. 20<br>Note: 2 |
| $T_J$ , $T_{stg}$ | Operating Junction and Storage Temperature | | -55 to +175 | ˚C | |
| $T_L$ | Solder Temperature, 1.6mm (0.063") from case for 10s | | 260 | ˚C | |

Note (1): Recommended turn off / turn on gate voltage $V_{GS}$ - 4V...0V / +15V
Note (2): Verified by design


4600 Silicon Drive | Durham, NC 27703 | Tel: +1.919.313.5300 | wolfspeed.com/power

## Electrical Characteristics ($T_C$ = 25˚C unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | 1200 | | | V | $V_{GS}$ = 0 V, $I_D$ = 100 μA | |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.8 | 2.7 | 3.8 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 8.77 mA | Fig. 11 |
| | | | 2.2 | | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 8.77 mA, $T_J$ = 175ºC | |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | | 1 | 50 | μA | $V_{DS}$ = 1200 V, $V_{GS}$ = 0 V | |
| $I_{GSS}$ | Gate-Source Leakage Current | | 10 | 250 | nA | $V_{GS}$ = 15 V, $V_{DS}$ = 0 V | |
| $R_{DS(on)}$ | Drain-Source On-State Resistance | | 39 | 53 | mΩ | $V_{GS}$ = 15 V, $I_D$ = 31.9 A | Fig. 4, 5, 6 |
| | | | 70 | | | $V_{GS}$ = 15 V, $I_D$ = 31.9 A, $T_J$ = 175ºC | |
| $g_{fs}$ | Transconductance | | 22 | | S | $V_{DS}$= 20 V, $I_{DS}$= 31.9 A | Fig. 7 |
| | | | 20 | | | $V_{DS}$= 20 V, $I_{DS}$= 31.9 A, $T_J$ = 175ºC | |
| $C_{iss}$ | Input Capacitance | | 2726 | | pF | $V_{GS}$ = 0 V, $V_{DS}$ = 0V to 1000 V<br>f = 100 kHz<br>$V_{AC}$ = 25 mV | Fig. 17, 18 |
| $C_{oss}$ | Output Capacitance | | 100 | | | | |
| $C_{rss}$ | Reverse Transfer Capacitance | | 6 | | | | |
| $E_{oss}$ | $C_{oss}$ Stored Energy | | 56 | | μJ | $V_{DS}$= 800 V, f = 100 kHz | Fig. 16 |
| $C_{o(er)}$ | Effective Output Capacitance (Energy Related) | | 127 | | pF | $V_{GS}$ = 0 V, $V_{DS}$ = 0 to 800V | Note: 3 |
| $C_{o(tr)}$ | Effective Output Capacitance (Time Related) | | 197 | | pF | | |
| $E_{ON}$ | Turn-On Switching Energy (Body Diode FWD) | | 432 | | μJ | $V_{DS}$= 800 V, $V_{GS}$= -4 V/15 V, $I_D$= 31.9 A,<br>$R_{G(ext)}$ = 2.5 Ω, L= 99 μH, $T_J$ = 175ºC<br>FWD = Internal Body Diode | Fig. 26, 28 |
| $E_{OFF}$ | Turn-Off Switching Energy (Body Diode FWD) | | 36 | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | | 13 | | ns | $V_{DD}$ = 800 V, $V_{GS}$ = -4 V/15 V, $I_D$ = 31.9 A,<br>$R_{G(ext)}$ = 2.5 Ω, L= 99 μH, $T_J$ = 175ºC<br>Timing relative to $V_{DS}$<br>Inductive load | Fig. 27, 28 |
| $t_r$ | Rise Time | | 16 | | | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | 22 | | | | |
| $t_f$ | Fall Time | | 7 | | | | |
| $R_{G(int)}$ | Internal Gate Resistance | | 1.9 | | Ω | f = 1 MHz, $V_{AC}$ = 25 mV | |
| $Q_{gs}$ | Gate to Source Charge | | 32 | | nC | $V_{DS}$ = 800 V, $V_{GS}$ = -4 V/15 V<br>$I_D$ = 31.9 A<br>Per IEC60747-8-4 pg 21 | Fig. 12 |
| $Q_{gd}$ | Gate to Drain Charge | | 22 | | | | |
| $Q_g$ | Total Gate Charge | | 91 | | | | |

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 800V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 800V

## Reverse Diode Characteristics ($T_C$ = 25˚C unless otherwise specified)

| Symbol | Parameter | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|
| $V_{SD}$ | Diode Forward Voltage | 4.8 | | V | $V_{GS}$ = -4 V, $I_{SD}$ = 16 A, $T_J$ = 25 °C | Fig. 8, 9, 10 |
| | | 4.3 | | V | $V_{GS}$ = -4 V, $I_{SD}$ = 16 A, $T_J$ = 175 °C | |
| $I_S$ | Continuous Diode Forward Current | | 39 | A | $V_{GS}$ = -4 V, $T_C$ = 25˚C | |
| $I_{S, pulse}$ | Diode pulse Current | | 127 | A | $V_{GS}$ = -4 V, pulse width $t_P$ limited by $T_{jmax}$ | |
| $t_{rr}$ | Reverse Recover time | 11 | | ns | $V_{GS}$ = -4 V, $I_{SD}$ = 31.9 A, $V_R$ = 800 V<br>$di_F/dt$ = 9511 A/μs, $T_J$ = 25 °C | |
| $Q_{rr}$ | Reverse Recovery Charge | 322 | | nC | | |
| $I_{rrm}$ | Peak Reverse Recovery Current | 53 | | A | | |
| $t_{rr}$ | Reverse Recover time | 18 | | ns | $V_{GS}$ = -4 V, $I_{SD}$ = 31.9 A, $V_R$ = 800 V<br>$di_F/dt$ = 2168 A/μs, $T_J$ = 25 °C | |
| $Q_{rr}$ | Reverse Recovery Charge | 161 | | nC | | |
| $I_{rrm}$ | Peak Reverse Recovery Current | 16 | | A | | |

## Thermal Characteristics

| Symbol | Parameter | Typ. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance from Junction to Case | 0.39 | 0.51 | °C/W | | Fig. 21 |

## Typical Performance

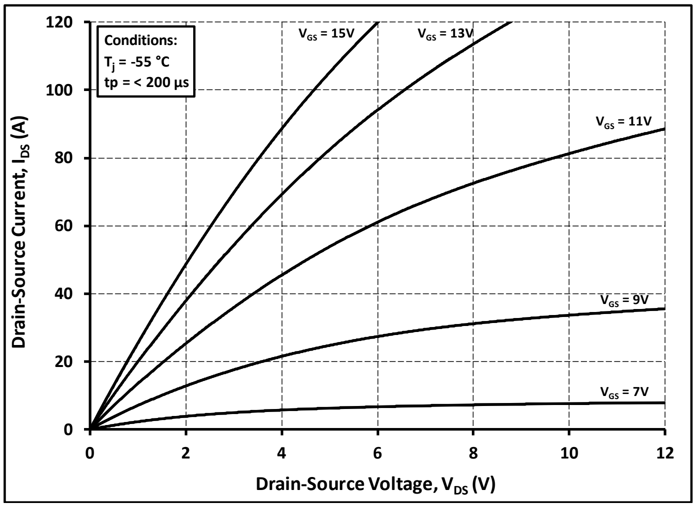



Figure 1. Output Characteristics $T_J$ = -55 °C

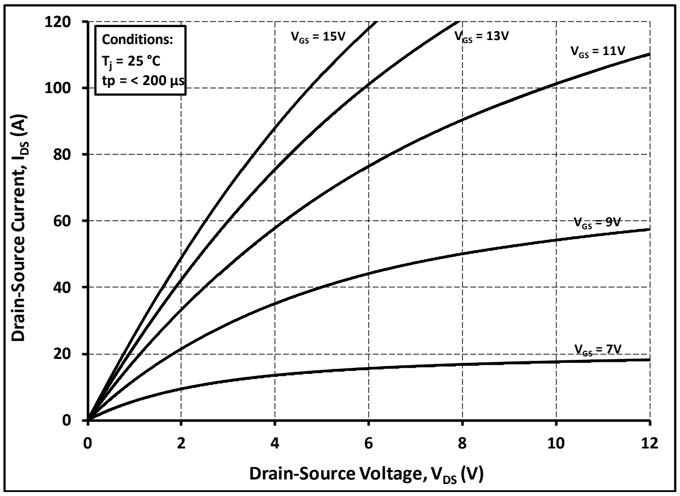



Figure 2. Output Characteristics $T_J$ = 25 °C

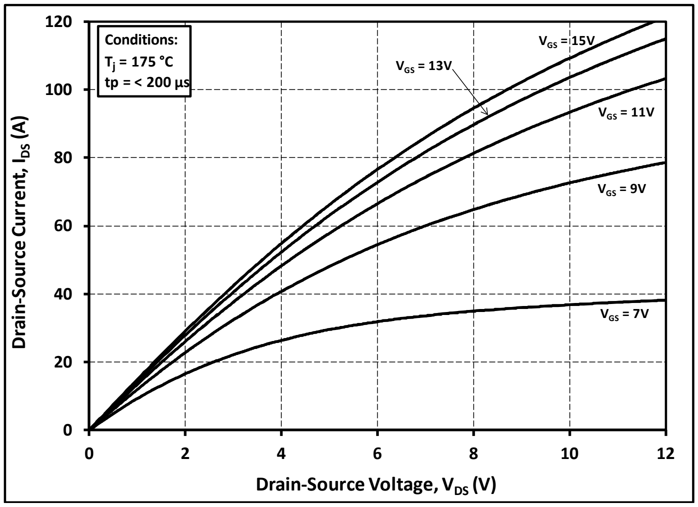



Figure 3. Output Characteristics $T_J$ = 175 °C

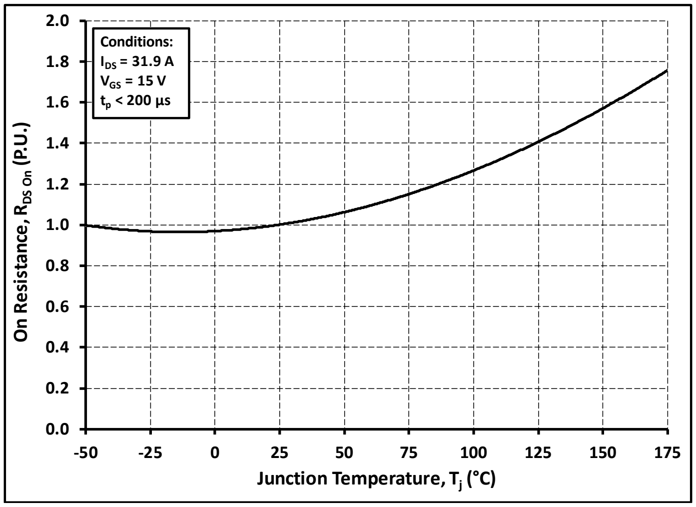



Figure 4. Normalized On-Resistance vs. Temperature

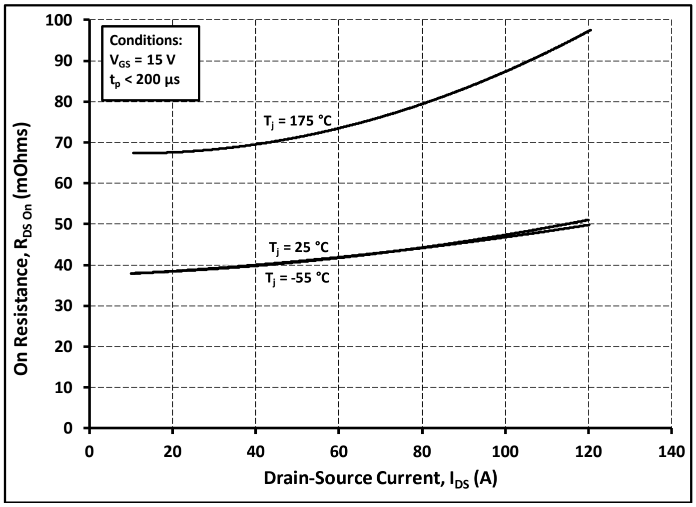



Figure 5. On-Resistance vs. Drain Current For Various Temperatures

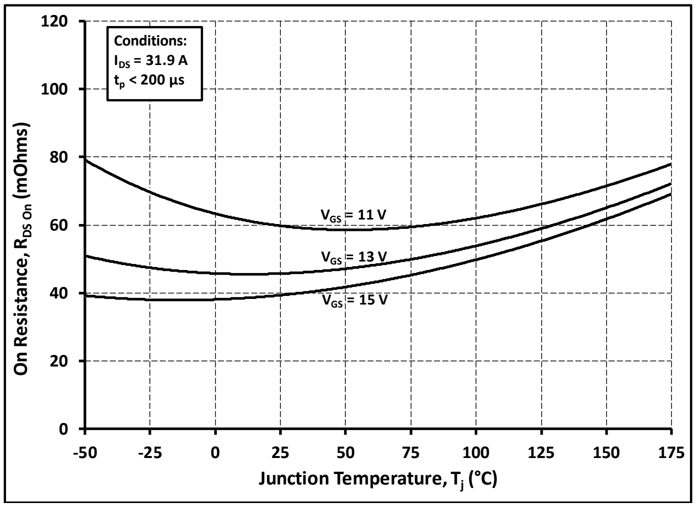



Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

## Typical Performance

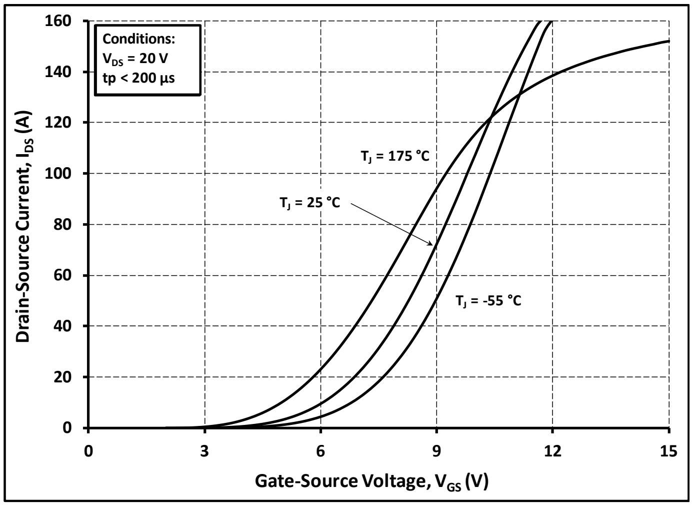



Figure 7. Transfer Characteristic for Various Junction Temperatures

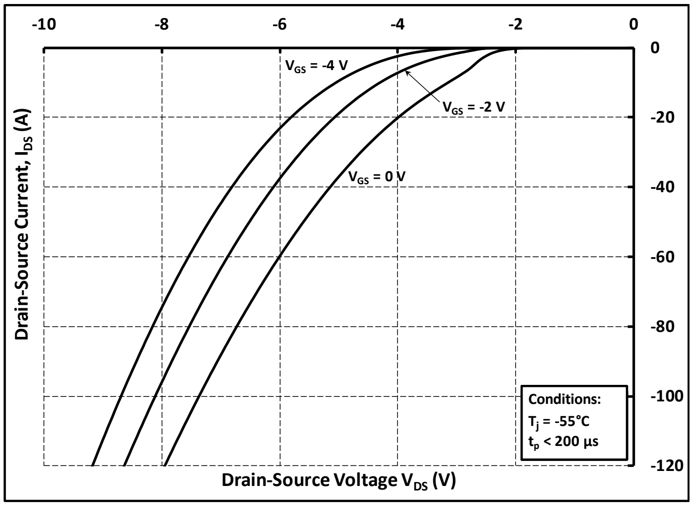



Figure 8. Body Diode Characteristic at -55 °C

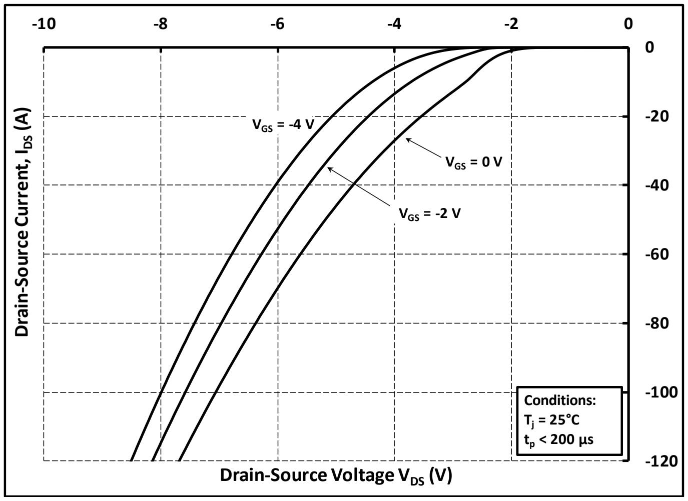



Figure 9. Body Diode Characteristic at 25 °C

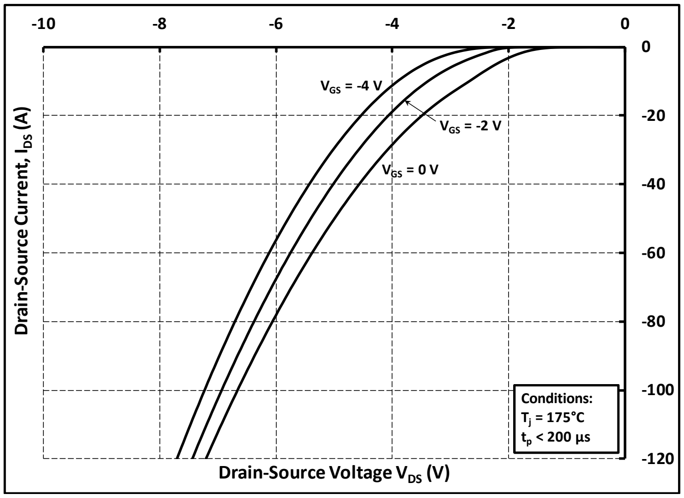



Figure 10. Body Diode Characteristic at 175 °C

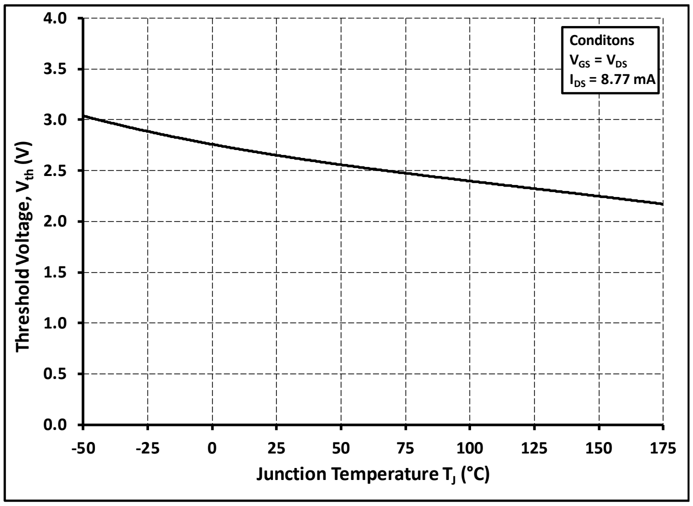



Figure 11. Threshold Voltage vs. Temperature

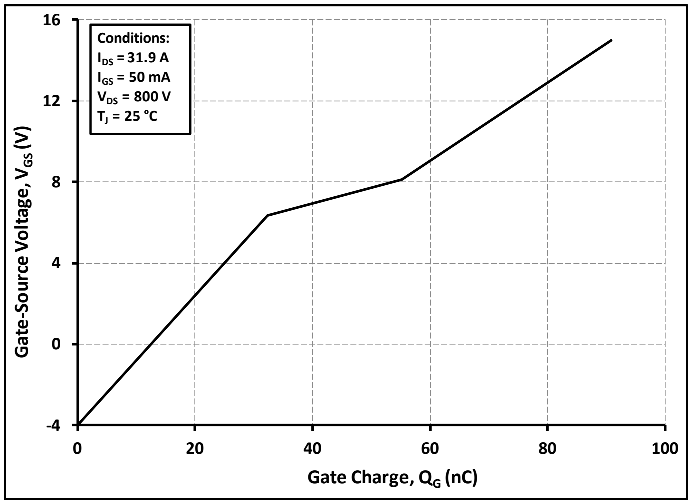



Figure 12. Gate Charge Characteristics

## Typical Performance

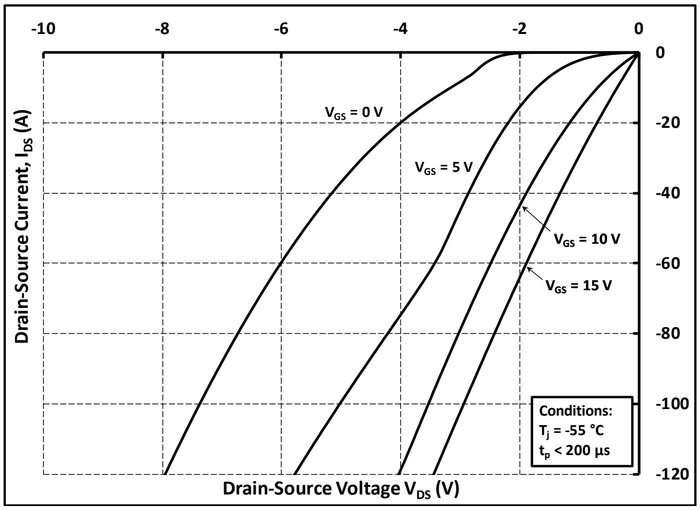



Figure 13. 3rd Quadrant Characteristic at -55 °C

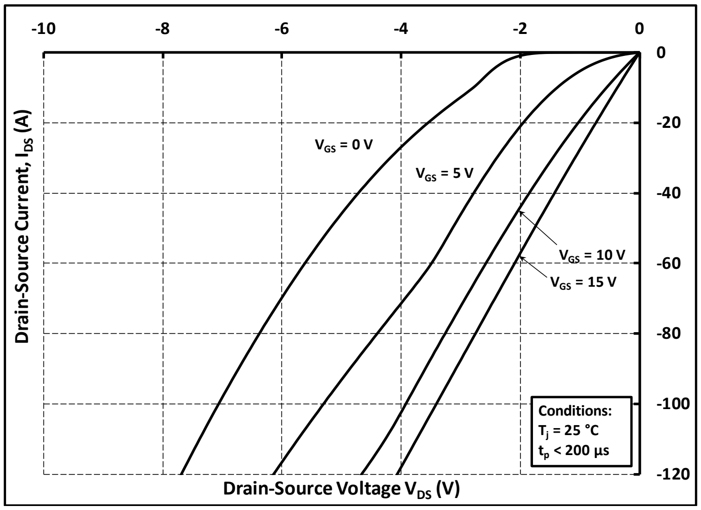



Figure 14. 3rd Quadrant Characteristic at 25 °C

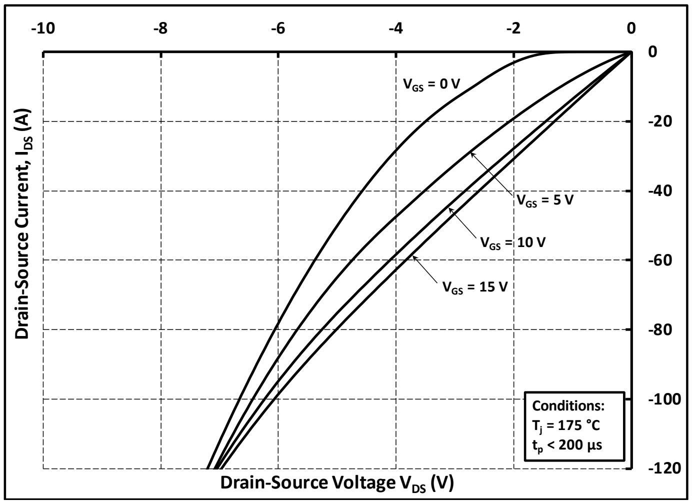



Figure 15. 3rd Quadrant Characteristic at 175 °C

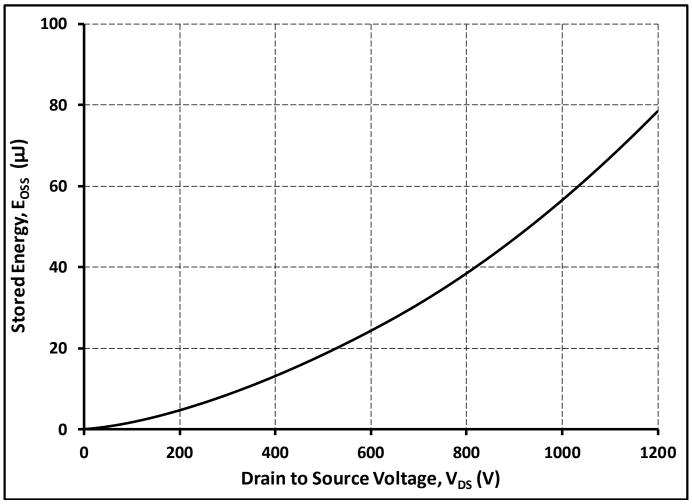



Figure 16. Output Capacitor Stored Energy

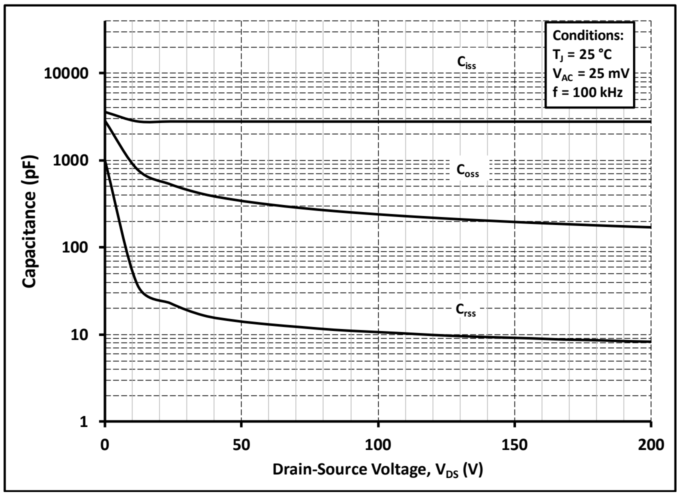



Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

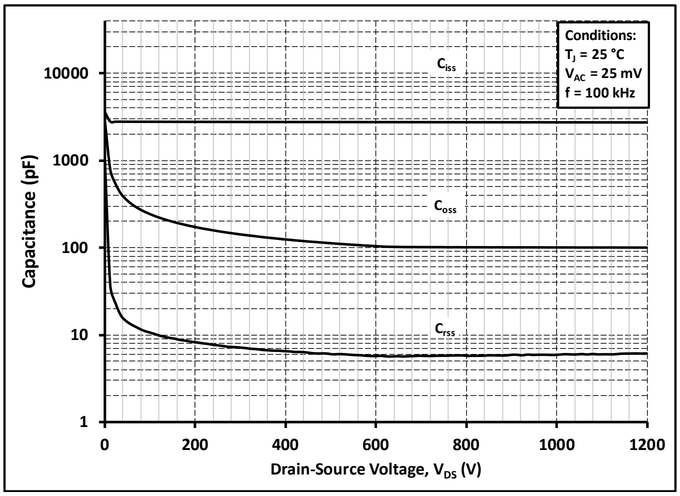



Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)

## Typical Performance

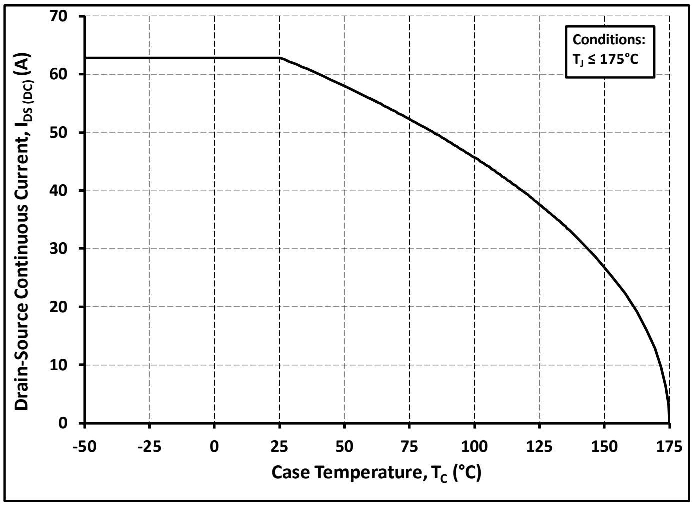



Figure 19. Continuous Drain Current Derating vs. Case Temperature

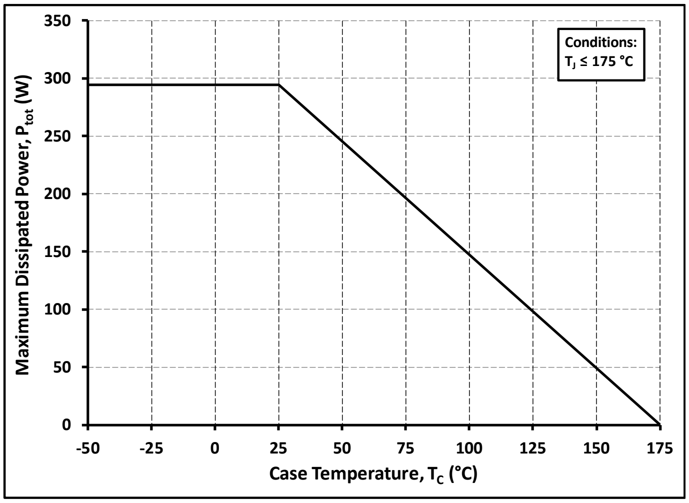



Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

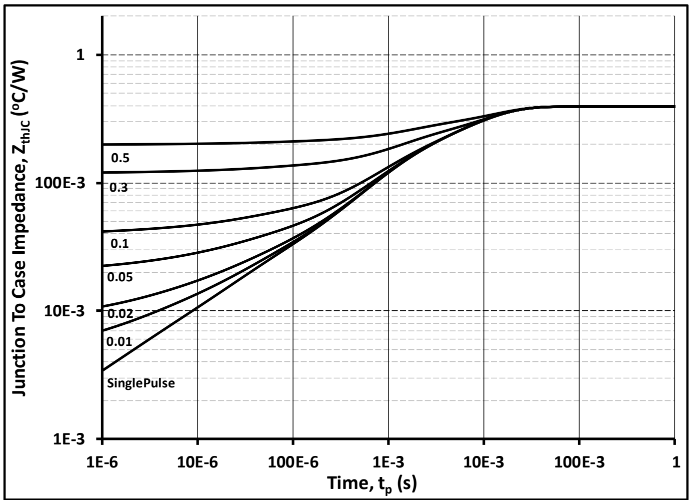



Figure 21. Transient Thermal Impedance (Junction - Case)

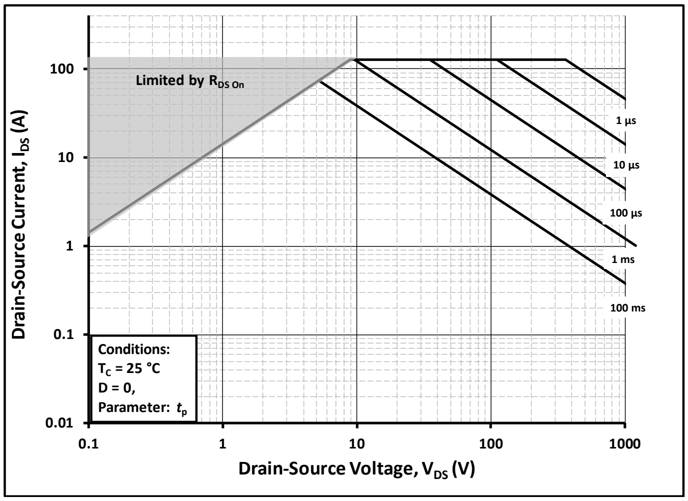



Figure 22. Safe Operating Area

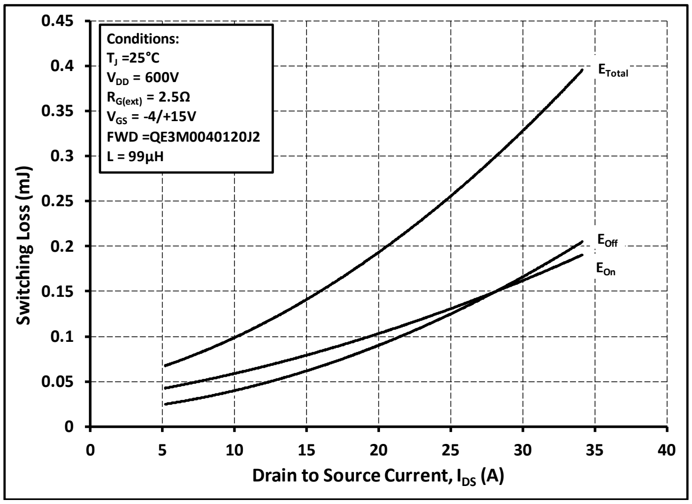



Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD}$ = 600V)

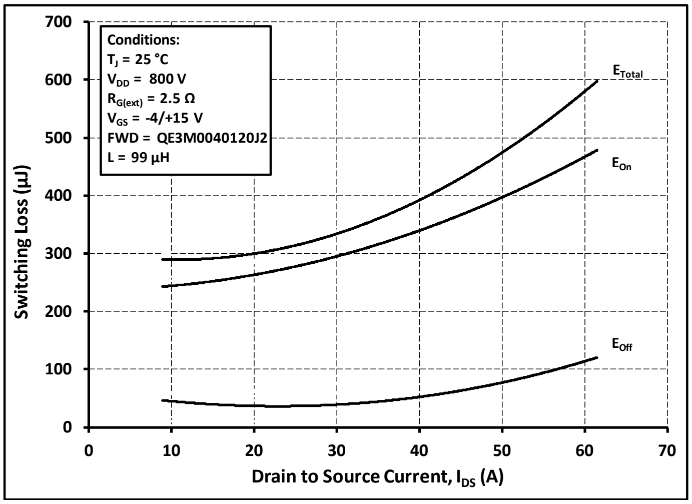



Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD}$ = 800V)

## Typical Performance

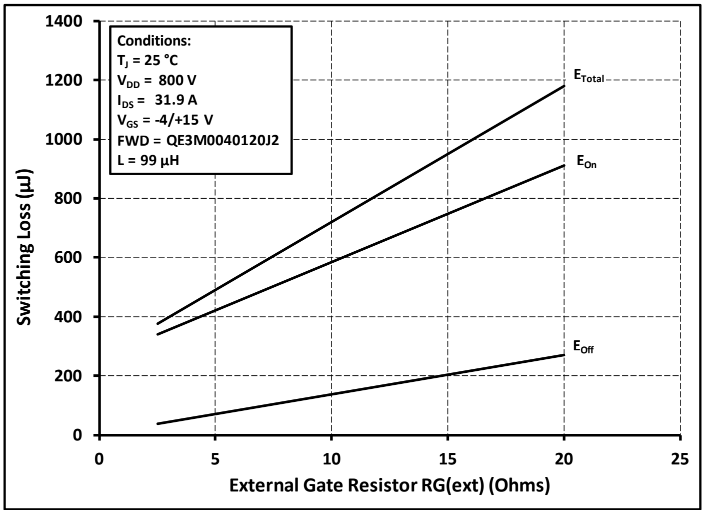



Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

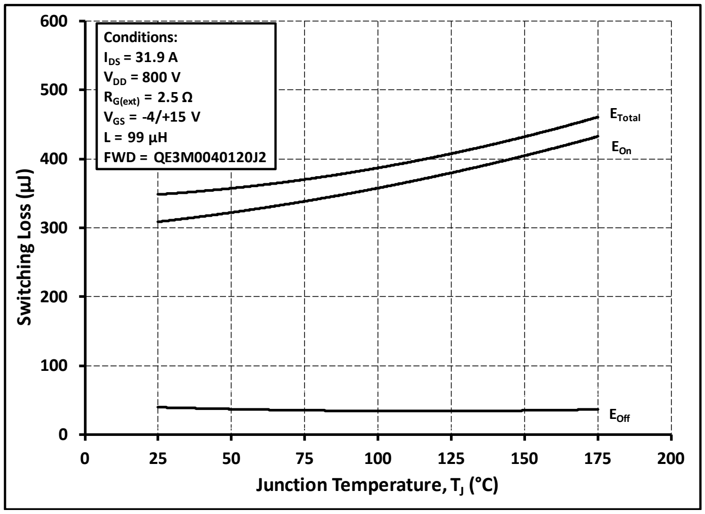



Figure 26. Clamped Inductive Switching Energy vs. Temperature

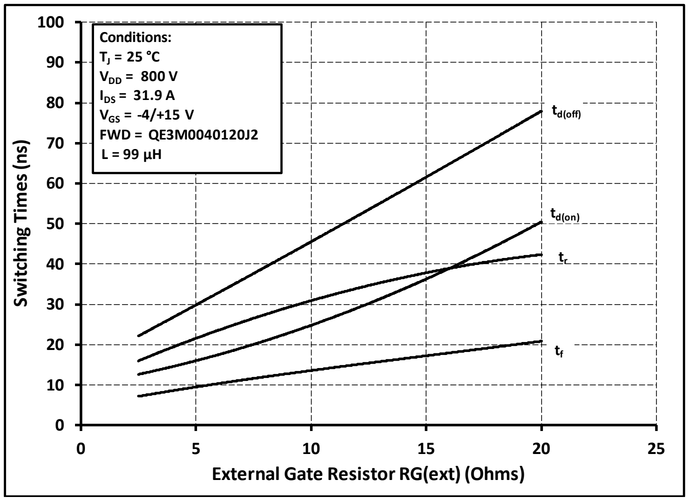



Figure 27. Switching Times vs. $R_{G(ext)}$

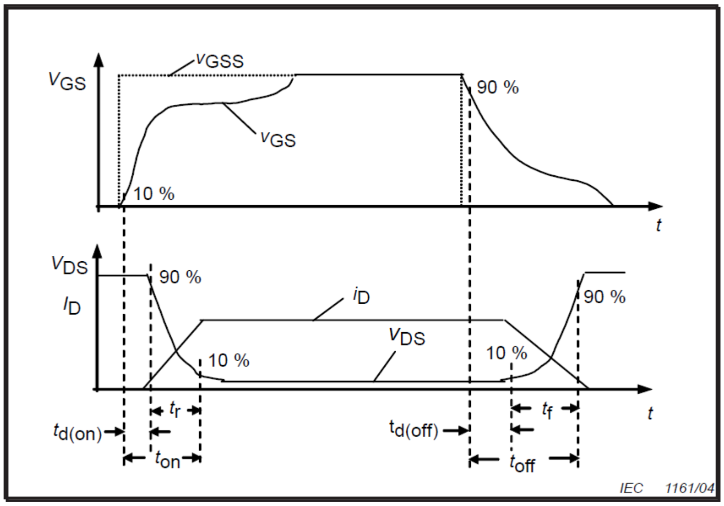



Figure 28. Switching Times Definition

## Test Circuit Schematic

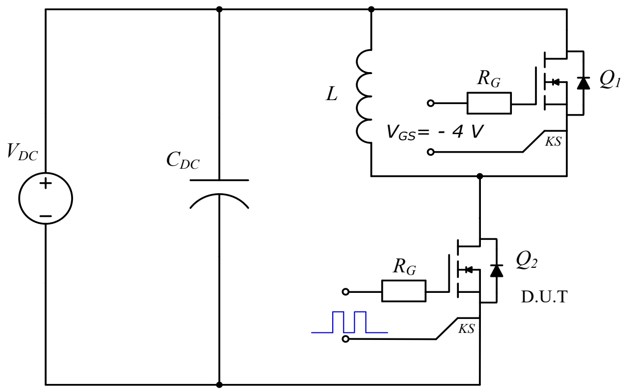
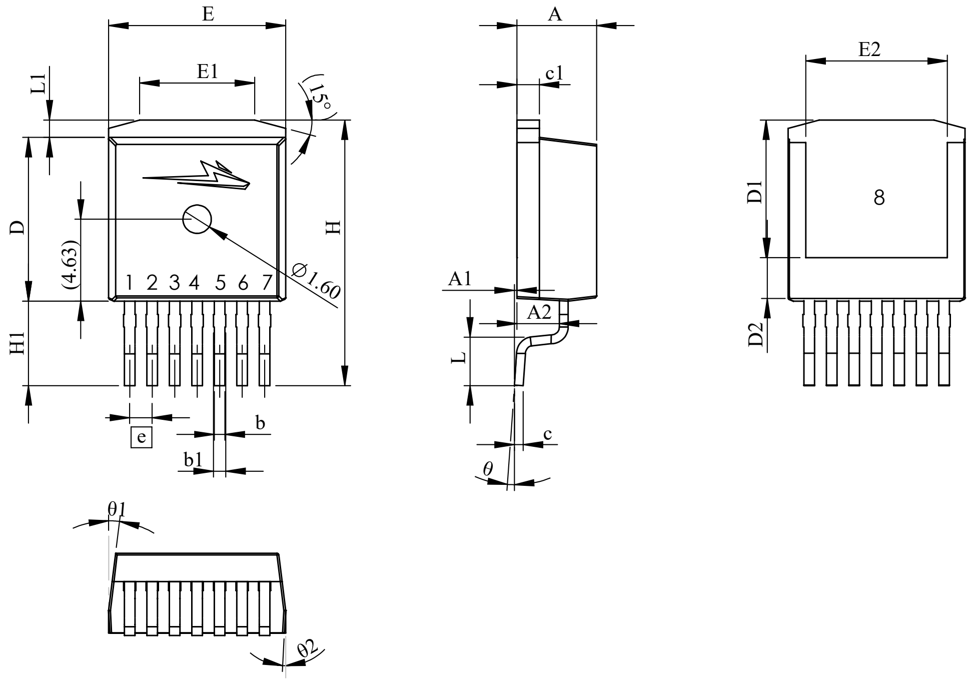



Figure 29. Clamped Inductive Switching Waveform Test Circuit

## Package Dimensions



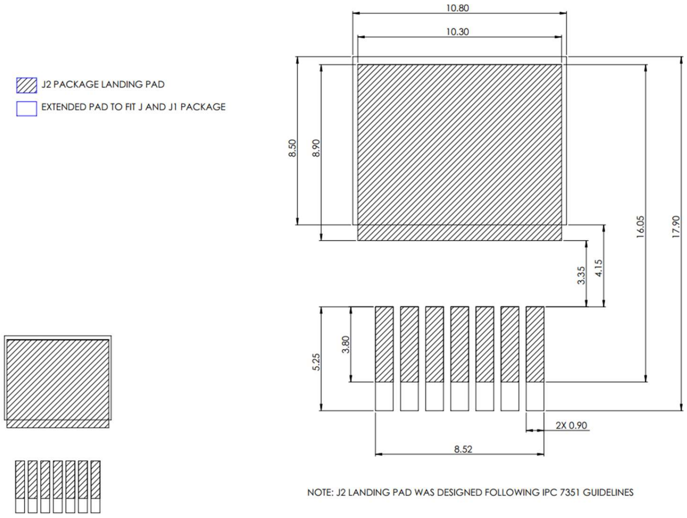

| SYMBOL | MIN (mm) | MAX (mm) |
|---|---|---|
| A | 4.30 | 4.70 |
| A1 | 0.00 | 0.25 |
| A2 | 2.20 | 2.60 |
| b | 0.52 | 0.72 |
| b1 | 0.60 | 0.80 |
| c | 0.42 | 0.62 |
| c1 | 1.07 | 1.47 |
| D | 9.05 | 9.45 |
| D1 | 7.58 | 7.98 |
| D2 | 2.05 | 2.45 |
| E | 9.80 | 10.20 |
| E1 | 6.30 | 6.97 |
| E2 | 7.80 | 8.20 |
| e | 1.27 BSC | |
| H | 14.87 | 15.27 |
| H1 | 4.55 | 4.95 |
| L | 2.48 | 2.88 |
| L1 | 0.87 | 1.27 |
| θ | 0° | 8° |
| θ1 | 4° | 10° |
| θ2 | 0° | 6° |

| | |
|---|---|
| 1 | GATE |
| 2 | KELVIN |
| 3 | SOURCE |
| 4 | SOURCE |
| 5 | SOURCE |
| 6 | SOURCE |
| 7 | SOURCE |
| 8 | DRAIN |

NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

## Recommended Solder Pad Layout

All dimensions in mm



## Revision history

| Document Version | Date of release | Descriptiion of changes |
|---|---|---|
| 1.0 | December 2023 | Initial release |

## Notes & Disclaimer

This document and the information contained herein are subject to change without notice. Any such change shall be evidenced by the publication of an updated version of this document by Wolfspeed. No communication from any employee or agent of Wolfspeed or any third party shall effect an amendment or modification of this document. No responsibility is assumed by Wolfspeed for any infringement of patents or other rights of third parties which may result from use of the information contained herein. No license is granted by implication or otherwise under any patent or patent rights of Wolfspeed.

Notwithstanding any application-specific information, guidance, assistance, or support that Wolfspeed may provide, the buyer of this product is solely responsible for determining the suitability of this product for the buyer's purposes, including without limitation for use in the applications identified in the next bullet point, and for the compliance of the buyers' products, including those that incorporate this product, with all applicable legal, regulatory, and safety-related requirements.

This product has not been designed or tested for use in, and is not intended for use in, applications in which failure of the product would reasonably be expected to cause death, personal injury, or property damage, including but not limited to equipment implanted into the human body, life-support machines, cardiac defibrillators, and similar emergency medical equipment, aircraft navigation, communication, and control systems, aircraft power and propulsion systems, air traffic control systems, and equipment used in the planning, construction, maintenance, or operation of nuclear facilities.

**RoHS Compliance**

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Documentation sections of www.wolfspeed.com.

**REACh Compliance**

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

**Contact info:**

4600 Silicon Drive
Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfspeed.com/power




© 2023 Wolfspeed, Inc. All rights reserved. Wolfspeed® and the Wolfstreak logo are registered trademarks and the Wolfspeed logo is a trademark of Wolfspeed, Inc.
The information in this document is subject to change without notice.