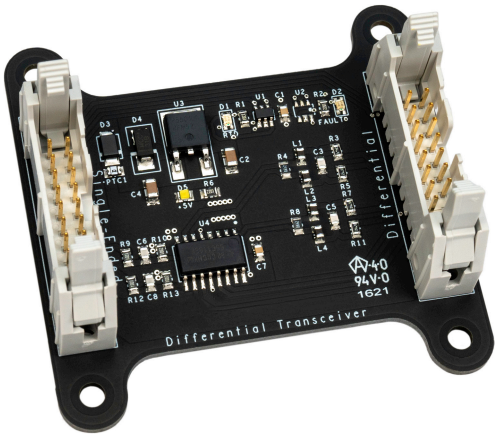
CGD12HB00D

2-Channel Differential Transceiver Companion Tool

Technical Features

- Optimized for use with Wolfspeed's High-Performance Gate Drivers
- Single-Ended Inputs for Interfacing with 3.3 V or 5 V Microcontrollers
- Differential Outputs for Increased Noise Immunity
- High-Frequency, Ultra-Fast Switching Operation
- Fault Indicator LEDs
- Reverse Polarity & Overvoltage Protections
- Enables Retrofitting Single-Ended Systems for Differential Signals



Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DC}	-0.5 to 18	V
Logic Level Inputs	V_I	-0.5 to 5.5	
Ambient Operating Temperature	T_{op}	-40 to +85	°C
Storage Temperature	T_{stg}	-40 to +125	

Gate Driver Electrical Characterization

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V_{DC}	9	12	18	V	
High Level Logic Input Voltage	V_{IH}	2.0		5.5		Single-Ended Inputs
Low Level Logic Input Voltage	V_{IL}	0		0.8		
Differential Input Common Mode Range	V_{IDCM}	-7		+12		Differential Inputs
Differential Input Threshold Voltage	V_{IDTH}	-200	-125	-50	mV	$V_{ID} = V_{Pos\text{-}Line} - V_{Neg\text{-}Line}$
Differential Voltage Hysteresis	V_{HYST}	15	70			
Differential Output Magnitude	V_{OD}	2	3.1		V	$R_L = 100\ \Omega$
Differential Output High Level	V_{ODH}	2.2	3.4			$I_{OD} = -20$ mA
Differential Output Low Level	V_{ODL}		0.2	0.4		$I_{OD} = 20$ mA
Propagation Delay	$t_{PHL/PLH}$		15		ns	$C_L = 30$ pF
PWM Inputs First-Order Low-Pass Filter Cutoff Frequency	f_C		1		MHz	

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Input Connector Information

Pin Number	Parameter	Description
1	V_{DC}	Power supply input pin (+12 V Nominal Input)
2	Common	Common
3	HS-PWM	High Side PWM Signal. 3.3 V or 5 V Logic Compatible. Active High.
4	Common	Common
5	LS-PWM	Low Side PWM Signal. 3.3 V or 5 V Logic Compatible. Active High.
6	Common	Common
7	$\overline{\text{Fault}}$	5 V Fault Condition. ***Caution for 3.3 V Systems: This Output is 5 V. Active Low.***
8	Common	Common
9	RTD	5 V Temperature Dependent Resistor Output. ***Caution for 3.3 V Systems: This Output is 5 V. Duty Cycle Modulated.***
10	Common	Common
11	$\overline{\text{PS-Dis}}$	Pull Down to Disable Power Supply. Pull Up, or Leave Floating to Enable. Gate-Source will be Connected with 10 kΩ when Disabled. *Straight Pass-Through to Gate Driver.*
12	Common	Common
13	PWM-EN	Pull Down to Disable PWM Input Logic. Pull Up or Leave Floating to Enable. Gate-Source will be Held Low Through Gate Resistor if Power Supplies are Enabled. *Straight Pass-Through to Gate Driver.*
14	Common	Common
15	Multi-Function	See Gate Drive Datasheet. *Straight Pass-Through to Gate Driver.*
16	Common	Common

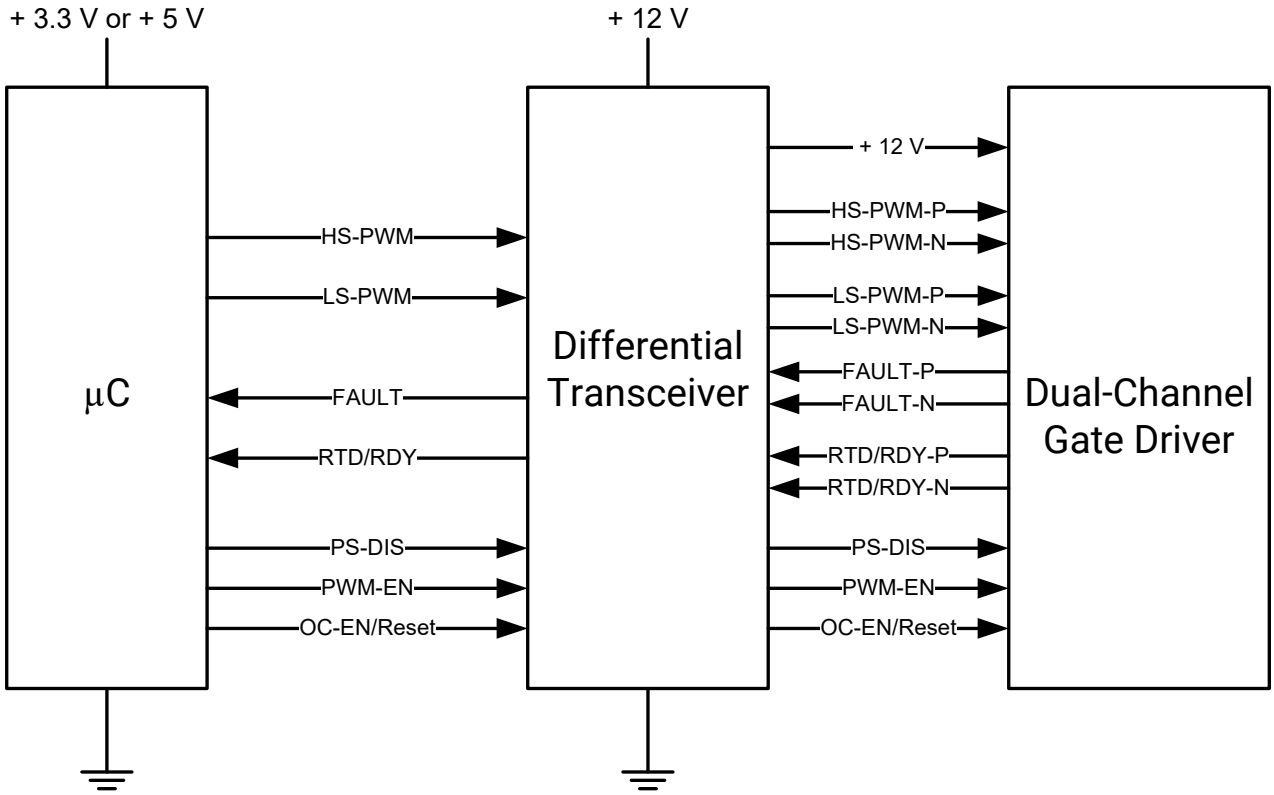
Notes:
[1] Output resistance of gate driver IC.
[2] Additional output resistance is added with SMD resistors. Separate resistors for turn-on and turn-off allowing tunable dynamic performance.
[3] Soft-Shutdown network will safely turn off the gate in the event an over-current is detected.

Output Connector Information

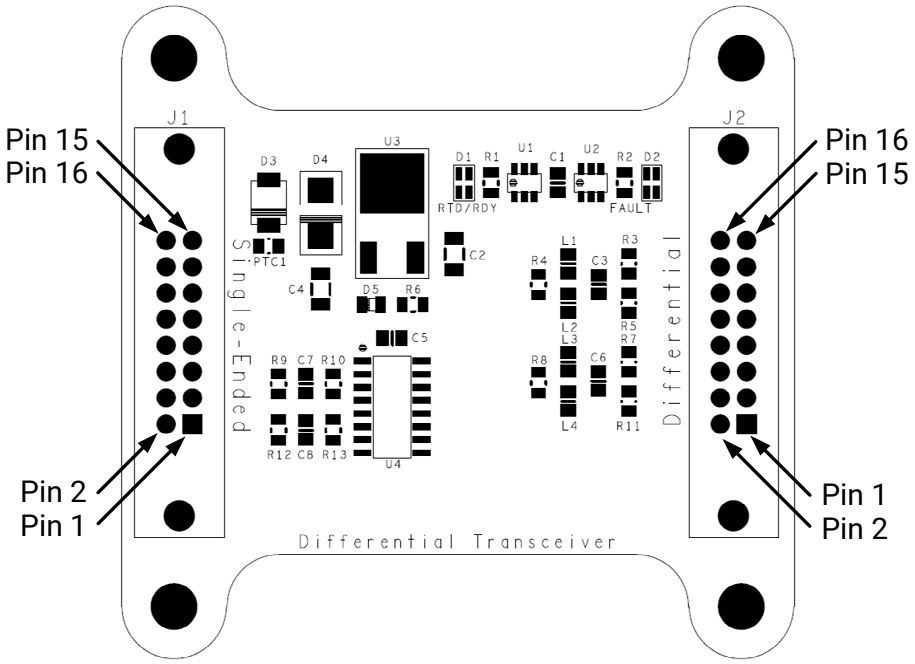
Pin Number	Parameter	Description
1	V_{DC}	Power supply input pin (+12 V Nominal Input)
2	Common	Common
3	HS-P (*)	Positive line of 5 V differential high-side PWM signal pair.
4	HS-N (*)	Negative line of 5 V differential high-side PWM signal pair.
5	LS-P (*)	Positive line of 5 V differential low-side PWM signal pair.
6	LS-N (*)	Negative line of 5 V differential low-side PWM signal pair.
7	$\overline{\text{FAULT-P}}$ (*)	Positive line of 5 V differential fault condition signal pair Drive strength 20 mA. A low state on FAULT indicates when a desaturation fault has occurred The presence of a fault precludes the gate drive output from going high
8	$\overline{\text{FAULT-N}}$ (*)	Negative line of 5 V differential fault condition signal pair. Drive strength 20 mA
9	RTD-P (*)	Positive Line of Temperature Dependent Resistor Output Signal Pair.
10	RTD-N (*)	Negative Line of Temperature Dependent Resistor Output Signal Pair.
11	$\overline{\text{PS-Dis}}$	Pull down to disable power supply. Pull up (+5 V) or leave floating to enable Gate and source are connected with 10 kΩ when disabled *Straight Pass-Through to Gate Driver.*
12	Common	Common
13	PWM-EN	Pull down to disable PWM input logic. Pull up (+5 V) or leave floating to enable. Gate driver output will be held low through turn-off gate resistor if power supplies are enabled *Straight Pass-Through to Gate Driver.*
14	Common	Common
15	Multi-Function	See Gate Driver Datasheet. *Straight Pass-Through to Gate Driver.*
16	Common	Common

Note:
(*) Inputs 3 – 10 are differential pairs.

Block Diagram



Board Interface



Connector	Name	Description
J1	Single-Ended	Signal Input (from microcontroller) ***It is Crucial to Keep the Single-Ended Connection as Short as Possible.***
J2	Differential	Signal Output (to Wolfspeed Dual-Channel Gate Driver)

Input Connector Information

- 71918-116LF - 16 Positions Header Connector 0.100” (2.54 mm) Through Hole Gold

Suggested Mating Parts

- 71600-016LF - 16 Position Rectangular Receptical Connector IDC Gold 28-30 AWG

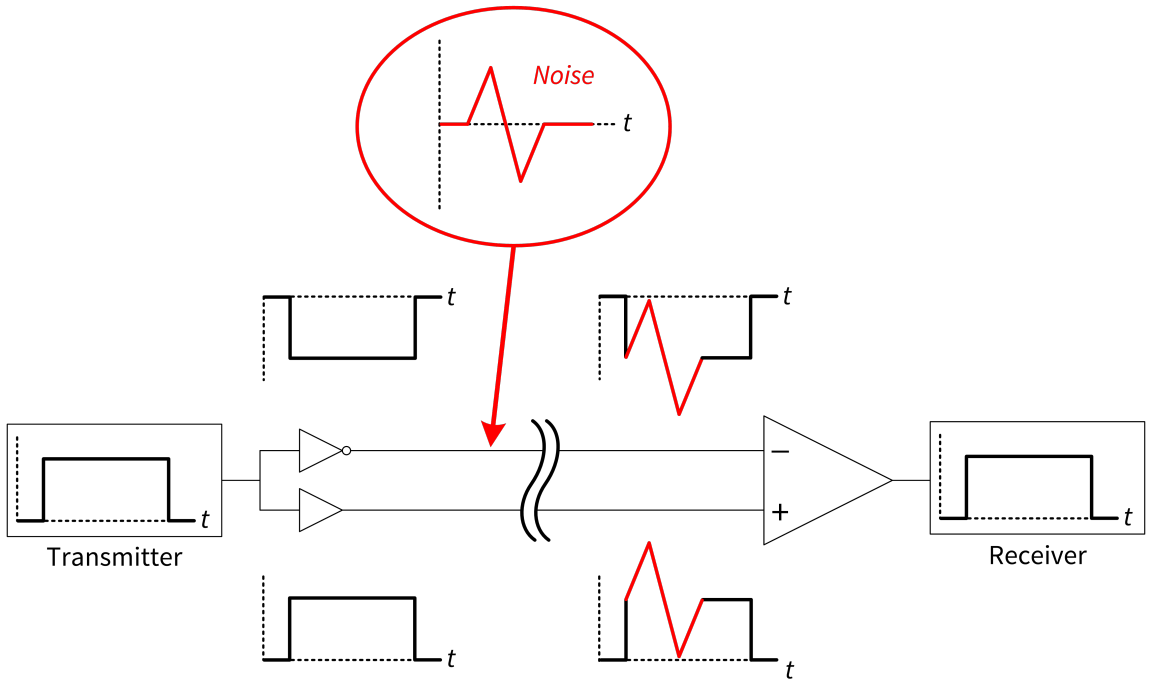
Output Connector Information

- HF365/16SF - Flat Ribbon Cable Gray 16 Conductors 0.050” (1.27 mm) Flat Cable 10.0’ (3.05 m)
- 1700/16 100SF - Flat Ribbon Cable Multiple 16 (8 Pair Twisted) Conductors 0.050” (1.27 mm) Flat Twisted Pair 10.0’ (3.05 m)

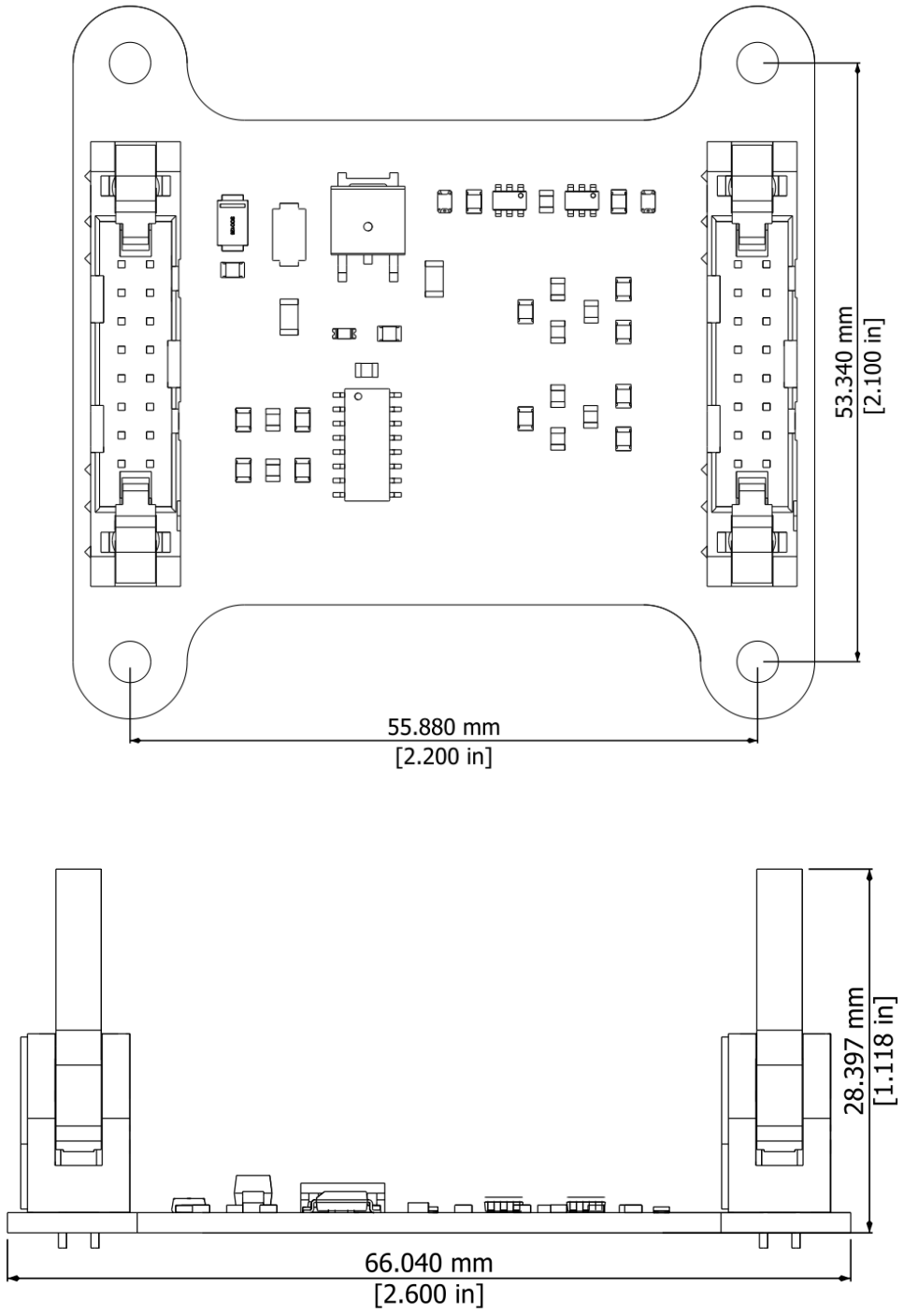
Differential Signal Explanation

Signal integrity is of the upmost importance when controlling power devices with a gate driver. A gate driver that is susceptible to the powerful interference generated by power devices can induce a shoot-through condition in the module. The extremely fast turn-on and turn-off times during the switching events in a SiC power system create immense EMI that can easily couple onto the gate control signals. For this reason, differential signaling was chosen to replace standard, single-ended connections between the gate driver and control board.

Differential signaling significantly reduces the impact of radiated noise from the switching events of a power module. A single-ended signal can easily be converted to a differential signal by transmitting both the original signal and its complement in two closely coupled wires. At the receiver, the two signals are compared in order to reconstruct the original signal. The figure below illustrates this principle with an example of induced noise forced onto the cable somewhere between the transmitter and receiver. The noise affects both the original signal and the complement by the same magnitude assuming that the cables are consistently coupled. Thus, when the receiver compares the two signals, the difference is unaffected by the noise induced on the line and the intended original signal is created.



Dimensions



Important Notes

This Wolfspeed-designed gate driver hardware for Wolfspeed components is meant to be used as an evaluation tool in a lab setting and to be handled and operated by highly qualified technicians or engineers. The hardware is not designed to meet any particular safety standards and the tool is not a production qualified assembly.

Each part that is used in this gate driver and is manufactured by an entity other than Wolfspeed or one of Wolfspeed's affiliates is provided "as is" without warranty of any kind, including but not limited to any warranty of non-infringement, merchantability, or fitness for a particular purpose, whether express or implied. There is no representation that the operation of each such part will be uninterrupted or error free.

This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.

The SiC MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.

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