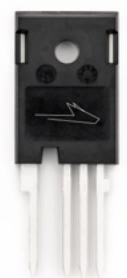
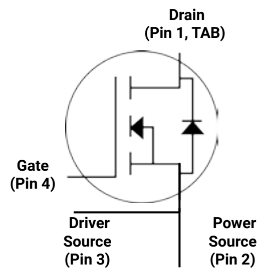
C3M0060065K

Silicon Carbide Power MOSFET C3M[TM] MOSFET Technology
N-Channel Enhancement Mode

Features

- 3^{rd} Generation SiC MOSFET technology
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant





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Ordering Part Number	Package	Marking
C3M0060065K	TO-247-4	C3M0060065K

Applications

- EV charging
- Server power supplies
- Solar PV inverters
- UPS
- DC/DC converters

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Easy to parallel and simple to drive
- Enable new hard switching PFC topologies (Totem-Pole)

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			650	V	$T_C = 25°C$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS\ op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			37	A	$V_{GS} = 15$ V, $T_C = 25$ °C, $T_J \leq 175$ °C	Fig. 19 Note 2
				27		$V_{GS} = 15$ V, $T_C = 100$ °C, $T_J \leq 175$ °C	
Pulsed Drain Current	I_{DM}			99		t_{Pmax} limited by T_{jmax} $V_{GS} = 15V$, $T_C = 25$ °C	Fig. 22
Power Dissipation	P_D			150	W	$T_C = 25$ °C, $T_J = 175$ °C	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	650	—	—	V	V_{GS} = 0 V, I_D = 100 μA	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.3	3.6		V_{DS} = V_{GS}, I_D = 5 mA	Fig. 11
		—	1.9	—		V_{DS} = V_{GS}, I_D = 5 mA, T_J = 175°C	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	50	μA	V_{DS} = 650 V, V_{GS} = 0 V	
Gate-Source Leakage Current	I_{GSS}	—	10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance	$R_{DS(on)}$	42	60	79	mΩ	V_{GS} = 15 V, I_D = 13.2 A	Fig. 4, 5, 6
		—	80	—		V_{GS} = 15 V, I_D = 13.2 A, T_J = 175°C	
Transconductance	g_{fs}	—	10	—	S	V_{DS} = 20 V, I_{DS} = 13.2 A	Fig. 7
			9			V_{DS} = 20 V, I_{DS} = 13.2 A, T_J = 175°C	
Input Capacitance	C_{iss}	—	1020	—	pF	V_{GS} = 0 V, V_{DS} = 600 V ƒ = 1 Mhz V_{AC} = 25 mV	Fig. 17, 18
Output Capacitance	C_{oss}	—	80	—			
Reverse Transfer Capacitance	C_{rss}	—	9	—			
Effective Output Capacitance (Energy Related)	$C_{o(er)}$	—	95	—		V_{GS} = 0 V, V_{DS} = 0 V to 400 V	Note 3
Effective Output Capacitance (Time Related)	$C_{o(tr)}$	—	132	—			
C_{oss} Stored Energy	E_{oss}	—	15	—	μJ	V_{DS} = 600 V, ƒ = 1 Mhz	Fig. 16
Turn-On Switching Energy (Body Diode)	E_{on}	—	70	—		V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 13.2 A, $R_{G(ext)}$ = 2.5 Ω, L= 135 μH, T_J = 175°C FWD = Internal Body Diode of MOSFET	Fig. 25
Turn Off Switching Energy (Body Diode)	E_{off}	—	5	—			
Turn-On Switching Energy (External Sic Diode)	E_{on}	—	67	—		V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 13.2 A, $R_{G(ext)}$ = 2.5 Ω, L= 135 μH, T_J = 175°C FWD = External SiC DIODE	
Turn Off Switching Energy (External Sic Diode)	E_{off}	—	6	—			
Turn-On Delay Time	$t_{d(on)}$	—	8	—	ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 13.2 A, $R_{G(ext)}$ = 2.5 Ω, L= 135 μH Timing relative to V_{DS} Inductive load	Fig. 26
Rise Time	t_r	—	11	—			
Turn-Off Delay Time	$t_{d(off)}$	—	17	—			
Fall Time	t_f	—	5	—			
Internal Gate Resistance	$R_{G(int)}$	—	3	—	Ω	ƒ = 1 MHz, V_{AC} = 25 mV	
Gate to Source Charge	Q_{gs}	—	13	—	nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 13.2 A Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—	17	—			
Total Gate Charge	Q_g	—	46	—			

Note:
[3] $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Reverse Diode Characteristics (T_C = 25°C unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Notes
Diode Forward Voltage, T_J = 25°C	V_{SD}	5.1	—	V	V_{GS} = -4 V, I_{SD} = 6.6 A, T_J=25C	Fig. 8, 9, 10
Diode Forward Voltage, T_J = 175°C		4.8	—		V_{GS} = -4 V, I_{SD} = 6.6 A, T_J=175C	
Continuous Diode Forward Current	I_S	—	23	A	V_{GS} = -4 V, T_J = 25°C	
Diode pulse Current	$I_{S, pulse}$	—	99		V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
Reverse Recovery Time	t_{rr}	11	—	ns	V_{GS} = -4 V, I_{SD} = 13.2 A, V_R = 400 V di_F/dt = 4500 A/µs, T_J = 175°C	
Reverse Recovery Charge	Q_{rr}	151	—	nC		
Peak Reverse Recovery Current	I_{RRM}	27	—	A		
Reverse Recovery Time	t_{rr}	16	—	ns	V_{GS} = -4 V, I_{SD} = 13.2 A, V_R = 400 V di_F/dt = 2400 A/µs, T_J = 175°C	
Reverse Recovery Charge	Q_{rr}	110	—	nC		
Peak Reverse Recovery Current	I_{RRM}	12	—	A		

Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.99	°C/W	Fig. 21
Thermal Resistance From Junction to Ambient	$R_{\theta JA}$	40		

Typical Performance

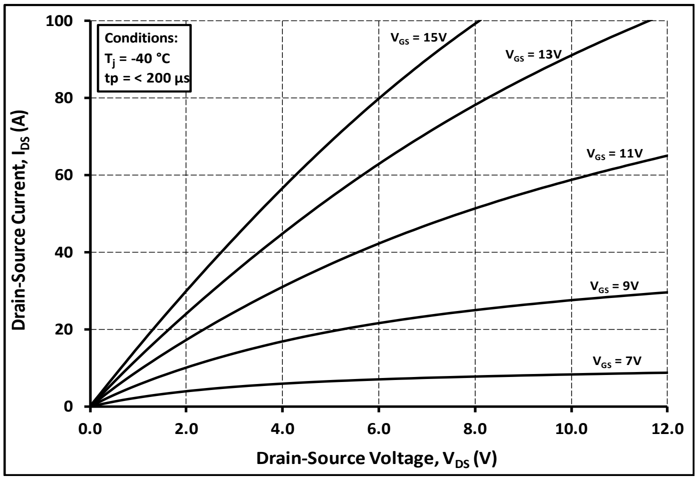


Figure 1. Output Characteristics T_J = -40°C

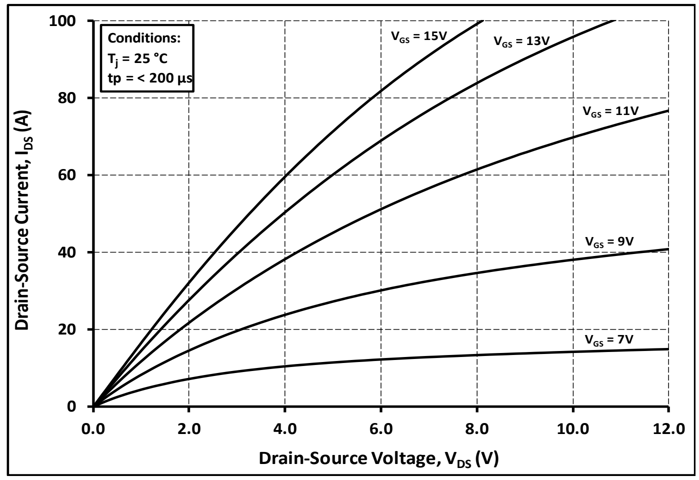


Figure 2. Output Characteristics T_J = 25°C

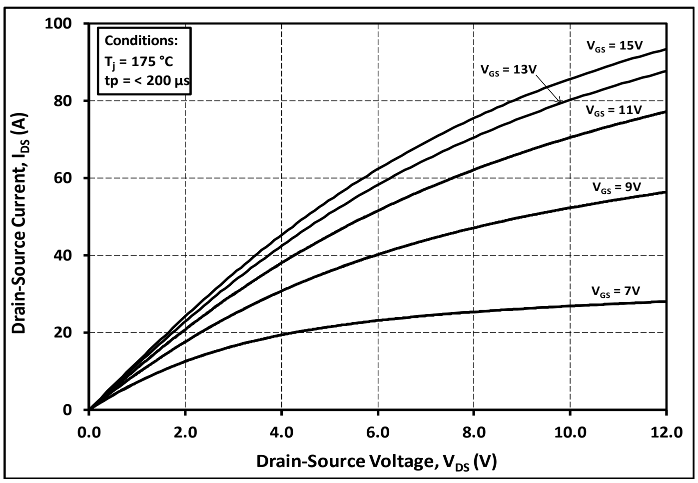


Figure 3. Output Characteristics T_J = 175°C

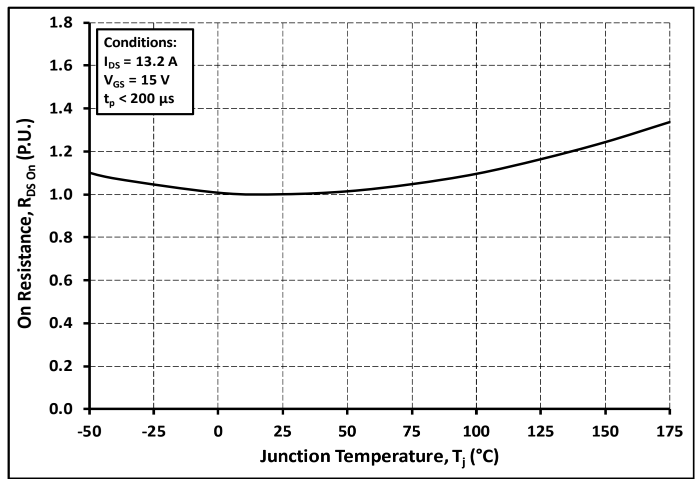


Figure 4. Normalized On-Resistance vs. Temperature

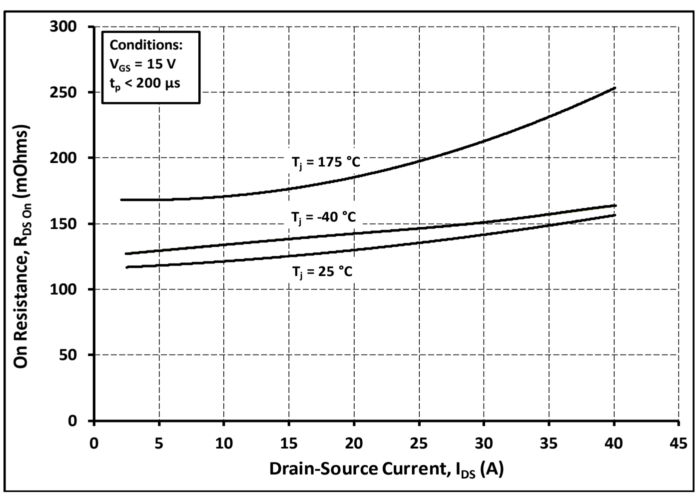


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

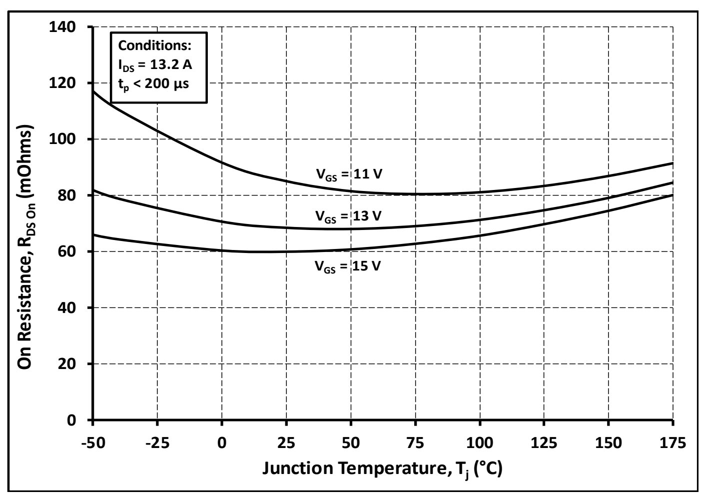


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

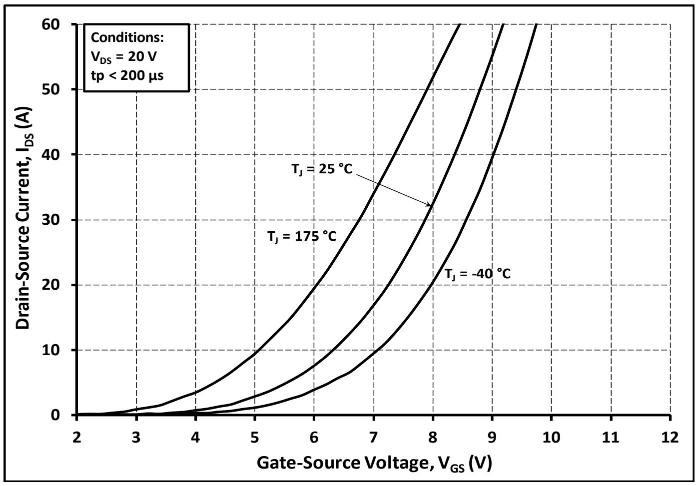


Figure 7. Transfer Characteristic for Various Junction Temperatures

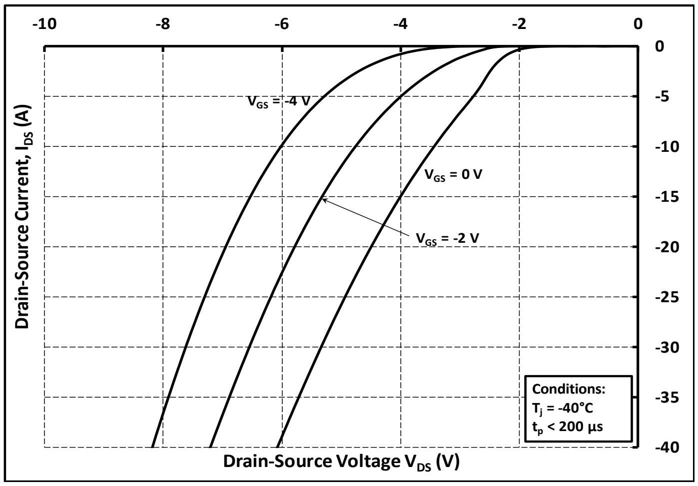


Figure 8. Body Diode Characteristic at -40°C

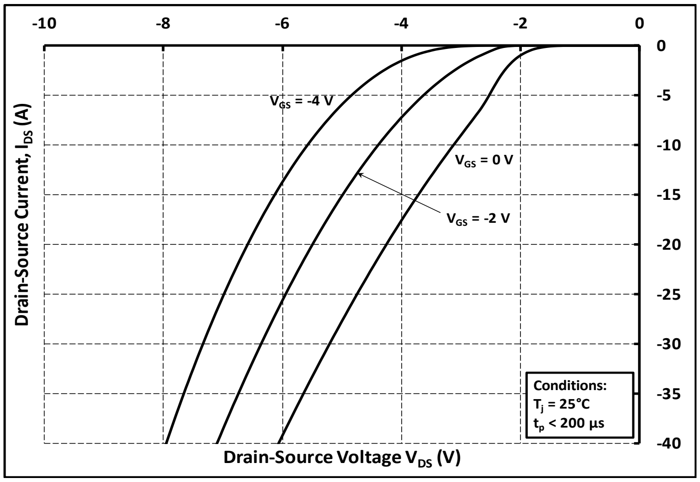


Figure 9. Body Diode Characteristic at 25°C

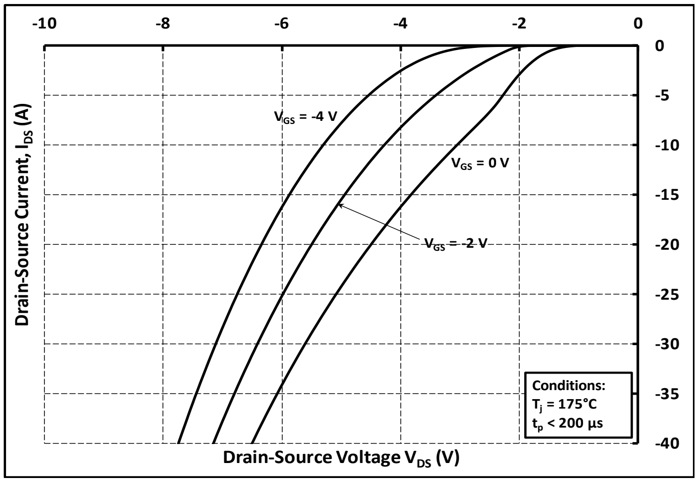


Figure 10. Body Diode Characteristic at 175°C

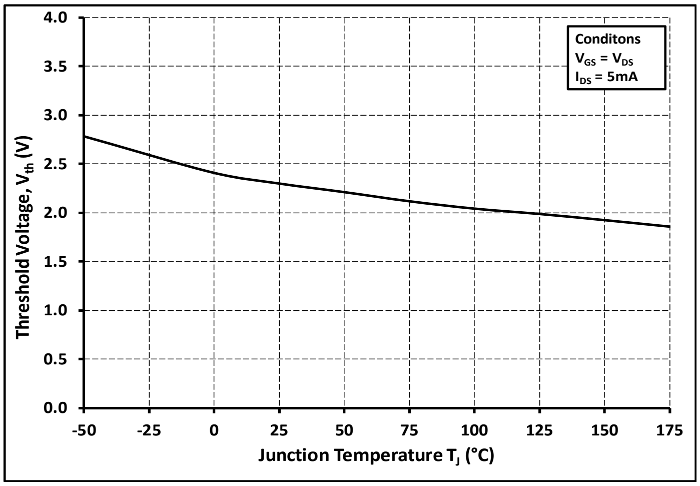


Figure 11. Threshold Voltage vs. Temperature

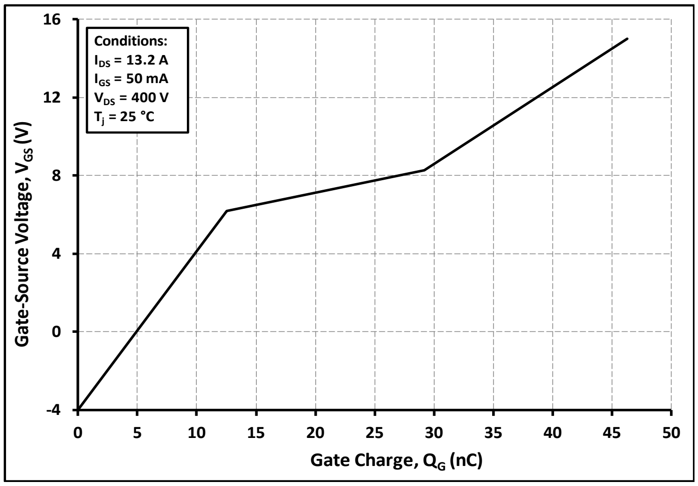


Figure 12. Gate Charge Characteristics

Typical Performance

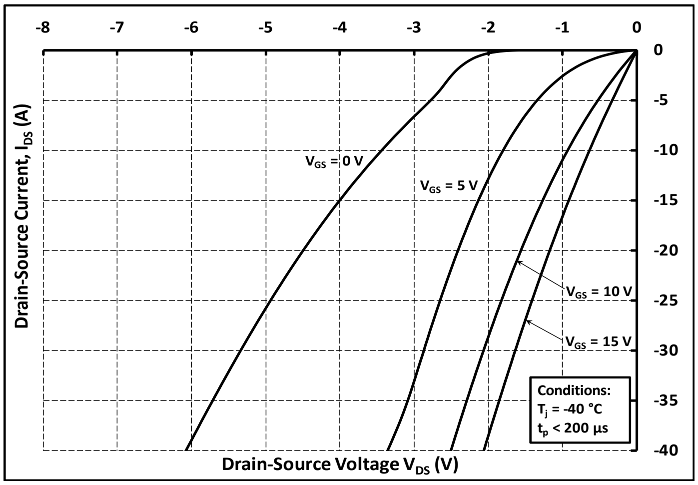


Figure 13. 3rd Quadrant Characteristic at -40°C

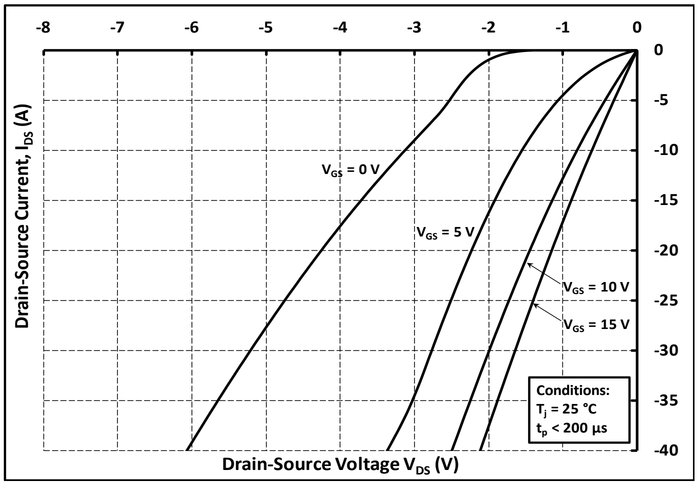


Figure 14. 3rd Quadrant Characteristic at 25°C

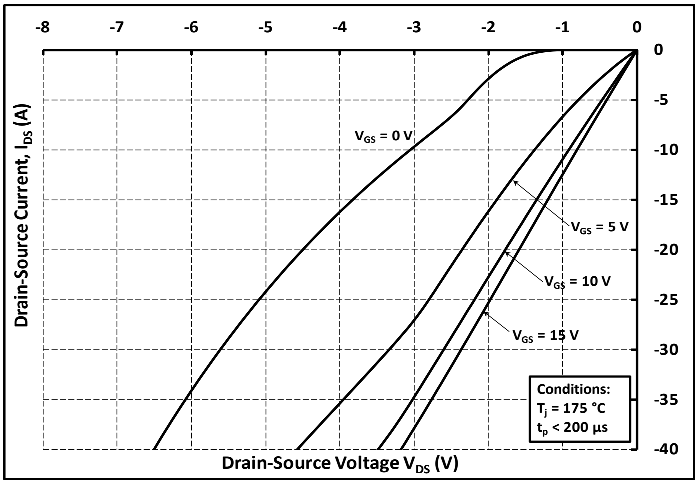


Figure 15. 3rd Quadrant Characteristic at 175°C

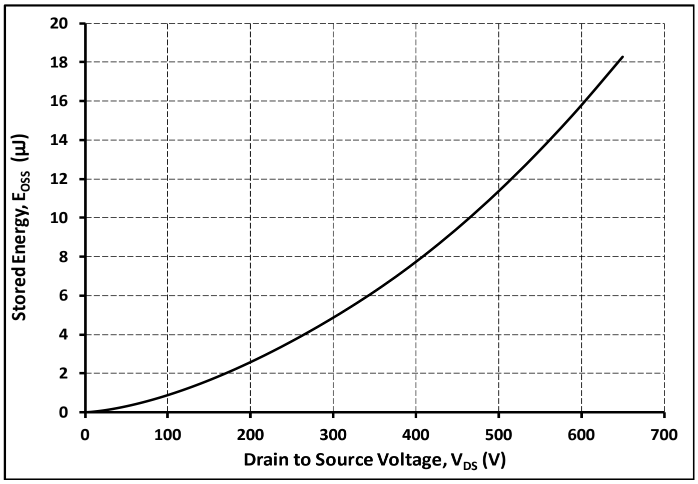


Figure 16. Output Capacitor Stored Energy

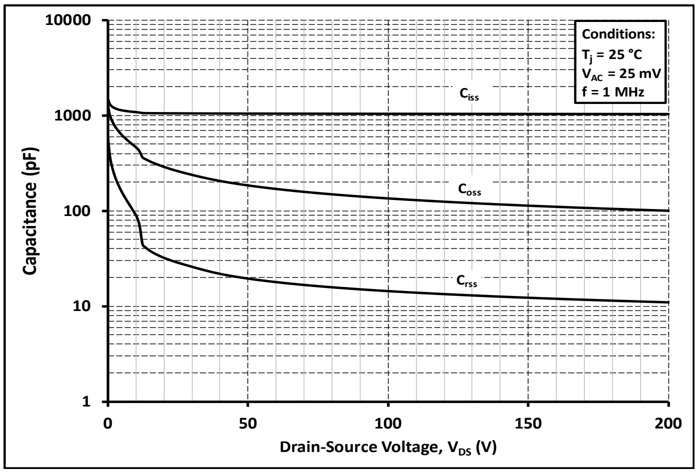


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

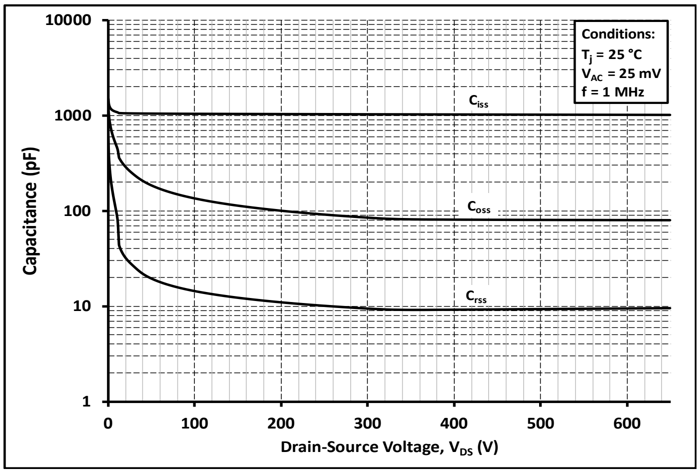


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650 V)

Typical Performance

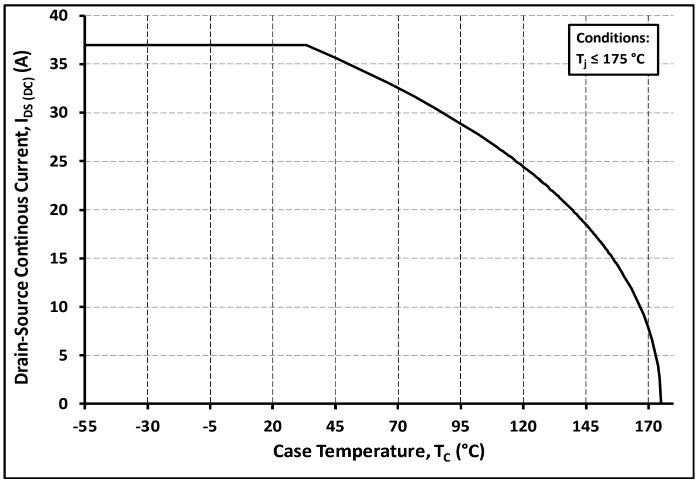


Figure 19. Continuous Drain Current Derating vs. Case Temperature

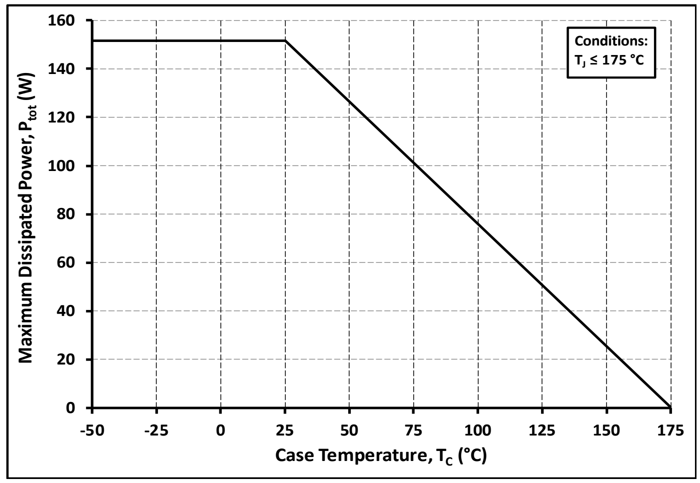


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

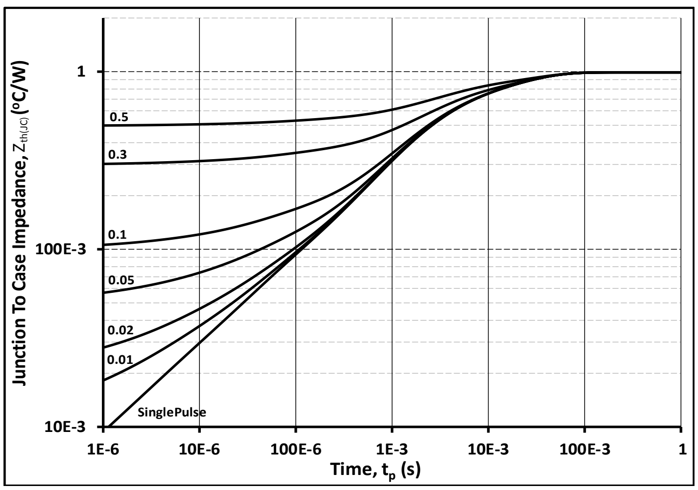


Figure 21. Transient Thermal Impedance (Junction - Case)

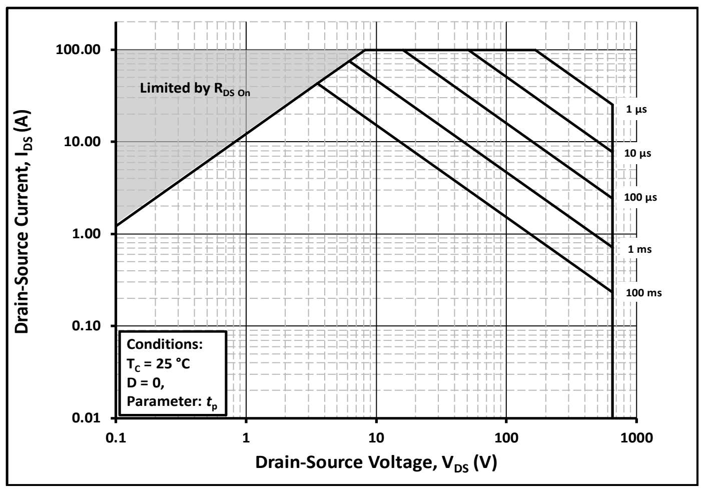


Figure 22. Safe Operating Area

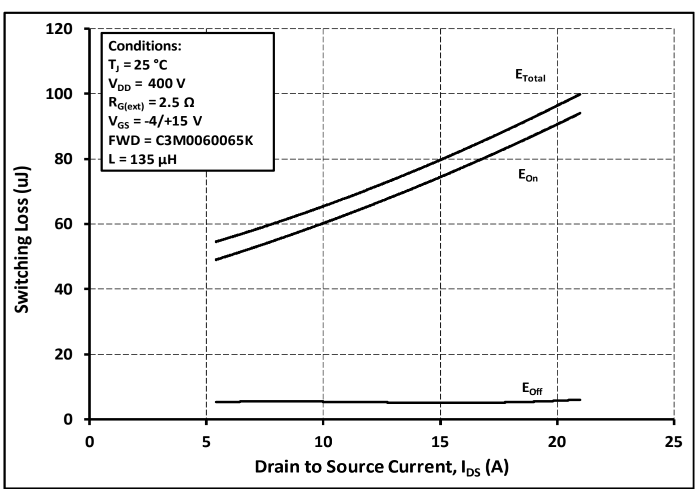


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 400 V)

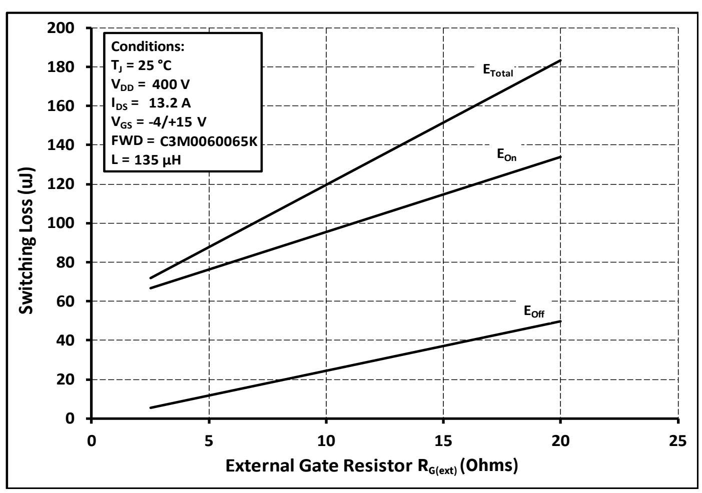


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

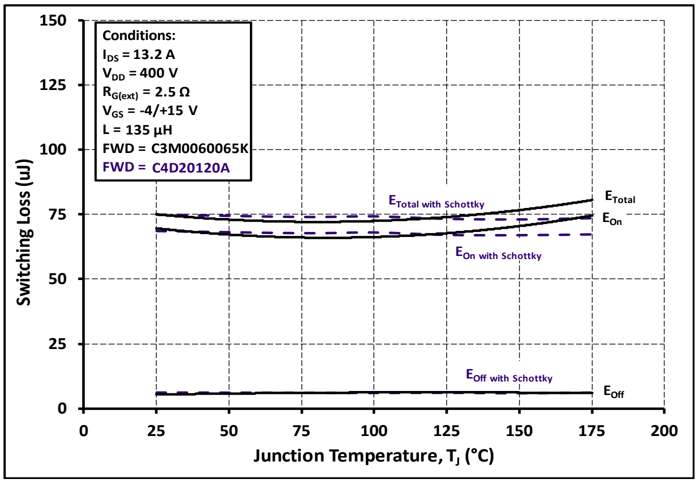


Figure 25. Clamped Inductive Switching Energy vs. Temperature

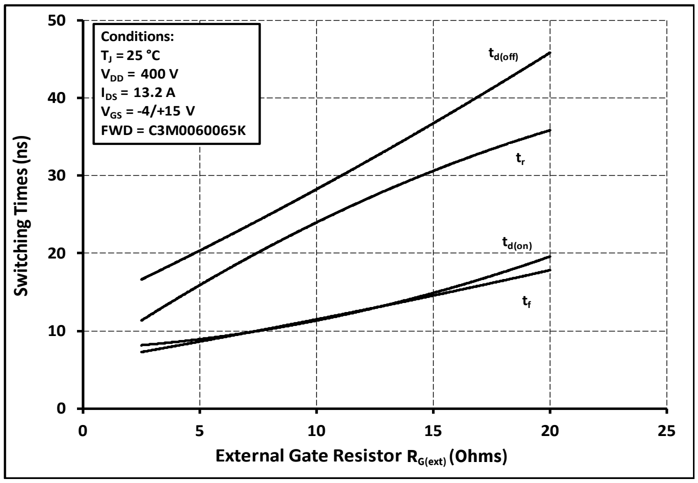


Figure 26. Switching Times vs. $R_{G(ext)}$

Test Circuit Schematic

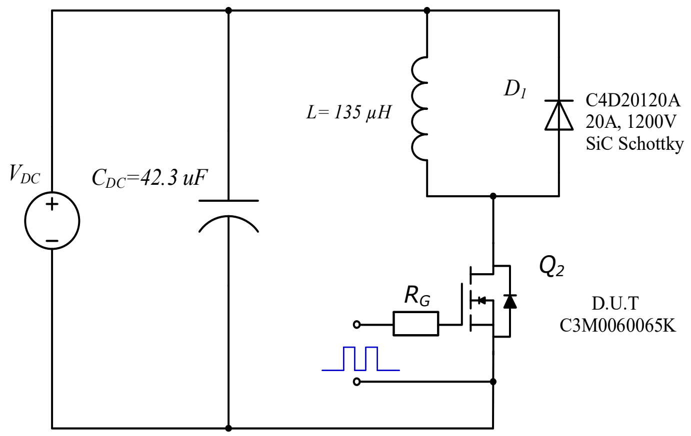


Figure 27. Clamped Inductive Switching Waveform Test Circuit

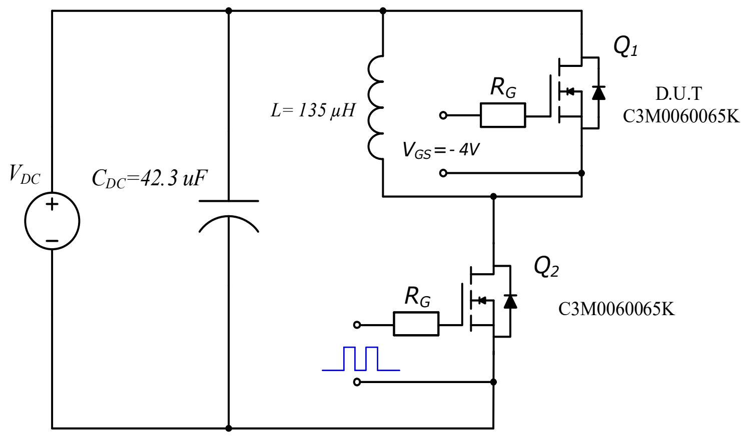
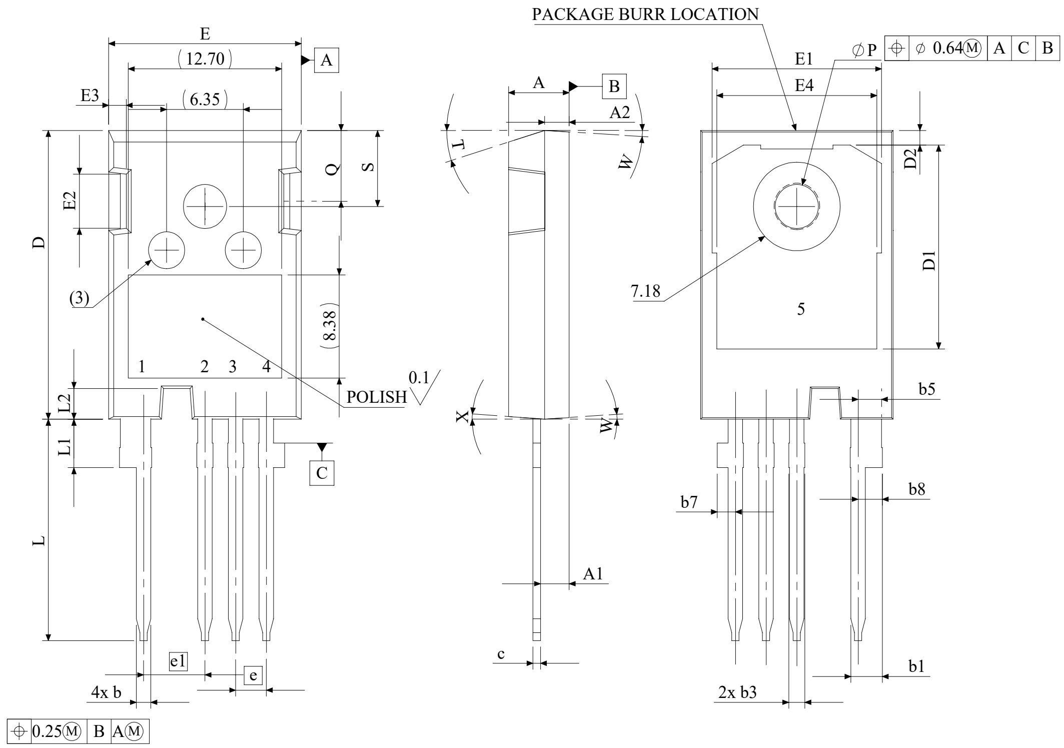


Figure 28. Body Diode Recovery Test Circuit

Package Dimensions – Package TO-247-4L



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b	1.07	1.33
b1	2.39	2.94
b3	1.07	1.60
b5	2.39	2.69
b7	1.30	1.70
b8	1.80	2.20
c	0.55	0.68
D	23.30	23.60
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13
E1	13.1	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	2.54 BSC	
e1	5.08 BSC	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
ØP	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	DRAIN
2	SOURCE
3	DRIVER SOURCE
4	GATE
5	DRAIN

NOTE:

1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

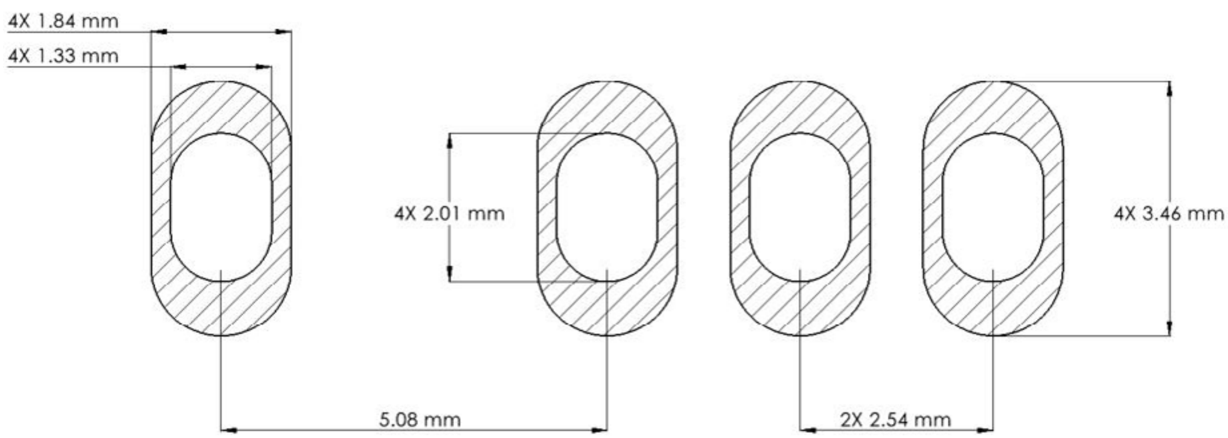
TITLE: PACKAGE OUTLINE DRAWING: TO-247-4L

Date: 05/05/22

REVISION NO. 01 | A4

SCALE:1:1 | SHEET 1 OF 1

Recommended Solder Pad Layout



Revision history

Document Version	Date of release	Description of changes
2	July-2020	N/A
3	December-2023	Update Package Drawing, package image, solder pad layout, added revision history table, Table 1 layout revised

Related Links

- SPICE Models
- SiC MOSFET Isolated Gate Driver reference design
- SiC MOSFET Evaluation Board

Notes & Disclaimer

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The Silicon Carbide MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Documentation sections of www.wolfspeed.com.

REACh Compliance

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

Contact info:

4600 Silicon Drive
Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfspeed.com/power