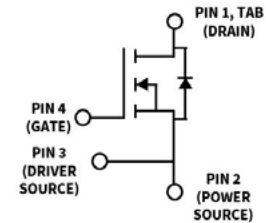
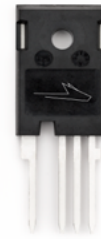


C3M0021120K

Silicon Carbide Power MOSFET
C3M™ MOSFET Technology
N-Channel Enhancement Mode

Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant



Part Number	Package	Marking
C3M0021120K	TO 247-4	C3M0021120K

Typical Applications

- Solar inverters
- EV motor drive
- High voltage DC/DC converters
- Switched mode power supplies
- Load switch

Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1200	v	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			100	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Fig. 19 Note 2
				74		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	
Pulsed Drain Current	I_{DM}			200		t_{Pmax} limited by T_{Jmax} $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			469	W	$T_c = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1	Nm lbf-in	M3 or 6-32 screw	
				8.8			

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design


Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200	—	—		$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6	V	$V_{DS} = V_{GS}, I_D = 17.7\ \text{mA}$	Fig. 11
		—	2.0	—		$V_{DS} = V_{GS}, I_D = 17.7\ \text{mA}, T_J = 175^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	50	nA	$V_{DS} = 1200\ \text{V}, V_{GS} = 0\ \text{V}$	
Gate-Source Leakage Current	I_{GSS}	—	10	250		$V_{GS} = 15\ \text{V}, V_{DS} = 0\ \text{V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$	—	21	28.8	m Ω	$V_{GS} = 15\ \text{V}, I_D = 50\ \text{A}$	Fig. 4, 5, 6
		—	38	—		$V_{GS} = 15\ \text{V}, I_D = 50\ \text{A}, T_J = 175^\circ\text{C}$	
Transconductance	g_{fs}	—	35	—	S	$V_{DS} = 20\ \text{V}, I_{DS} = 50\ \text{A}$	Fig. 7
		—	33	—		$V_{DS} = 20\ \text{V}, I_{DS} = 50\ \text{A}, T_J = 175^\circ\text{C}$	
Input Capacitance	C_{iss}	—	4818	—	pF	$V_{GS} = 0\ \text{V}, V_{DS} = 1000\ \text{V}$ $f = 100\ \text{kHz}$ $V_{AC} = 25\ \text{mV}$	Fig. 17, 18
Output Capacitance	C_{oss}	—	180	—			
Reverse Transfer Capacitance	C_{rss}	—	12	—			
C_{oss} Stored Energy	E_{oss}	—	99	—			μJ
Turn-On Switching Energy (SiC Diode FWD)	E_{on}	—	0.69	—	mJ	$V_{DS} = 800\ \text{V}, V_{GS} = -4\ \text{V}/+15\ \text{V}, I_D = 50\ \text{A},$ $R_{G(ext)} = 2.5\ \Omega, L = 157\ \mu\text{H},$ $T_J = 175^\circ\text{C}$	Fig. 26, 29
Turn Off Switching Energy (SiC Diode FWD)	E_{off}	—	0.42	—			
Turn-On Switching Energy (Body Diode FWD)	E_{on}	—	1.58	—			
Turn Off Switching Energy (Body Diode FWD)	E_{off}	—	0.34	—			
Turn-On Delay Time	$t_{d(on)}$	—	29	—	ns	$V_{DD} = 800\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $R_{G(ext)} = 2.5\ \Omega, L = 157\ \mu\text{H}$ Timing relative to V_{DS} inductive load	Fig. 27
Rise Time	t_r	—	33	—			
Turn-Off Delay Time	$t_{d(off)}$	—	57	—			
Fall Time	t_f	—	14	—			
Internal Gate Resistance	$R_{G(int)}$	—	3.3	—	Ω	$f = 1\ \text{MHz}, V_{AC} = 25\ \text{mV}$	
Gate to Source Charge	Q_{gs}	—	49	—	nC	$V_{DS} = 800\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 50\ \text{A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—	50	—			
Total Gate Charge	Q_g	—	162	—			

Note (3): $C_{o(er)}$, a lumped capacitance that gives the same stored energy as C_{oss} while V_{ds} is rising from 0 to 800V
 $C_{o(tr)}$, a lumped capacitance that gives the same stored time as C_{oss} while V_{ds} is rising from 0 to 800V



Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Notes
Diode Forward Voltage	V_{SD}	4.6	—	V	$V_{GS} = -4\text{ V}, I_{SD} = 25\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.2	—		$V_{GS} = -4\text{ V}, I_{SD} = 25\text{ A}, T_J = 175^\circ\text{C}$	
Continuous Diode Forward Current	I_S	—	90	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
Diode pulse Current	I_{SM}	—	200		$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{Jmax}	
Reverse Recover Time	t_{rr}	34	—	ns	$V_{GS} = -4\text{ V}, I_{SD} = 50\text{ A}, V_R = 800\text{ V}$ $dif/dt = 2600\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	928	—			
Peak Reverse Recovery Current	I_{RRM}	42	—	nC		

Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.32	$^\circ\text{C}/\text{W}$	Fig. 21
Thermal Resistance From Junction to Ambient	$R_{\theta JA}$	40		



Typical Performance

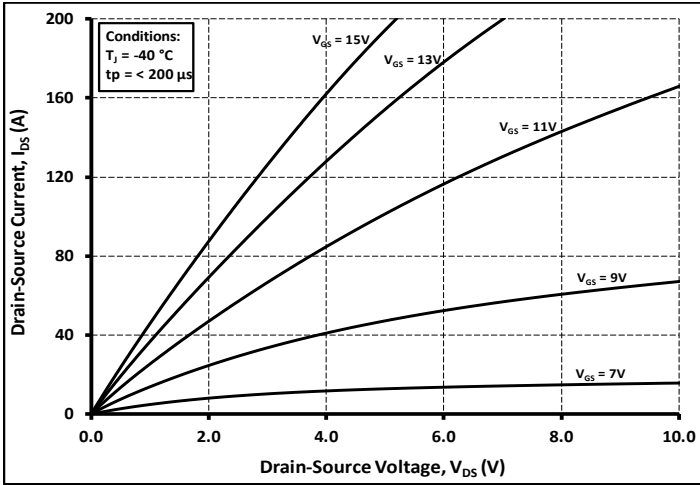


Figure 1. Output Characteristics $T_j = -40^\circ\text{C}$

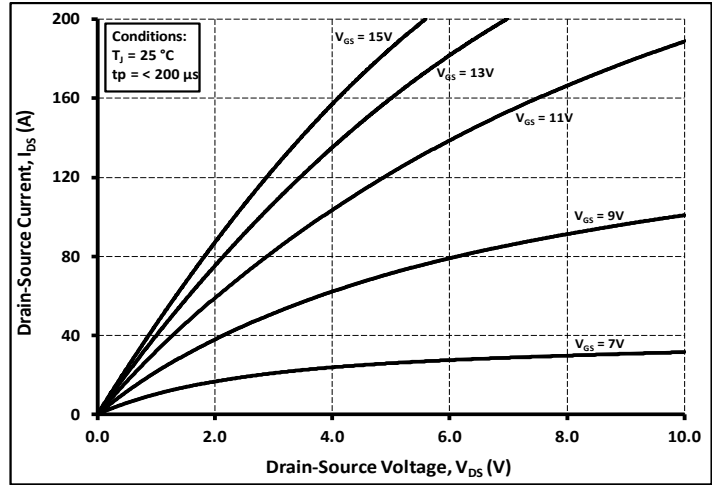


Figure 2. Output Characteristics $T_j = 25^\circ\text{C}$

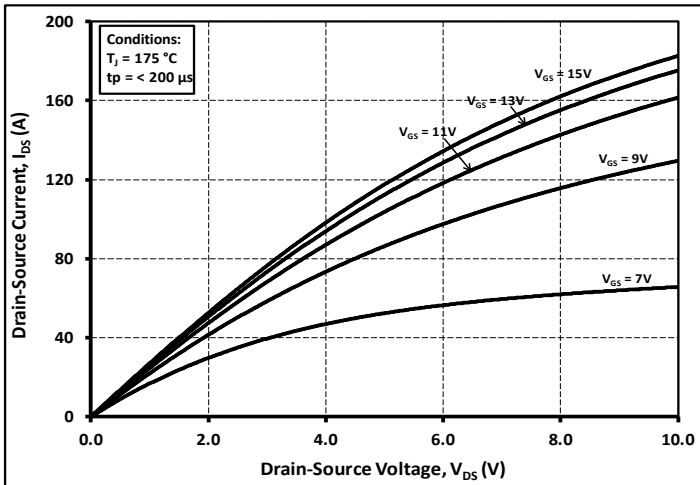


Figure 3. Output Characteristics $T_j = 175^\circ\text{C}$

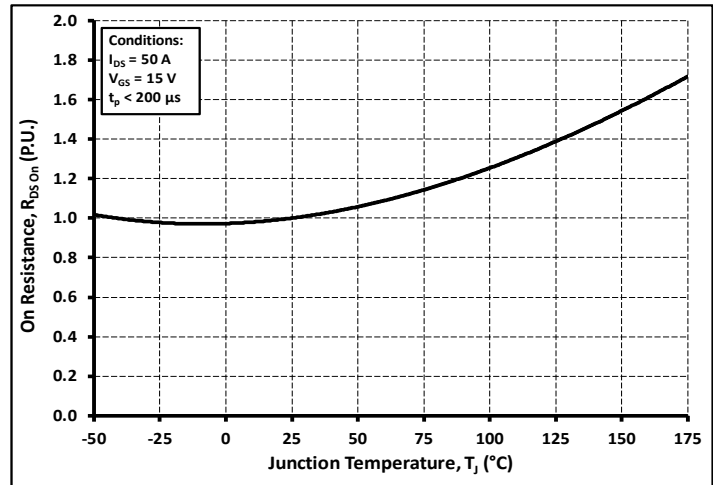


Figure 4. Normalized On-Resistance vs. Temperature

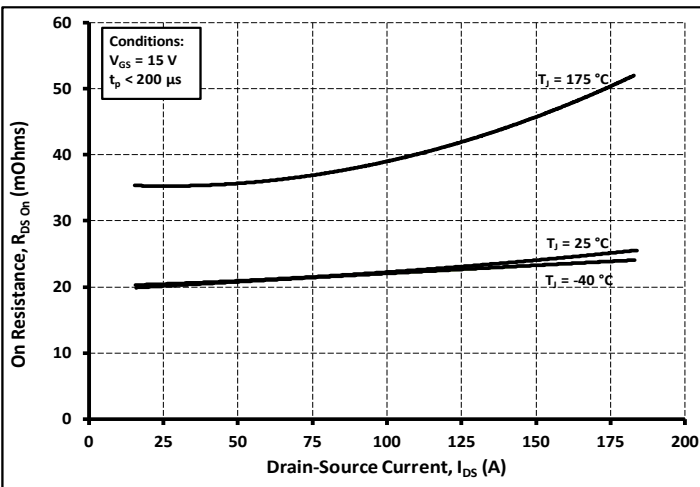


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

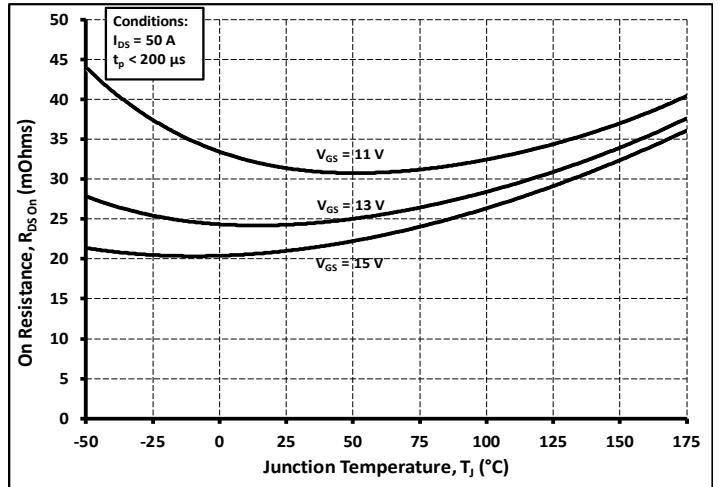


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

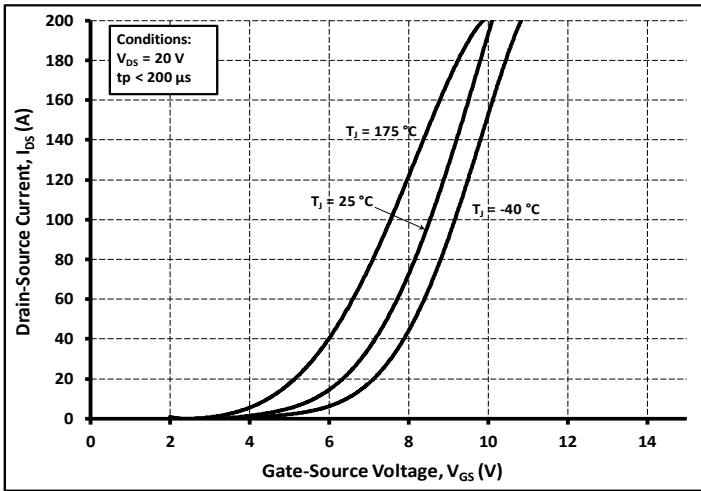


Figure 7. Transfer Characteristic for Various Junction Temperatures

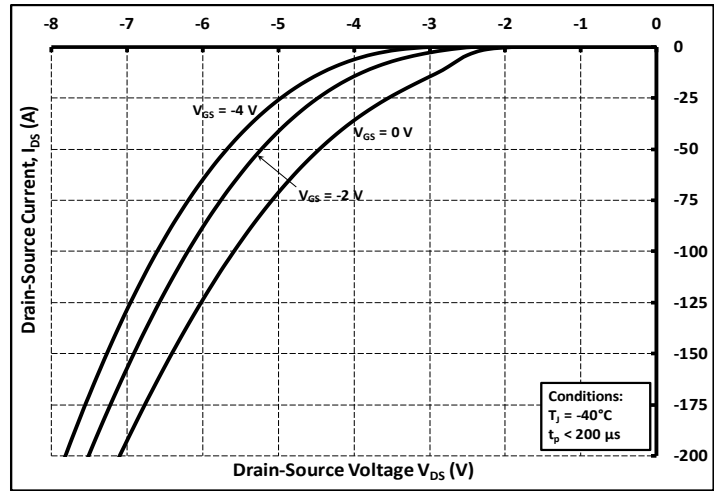


Figure 8. Body Diode Characteristic at -40 °C

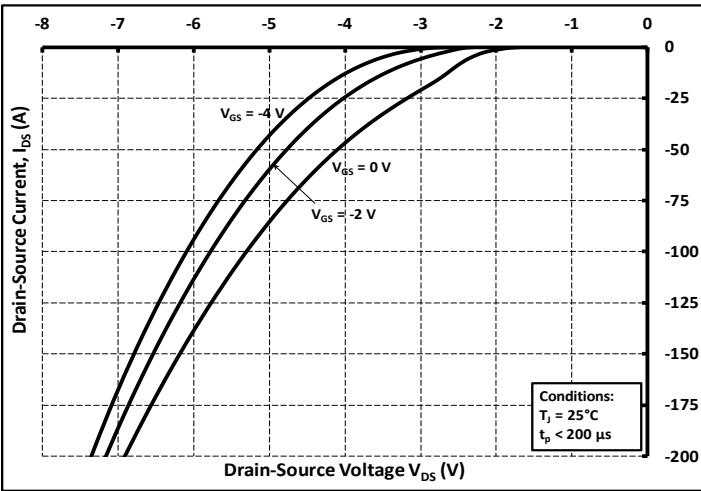


Figure 9. Body Diode Characteristic at 25 °C

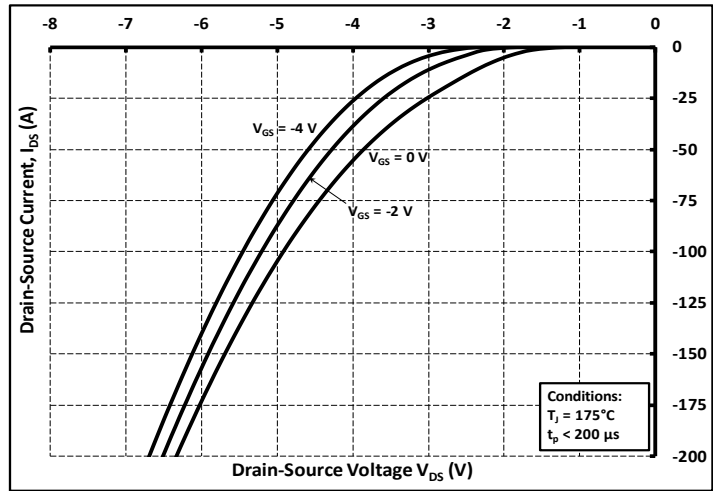


Figure 10. Body Diode Characteristic at 175 °C

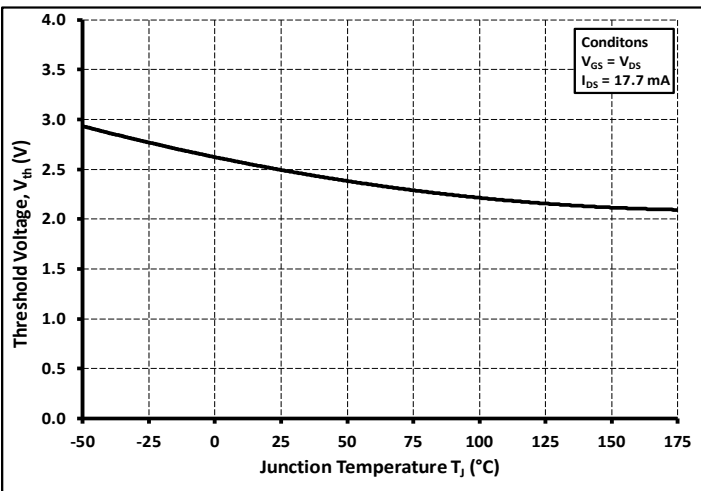


Figure 11. Threshold Voltage vs. Temperature

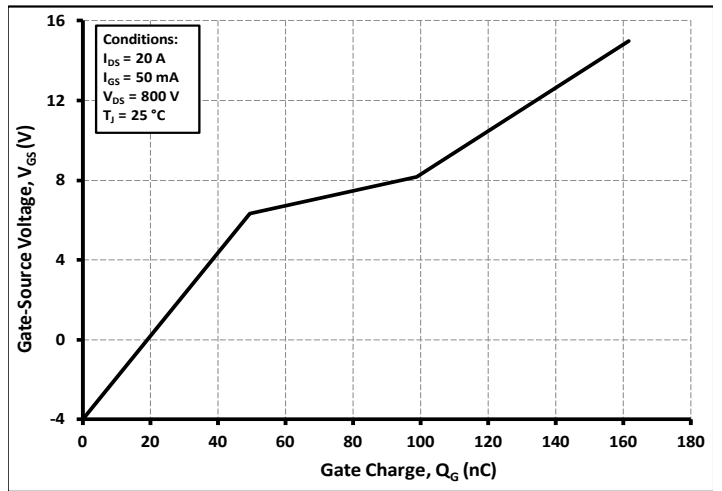


Figure 12. Gate Charge Characteristics



Typical Performance

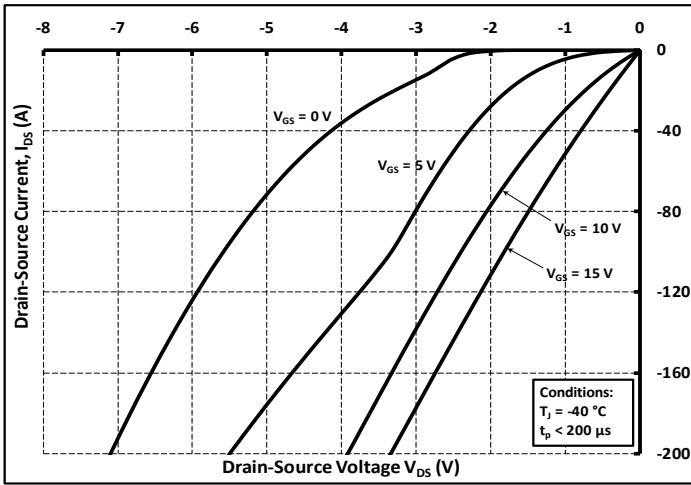


Figure 13. 3rd Quadrant Characteristic at -40°C

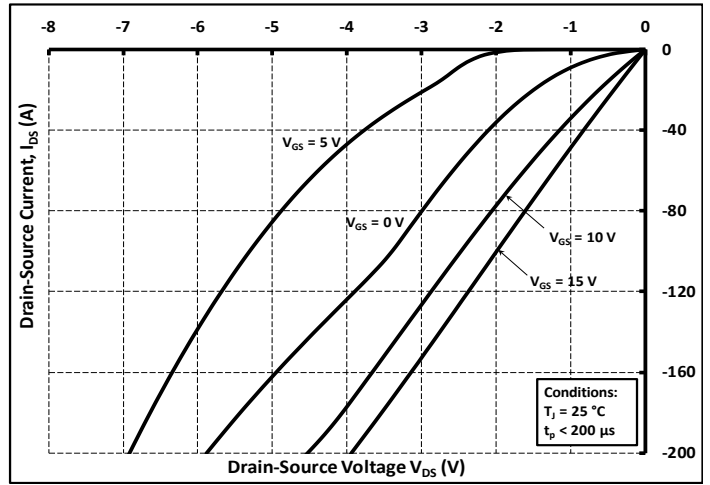


Figure 14. 3rd Quadrant Characteristic at 25°C

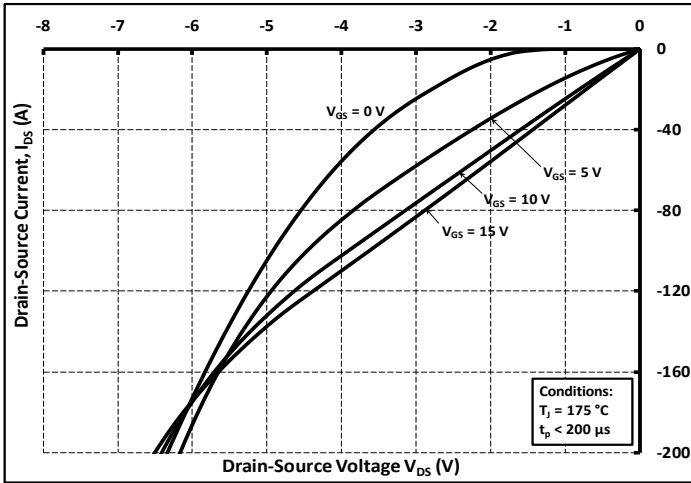


Figure 15. 3rd Quadrant Characteristic at 175°C

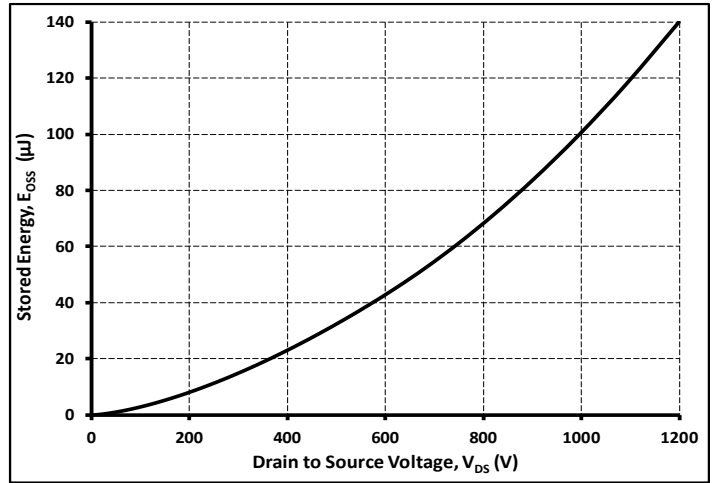


Figure 16. Output Capacitor Stored Energy

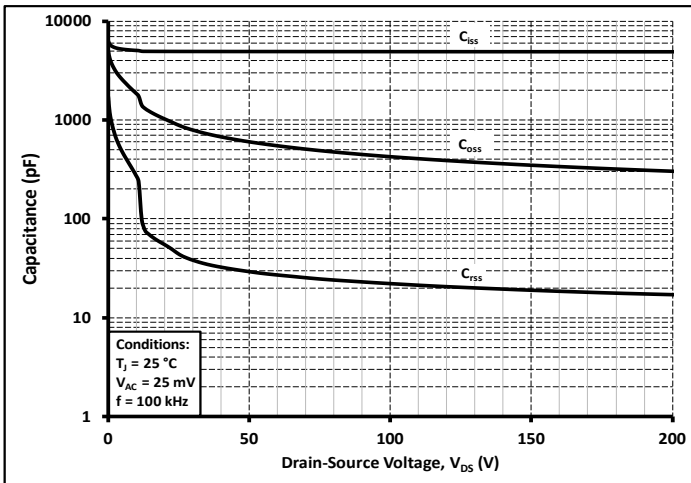


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

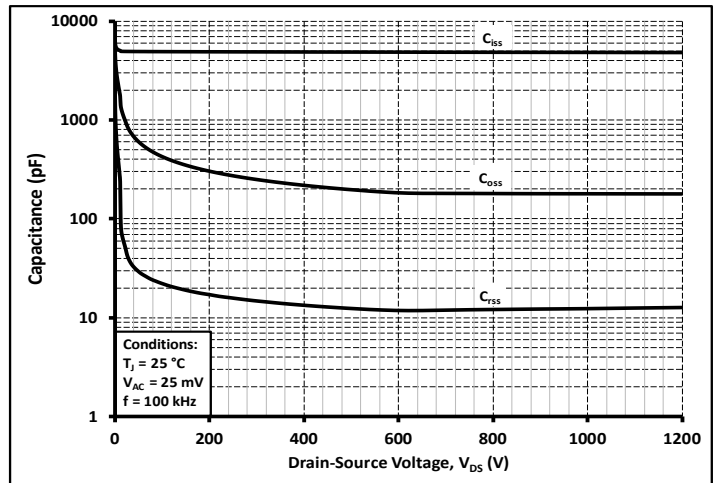


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)



Typical Performance

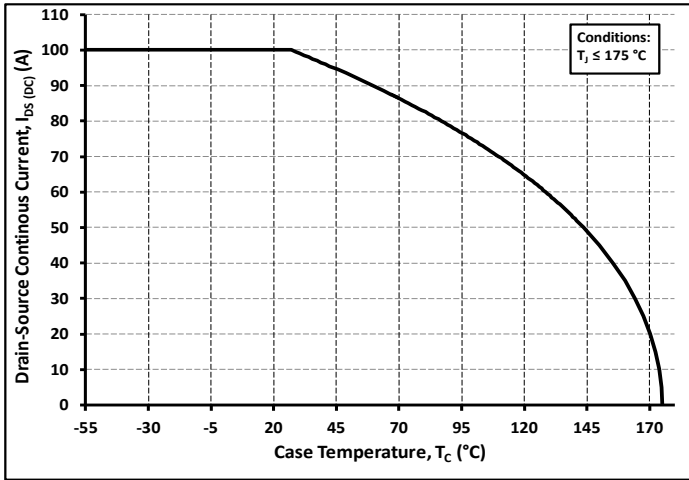


Figure 19. Continuous Drain Current Derating vs. Case Temperature

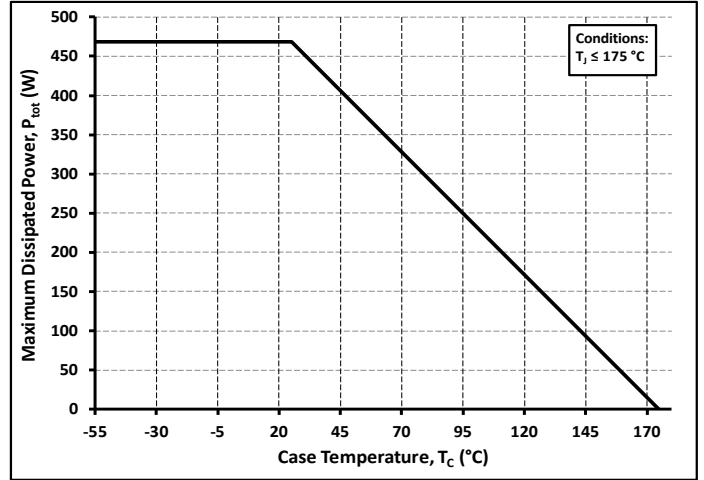


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

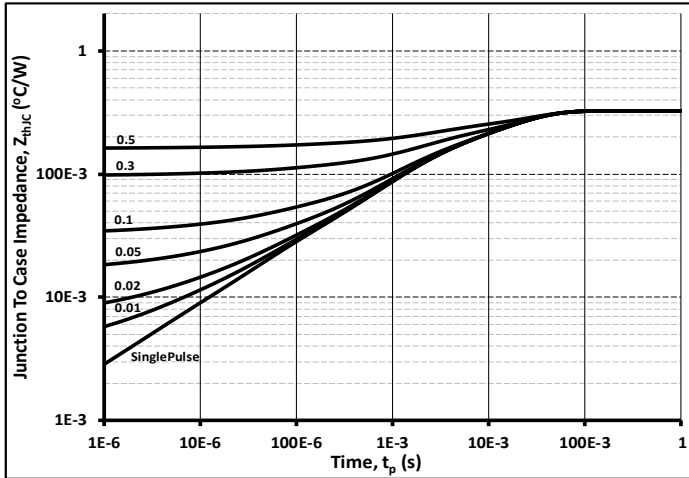


Figure 21. Transient Thermal Impedance (Junction - Case)

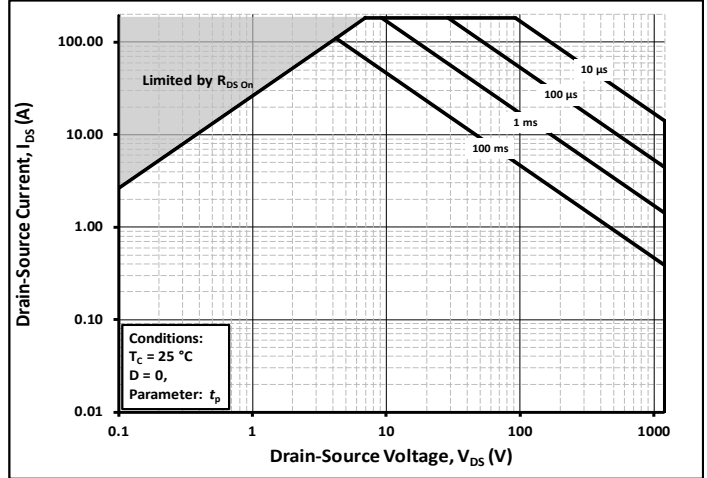


Figure 22. Safe Operating Area

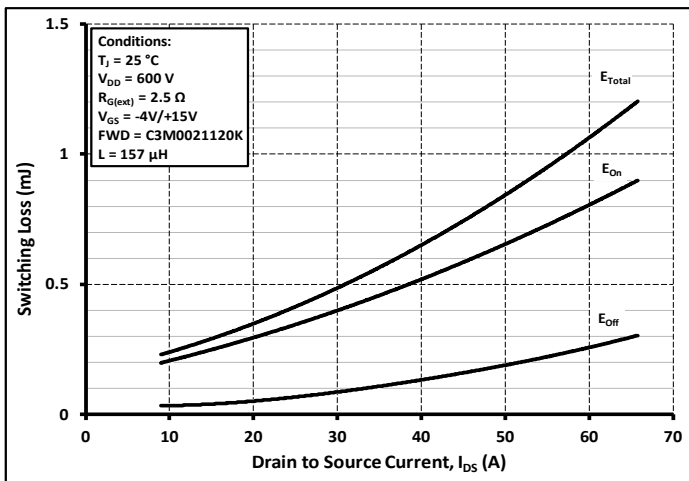


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 600\text{ V}$)

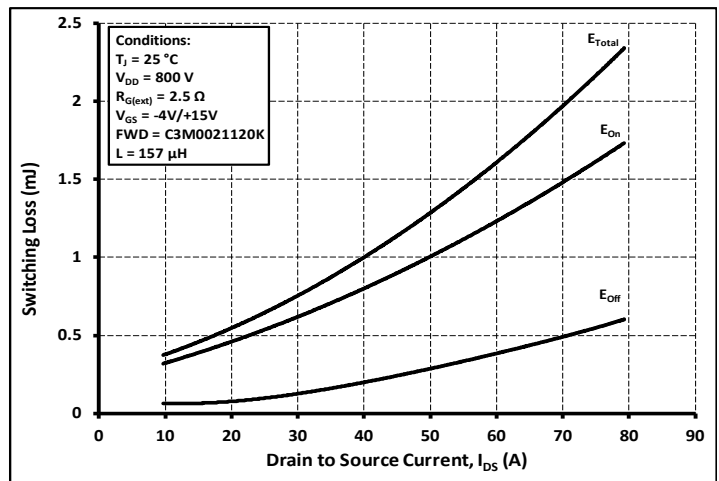


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 800\text{ V}$)

Typical Performance

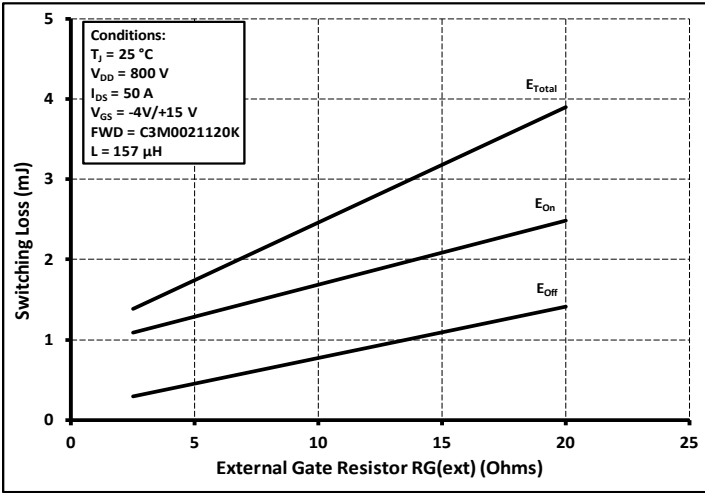


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

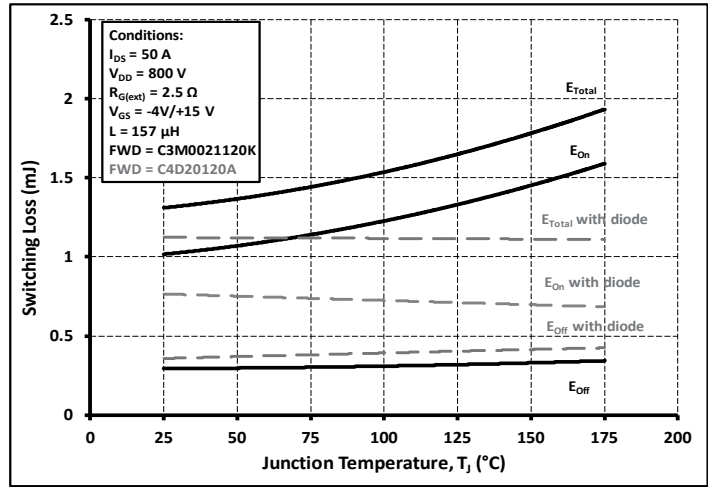


Figure 26. Clamped Inductive Switching Energy vs. Temperature

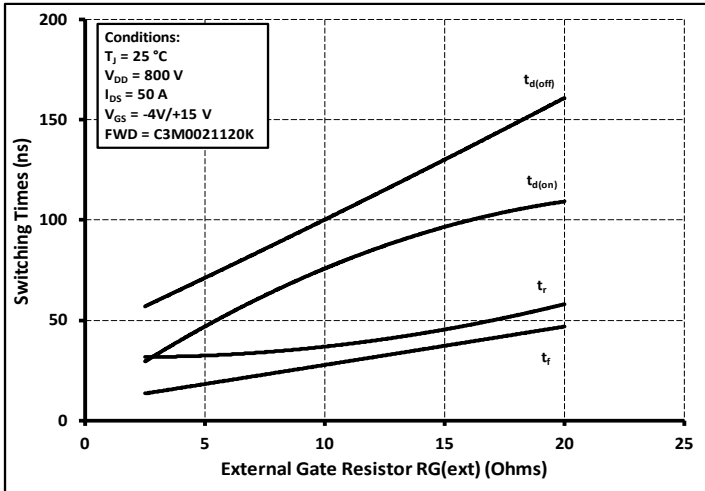


Figure 27. Switching Times vs. $R_{G(ext)}$

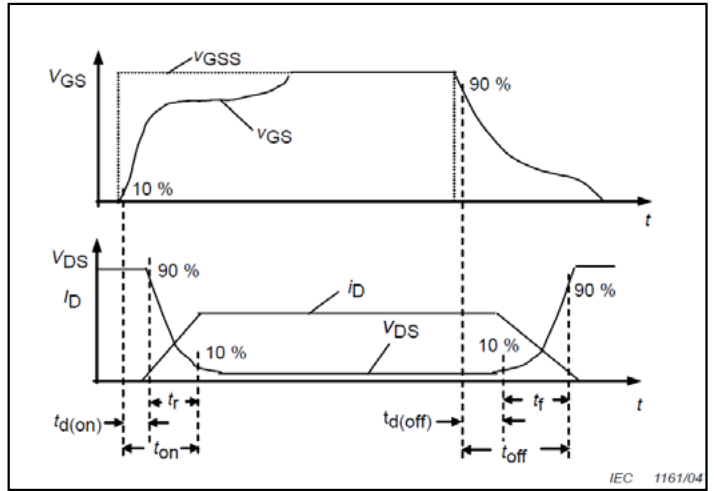


Figure 28. Switching Times Definition

Test Circuit Schematic¹

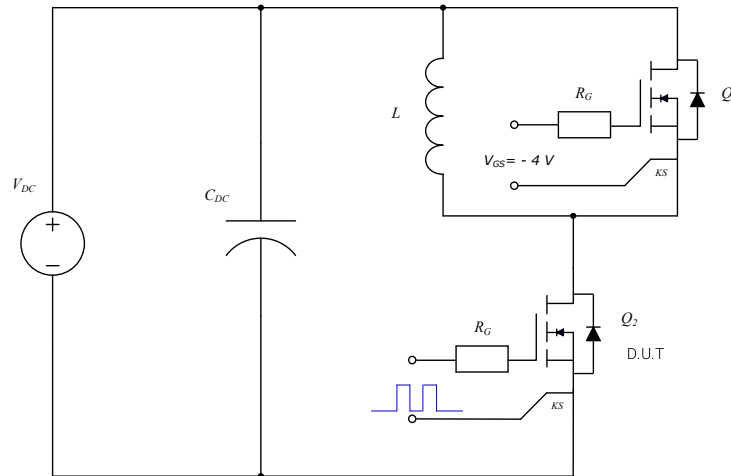
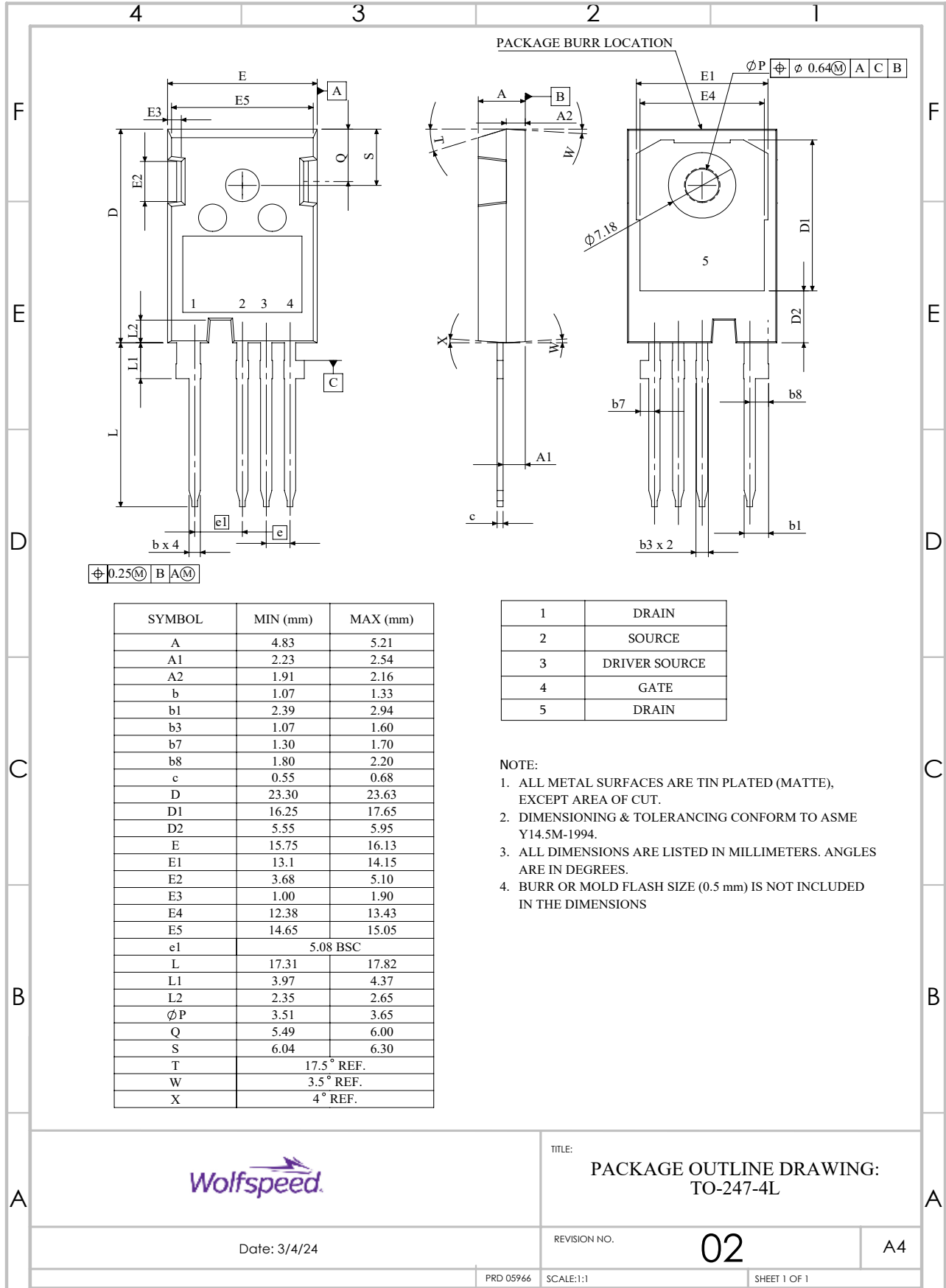


Figure 29. Clamped Inductive Switching Waveform Test Circuit

Note:

¹ Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

Package Dimensions – Package TO-247-4L



TITLE:
PACKAGE OUTLINE DRAWING:
TO-247-4L

Date: 3/4/24

REVISION NO.

02

A4

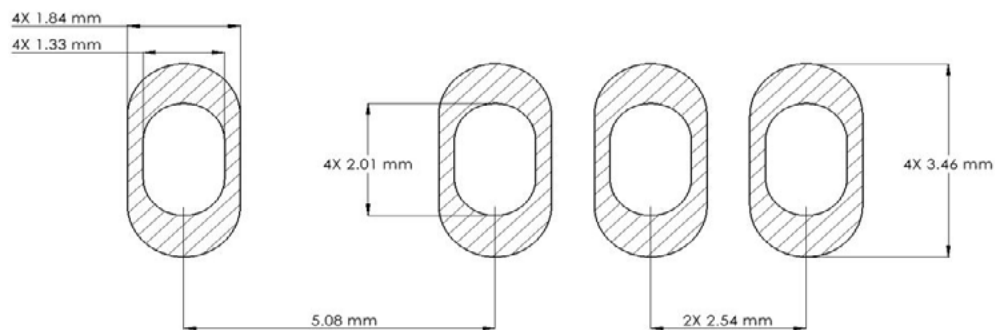
PRD 05966

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SHEET 1 OF 1



Recommended Solder Pad Layout



Revision History

Document Version	Date of Release	Description of Changes
1	March-2023	N/A
2	December-2023	Updated Package Image, solder pad layout, added revision history, Table 1 layout revised
3	September - 2024	Legal Disclaimer, POD, Diode Pulse Current Symbol



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