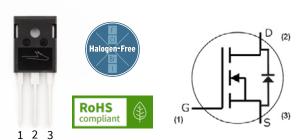


Silicon Carbide Power MOSFET C2M™ MOSFET Technology N-Channel Enhancement Mode

#### **Features**

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant



Wolfspeed, Inc. is in the process of rebranding its products and related materials pursuant to the entity name change from Cree, Inc. to Wolfspeed, Inc. During this transition period, products received may be marked with either the Cree name and/or logo or the Wolfspeed name and/or logo.

Ordering Part Number	Package	Marking
C2M0160120D	TO-247-3	C2M0160120

## **Applications**

- Solar inverters
- Switch Mode Power Supplies
- High Voltage DC/DC converters
- LED Lighting Power Supplies

#### **Benefits**

- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

## Maximum Ratings (T<sub>c</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit	Test Conditions	Note
Drain-Source Voltage	V <sub>DS max</sub>	1200		$V_{GS} = 0 \text{ V}, I_D = 100  \mu\text{A}$	
Gate-Source Voltage	V <sub>GS max</sub>	-10/+25	V	Absolute maximum values	
Gate-Source Voltage	V <sub>GS op</sub>	-5/+20		Recommended operational values	
Continuous Drain Current	I <sub>D</sub>	18		$V_{GS} = 20 \text{ V}, T_C = 25^{\circ}\text{C}$	Fig. 19
		12	Α	$V_{GS} = 20 \text{ V}, \ T_C = 100^{\circ}\text{C}$	
Pulsed Drain Current	I <sub>D(pulsed)</sub>	40		Pulse width t <sub>P</sub> limited by T <sub>j max</sub>	Fig. 22
Power Dissipation	P <sub>D</sub>	125	W	T <sub>C</sub> = 25°C, T <sub>J</sub> = 150°C	Fig. 20
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	0.6		
Solder Temperature	TL	260	°C	According to JEDEC J-STD-020	
Mounting Torque	M <sub>d</sub>	1 8.8	Nm lbf-in	M3 or 6-32 screw	

# **Electrical Characteristics** (T<sub>c</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Conditions	Note	
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200	_	_		$V_{GS} = 0 \text{ V}, I_{D} = 100 \mu\text{A}$		
Cata Thurshald Valtage	.,	2.0	2.9	4	V	$V_{DS} = V_{GS}, I_{D} = 2.5 \text{ mA}$	F: 44	
Gate Threshold Voltage	$V_{GS(th)}$	_	2.4	_		$V_{DS} = V_{GS}, I_{D} = 2.5 \text{ mA}, T_{J} = 150^{\circ}\text{C}$	Fig. 11	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	1	100	μΑ	V <sub>DS</sub> = 1200 V, V <sub>GS</sub> = 0 V		
Gate-Source Leakage Current	I <sub>GSS</sub>	_	_	250	nA	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$		
Durin Course On State Besistance		_	160	196	mΩ	$V_{GS} = 20 \text{ V}, I_D = 10 \text{ A}$	Fig. 4, 5, 6	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	_	290	_		$V_{GS} = 25 \text{ V}, I_D = 10 \text{ A}, T_J = 150^{\circ}\text{C}$		
			3.8			V <sub>DS</sub> = 20 V, I <sub>DS</sub> = 10 A	1	
Transconductance	<b>g</b> fs	_	5.3	_	S	$V_{DS} = 20 \text{ V}, I_{DS} = 10 \text{ A}, T_{J} = 150 ^{\circ}\text{C}$	Fig. 7	
Input Capacitance	C <sub>iss</sub>	_	606	_			Fig. 17, 18	
Output Capacitance	Coss	_	55	_	pF	$V_{GS} = 0 V$ $V_{DS} = 1000 V$		
Reverse Transfer Capacitance	C <sub>rss</sub>	_	5	_	1	f = 1  Mhz $V_{AC} = 25 \text{ mV}$		
C <sub>oss</sub> Stored Energy	E <sub>oss</sub>	_	28	_	μJ	VAC - 25 111V		
Avalanche Energy, Single Pluse	E <sub>AS</sub>	_	600	_	mJ	I <sub>D</sub> = 10A, V <sub>DD</sub> = 50V	Fig. 29	
Turn-On Switching Energy	Eon	_	121	_	1	$V_{DS} = 800 \text{ V}, V_{GS} = -5/20 \text{ V}, I_{D} = 10 \text{ A},$	Fig. 26	
Turn Off Switching Energy	E <sub>off</sub>	_	48	_	μJ	$R_{G(ext)} = 2.5 \Omega, L = 434 \mu H$		
Turn-On Delay Time	t <sub>d(on)</sub>	_	7	_		$V_{DD} = 800 \text{ V}, V_{GS} = -5/20 \text{ V},$		
Rise Time	t <sub>r</sub>	_	9	_	]	$I_{D} = 10 A,$	F: 27	
Turn-Off Delay Time	$t_{d(off)}$	_	13	_	ns	$\begin{array}{l} R_{G(ext)} = 2.5~\Omega,~R_L = 80~\Omega\\ Timing~relative~to~V_{DS}\\ Per~IEC60747-8-4~pg~83 \end{array}$	Fig. 27	
Fall Time	t <sub>f</sub>	_	14	_				
Internal Gate Resistance	R <sub>G(int)</sub>	_	6.5	_	Ω	$f = 1 \text{ MHz}, V_{AC} = 25 \text{ mV}$		
Gate to Source Charge	Q <sub>gs</sub>	_	11	_		V - 900 V V - 5/20 V		
Gate to Drain Charge	$Q_{\rm gd}$	_	17	_	nC	$V_{DS} = 800 \text{ V}, V_{GS} = -5/20 \text{ V}$ $I_{D} = 10 \text{ A}$	Fig. 12	
Total Gate Charge	Qg	_	40	_	1	Per IEC60747-8-4 pg 21		

#### **Reverse Diode Characteristics**

Parameter	Symbol	Тур.	Max.	Unit	<b>Test Conditions</b>	Notes
Diode Forward Voltage	V <sub>SD</sub>	3.9	_	V	$V_{GS} = -5 \text{ V}, I_F = 5 \text{ A}$	Fig.
		3.5	_		$V_{GS} = -5 \text{ V}, I_F = 5 \text{ A}, T_J = 150^{\circ}\text{C}$	8, 9, 10
Continuous Diode Forward Current <sup>1</sup>	Is	_	25	Α	T <sub>C</sub> = 25°C	
Reverse Recovery Time <sup>1</sup>	t <sub>rr</sub>	20	_	ns		
Reverse Recovery Charge <sup>1</sup>	Q <sub>rr</sub>	192	_	nC	$V_{GS} = -5 \text{ V}, I_{SD} = 10 \text{ A}, V_{R} = 800 \text{ V}$ $di_{F}/dt = 2400 \text{ A}/\mu\text{s}$	
Peak Reverse Recovery Current <sup>1</sup>	I <sub>RRM</sub>	16	_	Α	1 . , , , ,	

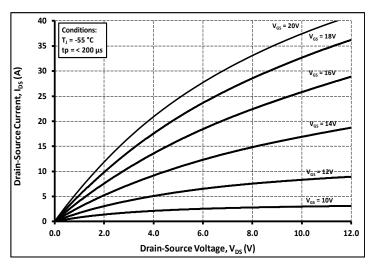
Note:

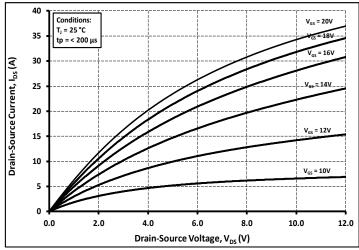
#### **Thermal Characteristics**

Parameter	Symbol	Тур.	Max.	Unit	<b>Test Conditions</b>	Notes
Thermal Resistance from Junction to Case	$R_{ heta JC}$	0.9	1.0	K/W		Fig. 21
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$		40	r/W		Fig. 21

 $<sup>^{1}</sup>$ When using SiC Body Diode the maximum recommended  $V_{GS} = -5V$ 

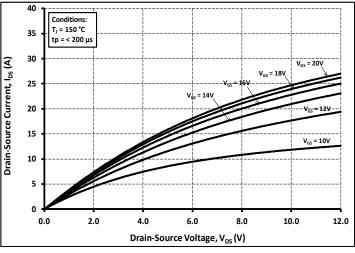
## **Typical Performance**





**Figure 1.** Output Characteristics  $T_J = -55^{\circ}C$ 

Figure 2. Output Characteristics  $T_J = 25^{\circ}C$ 



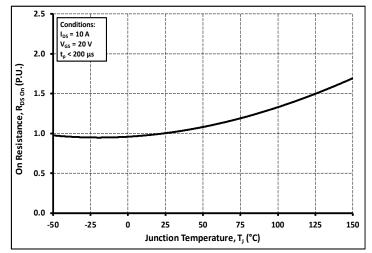
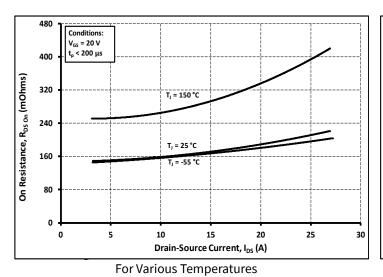
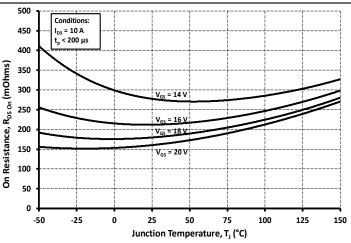


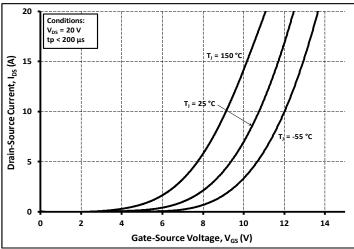
Figure 3. Output Characteristics T<sub>J</sub> = 150°C

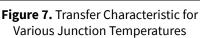
Figure 4. Normalized On-Resistance vs. Temperature





For Various Gate Voltage





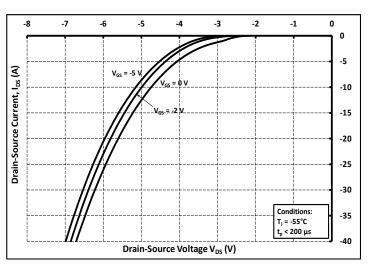


Figure 8. Body Diode Characteristic at -55°C

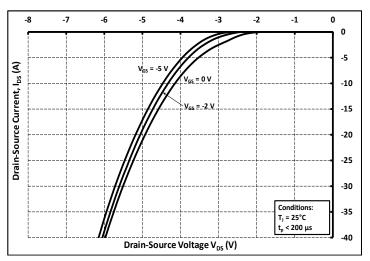


Figure 9. Body Diode Characteristic at 25°C

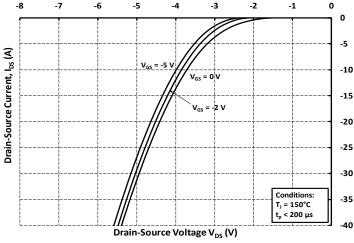
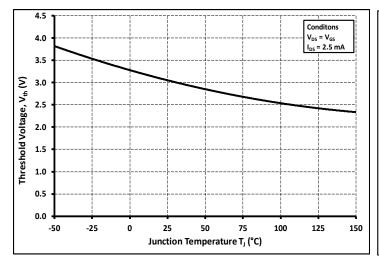


Figure 10. Body Diode Characteristic at 150°C



**Figure 11.** Threshold Voltage vs. Temperature

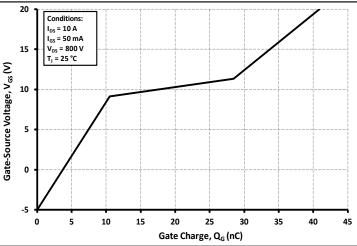


Figure 12. Gate Charge Characteristics

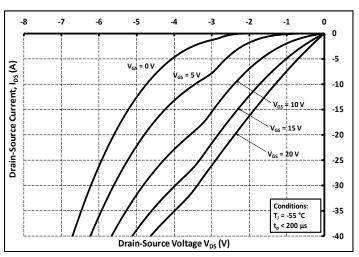


Figure 13. 3rd Quadrant Characteristic at -55°C

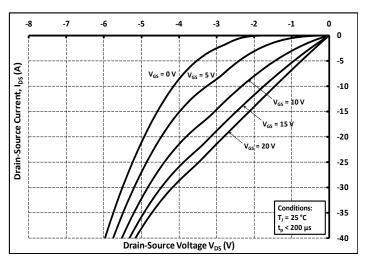


Figure 14. 3rd Quadrant Characteristic at 25°C

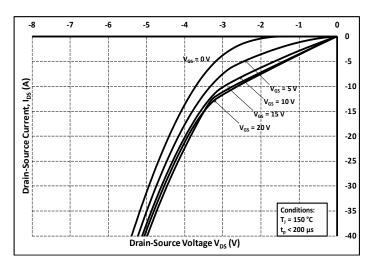


Figure 15. 3rd Quadrant Characteristic at 150°C

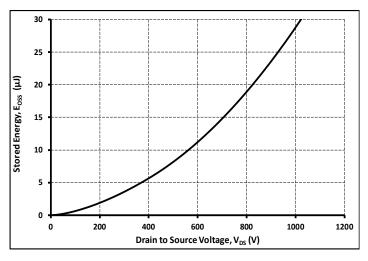
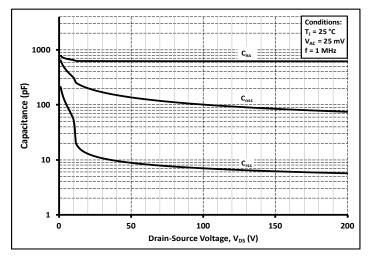
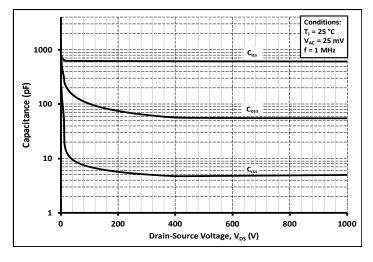


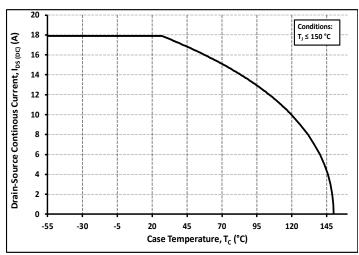
Figure 16. Output Capacitor Stored Energy



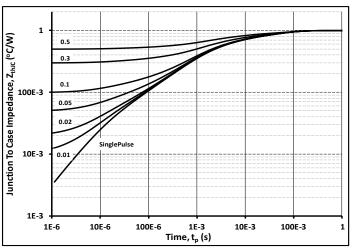
**Figure 17.** Capacitances vs. Drain-Source Voltage (0 - 200V)



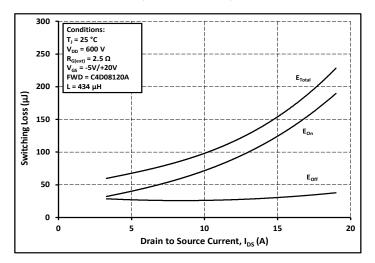
**Figure 18.** Capacitances vs. Drain-Source Voltage (0 - 1000V)



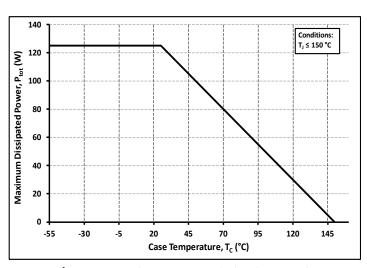
**Figure 19.** Continuous Drain Current Derating vs. Case Temperature



**Figure 21.** Transient Thermal Impedance (Junction - Case)



**Figure 23.** Clamped Inductive Switching Energy vs. Drain Current (V<sub>DD</sub> = 600 V)



**Figure 20.** Maximum Power Dissipation Derating vs. Case Temperature

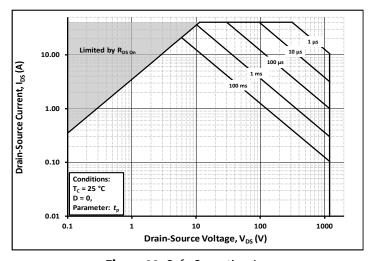
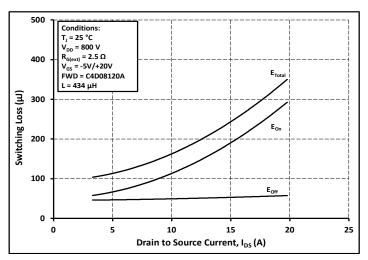


Figure 22. Safe Operating Area



**Figure 24.** Clamped Inductive Switching Energy vs. Drain Current (V<sub>DD</sub> = 800 V)

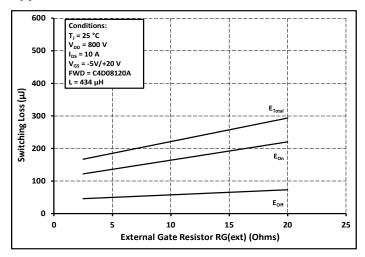


Figure 25. Clamped Inductive Switching Energy vs. R<sub>G(ext)</sub>

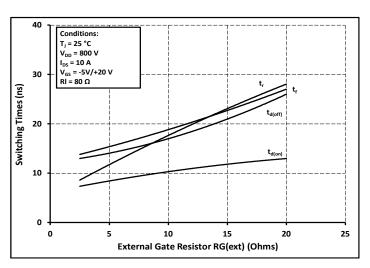


Figure 27. Switching Times vs. R<sub>G(ext)</sub>

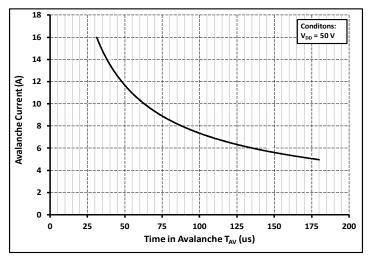
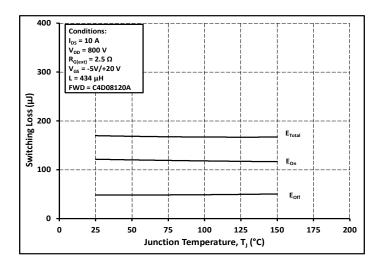


Figure 29. Single Avalanche SOA curve



**Figure 26.** Clamped Inductive Switching Energy vs. Temperature

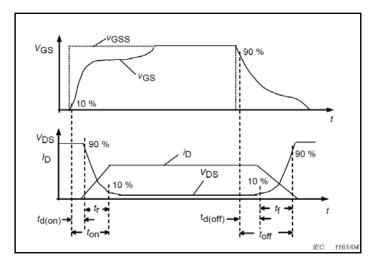


Figure 28. Switching Times Definition

#### Test Circuit Schematic<sup>1</sup>

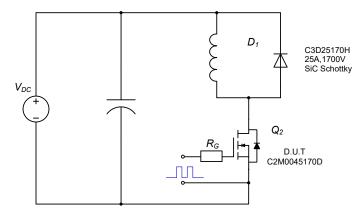


Figure 30. Clamped Inductive Switching Waveform Test Circuit

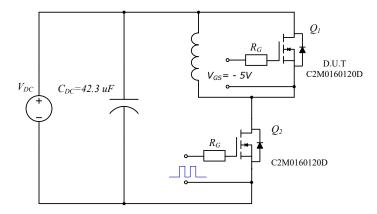


Figure 31. Body Diode Recovery Test Circuit

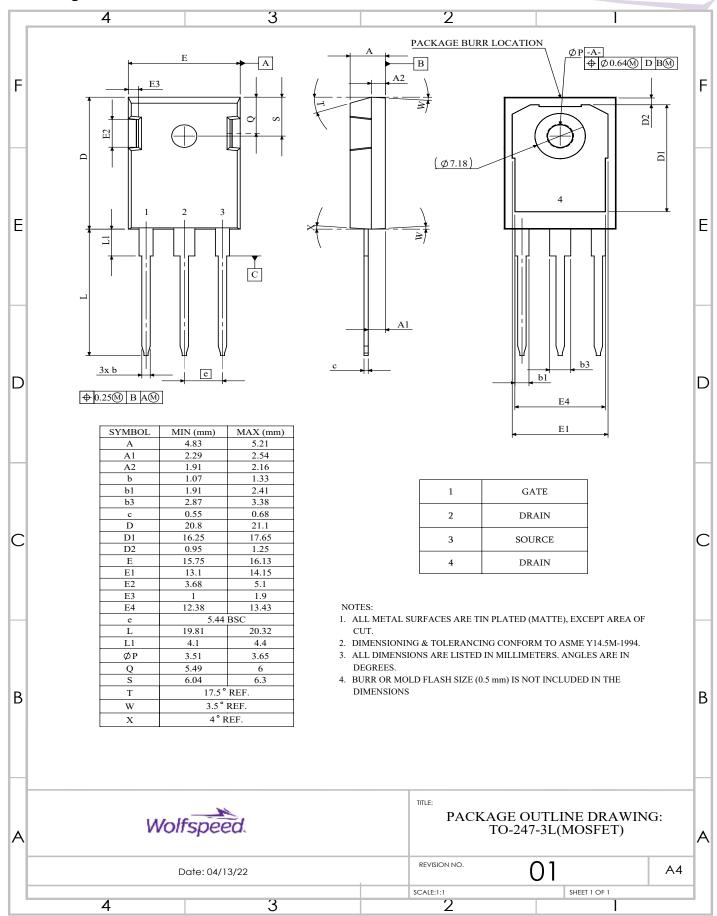
#### Note

<sup>1</sup> Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

# **ESD Rating**

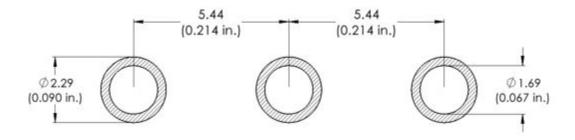
ESD Test	Total Devices Sampled	<b>Resulting Classification</b>	
ESD-HBM	All Devices Passed 1000V	3A (>2000V)	
ESD-MM	All Devices Passed 400V	C (>400V)	
ESD-CDM	All Devices Passed 1000V	IV (>=1000V)	

## Package Dimensions - TO-247-4L



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# **Recommended Solder Pad Layout**



# **Revision History**

<b>Current Revision</b>	Date of Release	Description of Changes
5	April-2021	N/A
6	November-2023	Updated Wolfspeed branding, package drawing, package image, and solder pad layout, added Revision History Table

#### **Related Links**

- <u>SPICE Models</u>: http://wolfspeed.com/power/tools-and-support
- <u>SiC MOSFET Isolated Gate Driver Reference Design</u>: http://wolfspeed.com/power/tools-and-support
- <u>SiC MOSFET Evaluation Board</u>: http://wolfspeed.com/power/tools-and-support

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The Silicon Carbide MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.

#### **RoHS Compliance**

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Documentation sections of www.wolfspeed.com.

#### **REACh Compliance**

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

#### **Contact info:**

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