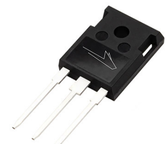
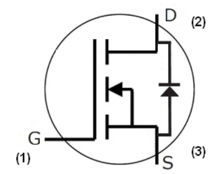
C2M0045170D

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology
N-Channel Enhancement Mode



TO-247-3L



Package Types: TO-247-3L
PN's: C2M0045170D

Wolfspeed, Inc. is in the process of rebranding its products and related materials pursuant to the entity name change from Cree, Inc. to Wolfspeed, Inc. During this transition period, products received may be marked with either the Cree name and/or logo or the Wolfspeed name and/or logo.

Features

- 2nd generation SiC MOSFET technology
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Resistant to latch-up
- Halogen free, RoHS compliant

Applications

- Solar inverters
- Switch mode power supplies
- High voltage DC/DC converters
- Motor drive
- Pulsed power applications

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency

Maximum Ratings (T_C = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Value	Unit	Test Conditions	Note
Drain - Source Voltage	V_{DSmax}	1700	V	V_{GS} = 0 V, I_D = 100 µA	
Gate - Source Voltage	V_{GSmax}	-10/+25		Absolute Maximum Values, AC (f >1 Hz)	Note: 1
Gate - Source Voltage	V_{GSop}	-5/+20		Recommended Operational Values	Note: 2
Continuous Drain Current	I_D	75	A	V_{GS} = 20 V, T_C = 25 °C	Fig. 19
		48		V_{GS} = 20 V, T_C = 100 °C	
Pulsed Drain Current	$I_{D\ (pulse)}$	160		Pulse Width t_P Limited by T_{jmax}	Fig. 22
Power Dissipation	P_D	338	W	T_C = 25 °C, T_J = 150 °C	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}	-40 to +150	°C		
Solder Temperature	T_L	260	°C	According to JEDEC J-STD-020	
Mounting Torque	M_d	1 8.8	Nm lbf-in	M3 or 6-32 Screw	

Note (1): When using MOSFET body diode V_{GSmax} = -5 V/+25 V.
Note (2): MOSFET can also safely operate at 0/+20 V.

Electrical Characteristics (T_C = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1700			V	V_{GS} = 0 V, I_D = 100 μA	
Gate Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4	V	V_{DS} = V_{GS}, I_D = 18 mA	Fig. 11
			2.5			V_{DS} = V_{GS}, I_D = 18 mA, T_J = 150 °C	
Zero Gate Voltage Drain Current	I_{DSS}		2	100	μA	V_{DS} = 1700 V, V_{GS} = 0 V	
Gate-Source Leakage Current	I_{GSS}			600	nA	V_{GS} = 20 V, V_{DS} = 0 V	
Drain-Source On-State Resistance	$R_{DS(on)}$		40	70	mΩ	V_{GS} = 20 V, I_D = 50 A	Fig. 4,5,6
			80			V_{GS} = 20 V, I_D = 50 A, T_J = 150 °C	
Transconductance	g_{fs}		24.7		S	V_{DS} = 20 V, I_{DS} = 50 A	Fig. 7
			23.4			V_{DS} = 20 V, I_{DS} = 50 A, T_J = 150 °C	
Input Capacitance	C_{iss}		3455		pF	V_{GS} = 0 V V_{DS} = 1200 V f = 1 MHz V_{AC} = 25 mV	Fig. 17,18
Output Capacitance	C_{oss}		171				
Reverse Transfer Capacitance	C_{rss}		6.7				
C_{oss} Stored Energy	E_{oss}		139		μJ		Fig. 16
Effective Output Capacitance (Energy Related)	$C_{o(er)}$		188		pF	V_{GS} = 0 V, V_{DS} = 0... 1200 V	Note: 3
Effective Output Capacitance (Time Related)	$C_{o(tr)}$		255		pF		
Turn-On Switching Energy (SiC Diode FWD)	E_{ON}		2.5		mJ	V_{DS} = 1200 V, V_{GS} = -5/20 V, I_D = 50 A, $R_{G(ext)}$ = 2.5 Ω, L = 99 μH, T_J = 150 °C, Using SiC Diode as FWD	Fig. 26, 29b Note 2
Turn Off Switching Energy (SiC Diode FWD)	E_{OFF}		1.4				
Turn-On Switching Energy (Body Diode FWD)	E_{ON}		4.9		mJ	V_{DS} = 1200 V, V_{GS} = -5/20 V, I_D = 50 A, $R_{G(ext)}$ = 2.5 Ω, L = 99 μH, T_J = 150 °C, Using MOSFET as FWD	Fig. 26, 29a Note 2
Turn Off Switching Energy (Body Diode FWD)	E_{OFF}		1.1				
Turn-On Delay Time	$t_{d(on)}$		68		ns	V_{DD} = 1200 V, V_{GS} = -5/20 V I_D = 50 A, $R_{G(ext)}$ = 2.5 Ω, Timing Relative to V_{DS} Inductive Load	Fig. 27, 29 Note 2
Rise Time	t_r		19				
Turn-Off Delay Time	$t_{d(off)}$		35				
Fall Time	t_f		19				
Internal Gate Resistance	$R_{G(int)}$		1.3		Ω	f = 1 MHz, V_{AC} = 25 mV	
Gate to Source Charge	Q_{gs}		43		nC	V_{DS} = 1200 V, V_{GS} = -5/20 V I_D = 50 A Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}		74				
Total Gate Charge	Q_g		200				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as coss while V_{DS} is rising from 0 to 1200 V.
$C_{o(tr)}$, a lumped capacitance that gives same charging time as coss while V_{DS} is rising from 0 to 1200 V.

Reverse Diode Characteristics

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	V_{SD}	3.8		V	V_{GS} = -5 V, I_{SD} = 25 A	Fig. 8, 9, 10 Note 1
		3.4			V_{GS} = -5 V, I_{SD} = 25 A, T_J = 150 °C	
Continuous Diode Forward Current	I_S		76	A	V_{GS} = -5 V, T_C = 25 °C	Note 1
Diode Pulse Current	$I_{S, pulse}$		160		V_{GS} = -5 V, Pulse Width t_P Limited by T_{jmax}	Note 1
Reverse Recovery Time	t_{rr}	53		ns	V_{GS} = -5 V, I_{SD} = 50 A , V_R = 1200 V dif/dt = 1000 A/µs, T_J = 150 °C	
Reverse Recovery Charge	Q_{rr}	461		nC		
Peak Reverse Recovery Current	I_{rrm}	14		A		
Reverse Recovery Time	t_{rr}	40		ns	V_{GS} = -5 V, I_{SD} = 50 A , V_R = 1200 V dif/dt = 3040 A/µs, T_J = 150 °C	
Reverse Recovery Charge	Q_{rr}	481		nC		
Peak Reverse Recovery Current	I_{rrm}	22		A		

Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.25	0.37	°C/W		Fig. 21
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$		40			

Typical Performance

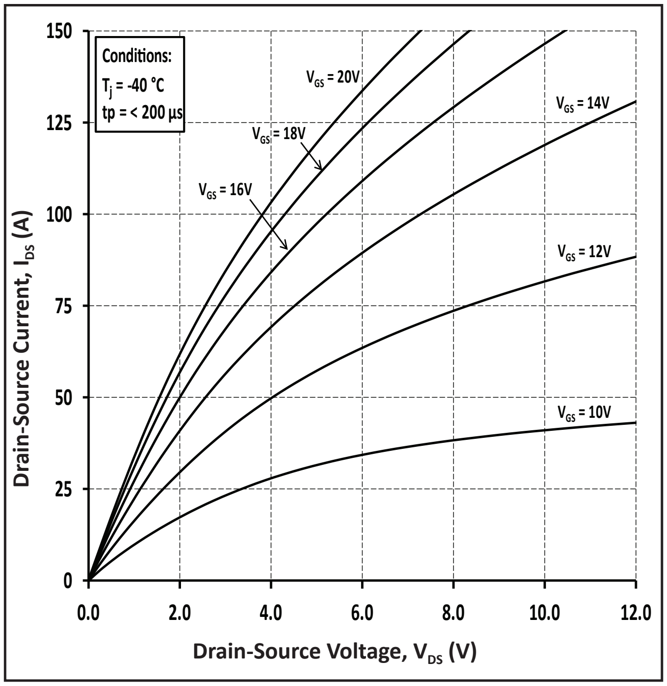


Figure 1. Output Characteristics T_J = -40 °C

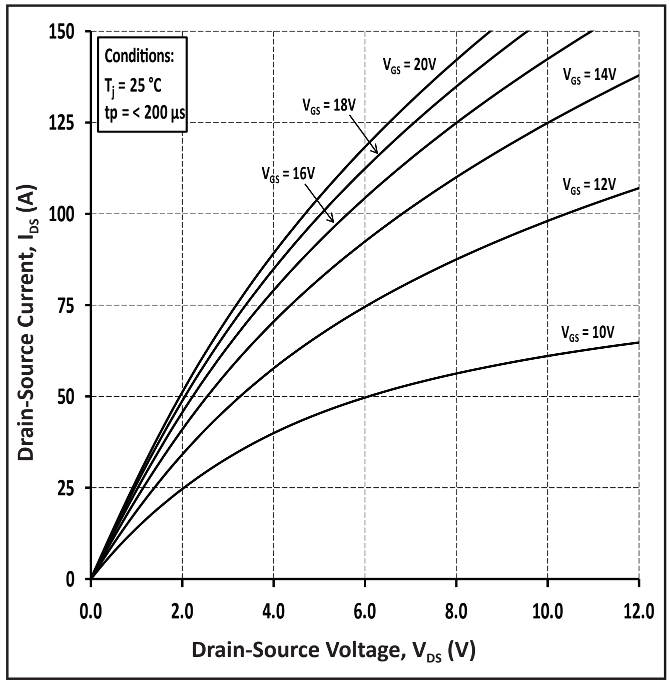


Figure 2. Output Characteristics T_J = 25 °C

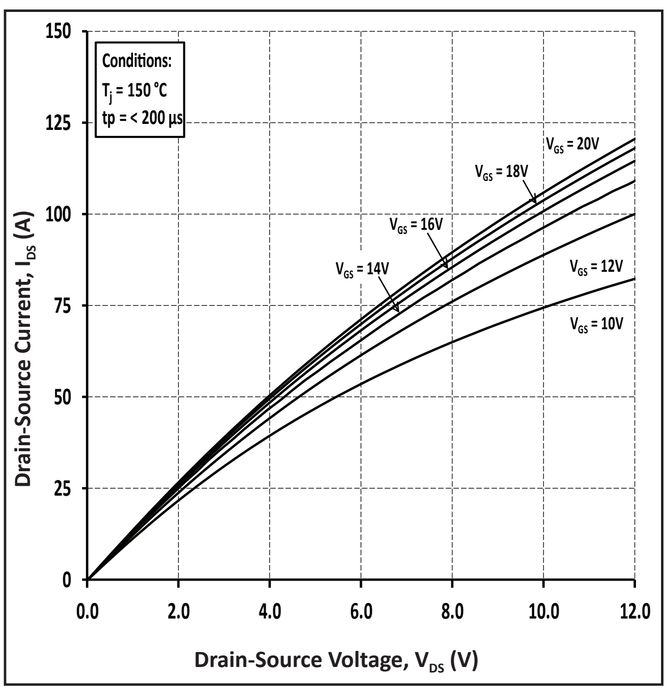


Figure 3. Output Characteristics T_J = 150 °C

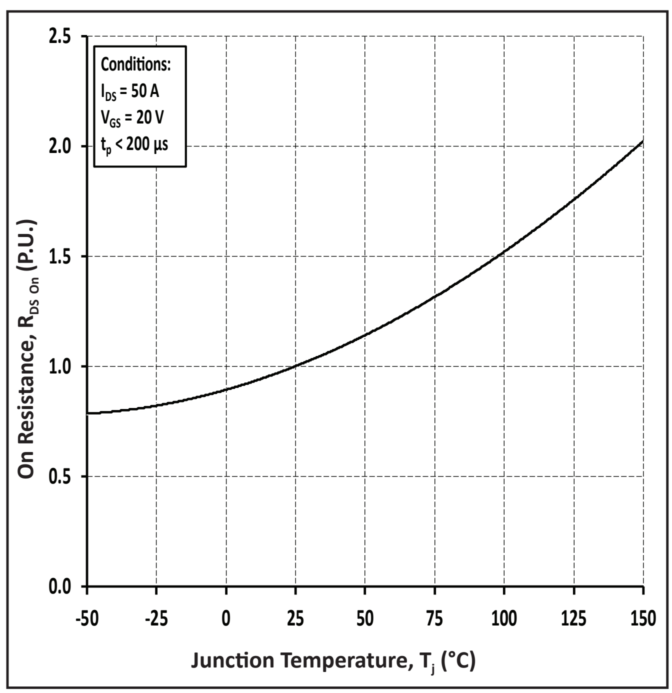


Figure 4. Normalized On-Resistance vs Temperature

Typical Performance

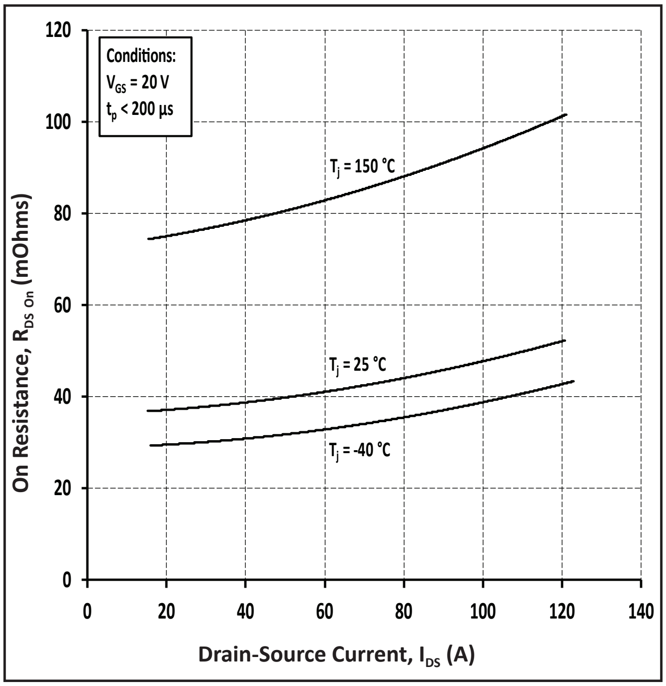


Figure 5. On-Resistance vs Drain Current for Various Temperatures

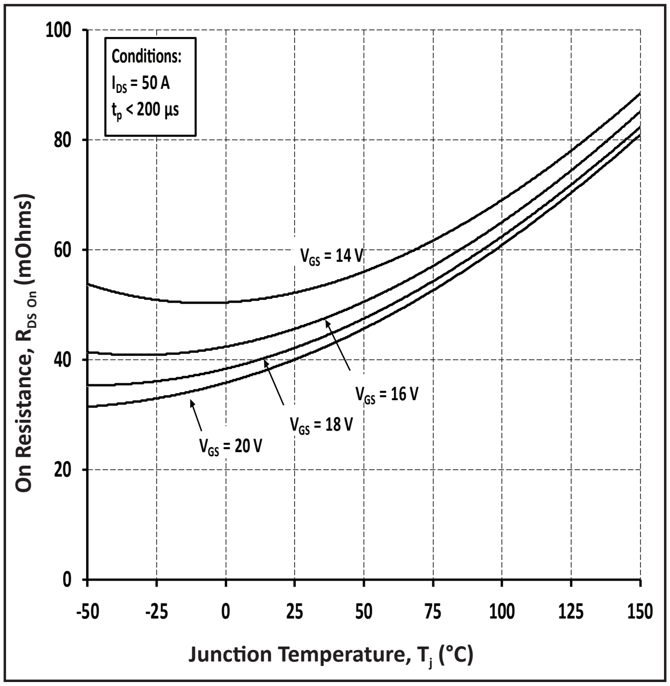


Figure 6. On-Resistance vs Temperature for Various Gate Voltage

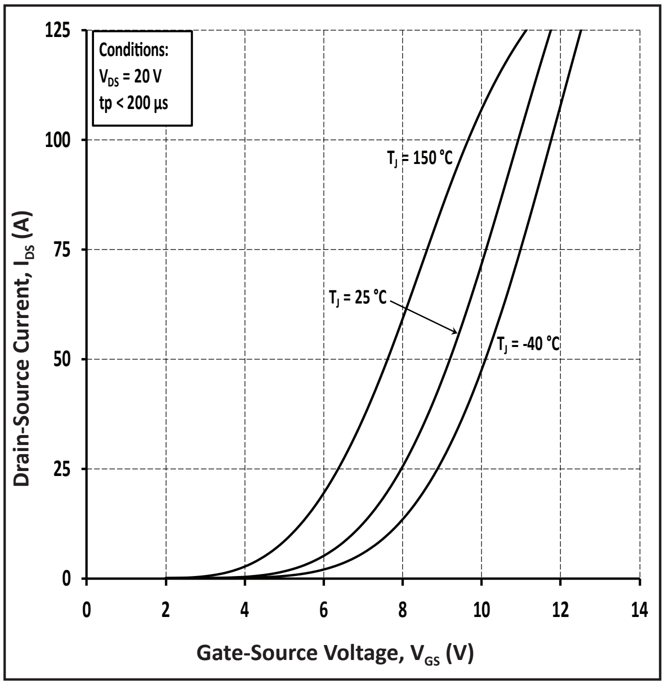


Figure 7. Transfer Characteristic for Various Junction Temperatures

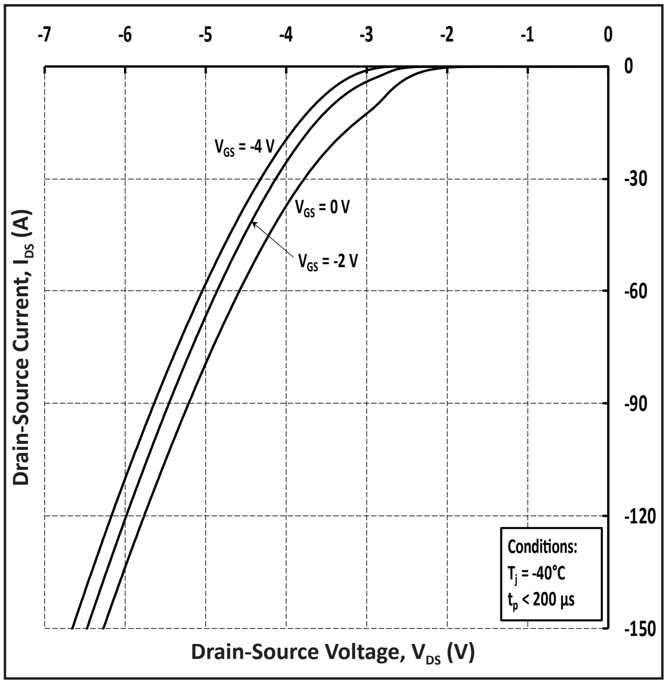


Figure 8. Body Diode Characteristic at -40 °C

Typical Performance

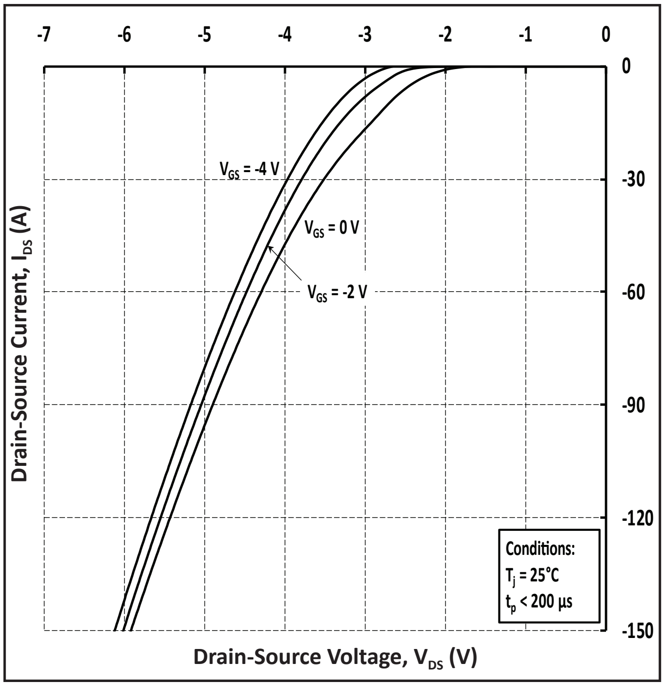


Figure 9. Body Diode Characteristic at 25 °C

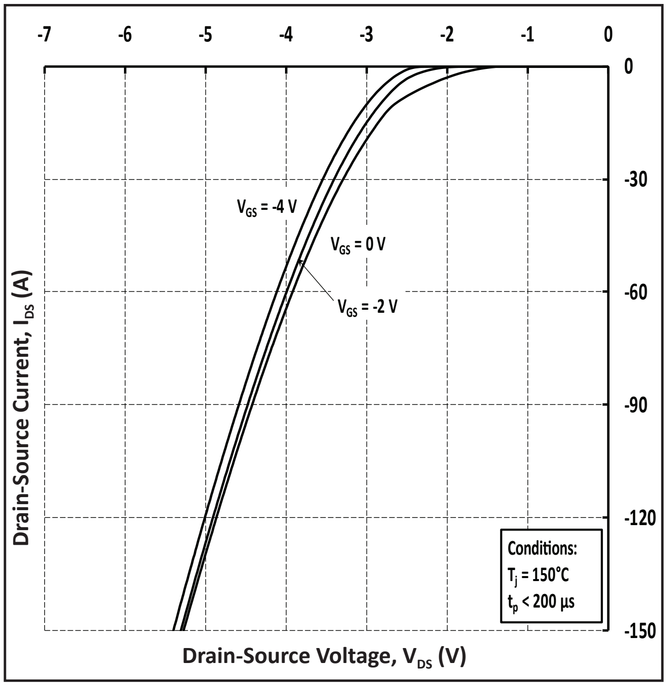


Figure 10. Body Diode Characteristic at 150 °C

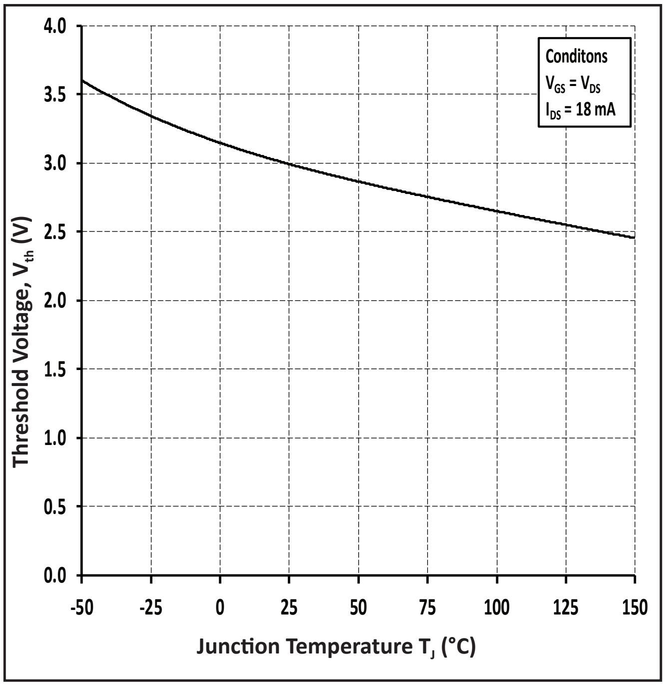


Figure 11. Threshold Voltage vs Temperature

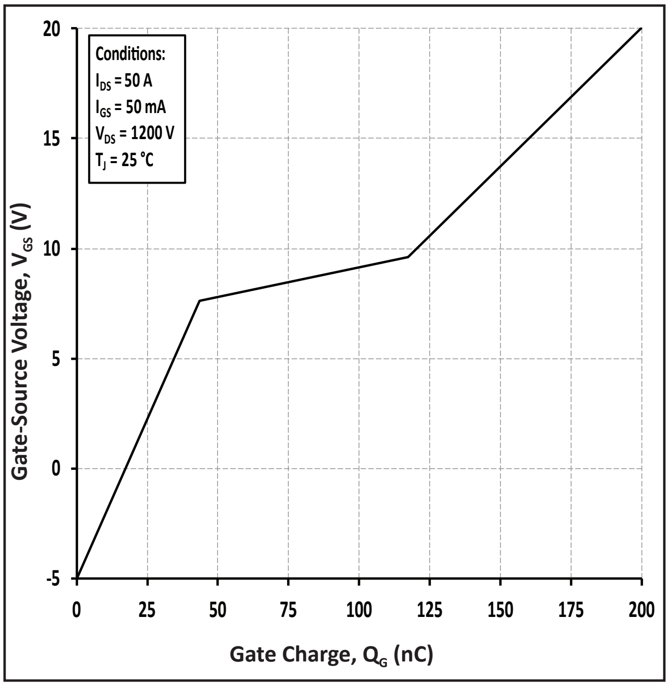


Figure 12. Gate Charge Characteristic

Typical Performance

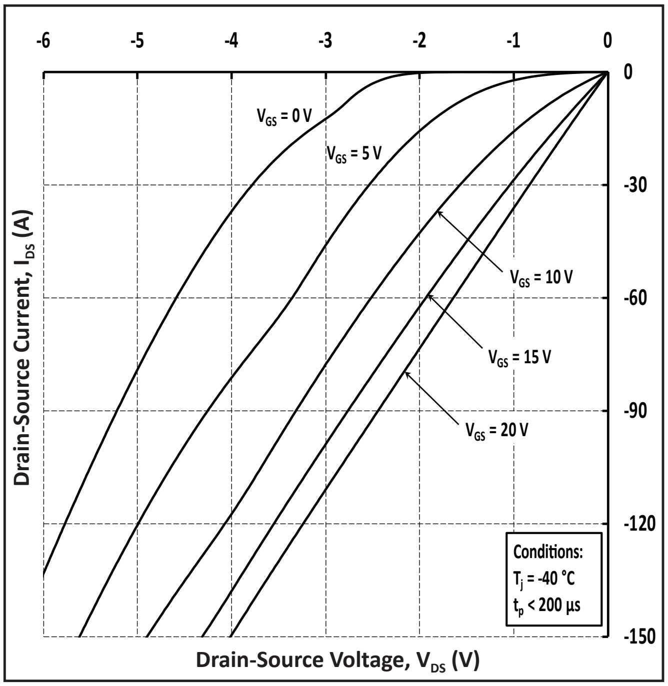


Figure 13. 3rd Quadrant Characteristic at -40 °C

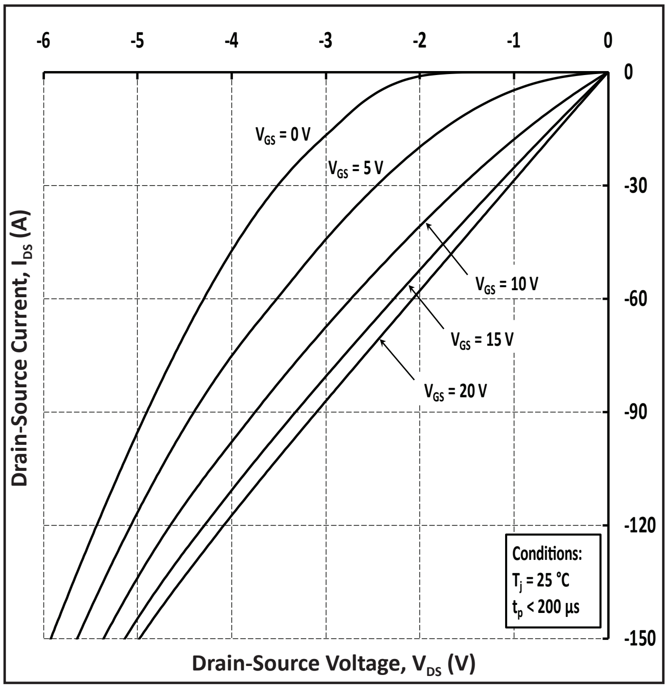


Figure 14. 3rd Quadrant Characteristic at 25 °C

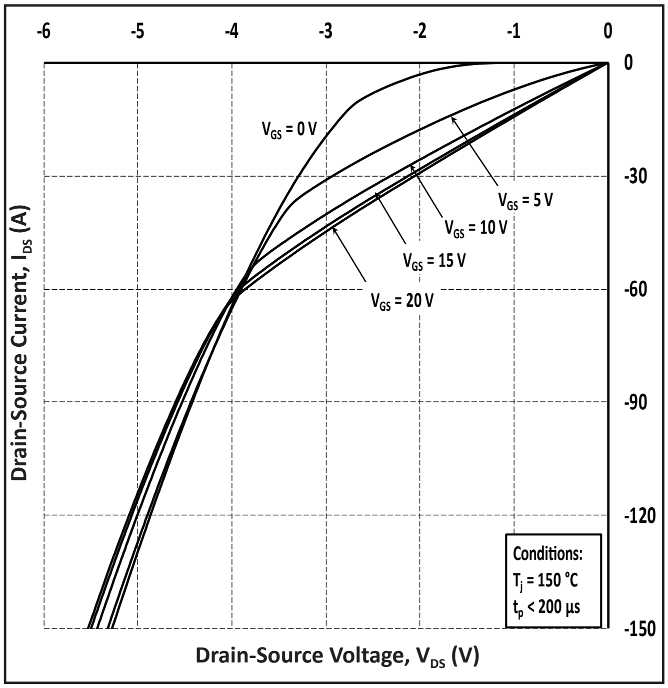


Figure 15. 3rd Quadrant Characteristic at 150 °C

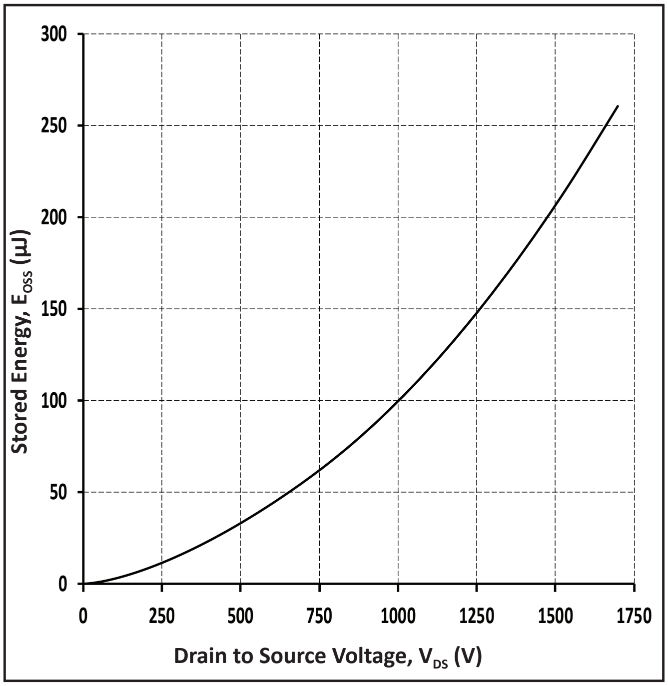


Figure 16. Output Capacitor Stored Energy

Typical Performance

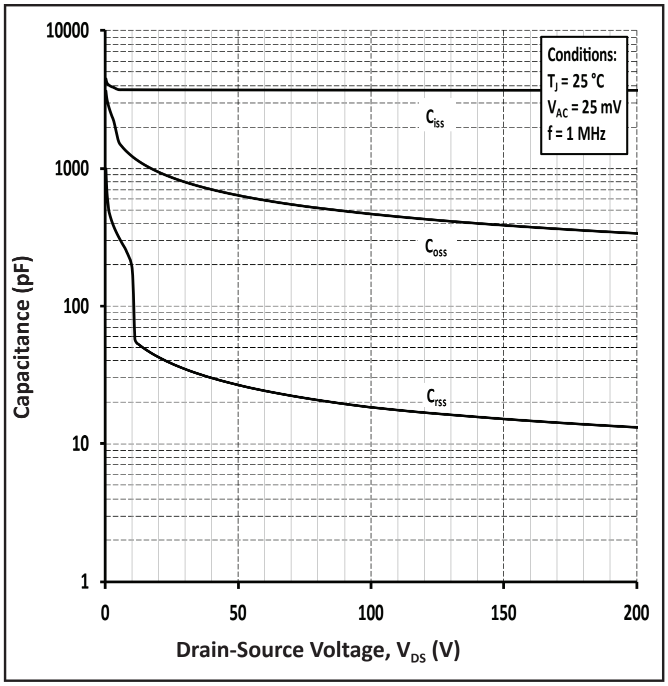


Figure 17. Capacitances vs Drain-Source Voltage (0-200 V)

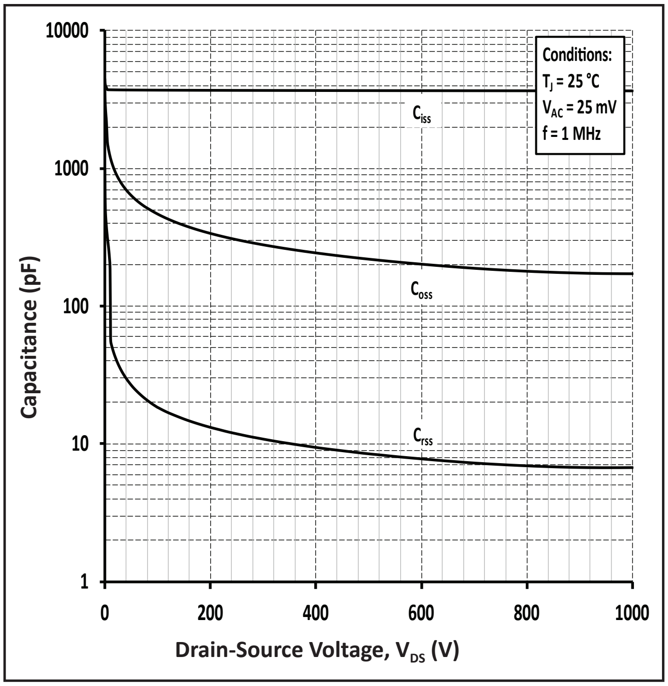


Figure 18. Capacitances vs Drain-Source Voltage (0-1000 V)

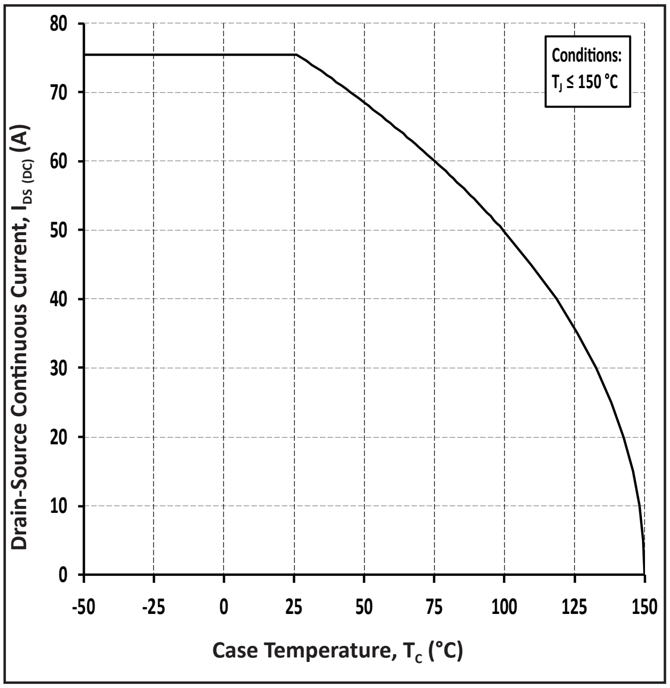


Figure 19. Continuous Drain Current Derating vs Case Temperature

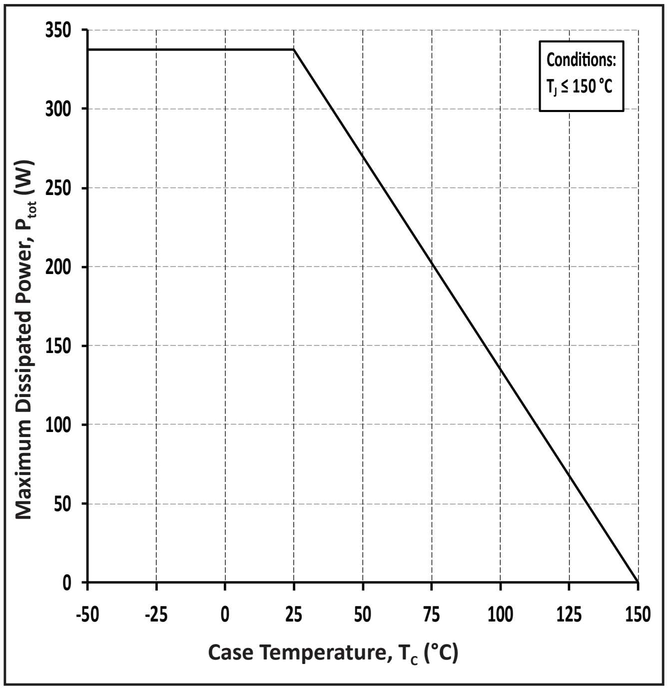


Figure 20. Maximum Power Dissipation Derating vs Case Temperature

Typical Performance

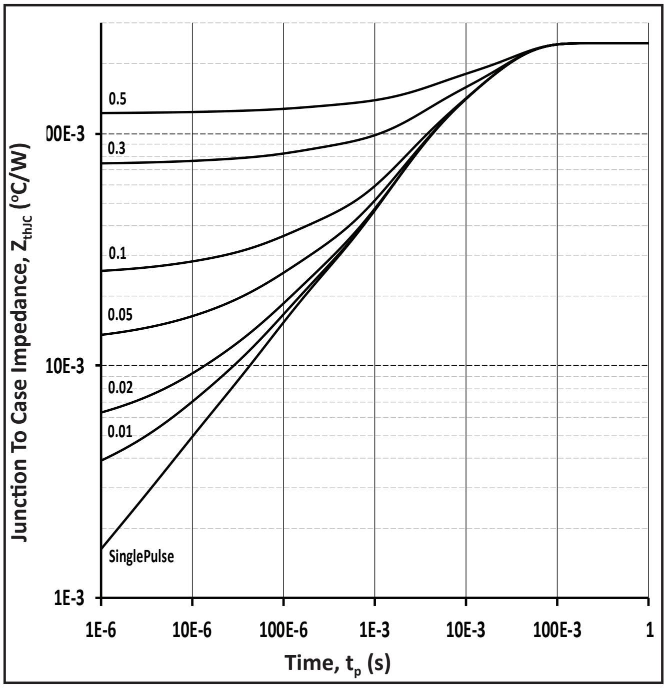


Figure 21. Transient Thermal Impedance (Junction - Case)

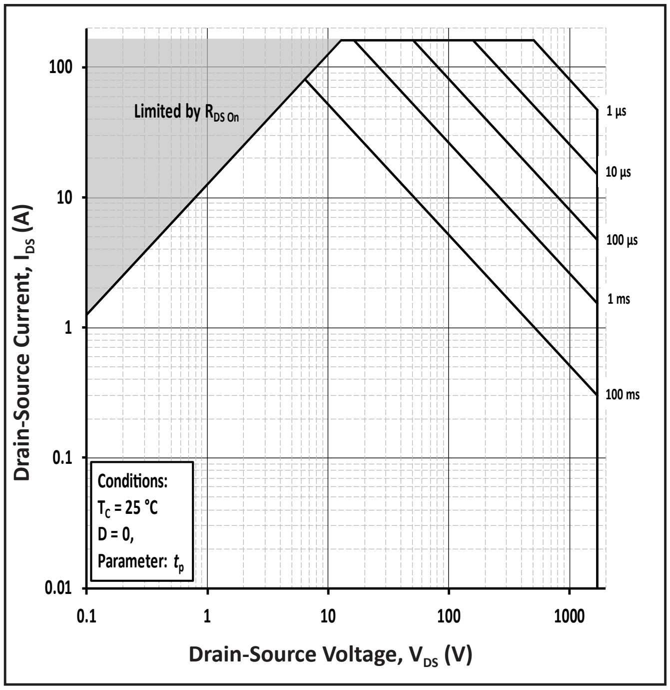


Figure 22. Safe Operating Area

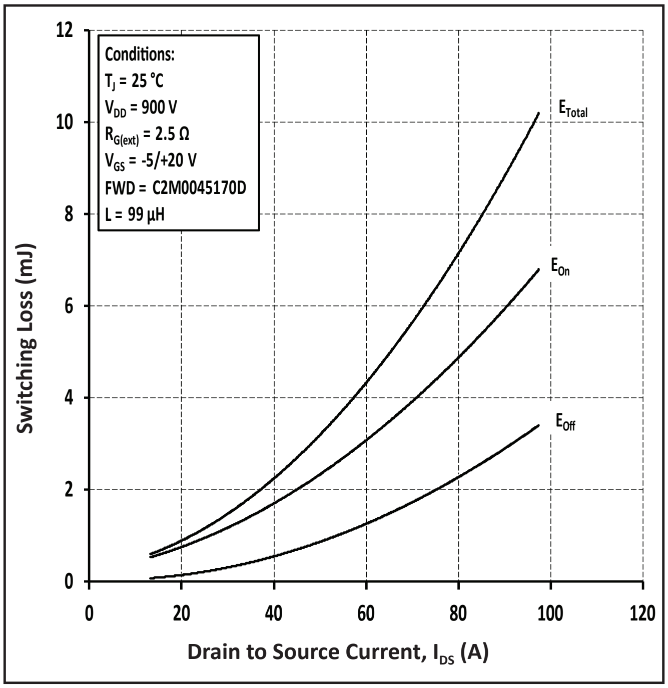


Figure 23. Clamped Inductive Switching Energy vs Drain Current (V_{DD} = 900 V)

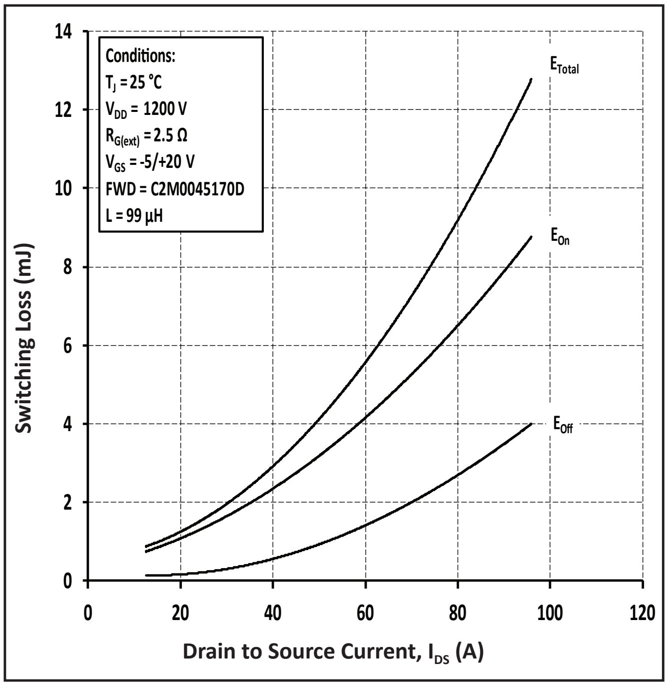


Figure 24. Clamped Inductive Switching Energy vs Drain Current (V_{DD} = 1200 V)

Typical Performance

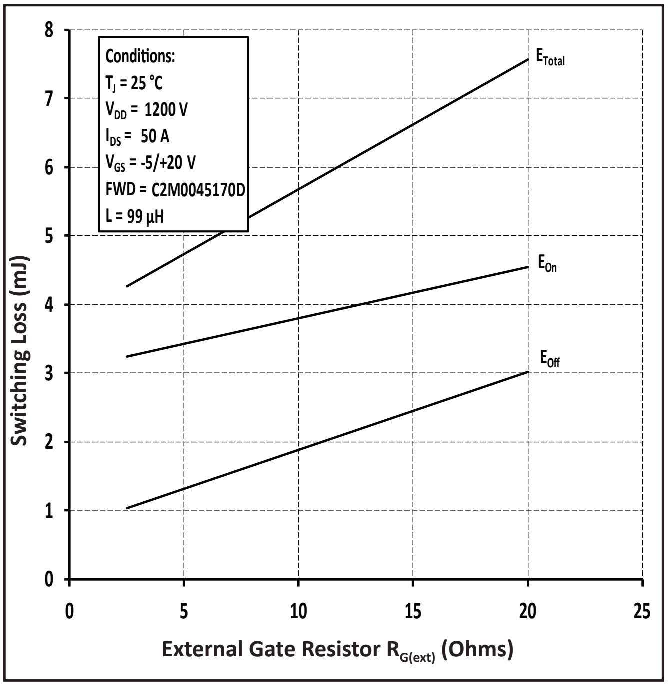


Figure 25. Clamped Inductive Switching Energy vs $R_{G(ext)}$

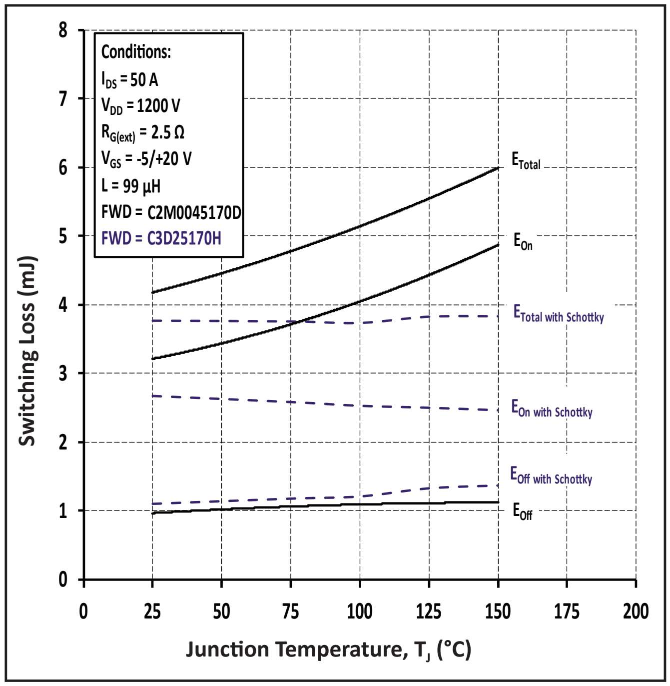


Figure 26. Clamped Inductive Switching Energy vs Temperature

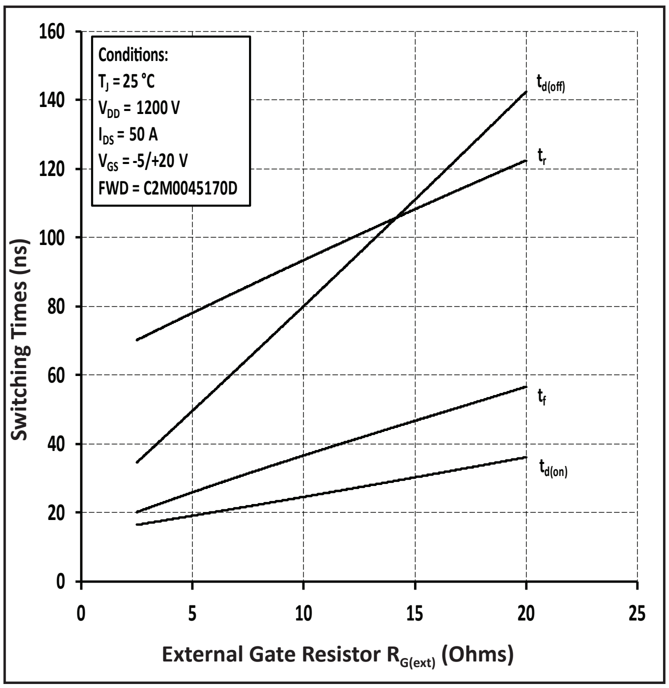


Figure 27. Switching Times vs $R_{G(ext)}$

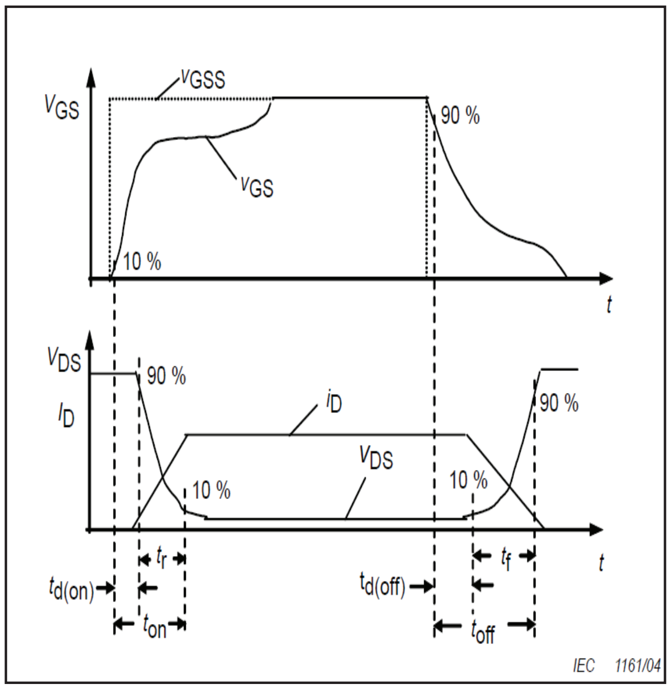


Figure 28. Switching Times Definition

Test Circuit Schematic

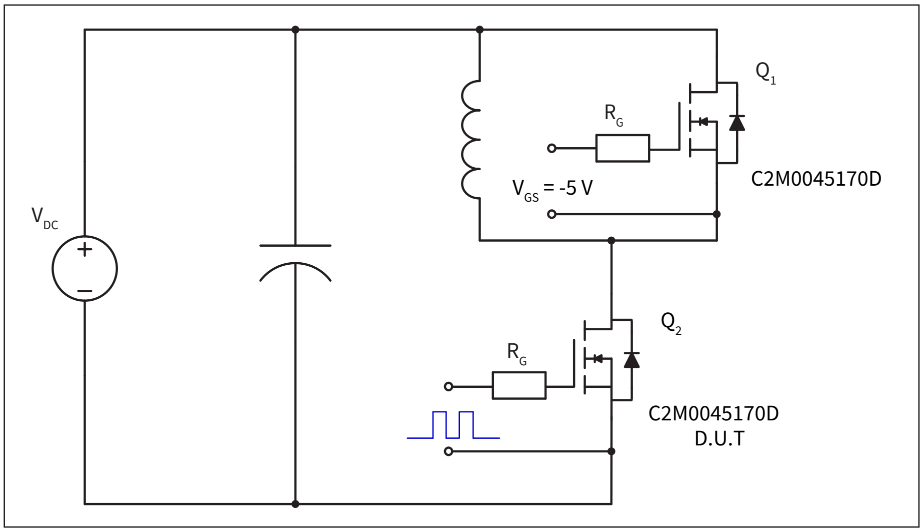


Figure 29a. Clamped Inductive Switching Test Circuit Using MOSFET Intristic Body Diode

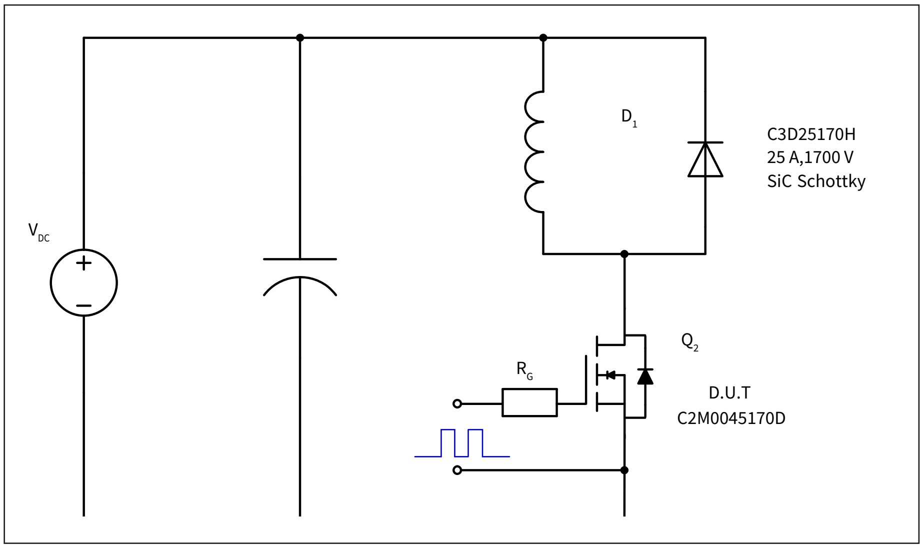
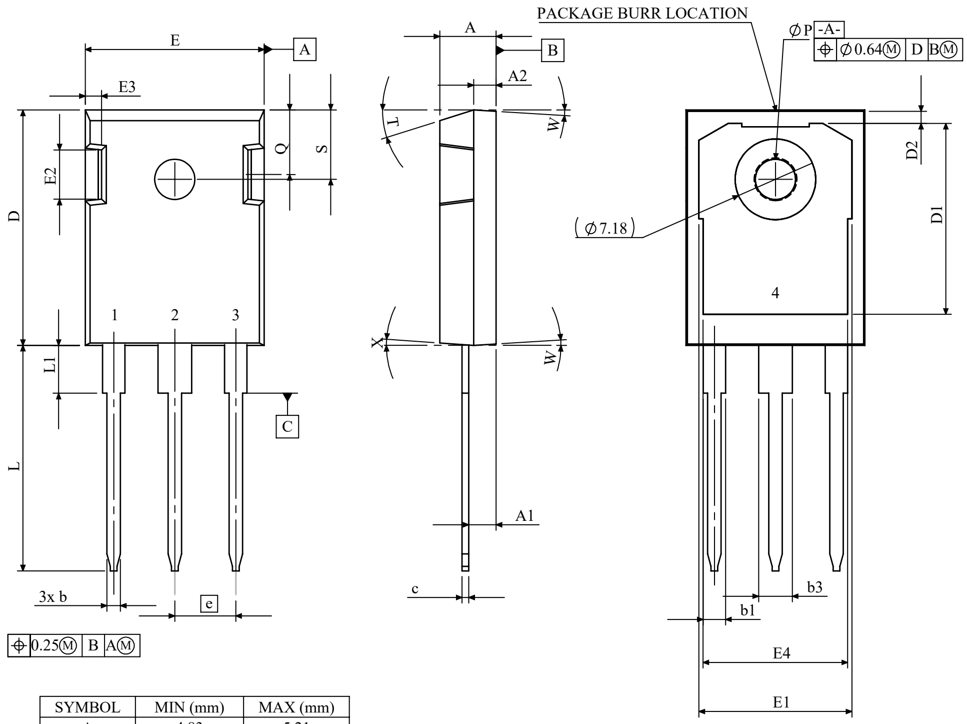


Figure 29b. Clamped Inductive Switching Test Circuit Using SiC Schottky Diode

Package Dimensions

Package: TO-247-3L



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b	1.07	1.33
b1	1.91	2.41
b3	2.87	3.38
c	0.55	0.68
D	20.8	21.1
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13
E1	13.1	14.15
E2	3.68	5.1
E3	1	1.9
E4	12.38	13.43
e	5.44 BSC	
L	19.81	20.32
L1	4.1	4.4
ØP	3.51	3.65
Q	5.49	6
S	6.04	6.3
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	GATE
2	DRAIN
3	SOURCE
4	DRAIN

NOTES:

1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

TITLE:

PACKAGE OUTLINE DRAWING:
TO-247-3L(MOSFET)

Date: 04/13/22

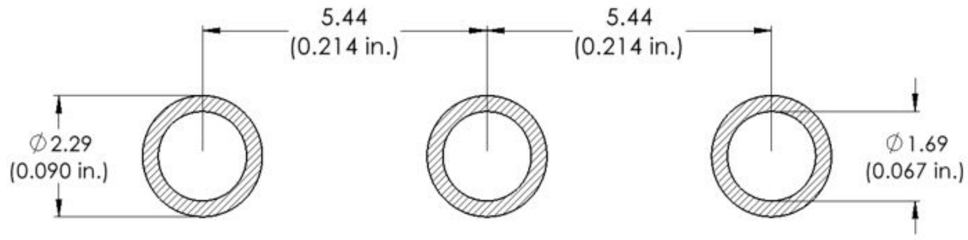
REVISION NO. 01

A4

SCALE:1:1

SHEET 1 OF 1

Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
1	May-2022	Initial Release
2	November-2023	Updated Wolfspeed branding, package drawing, and solder pad layout

Notes & Disclaimer

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RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Documentation sections of www.wolfspeed.com.

REACh Compliance

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

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www.wolfspeed.com/power

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