User Guide **PRD-07913**

Wolfspeed Power Module SPICE Models User Guide

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Models provided by Wolfspeed are not warranted by Wolfspeed as fully representing all specifications and operating characteristics of the semiconductor product to which the model relates. The model describes the characteristics of a typical device. **In all cases, the current data sheet information for a given device is the final design guideline and the only actual performance specification.** Although models can be a useful tool in evaluating device performance, they cannot predict exact device performance under all conditions, nor are they intended to replace hardware testing for final verification. The model is subject to change without notice. Wolfspeed is not responsible for any errors or simulation issues.

Contents

1. Introduction

Circuit-level simulation software are powerful tools for optimizing systems that utilize Wolfspeed's SiC power module devices. These tools can be used to predict detailed transient behavior of these devices in their systems to estimate voltage overshoots, efficiency, emissions, expected junction temperatures, and more. Leveraging SPICE models can assist designers in improving their system layout to take full advantage of the capabilities of Wolfspeed power modules. These models can reduce time and cost through virtual prototyping studies that inform hardware decisions or facilitate optimization. Suitable models can be used to predict the influence of parasitic elements and EMI behavior, as well as predict device failures due to destructive voltage overshoots or thermal stress.

1.1 Software Recommendations

The power module SPICE models described herein are developed for and in LTspice, electronic circuit simulation software by Analog Devices, Inc. For best results, please download the latest version of LTspice from https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html. Using these models in older LTspice versions or other SPICE simulation tools may result in convergence or accuracy errors. However, the models are intended to be compatible with SPICE2 syntax. Please report module-model specific simulation errors with details to our forum at https://forum.wolfspeed.com/.

Using these models in other SPICE simulation tools may result in convergence errors. Please use LTspice if possible.

1.2 Content Overview

The Wolfspeed power module SPICE model library encompasses current-generation parts available for purchase. Previous models, such as gen2 devices (CAS120M12BM2, CAS300M17BM2, etc.) are not included. There are two model types provided for every device: an LTspice library file, and an individual SPICE2 file. The LTspice library files combine all of the module types (half-bridge, six-pack) into a single .lib file, and also includes optimizations and customizability to change the model to suit the needs of users. The individual SPICE2 files only include a single module model in each .cir file, with limited customizability. However, the syntax is intended to be general and importable into other SPICE software. Inside each folder, example circuits and the recommended symbol for each part is provided for LTspice. It is the user's responsibility to generate symbols and example circuits for other SPICE software.

1.3 Quick Model Installation Guide

The organization of the files is up to the user's discretion. A recommended approach is to create a specific folder for the Wolfspeed LTspice models and add it to your LTspice search path. This method allows for all simulations to use the same model files and omits the need for .inc/.lib statements inside the simulation. It is highly recommended to avoid copy-and-pasting the library file into multiple locations.

1.3.1 LTspice Library Installation

1. Go to https://www.wolfspeed.com/tools-and-support/power/ltspice-and-plecs-models/
2. Download the 'All SPICE Models.zip' file
3. Unzip the downloaded file and navigate to the "\Modules\LTspice\Models\" folder
4. Create a folder to store the WS model files. For example, 'C:\Users\ExampleUser\WS_LTspice_Library\'
5. Copy the .asy and .lib files into your desired directory.
6. Open LTspice and go to Tools -> Control Panel -> Sym. & Lib. Search Paths. Enter your desired directory into both the symbol and library search paths (see Figure 1).

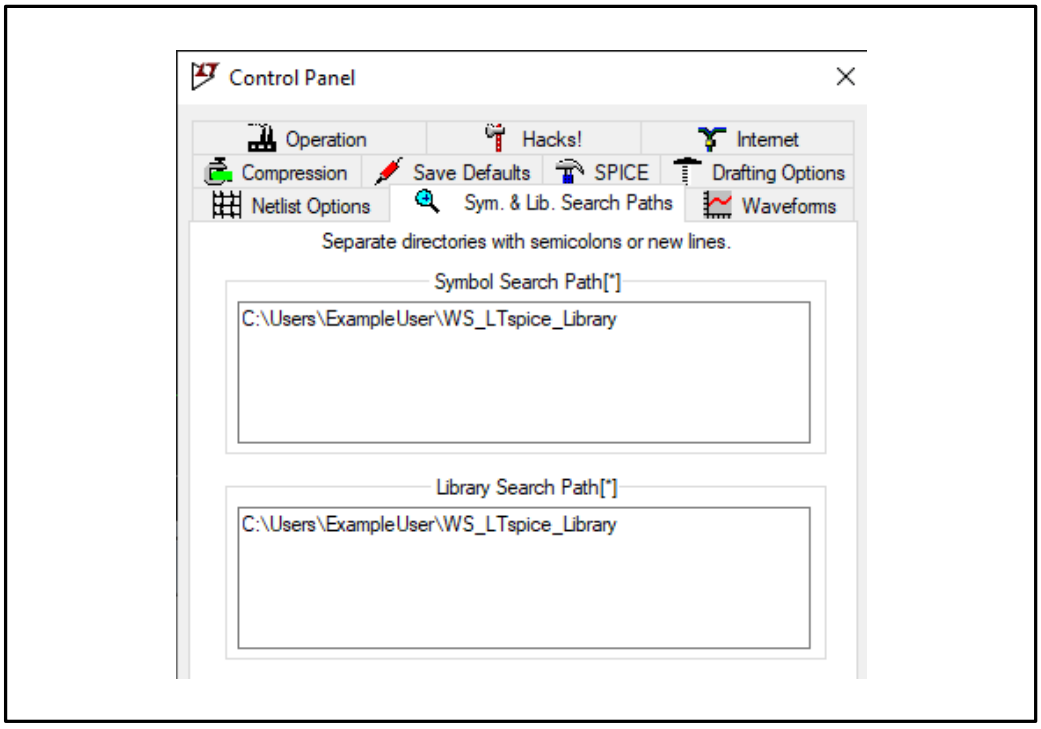

Figure 1: LTspice symbol and library search path screenshot

7. You may need to restart LTspice for these changes to take effect. Once completed, the symbol can be placed into any circuit by changing the drop-down arrow on the component symbol selection screen (see Figure 2).

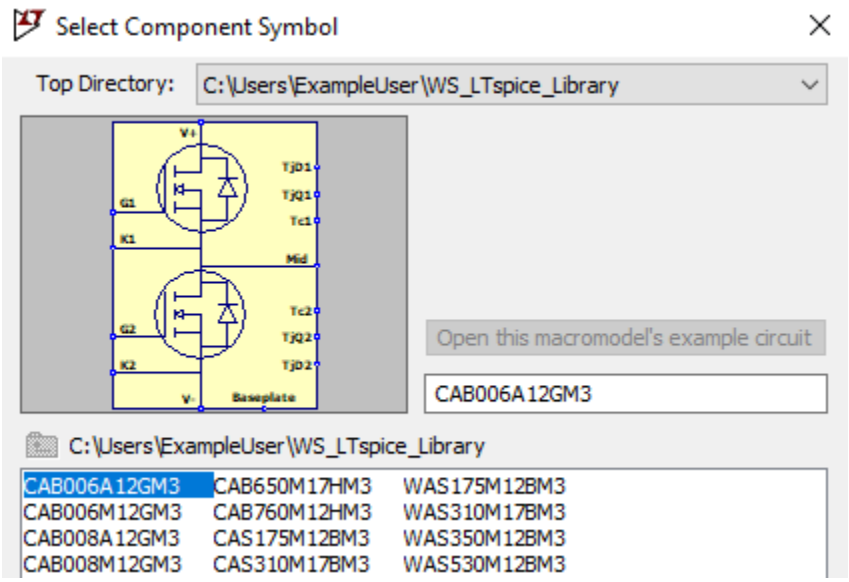

Figure 2: LTspice select component symbol screenshot

8. Once the part is placed in your simulation, right-click the symbol and change the Value field to your desired module part number (see Figure 3). Open the .lib file in a text editor to view the available models in the library.

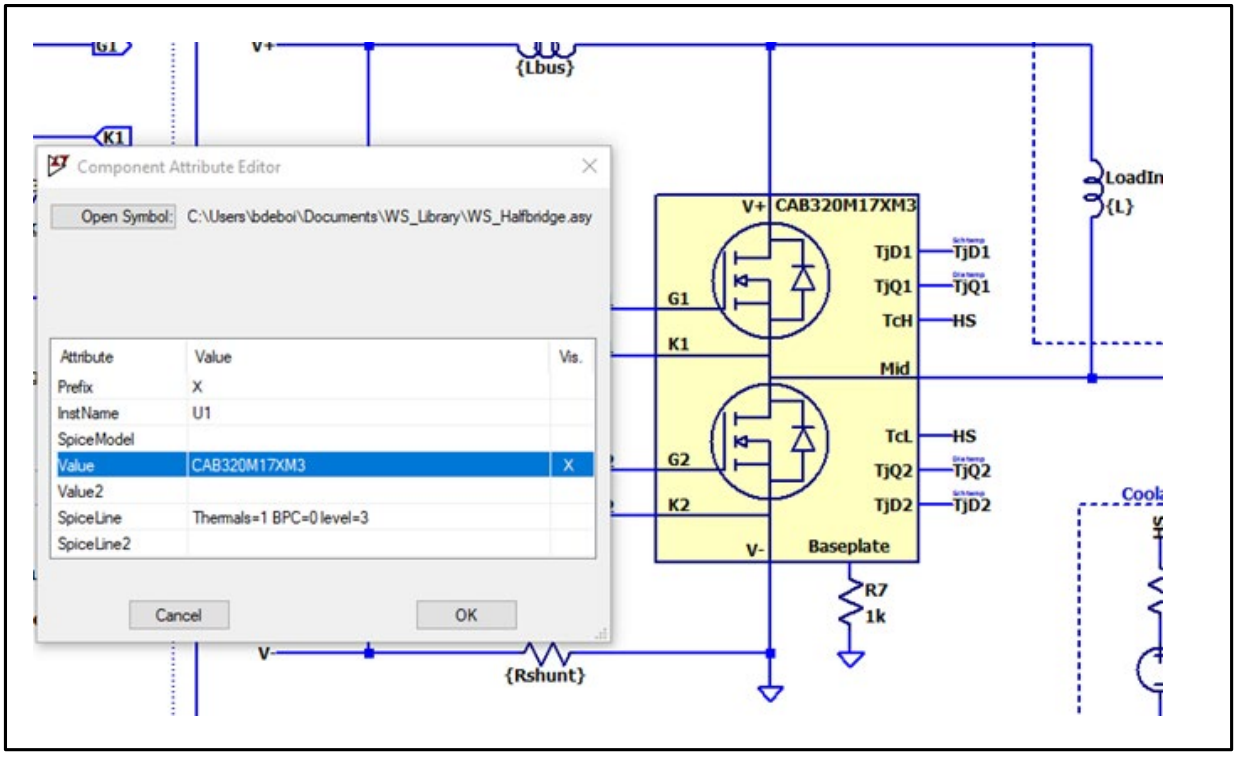

Figure 3: LTspice changing library model example

1.3.2 Simetrix Installation

To install the model library in Simetrix, navigate to 'All SPICE Models/Modules/Simetrix' and drag the 'Wolfspeed_Module_Library.cir' and 'Wolfspeed_Module_Symbols.sxslb' files into the command shell in Simetrix. The software will ask if you wish to install or edit the model file and symbol file (see Figure 4). Check 'Install' and click OK for both.

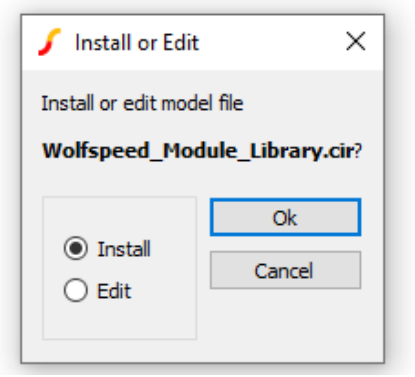

Figure 4: Model installation box on Simetrix

After installing, the installed module models will be available under 'Dual Schottky' and 'MOSFETs – Multiple' in the Simetrix model library (see Figure 5). Example circuits are available in the 'Example Circuits' folder to get started with the Simetrix SPICE models.

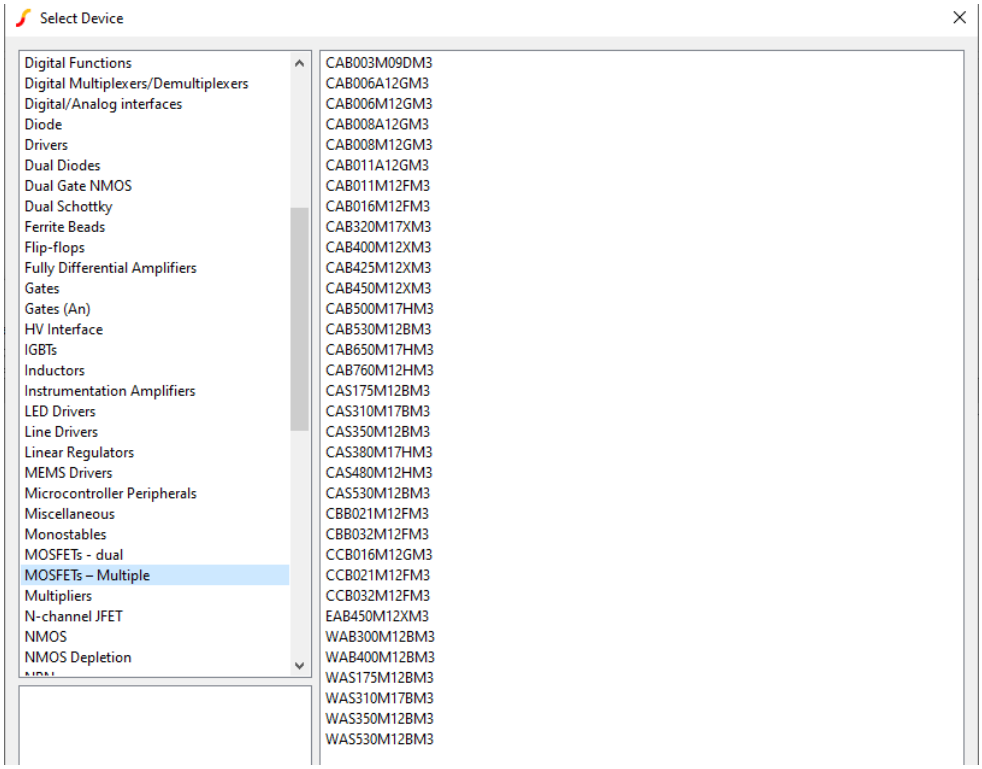

Figure 5: Wolfspeed model library in Simetrix

1.3.3 Installation for all other software

Wolfspeed SPICE models were designed and validated for use with LTspice. Alternative software syntax is supported, but the simulation files are not guaranteed to be correct. Example simulation files, symbols, and instructions for installation may not be provided.

1. Go to https://www.wolfspeed.com/tools-and-support/power/ltspice-and-plecs-models/
2. Download the 'All SPICE Models.zip' file
3. Unzip the downloaded file and navigate to the "\Modules\" folder
4. Navigate to your desired software folder
5. A .cir or .txt file will be provided for each device model. Import the contents of the file into your desired software.

1.4 Verification of model installation

To verify that the model was installed correctly, example circuits are provided. These vary from double pulse test circuits to more complex inverters. The example circuits (for LTspice only) are located under *Modules\LTspice\Example Circuits*.

It is recommended to begin with the double pulse test simulation file that is provided for every toplogy. This is an LTspice simulation for an ideal clamped inductive load (CIL) test sequence and does not reflect an empirical test configuration. Figure 6 below shows an example screenshot of the DPT_Test_Stand_HB.asc circuit located in *'\Modules\LTspice\Example Circuits\HalfBridge'*. The circuit may look different depending on the module topology. By default, these simulations do not contain the model symbols. An annotated space is provided to place your desired model using the 'add component' button in LTspice.

Several parameters can be edited in the simulation. Parameters *L* and *ChargePulseTime* can be edited to change the load current of the simulation, and *Vbus* can be edited to change the operating voltage. *Von*, *Voff*, and *Rg* change the gate drive settings of the simulation. *Lbus* changes the system-level parasitic inductance of the DC-link interface with the module. Finally, *TEMP* sets the global temperature of the simulation. This temperature is used to set the initial junction temperature of the device. The current I(Rlow) voltage V(mid) will provide typical double pulse testing (DPT) waveforms, shown in Figure 7.

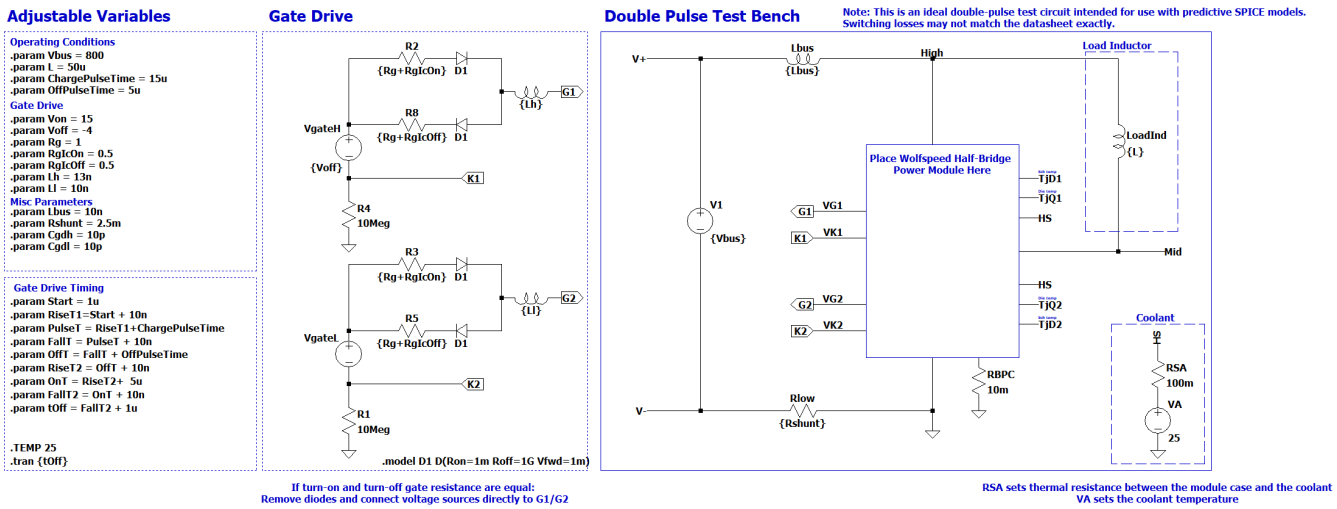

Figure 6: Example DPT_Test_Stand_HB.asc circuit for a half-bridge topology

It is critical to understand that the ideal CIL test circuit may not result in dynamic characteristics that exactly match the datasheet. SiC MOSFET devices are complex, and accurate predictions at any arbitrary bus voltage, load current, temperature, and gate resistance are challenging. In addition, non-idealities in the gate driver and CIL circuit board may not be modeled in the LTspice circuit. Critical parameters include the bus inductance, parasitic capacitance between the gate and drain of each switch position, parasitic capacitance of the load inductor, parasitic capacitance between V+ and V-, and parasitic resistance of the gate drive.

An ideal CIL test circuit may not provide switching loss and slew rate that match the datasheet due to unmodeled circuit parasitics

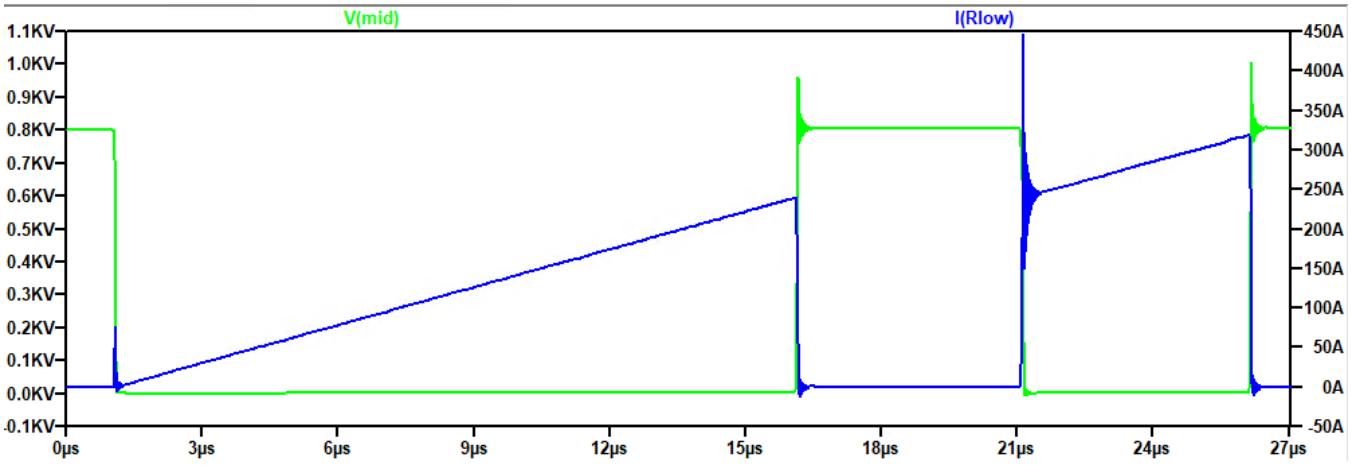

Figure 7: Example waveform from DPT_Test_Stand_HB.asc

2. Using the Model

Wolfspeed power module SPICE models feature optimizations that allow them to be tailored to particular applications. For example, long-duration simulations with a focus on control optimization may not need the influence of parasitic inductance or baseplate capacitance, and a simulation using the body diode for reverse conduction may not need the complexity of third-quadrant conduction. In this section, recommendations for implementing the power module SPICE models in LTspice will be provided, along with the various customization options.

It should be noted that a power module switch position is often comprised of several die in parallel. However, physically representing each individual die is computationally expensive and makes simulating complex circuits difficult and slow. Thus, Wolfspeed power module models leverage a scaled approach, where the behavior of the parallel die and diodes are each lumped into a single switching model, as shown in Figure 8. As such, the module models represent an averaged behavior of the paralleled die in both electrical and thermal characteristics. Throughout this document, discussion of a MOSFET temperature, connection, or characteristic refers to the entire switch position and paralleled die.

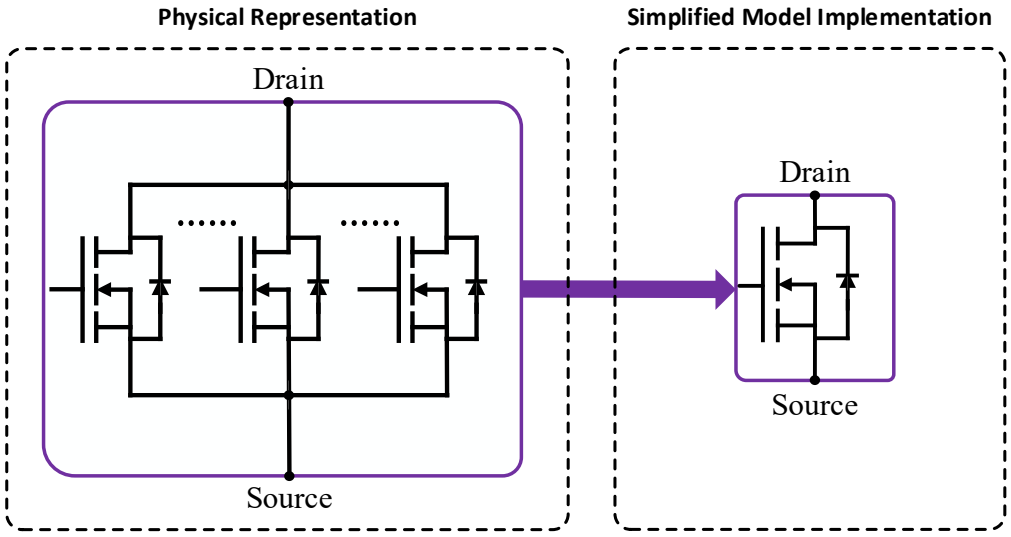

Figure 8: Scaled die model approach

2.1 Symbol Pin Descriptions / Connections

The naming convention for pins is consistent across package topologies; in this section, the half-bridge power module will be used as a representative example. Figure 9 shows the provided LTspice symbol for the half-bridge library models. The library models include all of the potential pins, but some may be disabled internally depending on the model being evaluated.

The electrical pins (V+, Mid, V-, G1/K1, and G2/K2) should be connected to the main electrical circuit. These pins are consistent with module datasheet nomenclature. G1/K1 control switch position 1, and G2/K2 control switch position 2 (such that Gn/Kn control any switch position n).

The case thermal pins are denoted 'Tcn' where n is the number of the switch position. For example, in Figure 9, Tc1 is the case port for the high-side switch, and Tc2 is the case port for the low-side switch. The case port is the

path for thermal energy / power loss for all parallel MOSFETs and diodes present in each switch position. In most cases, the Tc pins can be connected together, as the baseplate is common for all switch positions in a module. However, they are left unconnected internally to allow for studies involving asymmetric cooling. These pins are attached to ground internally with a 10 kΩ resistor and can be left floating. These pins can be connected to a coolant by applying a voltage source in series with a resistance to the pin. The voltage of the voltage source represents the coolant temperature, and the resistance represents the thermal impedance between the coolant and the baseplate of the module. Figure 6 shows an example of a heatsink connection. More complex thermal models of the thermal management system (e.g., Cauer networks) can also be implemented. The initial temperature of the Tc pins and all intermediate nodes are initialized to the global LTspice temperature parameter, 'TEMP'.

The MOSFET junction temperature pins are denoted 'TjQn' where n is the number of the switch position. These pins are intended as measurement ports and are typically left open. During operation, interactions between the die self-heating and the baseplate/coolant will cause the temperature of the die to change, which can be observed by measuring the voltage of TjQn to ground. A voltage source referenced to ground can also be applied to these pins to force a static temperature during simulation. This is particularly useful during DC simulations, where the electro-thermal model does not behave appropriately.

The Schottky diode junction temperature pins are denoted 'TjDn' where n is the number of the switch position. These pins behave identically to the MOSFET junction temperature pins. As will be discussed later, these pins become inactive when applied to a module that does not have Schottky diodes.

The Baseplate pin is an electrical connection for electromagnetic interference (EMI) simulations. It is disabled by default. Power modules contain parasitic capacitance between the electrical modules and the baseplate that provide a path for common-mode leakage currents to flow through the system. Including these parameters can be critical for users interested in estimating the EMI impact of the power modules on their system. This pin should be connected to ground with a resistor in series. The value of this resistance will depend on the system but is typically small.

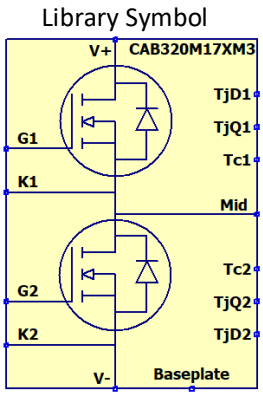

Figure 9: Half-bridge LTspice library symbol

Figure 10 shows example waveforms of a DPT with the temperature and baseplate pin measurements included. The junction temperature of the switch positions increases during high-loss conditions and decreases in low-

loss conditions as energy is dissipated to the baseplate. The leakage current through the baseplate spikes during high dv/dt switching events indicated by V(mid).

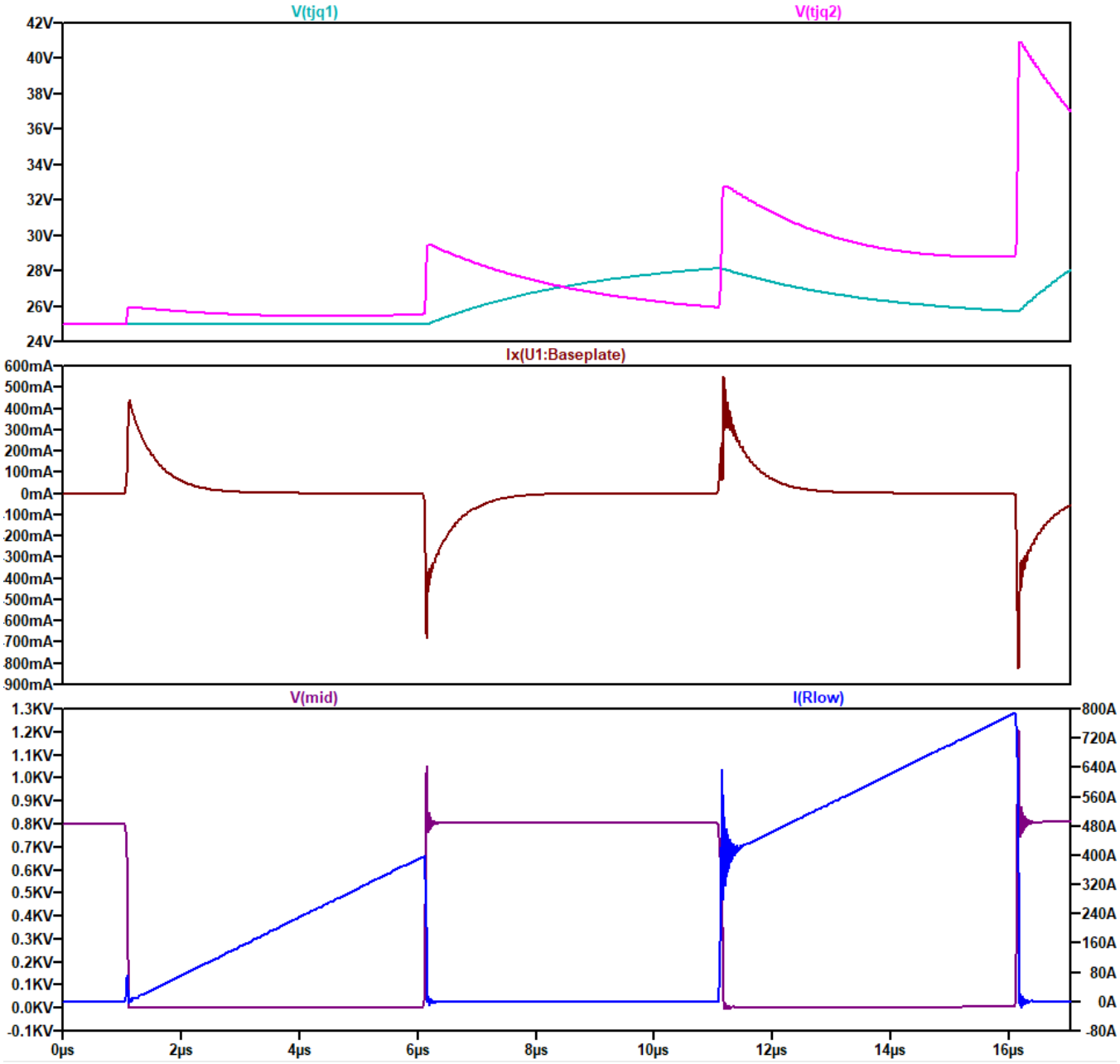

Figure 10: Example DPT waveforms including junction temperatures and baseplate current

2.2 Library File Customization

The LTspice library file features several options for customizability that will be discussed in this section. To edit the model behavior, right-click the model symbol in simulation. The component attribute editor shown in Figure 11 will open. The primary features that can be edited are shown in the 'Value' and 'SpiceLine' fields. The 'Value' field can be changed to another module part number to select another module. This can be useful for parameterizing the module model being simulated using the .TEXT feature in LTspice. The available module models are listed at the top of the library file.

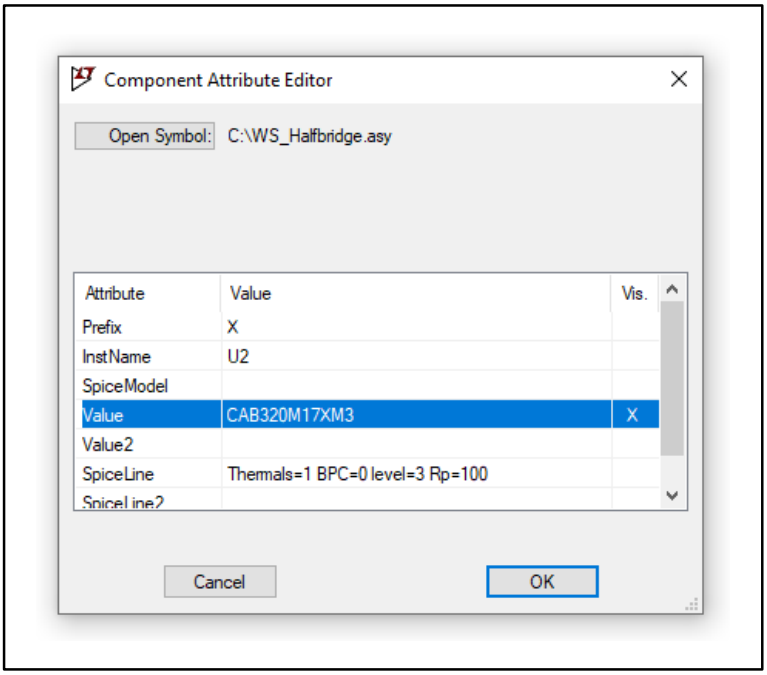

Figure 11: Library file component attribute editor window

In the SpiceLine field, the 'Thermals', 'BPC', 'level', and 'Rp' fields can be changed to adjust the complexity of the model:

Thermals

- Set to 1 to enable closed-loop electro-thermal modeling with Cauer network model (representing datasheet Zth), causing dynamic junction temperature which responds to semiconductor losses. The initial temperature of the junction is set by the global TEMP parameter. Adds complexity and accuracy.
- Set to 0 to disable the closed-loop electro-thermal model and use a constant temperature across the duration of the simulation. The temperature of the junction is set by the global TEMP parameter. Decreases complexity and accuracy.
- There are two methods to set a temperature other than TEMP to an individual switch position. The first is to specify a 'Tj' parameter on 'SpiceLine2'. For example, 'Tj=75' will set the initial temperature of the junction to 75°C, regardless of the global TEMP parameter. Another method is to directly apply a voltage source to the Tj pins.

BPC

- Set to 1 to enable the baseplate capacitances in the model. Adds significant computational complexity but is crucial for EMI simulations.
- Set to 0 to disable the baseplate capacitances in the model. The baseplate pin is disabled and tied to ground.

Level

- Set to 3 to enable the full third-quadrant model. This includes reverse recovery across temperature and conduction characteristics across V_{GS} and temperature. Provides the highest accuracy, but also the greatest complexity. Consider decreasing the level parameter to improve simulation speed or if reverse recovery behavior is not necessary. For modules with internal Schottky diodes, the level parameter is limited to level=2 since reverse recovery is negligible for these devices.
- Set to 2 to disable reverse recovery. The conduction characteristics are still provided across V_{GS} and temperature characteristics. This level is suitable for synchronous switching applications.
- Set to 1 to disable the third-quadrant model and replace it with a body diode model fit at VGS = -4 V. The model will still include reverse conduction in the ON state, but will not model the changes in body diode conduction across V_{GS} and temperature. Setting level=1 greatly improves simulation speed.

Rp

- Rp represents a parallel resistance across parasitic inductance within the package. At 100 Ω, this resistance creates a lowpass filter with a cutoff around 1 GHz. This frequency is sufficiently high for power electronics simulations but prevents the LTspice simulator from decreasing the timestep to calculate extremely small, high-frequency oscillations between the parasitic inductance and capacitances in the system. This resistance can be decreased to improve simulation speed further. At 1 mΩ, the influence of the parasitic inductance is removed entirely, and the simulation speed can be improved by several orders of magnitude. The model will not correctly predict voltage overshoot, but this can be extremely useful when performing long-duration simulations where detailed switching behavior is not the primary concern.

In addition to these main configuration parameters, several other parameters can be edited from the SpiceLine2 field. These are briefly described as follows:

- AFm: Sets the number of MOSFETs per switch position
- AFs: Sets the number of Schottky diodes per switch position
- Vths: Adds a Vth threshold shift to the die behavior
- Rdss: Adds an Rds(on) shift to the die behavior
- Package parameters: in 3.2, parasitic circuits of the models are provided. Any of these parasitic parameters can be set from the SpiceLine2 field.

2.3 Alternative Software Customization

The non-LTspice models do not feature the same level of customization as the library models. However, the netlist itself can be edited to suit the needs of a particular simulation. The netlist is designed to be readable, and any custom changes will be the responsibility of the user. The model files include commented baseplate capacitance lines that can be uncommented for EMC simulations (a baseplate pin must be added as well).

3. Detailed Model Behavior Overview

Circuit-level SPICE models of power electronic systems can be divided into three hierarchical categories: system-level, package-level, and die-level, as shown in Figure 12. The system-level model describes the overall circuit within which the device will be used and is specific to each application. Application circuits vary in complexity, ranging from simple setups such as clamped inductive load (CIL) circuits and buck converters to complex setups such as bidirectional multiphase DC/DC converters. The package-level model is embedded within the system-level model and describes the connections between the system and the semiconductor chips. These connections are not ideal and are accompanied by parasitic resistances, inductances, and capacitances that must be included to create an accurate package model. The characteristics of the die themselves are described by the die-level model, which lies at the lowest level of the hierarchy. The combination of package and transistor models represents a fully detailed SiC power module SPICE implementation that can be applied across a wide range of applications.

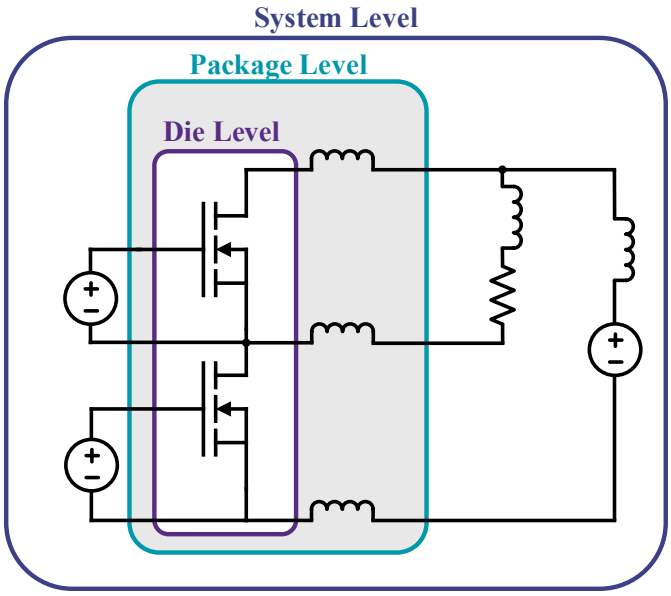

Figure 12: Description of SPICE model architecture

The implementation of the SiC MOSFET die-level model has a significant influence on the overall performance of the final packaged semiconductor model. Wolfspeed power module models use a behavioral approach that maximizes accuracy and efficiency. In addition, developing an accurate and efficient package-level model requires an understanding of the most influential parameters within a particular application or system. The package-level model is particularly important for simulations involving MCPMs. In this section, the Wolfspeed

power module die and package models will be discussed in detail. The compact model has also been presented in [1].

A notional circuit diagram of the package model is shown in Figure 13 (a). The package model includes electrical package parasitics (such as self-inductance, mutual coupling, and baseplate capacitance) and a model of the junction-to-case thermal impedance. The thermal impedance is modeled by a third order Cauer network fit to Z_{TH} curves. The shortest pulse width considered for fitting is 1 µs. The behavioral transistor model in Figure 13 (b) has electrically dependent device capacitances, a static gate resistance, and temperature-dependent forward characteristics that include short-channel effects at high drain-source voltages. The third-quadrant model captures reverse recovery behavior across temperature and reverse conduction characteristics across temperature and V_{GS} biases.

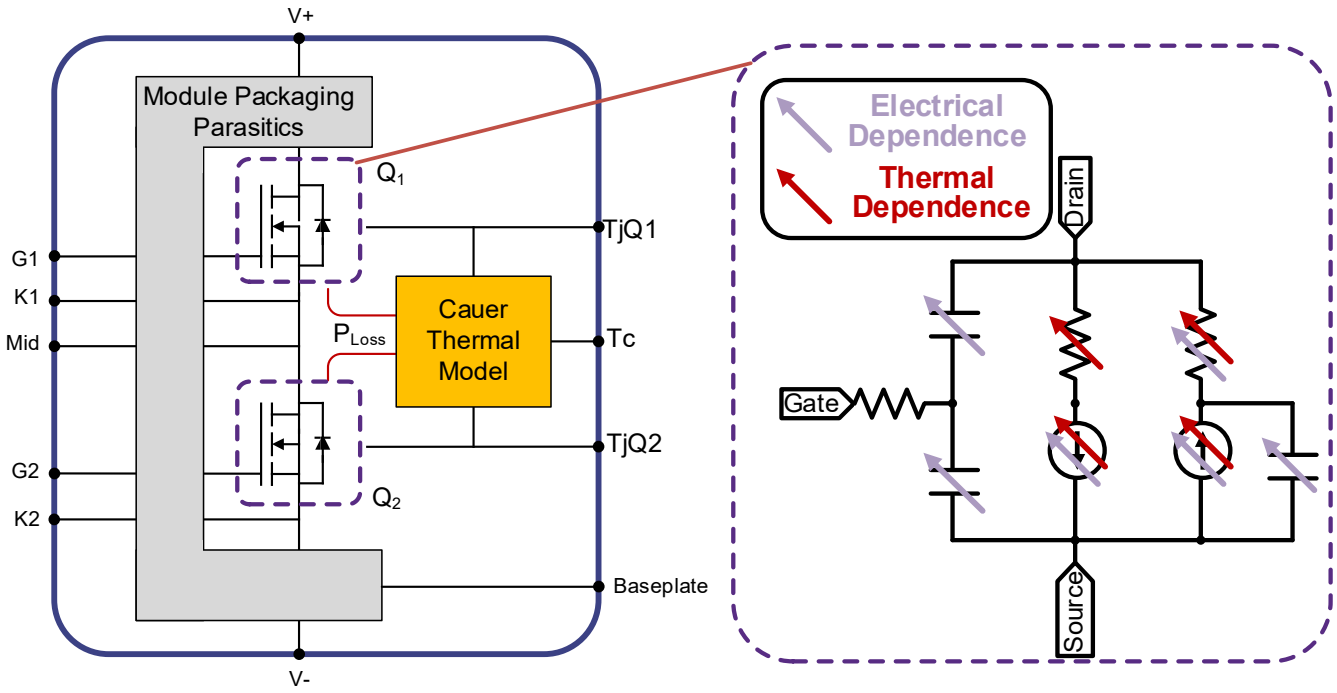

Figure 13: Half-bridge power module model, (a) package model, (b) transistor model

3.1 Die Model Description

Example fits for the forward characteristics for a subset of V_{GS} conditions at multiple temperatures are shown in Figure 14. The fits for the low V_{DS} region (0 V – 50 V) are shown in the top plots, and the fits for the high V_{DS} region (0 V – 600 V) are shown in the bottom plots.

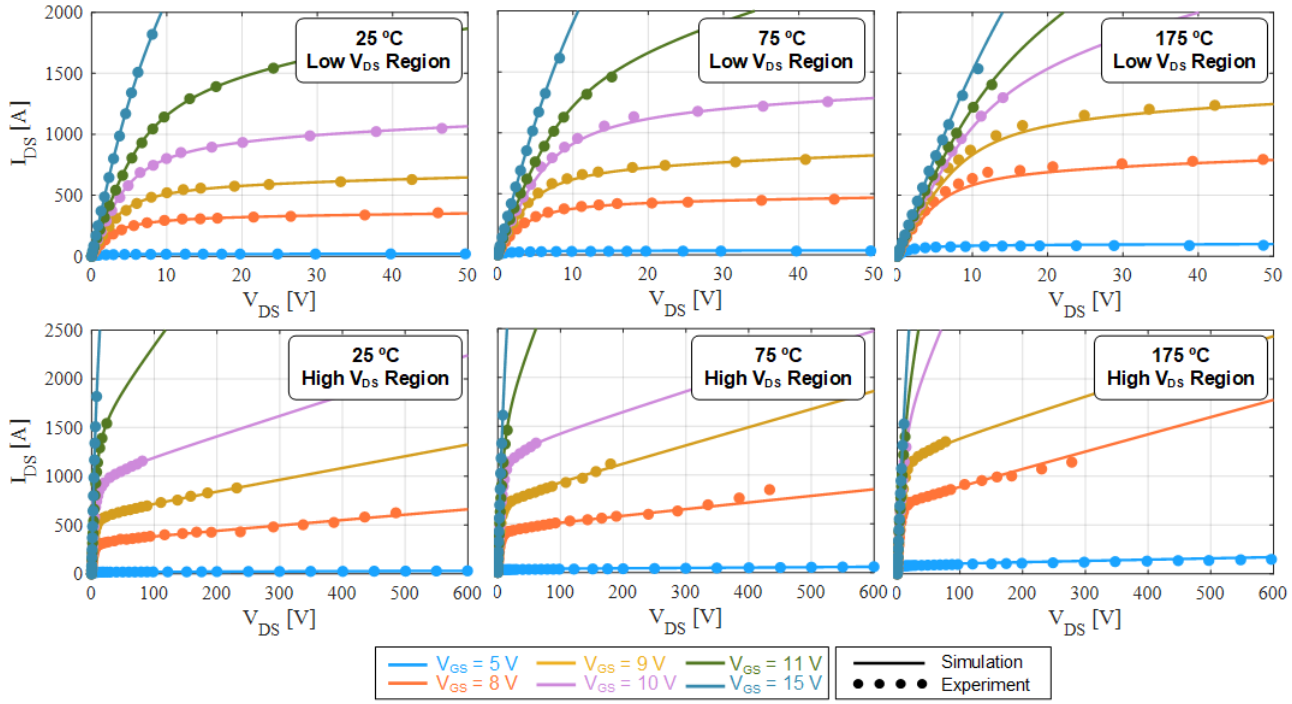

Figure 14: Demonstration of forward static characteristic fits at 25 °C, 75 °C, and 175 °C. Top: low V_{DS} region (0 V – 50 V), bottom: high V_{DS} region (0 V – 600 V)

Figure 15 shows example model fits for the third-quadrant conduction characteristics at a subset of V_{GS} conditions across temperature.

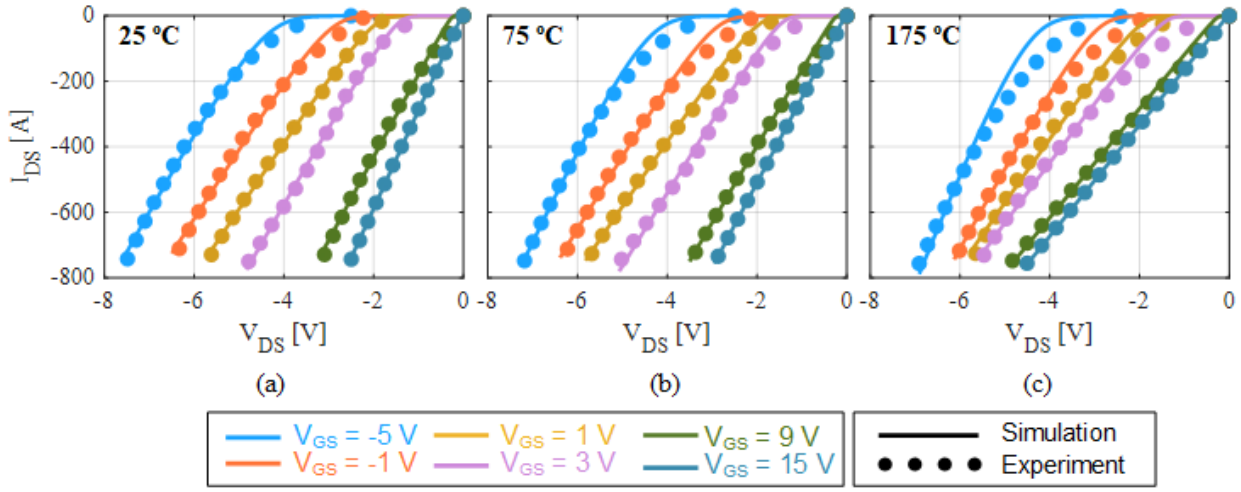

Figure 15: Demonstration of third-quadrant static characteristic fits at (a) 25 °C, (b) 75 °C, (c) 175 °C

In the presented model, C_{DS} and C_{GD} are modeled with dependence on V_{DS}, and C_{GS} is modeled with dependence on VGS. The model fits for these characteristics are provided in Figure 16.

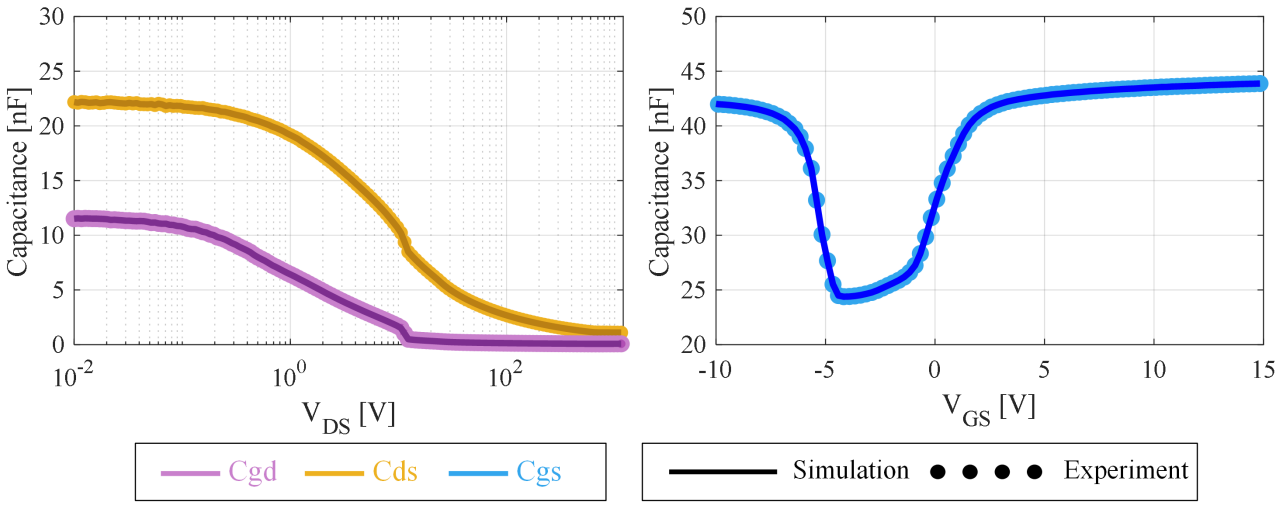

Figure 16: Demonstration of CV characteristics fits

Finally, the reverse recovery parameters of the model are tuned at multiple temperatures. Figure 17 demonstrates the model's reverse recovery behavior across temperatures after tuning. The implementation of reverse recovery into the device model allows for better prediction of losses.

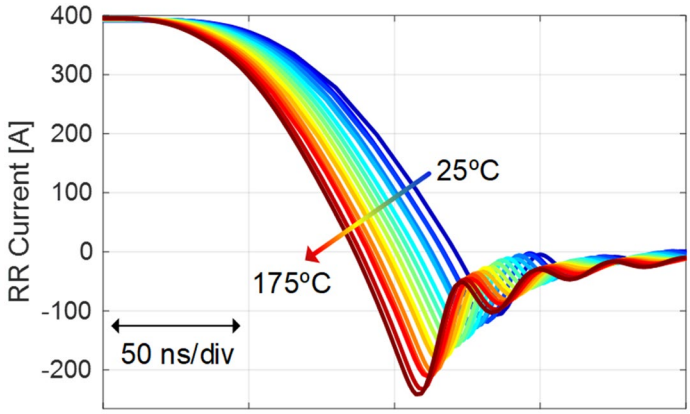

Figure 17: Demonstration of model reverse recovery behavior across temperature

3.2 Package Model Descriptions

The package model describes the non-ideal connections between the internal semiconductor and the module terminals. It is designed to contain the most influential parameters, and some elements are simplified or omitted to improve computational performance. The structure of the package model changes depending on the topology of the module. Currently, half-bridge, full-bridge, and six-pack module models have been released.

3.2.1 Half-Bridge

Figure 18 shows the complete package model for half-bridge module models. For Schottky modules, the diodes are connected directly in anti-parallel with the MOSFETs Q1 and Q2. The resistance Rgi describes both the package gate resistance and the die gate resistance as a single parameter. Some parasitic parameters only appear when specified. For example, LcsiQ1 and LcsiQ2 are only included in modules with common-source inductance. Any of these parameter values can be changed in the LTspice library file by editing the SpiceLine2 attribute (e.x. Rgi=1, LgQ1=30n).

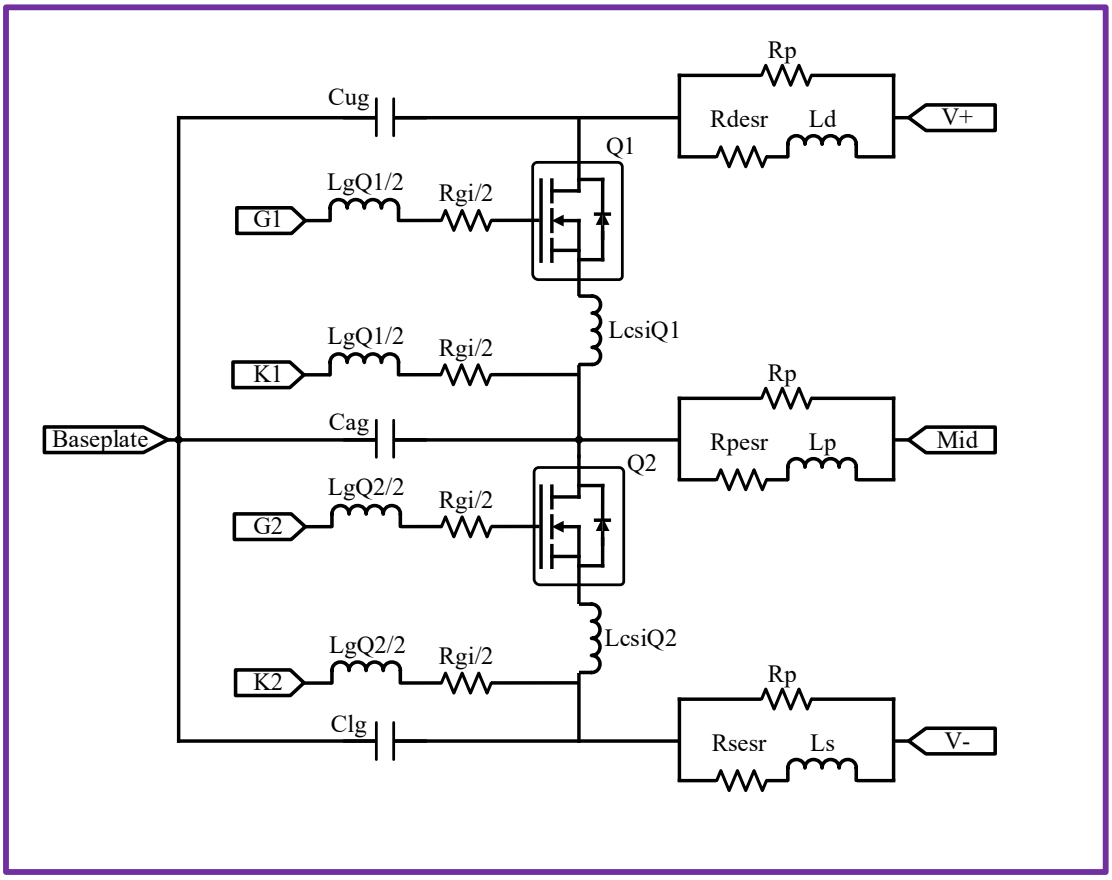

Figure 18: Half-bridge package model with parasitics

3.2.2 Full-Bridge

The full-bridge package model is provided in Figure 19. The model is effectively two half-bridge circuits in parallel, with some minor differences. The two DC- terminals are isolated internally, while the DC+ terminals are connected on the substrate. There is no parasitic inductance between the D terminals to each die; the drain of Q1 and Q3 are directly connected. This is a minor simplification of the parasitic model but improves the convergence and runtime behavior. Any of these parameter values can be changed in the LTspice library file by editing the SpiceLine2 attribute (e.x. Rgi=1, LgQ1=30n).

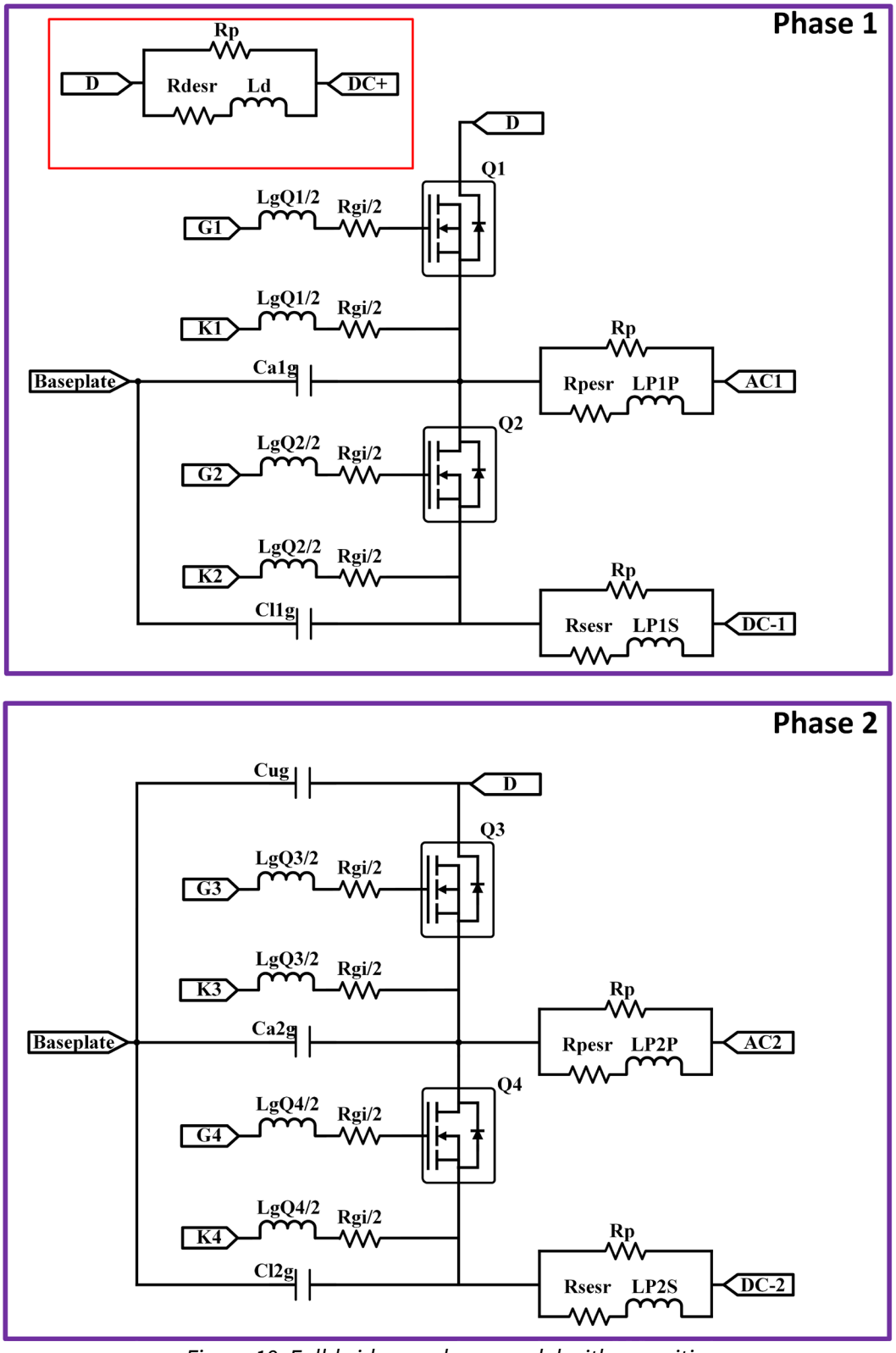

Figure 19: Full-bridge package model with parasitics

3.2.3 Six Pack

The six-pack package model is provided in Figure 20. The model is effectively three half-bridge circuits in parallel, with some minor differences. The three DC- terminals are isolated internally, while the DC+ terminals are connected through a parasitic inductance. Any of these parameter values can be changed in the LTspice library file by editing the SpiceLine2 attribute (e.x. Rgi=1, LgQ1=30n).

There are some distinctions in the model based on the platform. For FM six-pack modules (such as the CCB032M12FM3), all of the DC+ terminals are connected internally. Thus, RD2D3s and RD1D2s are very small (on the order of μΩ), and Cu2g is removed from the model. However, for GM six-pack modules (such as the CCB016M12GM3), phase 3 (DC+3) is isolated from the other two phases. Thus, RD2D3s and RD2D3p are set to very large values to represent the physical module, and Cu2g is included in the model.

Runtime can be improved by setting RD1D2p, RD2D3p, RD1D2s, and RD2D3s to 1 mΩ.

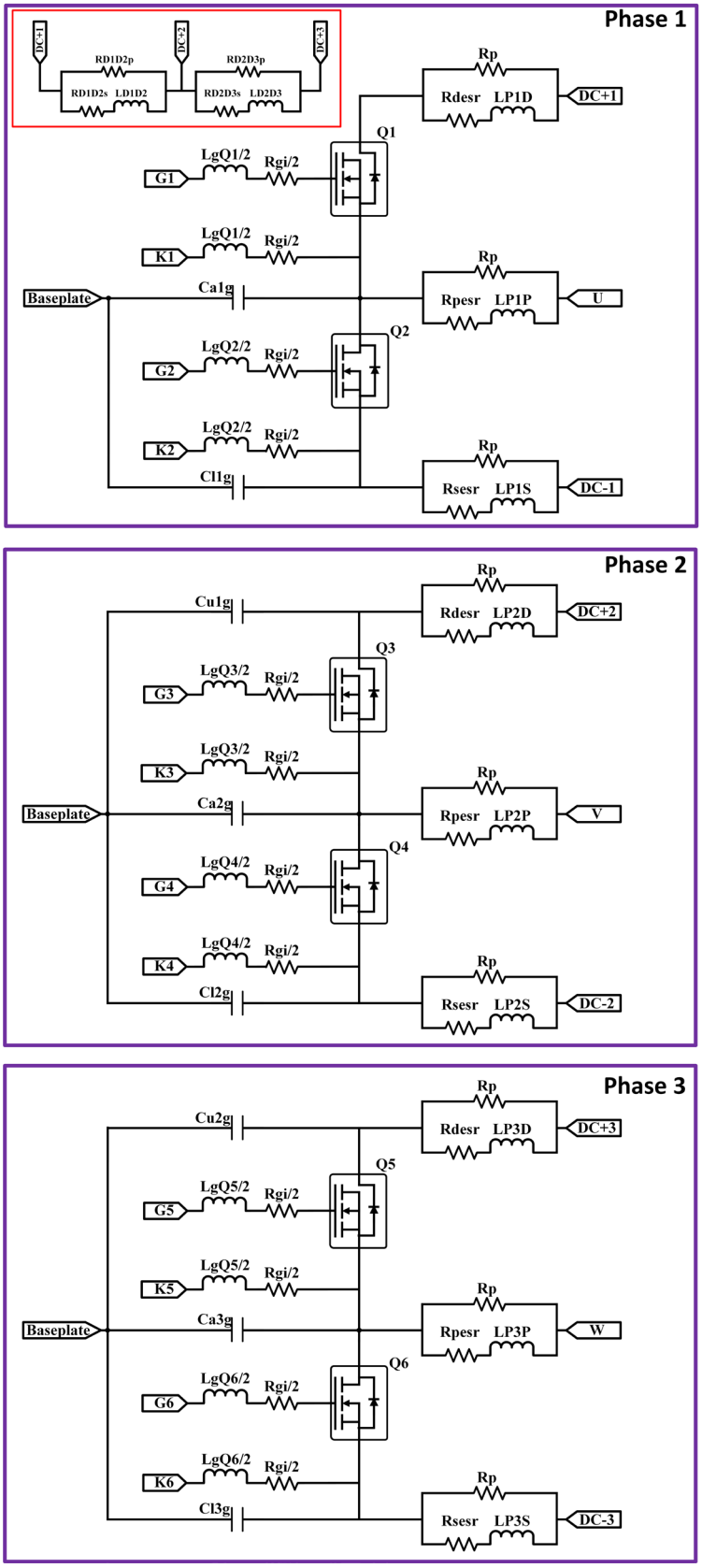

Figure 20: Six-pack package model with parasitics

Revision History

Date	Revision	Changes
September 2023	1	Initial Release
December 2023	2	Added Simetrix Installation Instructions

References

[1] B. T. DeBoi, B. W. Nelson, A. Curbow, T. McNutt and A. N. Lemmon, "Computational Efficiency Analysis of a Compact Behavioral SiC SPICE Model," in *PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2023.

Simulation Assistance

For any questions or comments about the model and its implementation, please post on our forum at https://forum.wolfspeed.com/ to receive assistance from a support engineer.