Application Note **PRD-07845**

Power Module Baseplate Capacitance and Electromagnetic Compatibility

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The high edge rates of power electronics switching devices can induce common-mode leakage currents that flow into the module baseplate through parasitic capacitances across the insulating ceramic. These leakage currents are often a major component of the electromagnetic signature of power electronics systems and are important to consider when designing for electromagnetic compatibility compliance. This application note provides a brief background on electromagnetic emissions produced by power semiconductors, describes a simple measurement technique to characterize power module baseplate capacitance, and leverages simulation to analyze the influence of baseplate capacitance on emissions.

CONTENTS

1. Introduction

Electronic devices that are in proximity or share common conductors are susceptible to electromagnetic interference (EMI) that can disrupt their operation. Minimizing emissions is necessary to ensure that electrical systems do not interfere with each other's normal operation when placed in the same environment. Devices must meet both electromagnetic emission and susceptibility requirements to achieve electromagnetic compatibility (EMC). Here, emissions refer to the generation of unwanted electromagnetic energy, and susceptibility refers to how a device reacts when exposed to unwanted electromagnetic energy. Designing power electronics systems to minimize EMI requires understanding the sources of the emissions and how they transmit to other devices. One parasitic element that is particularly important is the parasitic capacitance between the switching semiconductors and the baseplate of a power module. In this application note, the influence of this parasitic capacitance on EMC is explored.

2. Definitions

2.1 Emission Types

There are many examples of EMI, from microwave ovens interfering with home WiFi networks to an industrial power supply turning off a nearby computer. Effectively, any device can interfere with another at both short and long distances with many means by which emissions can be transmitted. In general, emissions are described by their mode of transmission, and have three primary categories: radiated EMI, conducted EMI, and coupled EMI. These transmission paths are depicted in the diagram in Figure 1.

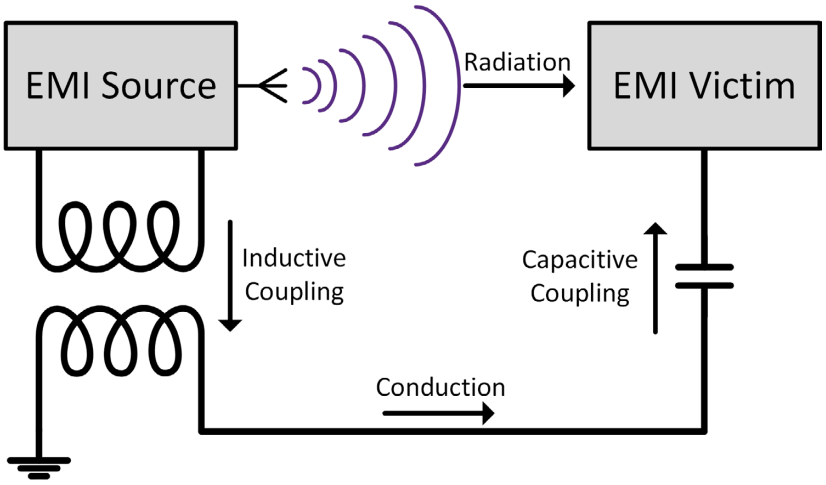

Figure 1: Visualization of EMI transmission paths

Radiated EMI occurs when a high-power transmitter produces a radio frequency (RF) that is coupled into another device, usually across a medium such as air. The primary challenge of radiated EMI is that it can affect devices across very large distances. If EMI is present but the source and victim are far apart, and not electrically connected, the transmission method is most likely radiated. Radiated emissions can be mitigated (at either the source or victim) by using proper shielding techniques. For an example of radiated emissions, in the early days of analog TV, appliances like vacuums would often interfere with the signal reception as designers were not considering EMC at that time.

Conducted EMI occurs when a source and victim are connected by an electrical path. This most commonly occurs on devices that share the same power source. For example, when a high-power device (such as a dryer or air conditioning unit) turns on and other devices in the home malfunction. Conducted emissions can be reduced by isolating systems such that no direct conduction path exists.

The final method is coupled EMI. Coupled EMI is similar to conducted EMI, however instead of occurring over a direct galvanic connection, emissions are transmitted through parasitic inductive coupling or capacitive coupling. Inductive coupling occurs when closely routed conductors transfer energy in the magnetic field due to *di/dt* in the system. This most often occurs in closely routed wires, bussing structures, or printed circuit board (PCB) traces. Capacitive coupling occurs when two closely coupled conductors transfer energy in the electric field due to *dv/dt* in the system. This type of coupling usually requires conductors to be close together but can occur at longer distances when large conductive planes are involved.

In high-voltage power conversion applications that leverage Wolfspeed® power modules, the high-voltage and currents produced by the semiconductors are galvanically isolated from surrounding systems. In addition, the frequencies of the generated emissions are typically too low for radiated transmission to be significant. However, coupled inductors and parasitic capacitances provide a path for EMI to transmit into surrounding systems. Thus, this application note will focus on coupled EMI of power electronics systems.

2.2 Differential and Common Mode Signals

Conducted emissions can be in the form of either differential mode (DM) or common mode (CM) signals. As shown in Figure 2, differential mode currents follow an equal but opposite path back to the source. On the other hand, common mode signals return through a common path and flow through the two or more lines in the same direction and phase. While both signal types are able to interfere with other devices, the difference in the differential mode and common mode impedance in a system causes the signals to behave differently.

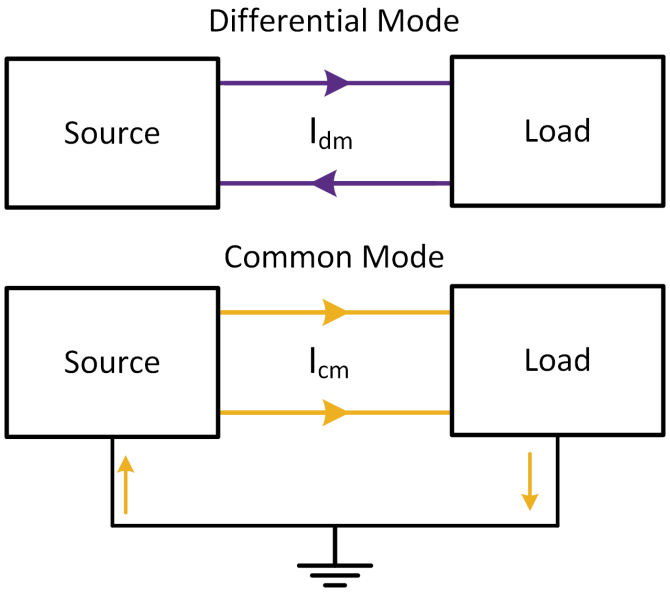

Figure 2: Differential vs common mode noise sources

Distinguishing between CM and DM noise when evaluating the EMI of a system is important for two reasons. First, the source of the noises in a system often differs. DM noise sources typically arise from the "expected" sources, such as pulse width modulation (PWM) switching harmonics or magnetic coupling from conductors carrying high *di/dt* signals. CM noise sources, on the other hand, are typically induced by "unintended" signals, such as the voltage differential between circuit nodes and ground, flowing through parasitic capacitances. Second, mitigation techniques that are effective for DM noise are not necessarily effective for CM noise and vice-versa. Knowing where CM and DM noise appear in a conducted emission spectrum enables designers to apply targeted EMI suppression or prevention techniques, thereby saving on design time and cost.

A common mode choke is an example of a filter that is effective at impeding common mode current while allowing for differential mode current to flow freely. A diagram of a common mode choke for differential and common mode current flow is shown in Figure 3. In the differential mode, current travels on one line from the source to the load and returns in the opposite direction to complete the circuit. The induced flux in the core cancels out and thus the field does not oppose the signal. In the common mode, the current travels in the same direction and the magnetic fields add to create an opposing field that impedes the signal. Thus, the CM choke reduces CM noise but has minimal effect on DM signals.

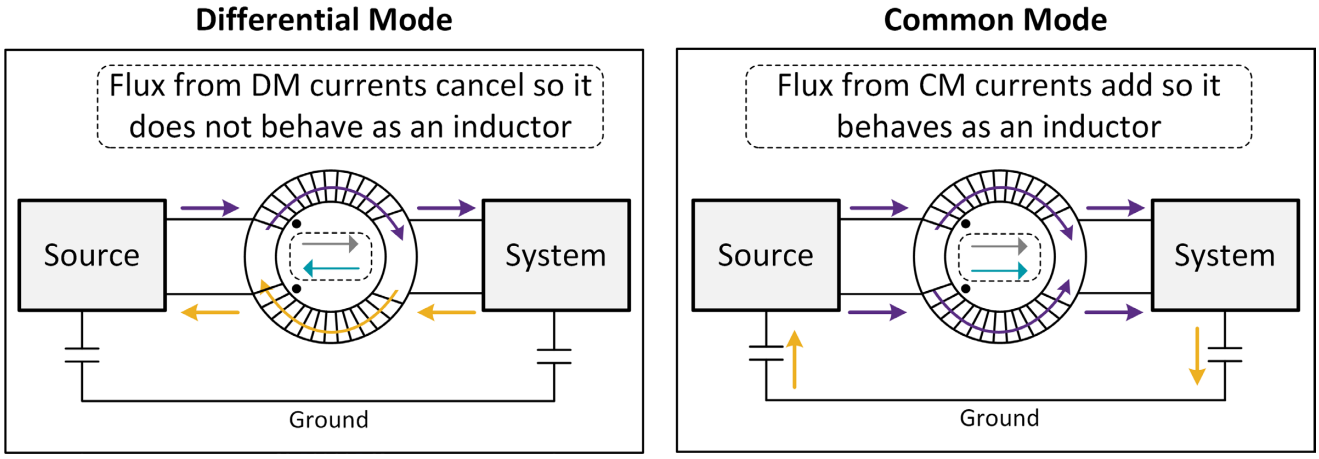

Figure 3: Differential and common mode current flow through a CM choke

2.3 EMC Standards

Given the prevalence of electronic equipment and the complexity of electromagnetic compatibility, several standards have been established to ensure that commercial equipment will operate correctly. These standards provide guidelines and specifications for performing EMI testing and limitations on the emission spectra of devices. The guidelines and requirements differ across standards based on the region, device type, and application.

Two EMC standards commonly employed for power electronics devices are CISPR 22 and MIL-STD-461 [1]. In these standards, testing consists of both conducted and radiated emission testing. Conducted emission testing is performed in the frequency range of approximately 10 kHz to 30 MHz, whereas radiated emission testing is performed in the RF range of 30 MHz and above. This application note will focus on conducted emissions, as it is the most prevalent source of emissions for power conversion systems that leverage Wolfspeed power modules.

2.3.1 Conducted Emissions Testing

The exact configuration and testing requirements for conducted emission testing are dictated by the standard being followed. Even within standards, the configuration may change based on the equipment under test (EUT). An example of a notional test setup described by MIL-STD-461 CE102 is provided in Figure 4. The equipment is raised above the floor and placed on a conductive ground plane, which provides a reference for the equipment that is separate from the surrounding environment. A line impedance stabilization network (LISN) is connected between the power supply unit (PSU) and EUT on each power input. The LISNs assist in making reliable measurements of the EUT noise by isolating the EUT from the grid, ensuring a consistent metrology setup, and providing a precise impedance to the power input of the EUT. During testing, the EUT is operated continuously in its highest-emission configuration, and the measurement equipment attached at each LISN quantifies the EMI of the system.

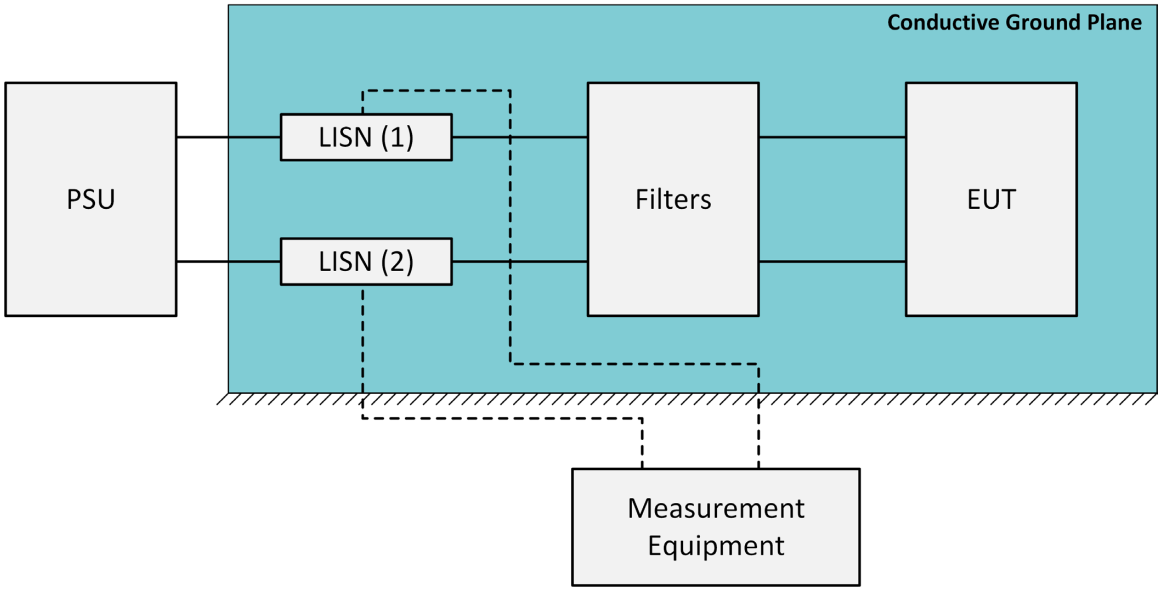

Figure 4: MIL-STD-461 CE102 general test diagram

A circuit diagram of the MIL-STD-461 CE102 LISN is provided in Figure 5. When a 50 Ω impedance is connected across the 1 kΩ resistor, the system maintains a ~50 Ω impedance across a wide range of frequencies. The 50 Ω impedance is usually provided by the termination internal to the measurement equipment. However, if no measurement equipment is connected, then a 50 Ω terminator should be attached. The voltage measured (V_{meas}) at this node on each LISN is used to determine the emissions in the system. For a system with a single power input and return line, the differential mode emissions can be calculated through equation (1), where V_1 and V_2 are the measured voltages at LISN (1) and LISN (2) in Figure 4, respectively. The common mode emissions are similarly calculated in equation (2). For compliance testing, the spectra of V_1 and V_2 individually are used to measure emissions. These measurements will differ in a physical test due to asymmetries in the system.

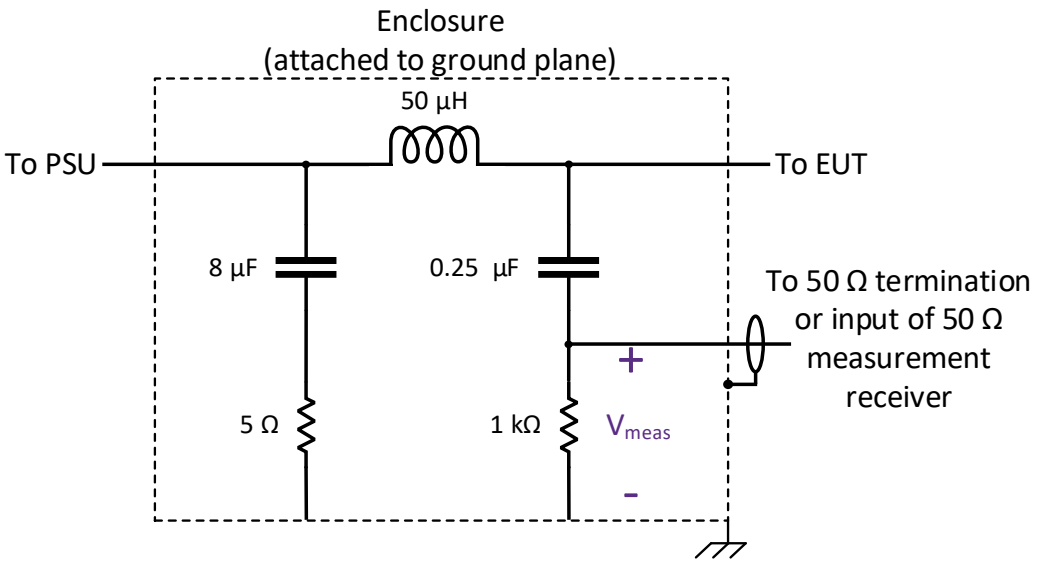

Figure 5: MIL-STD-461 CE102 LISN circuit and connection guide

$$V_{dm} = V_1 - V_2 \quad (1)$$

$$V_{cm} = \frac{V_1 + V_2}{2} \quad (2)$$

2.3.2 Conducted Emission Limit Lines

Similar to EMI testing configurations, the allowable emissions differ by each standard and by device type or characteristics. Examples of emission limits from MIL-STD-461 and CISPR 22 are provided in Figure 6. In MIL-STD-461 CE102, a basic curve for conducted emission limits are defined from 10 kHz to 10 MHz. An additional offset is applied based on the operating voltage of the device, as higher voltage systems will inherently produce higher emissions. In CISPR 22 (referred to as EN 55022 in Europe), conducted emission limits are defined from 150 kHz to 30 MHz and are divided into different classes. Class B defines equipment, devices, and apparatus that are intended to be used in the domestic environment and meet CISPR 22 Class B emission requirements. Class A defines equipment, devices, and apparatus that do not meet the Class B requirement but comply with the less stringent Class A requirement. Class A equipment is required to display a warning that it may cause interference in a domestic environment. In addition, CISPR 22 also defines different standards based on average emissions and quasi-peak (QP) emissions. Figure 6 shows the CISPR 22 QP limits compared to the MIL-STD-461 CE102 emissions. In summary, when designing applications to comply with EMC standards, it is important to understand the requirements for testing and evaluating the device based on the appropriate standard. Optimizing systems to meet their necessary EMC requirements early in the design cycle can reduce redesign and filter costs when installing the product in applications.

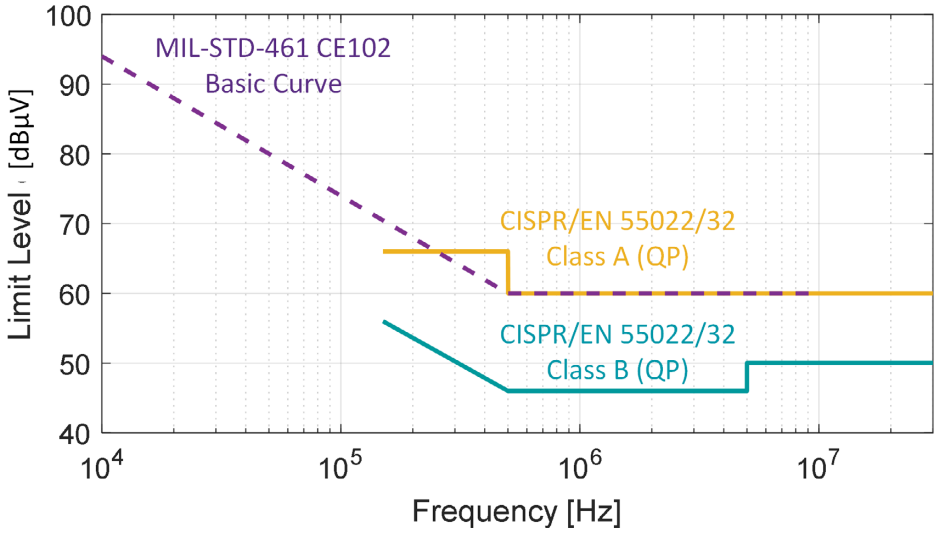

Figure 6: Maximum emissions across frequency for MIL-STD-461 CE102, CISPR 22 Class A , and CISPR 22 Class B

2.4 EMI and Power Electronics

Power semiconductor devices are a common source of EMI due to the fast switching required for their operation. In most modern power processing applications, a voltage is applied across the semiconductors, and a gate driver is used to generate PWM signal that is used to turn the device on and off to produce a regulated output to a load. During the switching transitions, the voltage across and current through the device rapidly changes states. Figure 7 shows typical voltage and current waveforms with finite rise and fall times of a MOSFET during operation. The change between off and on states produces a *dv/dt* and *di/dt* that generates EMI at harmonic frequencies of the switching frequency (F_{SW}).

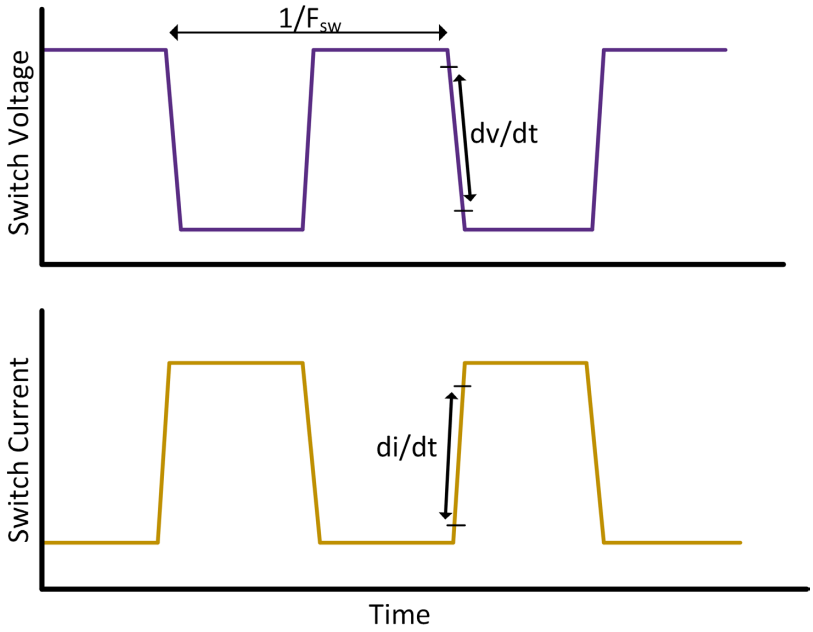

Figure 7: Typical MOSFET voltage and current switching waveforms

The switching frequency and edge rates determine the EMI generated during switching. Typically, the highest level of emissions will occur at the switching frequency and smaller peaks at integer multiples of the fundamental switching frequency. For example, if the switching frequency is 100 kHz, then the emissions spectra will have spikes at 100 kHz, 200 kHz, 300 kHz, and so on. For an ideal square wave (with infinite *dv/dt* and *di/dt*), the magnitude of the emitted spectra will decrease by 20 dB/decade, as shown by the purple waveform in Figure 8. For an ideal triangle wave, which has the slowest possible *dv/dt* and *di/dt* for a given switching frequency, the spectra will decrease by 40 dB/decade. Thus, for a power electronics device, which has a trapezoidal shape, the decay in spectra will decrease between 20 dB/decade to 40 dB/decade, the magnitude of which is determined by the edge rates. As devices are switched faster, it is expected that the emissions spectra at the harmonic frequencies will increase and decay slower across frequency.

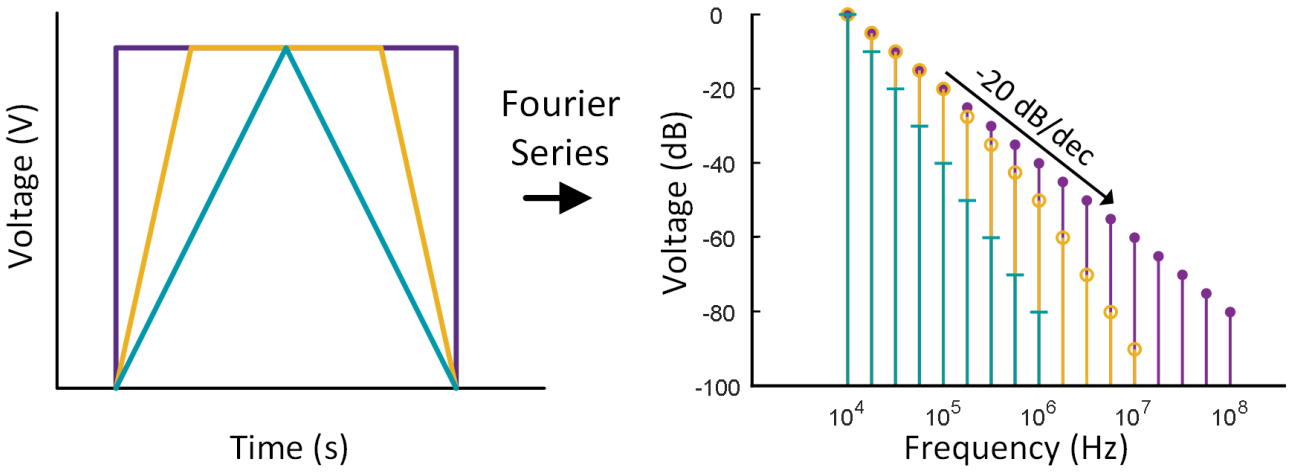

Figure 8: Notional spectra for a square, trapezoidal, and triangular signal

The relationship between switching frequency, edge rates, and EMI produces a series of tradeoffs for power electronics designers illustrated in Figure 9. In order to increase density, designers may opt to increase the switching frequency. This will reduce low-order harmonics but may increase emissions by shifting the spectral envelope toward higher frequencies. In addition, the more frequent switching will increase switching losses. To compensate for the overall increase in losses, designers may then opt to increase the edge rates (*di/dt* and *dv/dt*) in order to reduce switching losses. Unfortunately, the faster edge rates will in turn further increase the emissions of the system at higher frequencies. Thus, designers must consider the impact of EMI as applications increase switching frequencies and adopt faster-switching, high-performance devices.

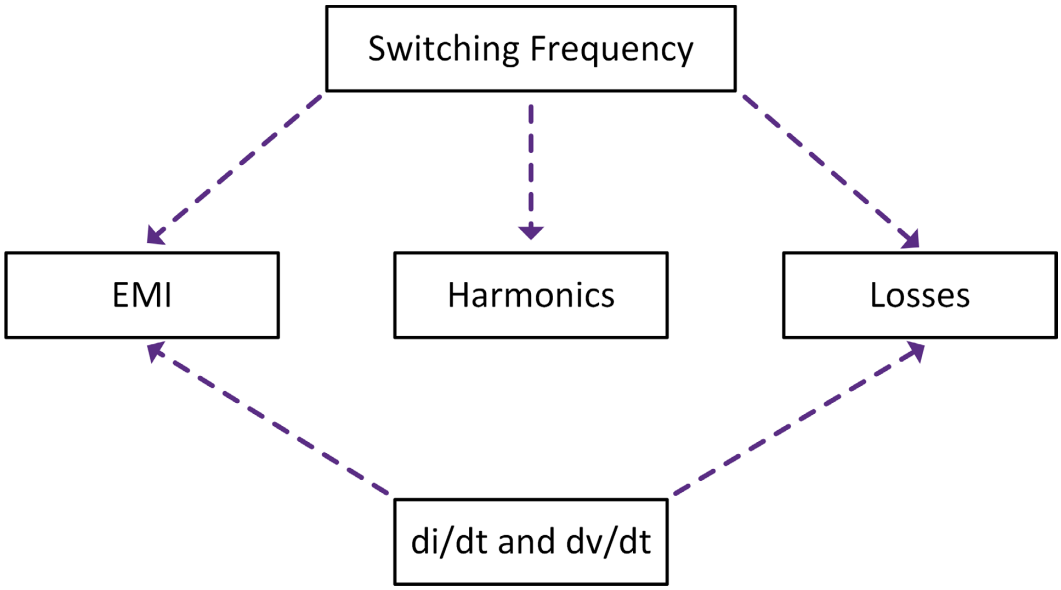

Figure 9: Tradeoffs in power electronics between efficiency and EMI

2.5 Power Module Baseplate Capacitance

Power modules provide significant advantages over discrete devices in their electrical and thermal characteristics, offering greater power density and reducing design cycles. One advantage is the use of a ceramic insulator to separate the high voltage conductors of the semiconductor chips and the metallic baseplate of the module. This allows modules to be attached directly to grounded heatsinks or other thermal management systems without additional insulation. In addition, modules can be placed in multi-level configurations without risk of short circuit. However, the conductor bonded to both layers of the insulating ceramic forms a parallel-plate capacitance between the switching nodes and the baseplate of the module, as shown in Figure 10. These baseplate capacitances (BPC) are separated by the switching nodes and allow for high-frequency CM currents to flow to the (typically grounded) baseplate and to the rest of the system. It should be noted that this issue is not unique to power modules; discrete devices that use insulating silicone pads will also have a parasitic capacitance with CM leakage currents. However, power modules provide a consistent capacitance across samples, providing a more predictable emission path than discrete devices. This consistency enables simulation and mitigation opportunities in the design phase of a power converter.

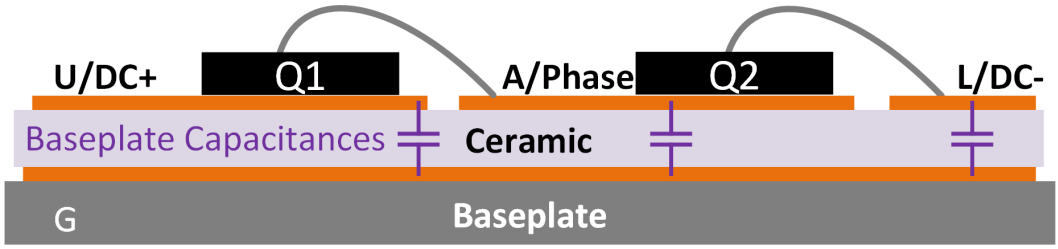

Figure 10: Notional diagram of a half-bridge power module device and baseplate capacitances

As previously mentioned, the power module baseplate capacitance provides a path for CM currents to flow from the switching semiconductors to the surrounding system. Figure 11 provides an example of the CM current flow in an EMC compliance test. Both the LISNs and the power module heatsink are connected to the same ground reference. During operation, high-frequency CM noise generated by the EUT can flow through the baseplate capacitance of the power module to the baseplate, then to the heatsink, and then to other system components such as the LISNs. This may result in elevated emission spectra that can cause an EUT to fail emission compliance testing. This situation is similar to a real-world system, where the heatsink is almost always grounded for safety concerns and ease of implementation. In addition, a floating heatsink will likely have parasitic capacitance to surrounding conductors through which the CM current will flow. Thus, applications must be designed considering this CM noise path to meet EMC requirements.

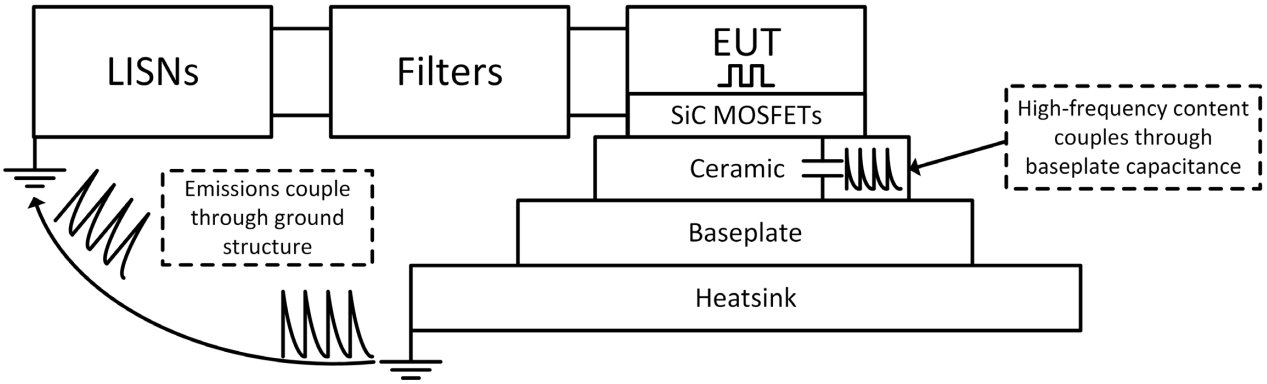

Figure 11: CM current flow through the module baseplate

It is also important to understand the importance of the distribution of parasitic baseplate capacitances on EMI. In addition to the total baseplate capacitance, the ratio between these capacitances determines the overall CM emissions. In some cases, these capacitances can even be manipulated to specific ratios to significantly reduce CM current without the use of filters [2]. An example of how baseplate capacitance is distributed in a Wolfspeed CAS350M12BM3 module is provided in Figure 12. Substrate regions are colored together if they are galvanically connected and should be modeled as a single lumped capacitance. Since the kelvin-source traces attach to the respective source pin at the top of the die, they are lumped together with the source node. For a half-bridge module, a full BPC model includes five baseplate capacitances: one for each power terminal, and one for each gate. This logic of separating individual baseplate capacitances can be applied to any module topology, such as full-bridge or six-pack modules.

The distribution of baseplate capacitances in Figure 12 can be represented by the circuit in Figure 13 (a). However, in some cases, the model can be simplified to the representation in Figure 13 (b) by adding the baseplate capacitance of each gate to the baseplate capacitance of the low side of its respective switch (since $C_{GS} >> C_{GD}$). This is particularly applicable for geometries in which C_{G1G} and C_{G2G} are significantly smaller than $C_{UG}/C_{AG}/C_{LG}$. The simplified network facilitates analytical analysis and improves the computational efficiency of EMI simulations.

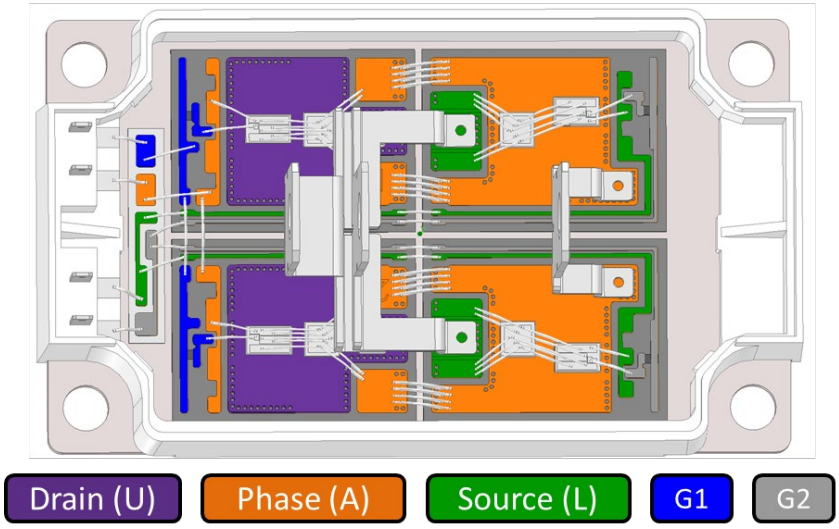

Figure 12: Distribution of baseplate capacitance in a CAS350M12BM3 power module

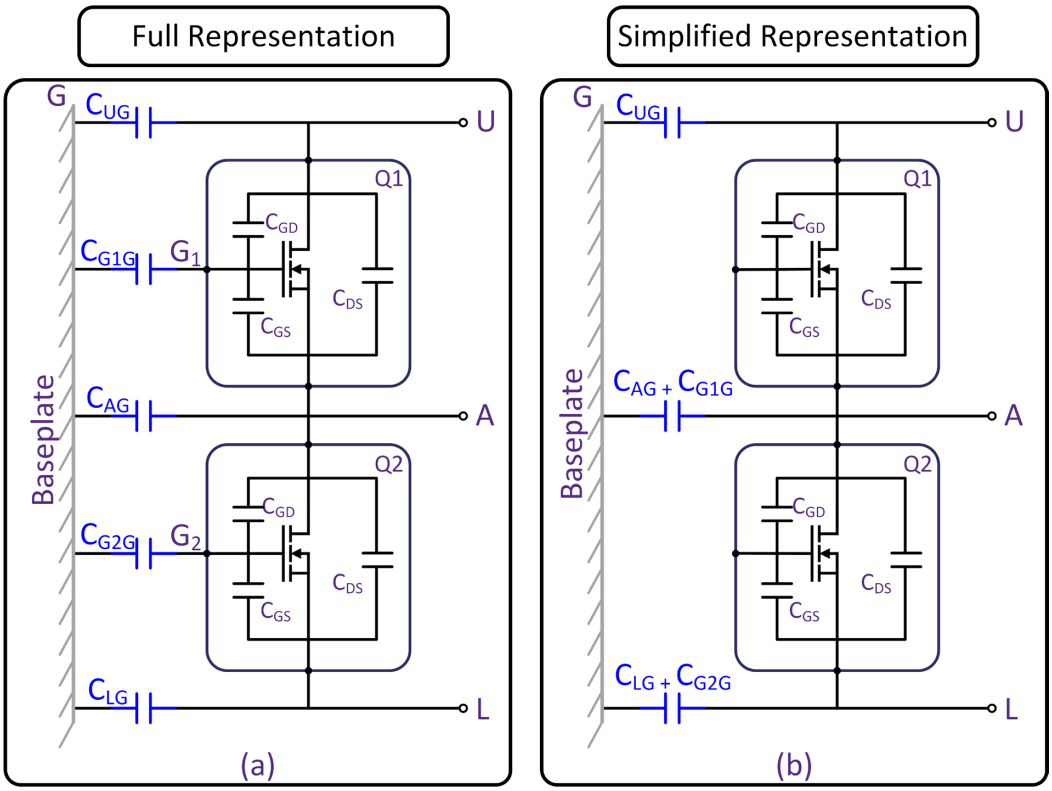

Figure 13: Circuit diagrams for half-bridge baseplate capacitance model, (a) full representation and (b) simplified representation

3. EMI Simulation Study

Circuit-level simulation software (e.g., LTspice) is useful for studying the influence of parasitics and other parameters on EMI. Wolfspeed's power module SPICE models are optimized for speed and accuracy, and include parasitic baseplate capacitance in the package model, allowing them to be used effectively for EMI simulations. To download the LTspice model library, go to https://www.wolfspeed.com/tools-and-support/power/ltspice-and-plecs-models/ and download the 'All LTspice Module Models.zip' file. The included user guide will provide information on how to install and use the models. It should be noted that, due to the complexity of small parasitic coupling between a system and the surrounding environment, it is difficult to accurately predict emissions of a physical system. However, simulation can allow designers to study the influence of parasitic elements on emissions, or to experiment with filter designs.

A simple example LTspice simulation of a boost converter in a MIL-STD-461 CE102 EMC test environment is shown in Figure 14. No DM or CM filters are included in the design. The SpiceLine settings of the model are changed to facilitate analysis, as shown in Figure 15. Setting "Thermals=0" simplifies the simulation by applying a static junction temperature throughout the simulation. Setting "BPC=1" enables the baseplate capacitance in the package model, which is necessary for EMC simulation. Setting level=1 simplifies the third-quadrant model to greatly improve simulation speed. Setting "Rp=100" improves simulation speed by damping high-frequency ringing caused by parasitic inductances in the module. By default, the gate resistance is set to 1 Ω, the DC link capacitance is 300 µF, the switching frequency is 100 kHz, the dead time is 300 ns, and the duty cycle is 50%. A 15 nH parasitic inductance is added in series with the Cdc capacitance, and a 25 pF parasitic capacitance is added in parallel to the Lf1 filter inductor.

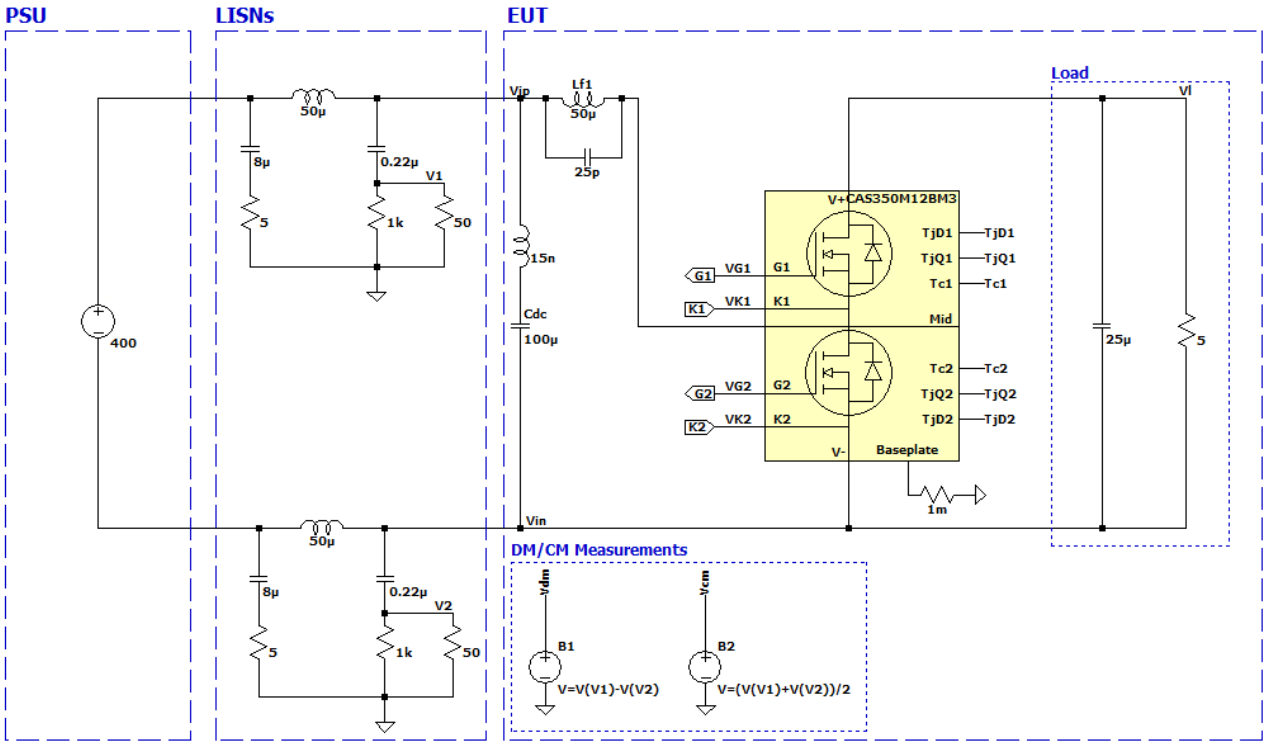

Figure 14: LTspice EMC boost converter simulation without filters

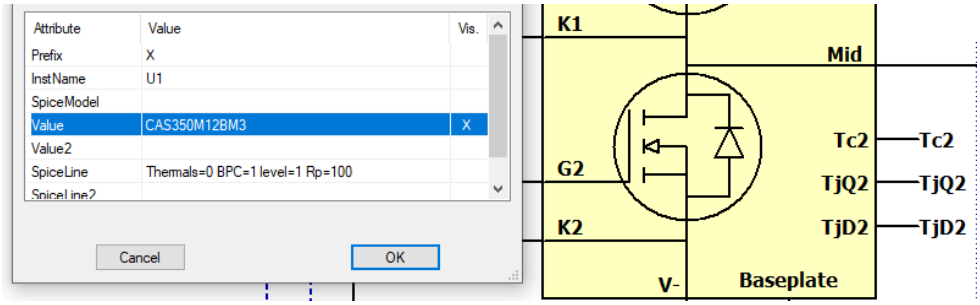

Figure 15: LTspice SpiceLine settings

3.1 Influence of BPC on Emissions

To demonstrate the influence of baseplate capacitance on EMI, the EMC boost converter simulation in Figure 14 was evaluated with and without the baseplate capacitances ("BPC=0" and "BPC=1"). For each simulation, the system was evaluated for 10 ms after steady-state was reached. The voltages V1 from Figure 14 was converted to the frequency domain with LTspice's built-in FFT function (the emissions of V1 and V2 are identical in a symmetric system). The spectral waveforms of V1 with and without baseplate capacitance are shown in Figure 16. The emissions limit for MIL-STD-461 CE102 is overlaid; any spectral content above this line indicates an EMC failure for this standard. While the system does not meet the EMC requirements in either configuration, the system with the baseplate capacitance has spectral content from 100 kHz to 10 MHz that lies above the emissions line. On the other hand, the system without baseplate capacitance is compliant above 2 MHz. It should be noted that this is an idealistic example; a physical system will have other CM paths in parallel with the baseplate capacitances.

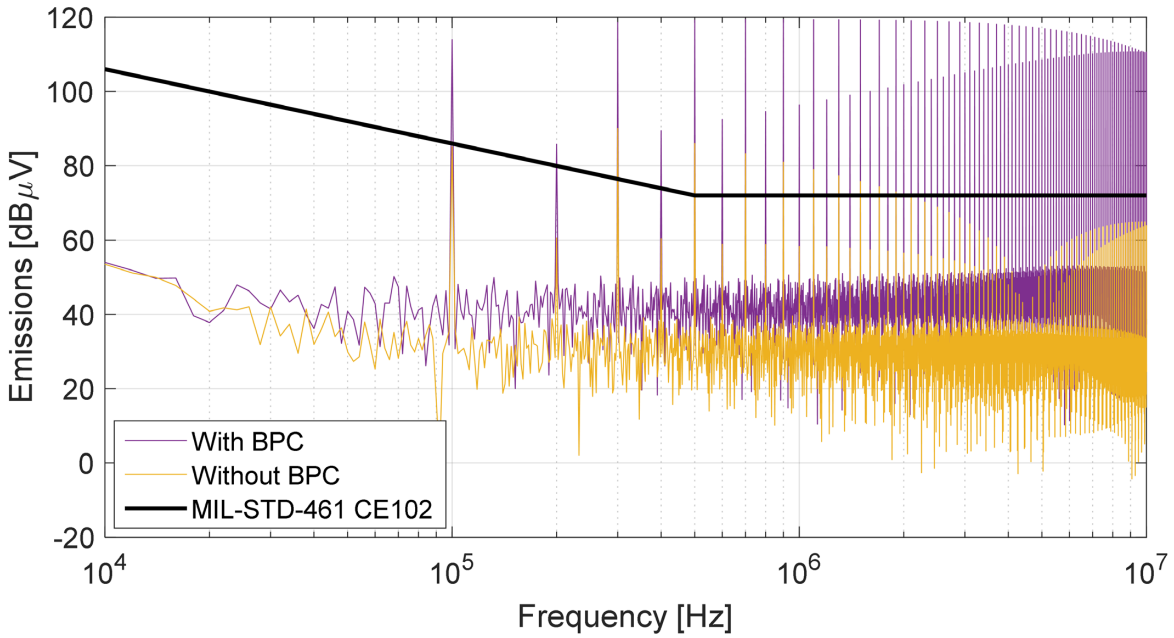

Figure 16: Emission spectra (CM + DM) of boost converter system with and without baseplate capacitance

The cause of the difference in emissions is due to the elevation of CM currents flowing through the power module baseplate. This is demonstrated by both Figure 17 and Figure 18. In Figure 17, it can be seen that the fast-switching edge during a turn-off transition of the low-side switch correlates with a leakage current through the baseplate. This leakage current elevates the CM currents, as shown in Figure 18, which shows an approximately 100 dBµV increase in CM emissions across frequency when the baseplate capacitance path is added.

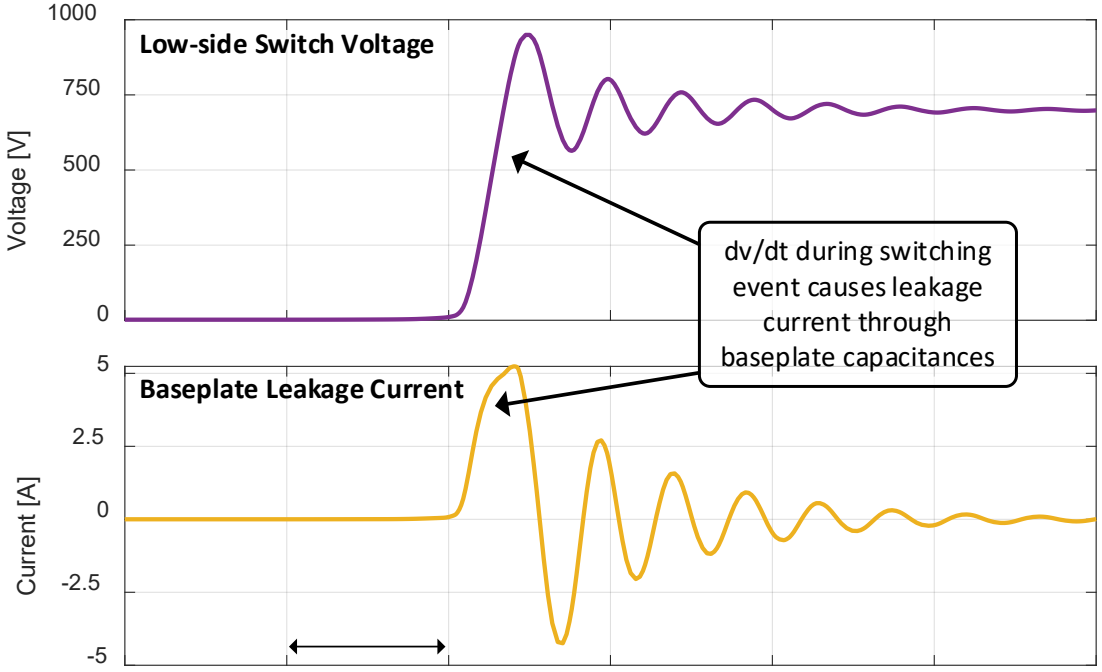

Figure 17: Switch voltage and baseplate leakage current during boost converter operation

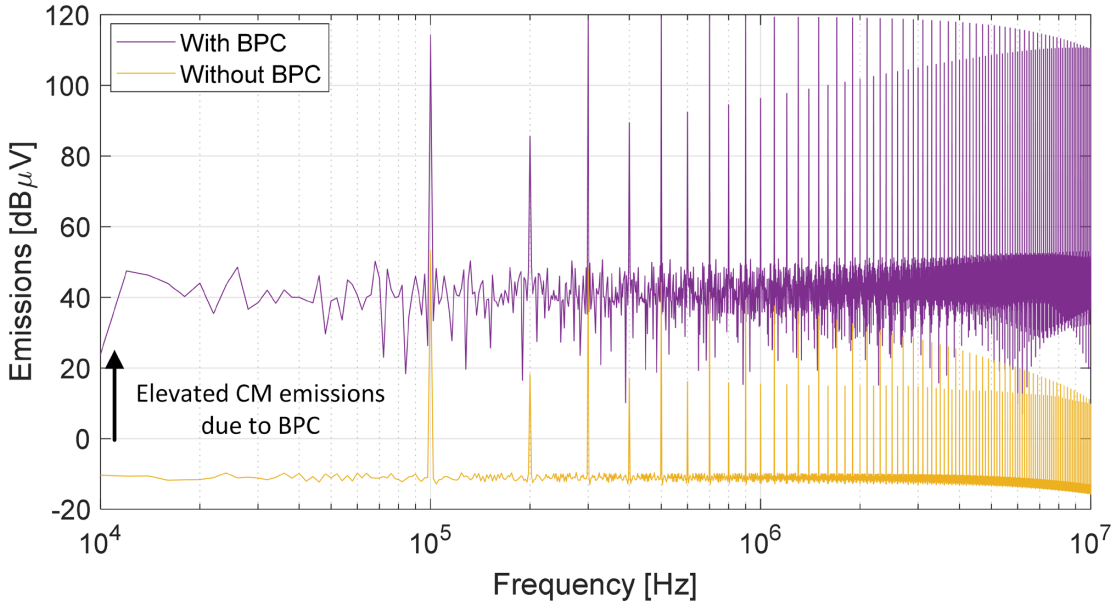

Figure 18: Emission spectra (CM only) of boost converter system with and without baseplate capacitance

3.2 Standard Filtering Example

Understanding the emission sources and paths can help apply targeted and efficient filters. Figure 19 shows the simulated CM and DM contributions to the total emissions for the boost converter in Figure 14 when modeling baseplate capacitance. Because the DM emissions only slightly exceed the MIL-STD-461 CE102 limit line, a large DM filter is not necessary. However, significant CM attenuation is necessary to meet compliance. Thus, one approach would be to combine a small low-pass DM filter with a larger CM choke with Y-capacitors. It should be noted that separating the CM and DM noise components is only useful for identifying which noise type is problematic. Even if the individual CM and DM components are below the emissions limit, the total emissions of the system may still fail.

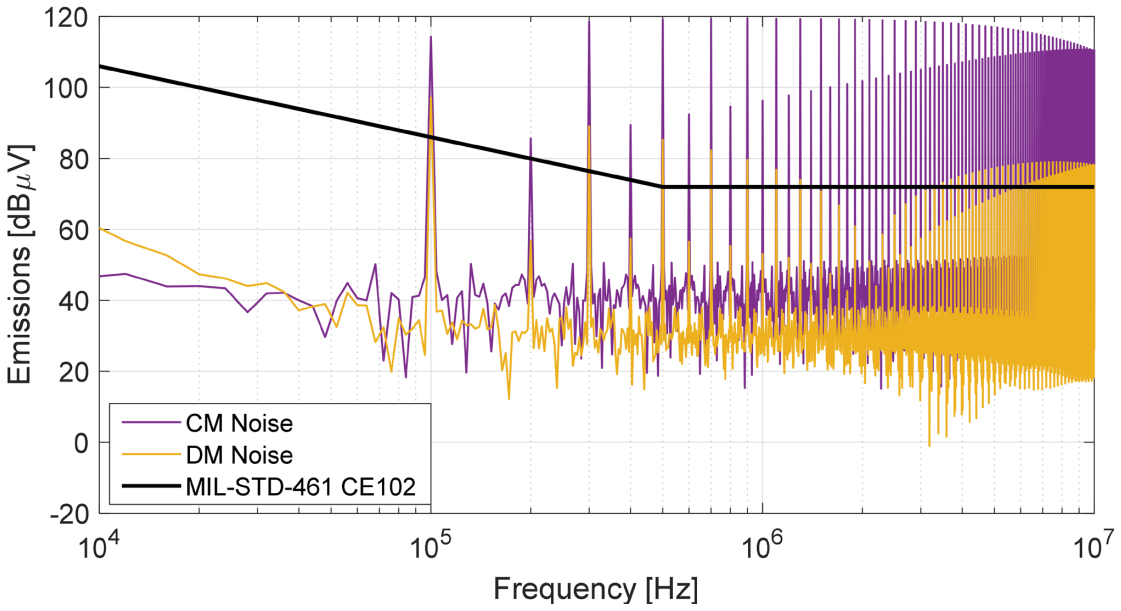

Figure 19: Comparison of CM and DM emissions for simulated boost converter with baseplate capacitance

The updated LTspice EMC simulation with the addition of the DM and CM filters is shown in Figure 20. The component values were chosen based on the necessary attenuation needed to meet the MIL-STD-461 CE102 specification. To reduce the DM emissions, a 10 µF X-capacitor (CDM) and a 50 µH DM inductor (LDM) were added. A 5 nH parasitic inductance is included in series with the CDM capacitor. To reduce the CM emissions, 500 µH CM chokes (LCM1 and LCM2) and 75 nF Y-capacitors (CY1 and CY2) were added. To accurately model a CM choke in LTspice, an ideal coupling coefficient is defined by the SPICE statement, “K LCM1 LCM2 1”. With the addition of these filter components, the simulation predicts that emissions will lie below the limit line, as shown in Figure 21. However, at the high current levels in this application, the 500 µH CM choke would be a large, costly, and lossy component in the system. Another option is to use significantly larger Y-capacitors (>1 µF) to reduce the size of the CM choke, but this introduces several challenges and some applications prohibit excessive line-ground capacitance.

Alternatively, it is better to consider the emissions requirements early in the design of the system. Selecting an appropriate module, switching frequency, edge rates, and applying strategic CM mitigation techniques [2] can reduce the required filters to meet compliance at the end of the design cycle. In addition, there are

opportunities to optimize the system and reduce parasitic elements to achieve EMC with reduced filterering requirements.

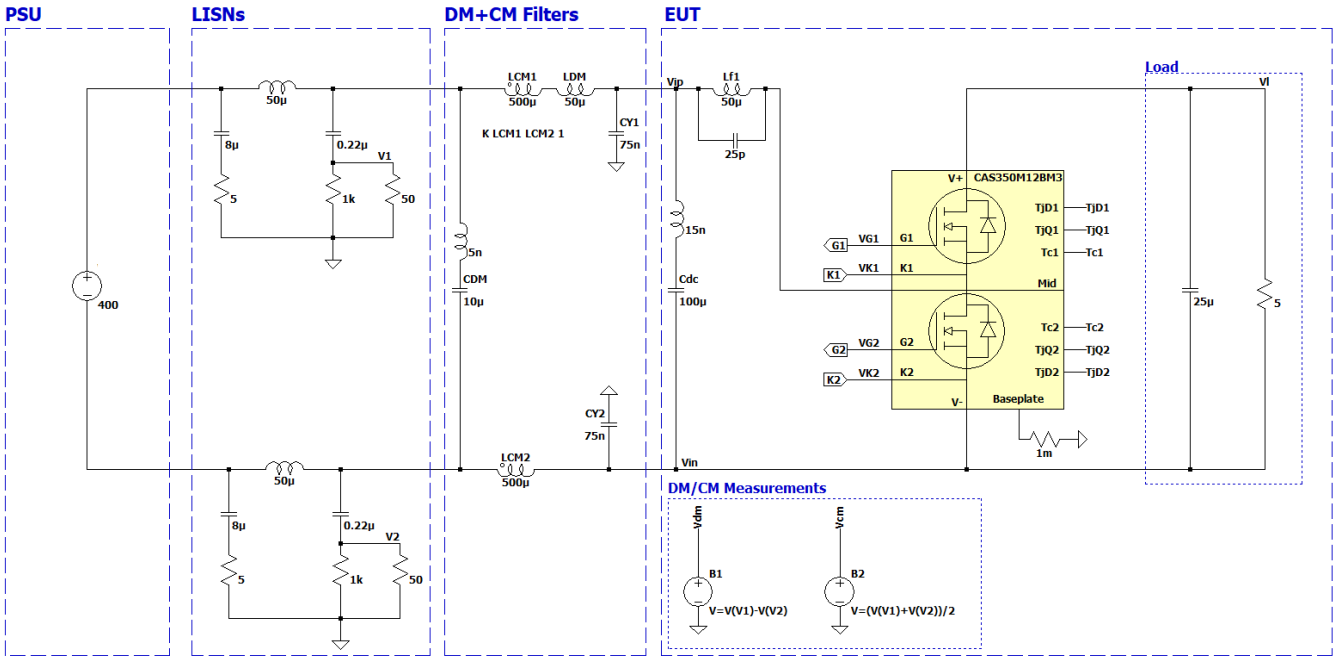

Figure 20: LTspice simulation with DM and CM filters added

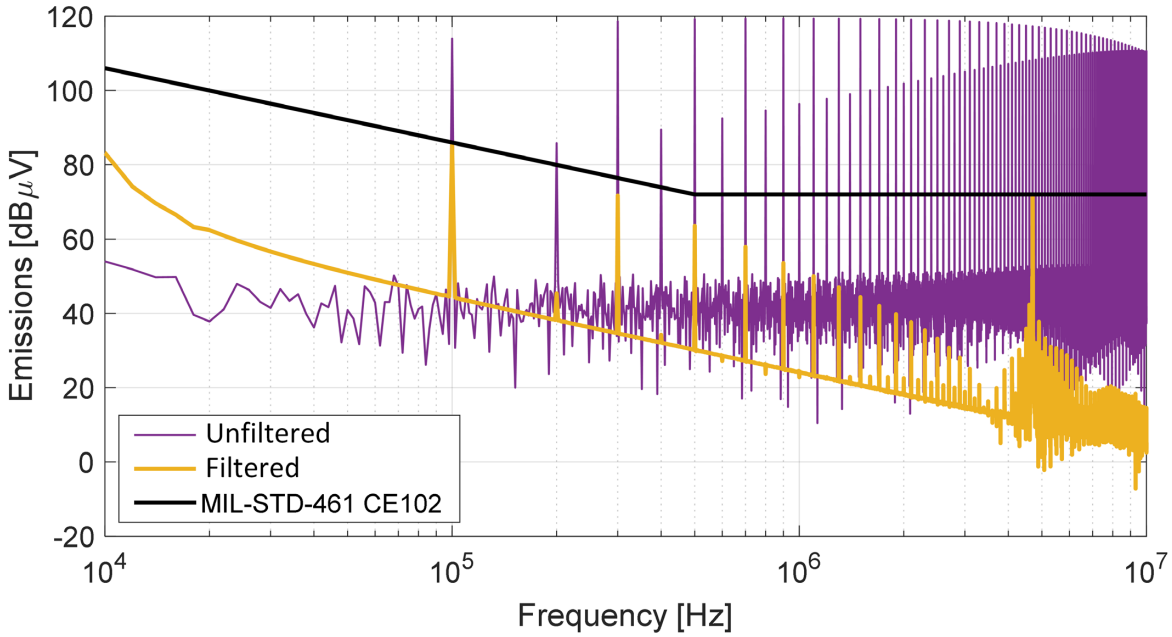

Figure 21: Unfiltered and filtered emissions compared to MIL-STD-461 CE102

3.3 Advanced EMI Mitigation Example

While filtering is effective at reducing EMI, the large filters required to do so are often expensive, bulky, and lossy. When designing high-performance systems, it is necessary to meet EMC requirements while minimizing the size of the EMI filters. This can be done by examining the topology of the power conversion circuit and strategically manipulating the layout or components to cancel CM and DM noise sources. In this section, the CM emissions of a boost converter will be analyzed in order to meet EMC compliance with reduced filter requirements. A circuit diagram of the boost converter is provided in Figure 22. The filter inductor is split onto the upper and lower rails (L_{f1} and L_{f2}). The power loop baseplate capacitances used in this analysis are C_{ug} = 115.1 pF, C_{ag} = 176.9 pF, and C_{lg} = 90.5 pF. These values are equal to the baseplate capacitance of the Wolfspeed BM3 power module.

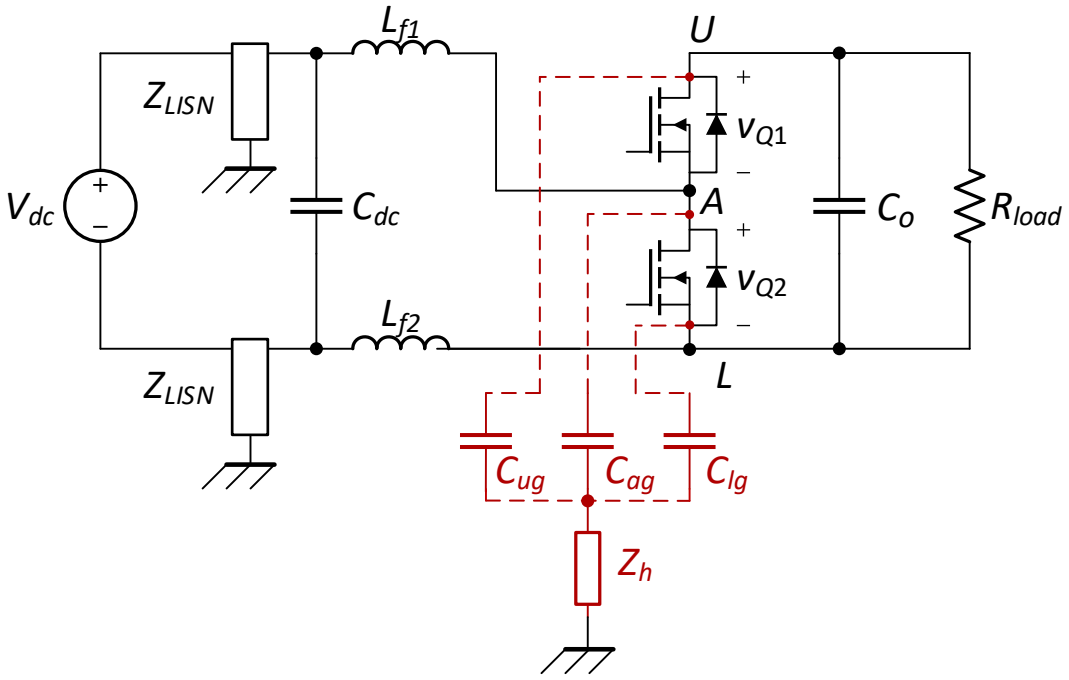

Figure 22: Boost converter circuit with split filter inductors and baseplate capacitances [3]

Per the analysis in [3] and [4], the CM emissions of the boost converter can be decomposed into a common-mode equivalent circuit shown in Figure 23. The voltage sources V_{CM1} and V_{CM2} are defined in equations (3) and (4), respectively. C_{bp} is defined by the sum of the individual baseplate capacitances in equation (5). The voltages V_{Q1} and V_{Q2} are defined across the high-side and low-side switch positions in Figure 22. V_{dc} is defined by the voltage across the C_{dc} capacitor, and V_{Co} is defined by the voltage across the output C_O capacitor. The impedance of the LISN and the filter inductor are added with respect to common-mode currents. The parameter *a* defines the asymmetry of the filter inductors as per equation (6). For example, a system with $a = 0$ would be perfectly balanced, with $L_{f1} = L_{f2}$, and a system with $a = 1$ would be perfectly imbalanced, with all of the inductance on the upper rail.

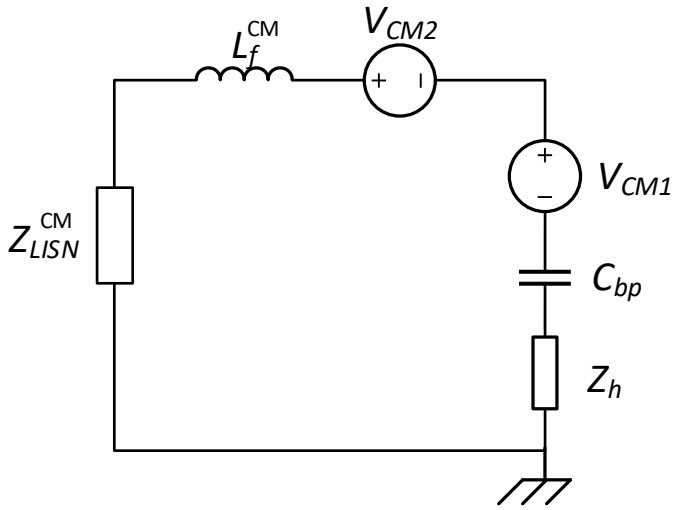

Figure 23: Boost converter common-mode equivalent model circuit [4]

$$V_{CM1} = \frac{1}{2}\left(\frac{C_{ag}}{C_{bp}}\left(V_{Q1} - V_{Q2}\right) + \frac{\left(C_{lg} - C_{ug}\right)}{C_{bp}}V_{Co}\right) \quad (3)$$

$$V_{CM2} = \frac{1}{2}\left(V_{Q2} - a\left(V_{Q2} - V_{dc}\right) - V_{Co}\right) \quad (4)$$

$$C_{bp} = C_{ug} + C_{ag} + C_{lg} \quad (5)$$

$$L_{f1} = \frac{1+a}{1-a}L_{f2}, where\ a \in [-1\ 1] \quad (6)$$

Based on inspection of Figure 23 and equations (3) and (4), several conclusions can be drawn. First, the CM emissions are dependent on the switch voltages V_{Q1} and V_{Q2}. As expected, emissions will increase with 1) faster edge rates, 2) oscillations on transitions, and 3) higher bus voltage. Reduction of parasitic inductance in the high-frequency switching loops and decreasing switching speed (by increasing the gate resistance) will thus reduce emissions. Second, the CM emissions are also dependent on the voltage across the input and output capacitors. Systems with stable voltage across these capacitors will have reduced emissions. This can be achieved by increasing the value of the capacitances and, critically, reducing any parasitic equivalent series inductance on the input and output capacitors. Third, the baseplate capacitances are directly involved in the CM emissions. In particular, the C_{ag} capacitance is multiplied by the switch node voltages (V_{Q1} and V_{Q2}). Thus, devices with higher C_{ag} capacitance ratios will have increased emissions. There is also potential for emission reduction by setting C_{lg} equal to C_{ug}, but this increases complexity and it is often not desired to add additional capacitance near the switching nodes in a real system.

The filter inductor asymmetry, *a*, is easy to change in a real system and offers the potential for cancellation of CM emissions. In [4], the authors manipulate equation (3) to find a general method for determining *a* in order to minimize emissions, given in equation (7). Applying equation (7) to this boost converter system yields a necessary asymmetry factor of *a = 0.0753*. Thus, for this system, the filter inductors can be split to 27 µH and

23.22 µH. This approximately matches the initial L_f specification of 50 µH and meets the asymmetry requirements. The updated LTspice schematic with the split filter inductor is shown in Figure 24.

$$a = 1 - \frac{2C_{ag}}{C_{bp}} \qquad (7)$$

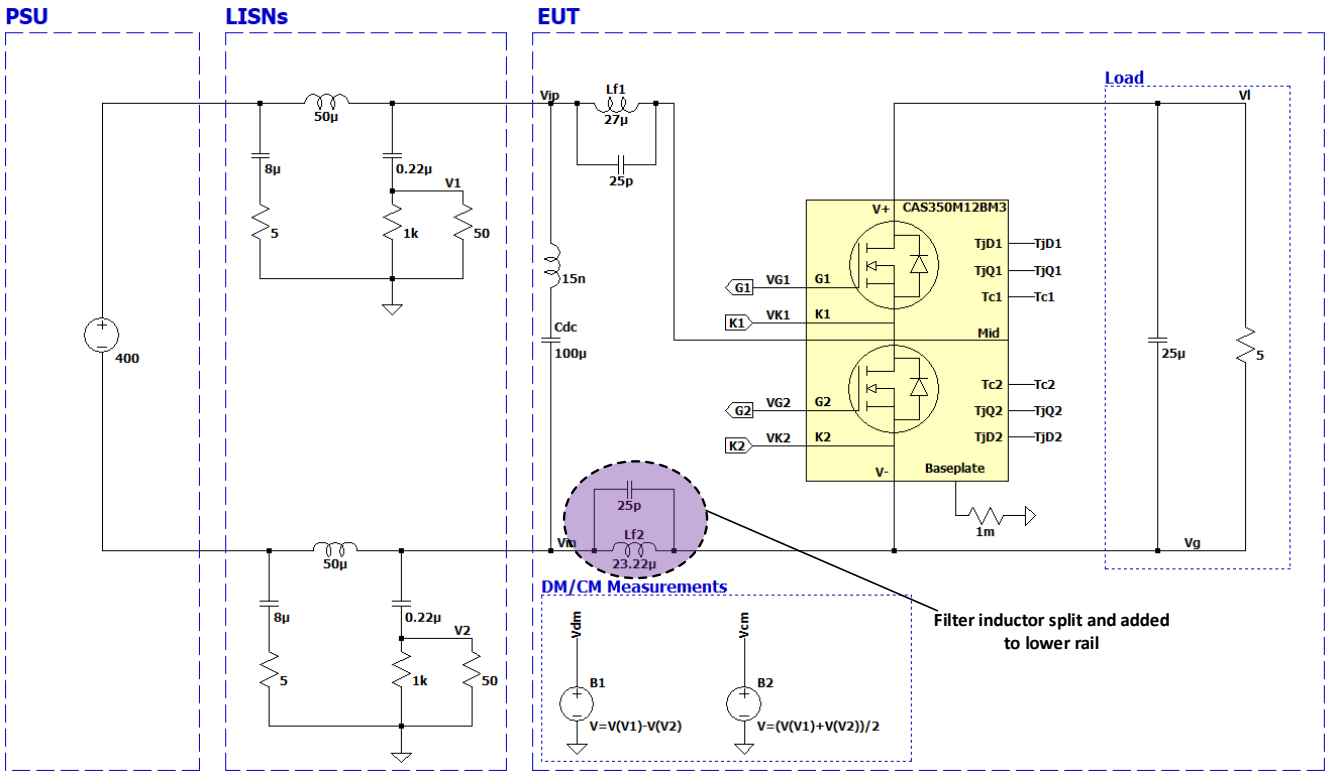

Figure 24: LTspice simulation with asymmetric filter inductor

A comparison of the spectra between the original boost converter with the single filter inductor (Figure 14) and the split filter inductor (Figure 24) is provided in Figure 25. The configuration with the split inductor shows a dramatic decrease in emissions, with up to a 36 dBµV reduction in emissions within the frequency range of MIL-STD-461 CE102. This reduction in emissions is associated with little to no increase in the complexity, size, or cost of the system, and demonstrates a cost-effective method for EMC mitigation for this topology. However, while the system is improved significantly, the emissions still lie above the emission limit line, and must be filtered or mitigated further. Separating the emissions into CM and DM components can provide insight into what types of filters are necessary. Figure 26 shows the CM and DM emission spectra for the split inductor case in . Both the DM and CM noise sources require attenuation across frequency, and therefore the final design will require both DM and CM filters.

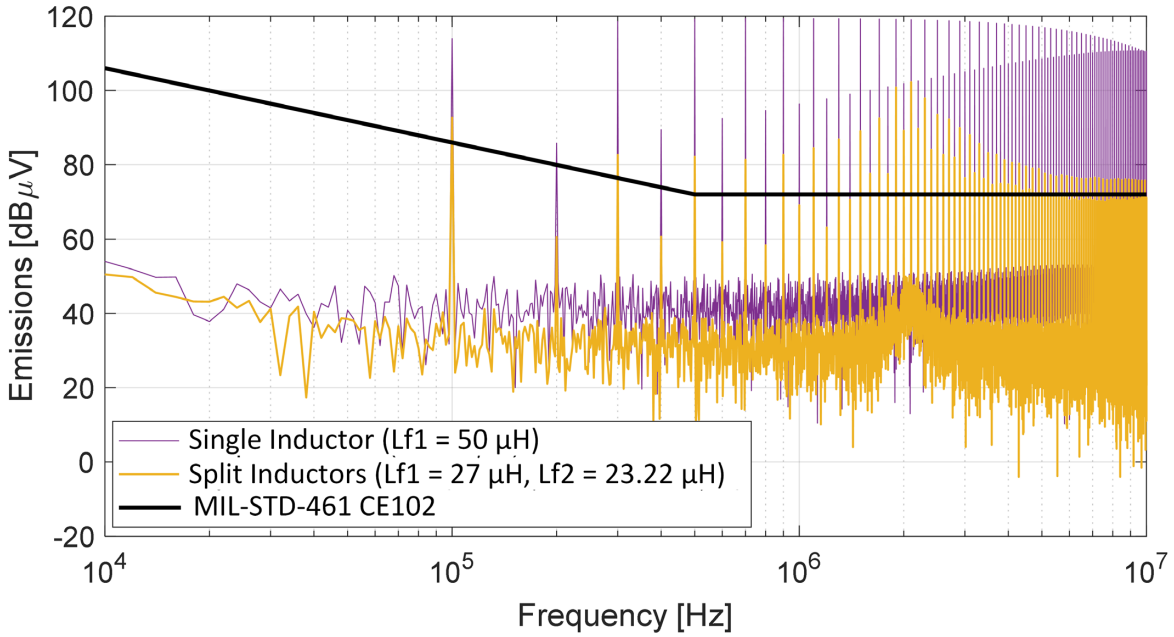

Figure 25: Emission comparison (CM + DM) with single and split filter inductor configuration

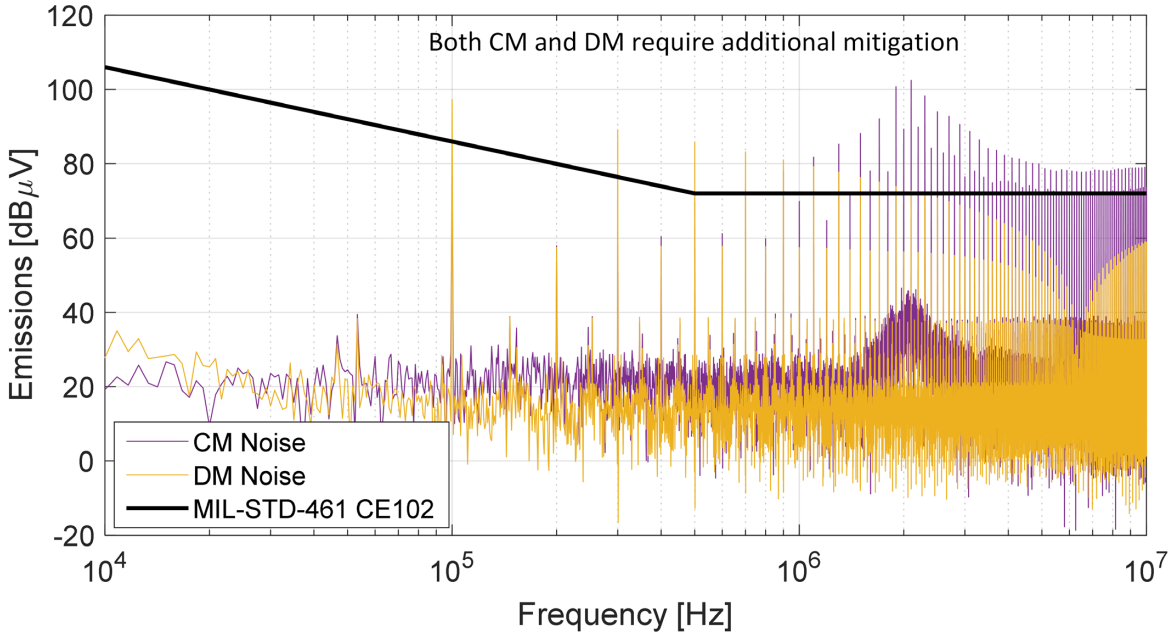

Figure 26: Separated CM and DM emissions for split inductor configuration

The updated LTspice EMC simulation with the addition of the DM and CM filters is shown in Figure 27. The component values were chosen based on the necessary attenuation needed to meet the MIL-STD-461 CE102 specification. To reduce the DM emissions, a 5 µF X-capacitor (CDM) and a 5 µH DM inductor (LDM) were added. To reduce the CM emissions, a 30 µH CM choke (LCM1 and LCM2) and 10 nF Y-capacitors (CY1 and CY2) were added. To accurately model a CM choke in LTspice, an ideal coupling coefficient is defined by the SPICE statement, “K LCM1 LCM2 1”. In addition to these filter components, some resistance was added to the circuit to damp high frequency noise. These are the 100 mΩ resistors in series with CY1 and CY2, and the 1 kΩ resistors in parallel with the filter inductors Lf1 and Lf2. With the addition of these filter components, the simulation predicts that emissions will lie well below the limit line, as shown in Figure 28. Using these strategic CM mitigation techniques, the filter components required to meet compliance are much smaller than was shown in Figure 20. For the DM filter, the required inductance is decreased by 90%, and the required capacitance was decreased by 50%. For the CM filters, the required choke inductance is decreased by 94%, and the required Y capacitors is decreased by 87%. Overall, this demonstrates a significant improvement in the size, cost, and efficiency of the system that was achieved by considering the value of the individual baseplate capacitances in the design.

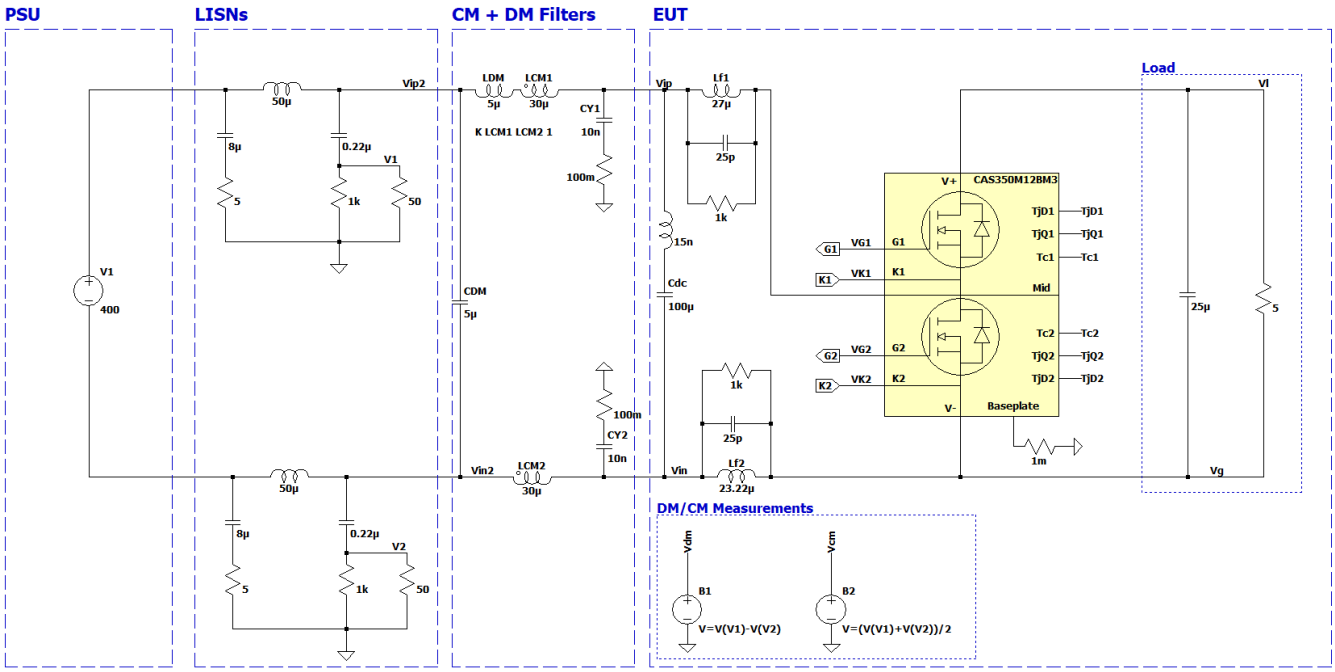

Figure 27: Final simulation design using strategic CM mitigation techniques to minimize filter size

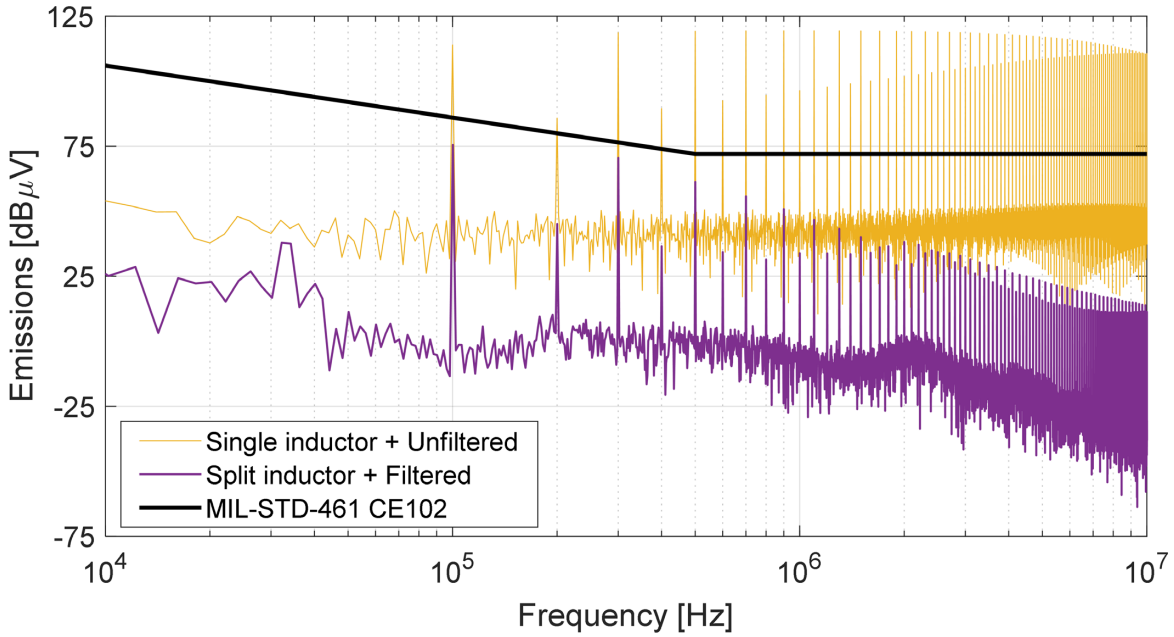

Figure 28: Comparison of the original boost converter circuit with a single inductor to the filtered split inductor configuration

3.4 Notes on using the LTspice Simulation

In this case study, Wolfspeed LTspice models were leveraged to predict the emissions of a boost converter and apply mitigation techniques that leverage the baseplate capacitance values of a module. In some cases, it may be desired to edit or sweep these values in simulation. While this can be done directly in the netlist, it can also be edited on the SpiceLine in LTspice. Right-click the module symbol to bring up the attribute editor, and values for the baseplate capacitances can be specified under either SpiceLine or SpiceLine2. Refer to Figure 29 for an example on how to apply this to a half-bridge power module. The Wolfspeed SPICE User Guide provides additional details on how to customize the model to edit any embedded parasitic parameters.

Attribute	Value	Vis.
Prefix	X	
InstName	U1	
SpiceModel		
Value	CAS350M12BM3	X
Value2		
SpiceLine	Thermals=0 BPC=1 level=1 Rp=100	
SpiceLine2	Cug=115.1p Cag=176.9p Clg=90.5p	

Figure 29: Example on how to specify the baseplate capacitance values of a half-bridge LTspice module

4. Baseplate Capacitance Measurement Techniques

Determining the baseplate capacitance of each individual substrate region is crucial for accurately predicting the CM leakage currents through the baseplate in applications. There are several established methods for determining the baseplate capacitance, each with their own tradeoffs. The first is through the use of finite element analysis (FEA) simulation software, as demonstrated in [5], [6]. However, this method requires detailed knowledge of the power module internal structure, geometry, and dielectric constants, which is not generally available. The second method is to isolate each individual substrate by removing the wirebonds within the module, which was performed by the authors of [7], [8]. This method provides accurate results, and the measurements can be performed using commercially available impedance analyzers and LCR meters. However, destroying a module for measurement purposes is generally undesirable, particularly in the case of prototype modules. In addition, this technique prevents system designers from using the characterized sample in emissions testing. Instead, a non-destructive impedance analysis method that can be applied to functional power modules [9] will be described.

4.1 Challenges

The challenge associated with measuring the per-terminal parasitic baseplate capacitance of a power modules stems from the interaction of the individual substrate areas due to the semiconductor capacitances. A notional diagram of attempting to measure a half-bridge power module is provided in Figure 30. The DC+, phase, and DC- terminals of the half-bridge power module are denoted U, A, and L, respectively. The gate terminals are omitted from this diagram for simplicity. The semiconductor capacitances ($C_{gd,}$ C_{ds}, C_{gs}) are often several orders of magnitude larger than the baseplate capacitances. Thus, even when the devices are turned off, they present a lower impedance at high frequency than the capacitances due to the ceramic, and therefore the top layers (U, A, and L) are effectively shorted together at high frequency, preventing direct measurement of the per-terminal baseplate capacitances. For the notional half-bridge module, these capacitances can be divided into three quantities: the capacitance between nodes U and G (C_{UG}), between A and G (C_{AG}), and between L and G (C_{LG}), where G denotes the baseplate of the module.

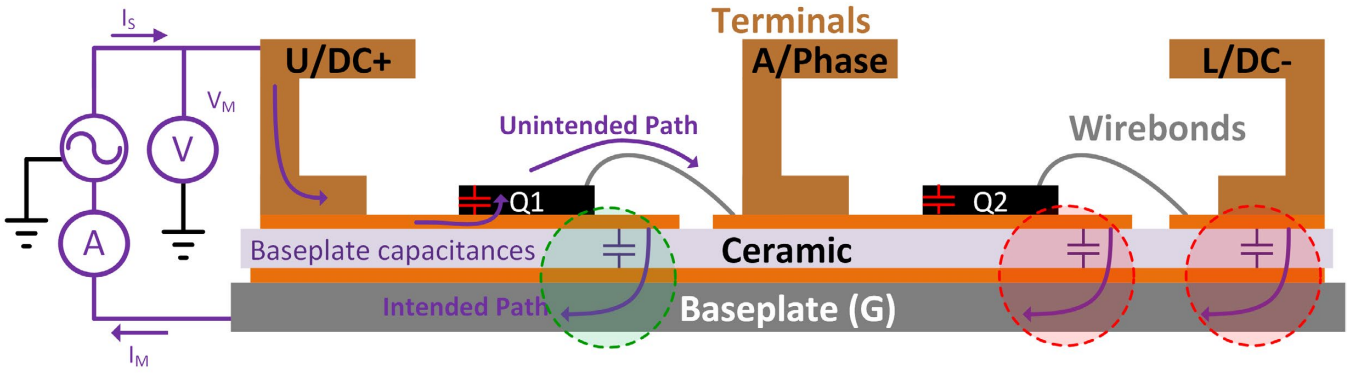

Figure 30: Notional diagram attempting to measure the C_{UG} with an impedance analyzer

As an example, attempting to measure C_{UG} for a fully populated module involves the circuit shown in Figure 31. During measurement, the stimulus current from the impedance analyzer flows through two paths: the first is the desired path through C_{UG}, and the second is an undesired path through C_{Q1}. Because the device capacitances

are much larger than the baseplate capacitances, this undesired current will readily flow through both C_{AG} and C_{LG}. As a result, the observed capacitance measurement effectively becomes the sum of all three baseplate capacitances, as indicated in (8). This will also occur when measurements are performed from the A or L terminals. To demonstrate this issue, C_{UG}, C_{AG}, and C_{LG} measurements were performed using this method on a Wolfspeed CAS350M12BM3 half-bridge power module. The total baseplate capacitance (C_{BP}) was also measured by physically shorting the power terminals (U, A, L) together and measuring between this combined node and the baseplate. The results for these four measurements are provided in Table 1. The individual BPC measurements are all nearly equivalent to the total BPC, as predicted by (8). Thus, this technique cannot be used to determine the desired per-terminal coupling values, and alternative measurement methods are needed.

$$C_{Meas} = C_{UG} + C_{AG} + C_{LG} \qquad (8)$$

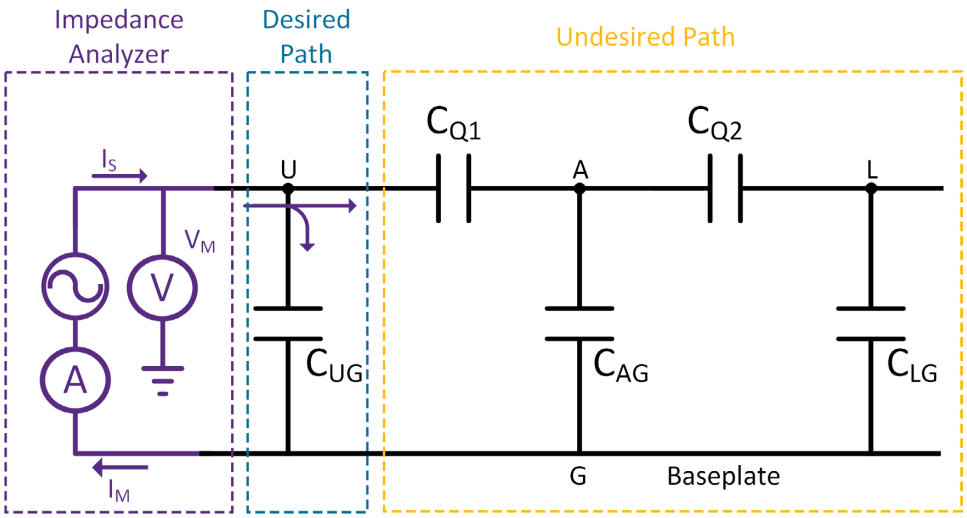

Figure 31: Circuit diagram of a C_{UG} measurement performed on a populated module

Table 1: Invalid Baseplate Capacitance Measurements

Measurement	Measured Value, 10 kHz (pF)
C_{BP}	382.9
C_{UG}	381.0
C_{AG}	382.6
C_{LG}	380.5

4.2 Destructive Technique

The traditional method for removing parallel paths introduced by the device capacitances is to cut the wirebonds (or other interconnections) between each substrate region, as shown in Figure 32. Because no path exists for the stimulus current to travel across the substrate regions, the baseplate capacitances can be measured individually. Figure 33 shows an example of a Wolfspeed CAB450M12XM3 power module with severed wirebonds for BPC measurements. However, this technique has several issues. First, this method is destructive and prevents future use of the module. This is particularly problematic for prototype devices, but in general prevents EMI testing on the characterized module. Second, the results obtained from this method are sensitive to the module tear-down approach. If the substrates are not isolated properly, the measurements will not be correctly isolated and there may be no indication that this has occurred. Finally, while removing the wirebonds removes the contribution of the device capacitances, there may still be a parasitic capacitance between the substrate regions or terminals themselves. While this capacitance is generally small, it presents a parallel current path similar to the device capacitances that can skew the measured results. This error is most prevalent for smaller modules which have correspondingly smaller baseplate capacitances

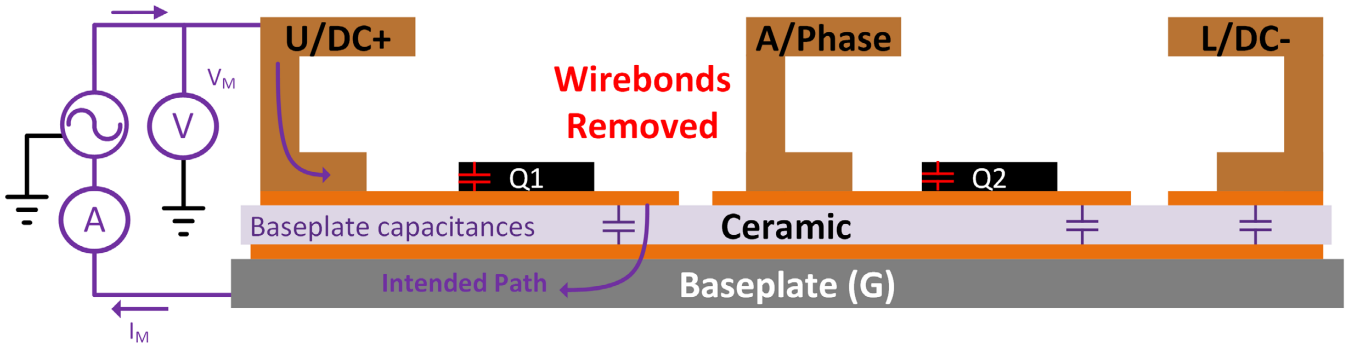

Figure 32: Notional diagram of traditional C_{UG} measurement approach with the wirebonds removed

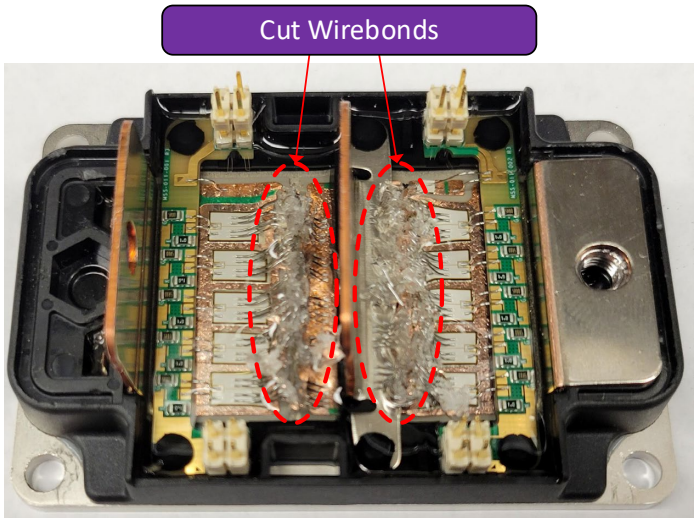

Figure 33: CAB450M12XM3 power module with severed wirebonds for BPC measurements

4.3 Guard-Sink Technique

A preferred method is to employ an approach that leverages the guard terminal of the impedance analyzer (or LCR meter) to sink any current that flows through the undesired parallel path during measurement. This method is inspired by techniques used to measure C_{RSS} of SiC MOSFETs as discussed in [10]. It can be applied directly to the module terminals and does not require access to the internal geometry. It is also less prone to measurement error because it removes any current that flows through parasitic capacitances from the measurement and does not require isolating the substrate regions. Figure 34 shows a notional diagram of applying this technique to a power module for a C_{UG} measurement, and Figure 35 presents the equivalent circuit. A cable is connected from the 'A' terminal to the guard terminal of the impedance analyzer. The current that flows through C_{Q1} will flow through the guard terminal and not flow through the ammeter of the impedance analyzer. Thus, the measurement current is isolated to the contribution of C_{UG}. This process is then repeated by changing the location of the stimulus and guard terminals to measure the baseplate capacitance of each substrate region. The guard connection should be applied to any terminals that are coupled capacitively to the measurement terminal.

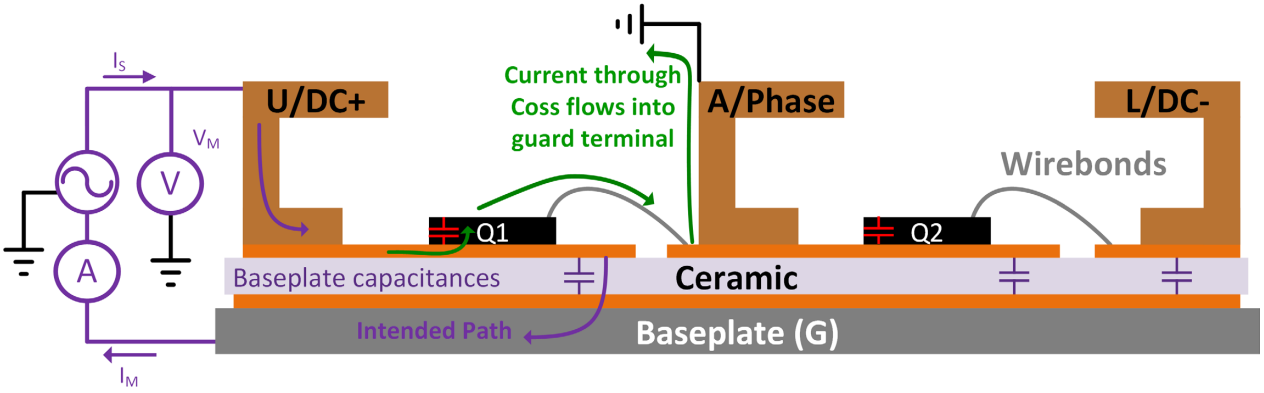

Figure 34: Notional diagram of C_{UG} measured using the guard-sink technique

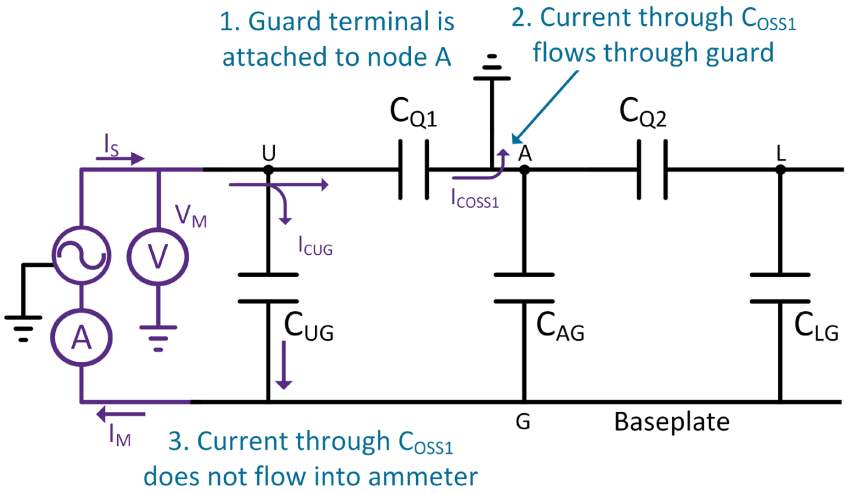

Figure 35: Circuit diagram of a proposed measurement technique with addition of the guard terminal

4.4 Case Study

A case study was performed to validate the proposed measurement technique. The baseplate capacitances of three Wolfspeed power modules were measured using both the traditional (i.e., destructive) measurement technique and the proposed measurement technique. The selected power modules and their representative circuit diagrams are shown in Figure 36. The blue node labels on the circuit diagrams indicate the baseplate capacitance regions that are measured. For example, the baseplate capacitance measured from node G_1 would be referred to as C_{G1G}. Two Wolfspeed half-bridge power modules (CAS350M12BM3 and CAB450M12XM3) and a Wolfspeed six-pack power module (CCB021M12FM3) were selected for analysis. Performing the analysis on the half-bridge and six-pack modules will demonstrate the that the approach can be applied to different module topologies. The half-bridge BM3 and XM3 power modules also feature differences in their layout of the gate terminals that influences the analysis. For the BM3 module, the gate interconnects are located directly on the substrate that is attached to the ceramic. For the XM3 module, the gate interconnects are located on a PCB that is located *above* the ceramic. This difference leads to significantly higher baseplate capacitances on the gate terminals for the BM3 module. This nuance is important because the individual contribution of the gate terminals is not always considered.

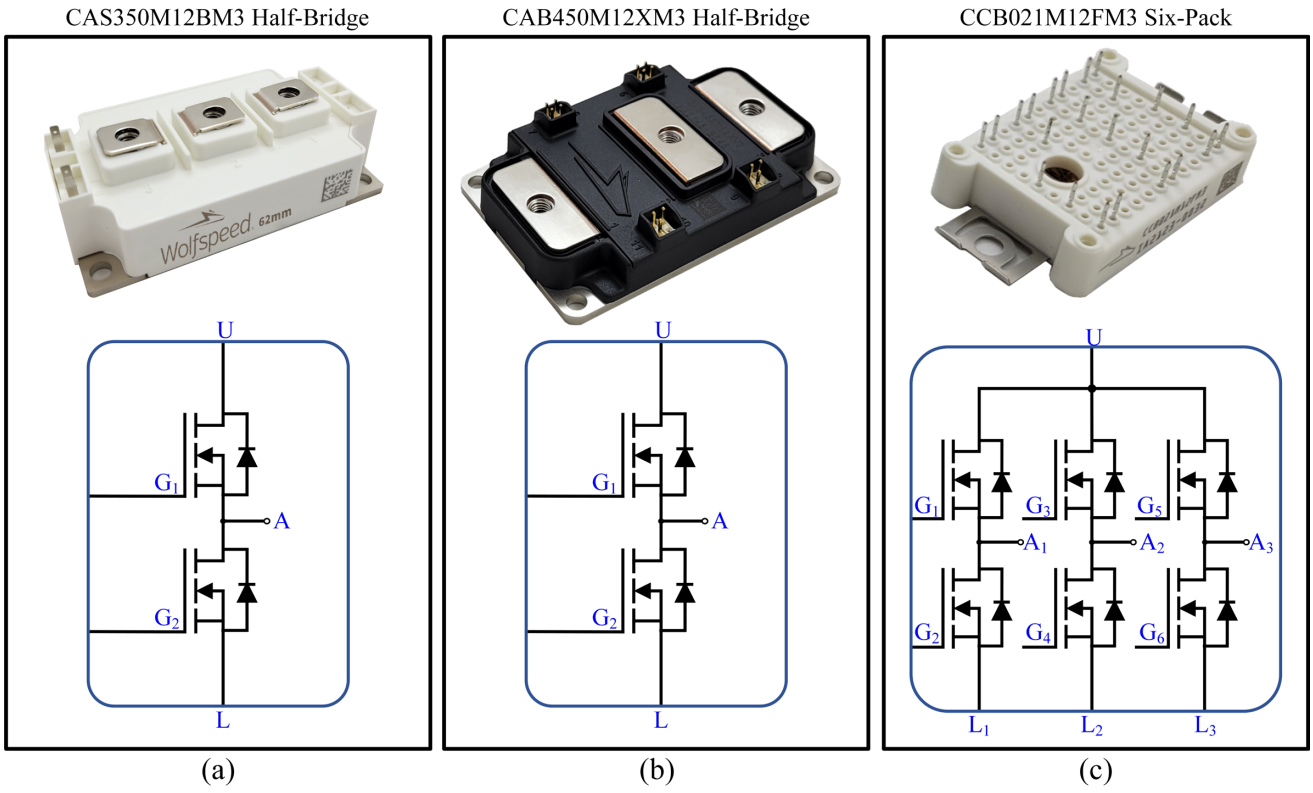

Figure 36: Circuit diagrams with baseplate capacitance nodes in blue for (a) a CAS350M12BM3 half-bridge power module, (b) an CAB450M12XM3 half-bridge power module, and (c) a CCB021M12FM3 six-pack power module

In order to achieve the most direct comparison of the proposed and traditional measurement methods, each technique is performed on the same module. However, because the traditional technique is destructive, it must be performed last. Thus, the sequence for this testing is as follows. First, the guard-sink technique is applied to

the module to measure each baseplate capacitance. Second, the module is de-lidded and the necessary wirebonds are removed. This includes the kelvin wirebonds, as the kelvin interconnects are measured separately and added to the appropriate substrate value. Third, each module terminal (including the kelvin terminals) is measured with respect to the baseplate, but no guard terminals are attached. Finally, the kelvin interconnect contributions are added to its respective source node. For example, for the half-bridge modules in Figure 36 (a) and Figure 36 (b), the contribution of the high-side kelvin is added to *A*, and the contribution of the low-side kelvin is added to *L*. The results from these measurements are referred to as the "traditional technique."

4.4.1 Half-Bridge Power Modules

The proposed measurement technique was first applied to the half-bridge modules in Figure 36 (a) and Figure 36 (b). Because the topology of the modules is the same, the measurement process for each is identical. An example measurement for C_{LG} of the BM3 power module using an E4990A impedance analyzer is provided in Figure 37. The positive stimulus lead of the test fixture is connected to the 'L' terminal, and the return lead is attached to the baseplate. Stranded copper cables are used to attach the 'A' and 'G_2' nodes to the guard terminal of the impedance analyzer. The measurements of these capacitances have metrology requirements that are not stringent; low inductance leads and tight measurement loops are not necessary for accurate results. Instead, focus should be on reducing parasitics capacitance between the leads and properly applying an open compensation.

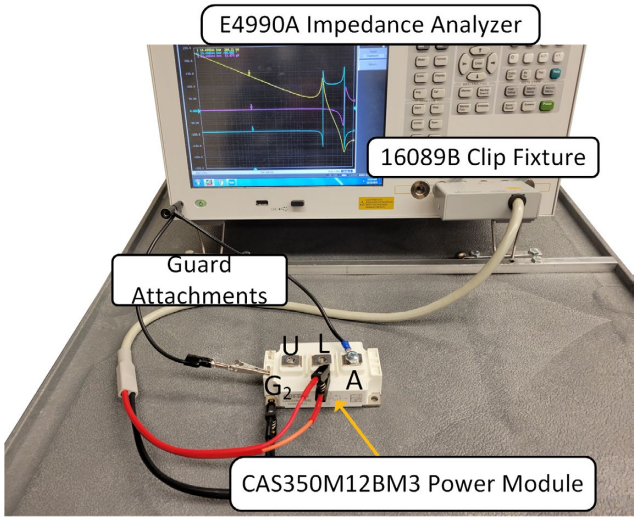

Figure 37: Example measurement of C_{LG} using the proposed measurement technique on a CAS350M12BM3 power module with an E4990A impedance analyzer

One consideration when performing this analysis is the length of the guard connections and the frequency of extraction. Figure 38 shows an example measurement of C_{LG} for a CAS350M12BM3 power module. The capacitance measurement is constant between 1 kHz to 50 kHz, but begins decreasing. Multiple resonances are observed in the impedance and phase measurements between 250 kHz – 1 MHz. These resonances are caused by interactions between the inductance of the guard terminal cable and the baseplate capacitance. At higher frequencies, the impedance of the guard cable inductance will exceed the impedance of the baseplate

capacitance, and a resonance will occur. Measurements near and after the resonance are invalid. Thus, minimizing the impedance of the guard connection will improve the valid frequency range for measurement. For the metrology shown in Figure 37, the maximum valid frequency for measuring C_{UG} is 50 kHz; therefore, results were extracted at 10 kHz.

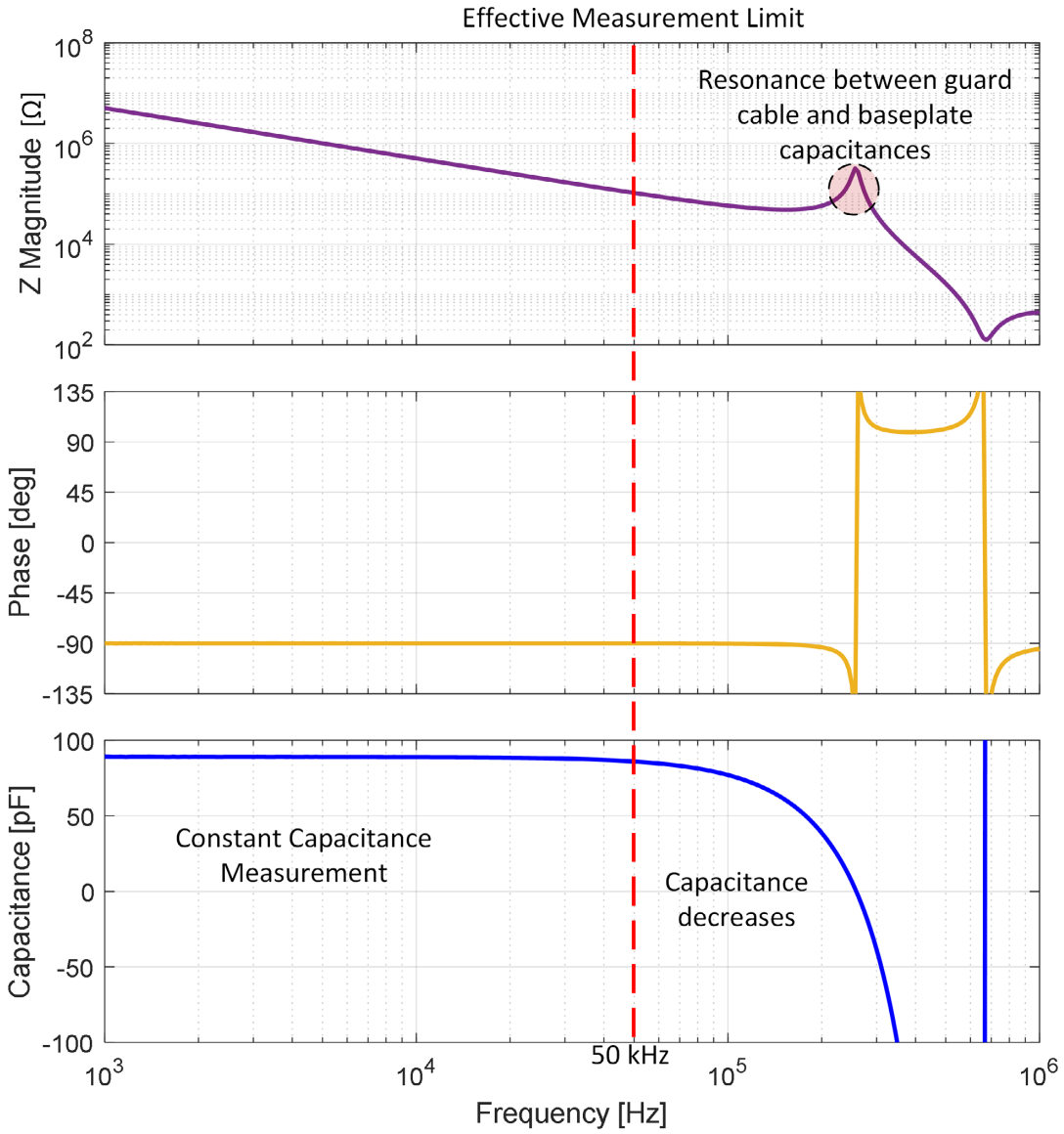

Figure 38: Example baseplate capacitance measurement across frequency using the guard-sink technique

This process was repeated for each of the five baseplate capacitance measurements described for the half-bridge case. The necessary connection of the stimulus and the guard terminals for each measurement is provided in Table 2. For all measurements, the stimulus return path is connected to the module baseplate. A comparison of the results obtained with this technique and results obtained using the traditional (destructive) technique for both the CAS350M12BM3 and CAB450M12XM3 power modules is also provided in Table 2. 'C_{BP}' is the measured total baseplate capacitance and 'C_{total}' is the sum of C_{UG}, C_{AG}, C_{LG}, C_{G1G}, and C_{G2G}. Any observed

difference between the calculated and measured total baseplate capacitance indicates the presence of error, as these two quantities should be equivalent.

Table 2: Measurement Connections and Results for Half-Bridge Modules

Meas.	Stim+	Guards	CAS350M12BM3 Guard-sink (10 kHz) [pF]	CAS350M12BM3 Traditional (10 kHz) [pF]	CAB450M12XM3 Guard-sink (10 kHz) [pF]	CAB450M12XM3 Traditional (10 kHz) [pF]
C_{UG}	U	A	115.1	115.0	175	178.4
C_{AG}	A	U, L	158.9	156.5	255.4	264.5
C_{LG}	L	A	52.9	55.9	4.1	17.6
C_{G1G}	G1	U, A	18	17.3	0.3	7.9
C_{G2G}	G2	A, L	37.6	34.9	0.7	6
C_{BP}	U, A, L, G1, G2	None	382.9	382.9	436.1	436.1
C_{total}	-	-	382.6	379.6	435.5	474.4

For the CAS350M12BM3 power module, the individual baseplate capacitance measurements made with the guard-sink technique agree well with those from the traditional technique. Discrepancies of 0.1 pF (0.1%), 2.4 pF (1.5%), 3 pF (5.5%), 0.7 pF (3.9%), and 2.7 pF (7.4%) are observed for C_{UG}, C_{AG}, C_{LG}, C_{G1G}, and C_{G2G}, respectively. Not only do these results demonstrate good agreement between the guard-sink technique and the traditional technique, but the observed differences are not indicative of error in the proposed method. In fact, the guard-sink technique shows better agreement between C_{BP} (382.5 pF) and C_{total} (382.6 pF) than the traditional technique (379.6 pF). The disagreement between C_{total} and C_{BP} for the traditional technique suggests that there is some error in the measurements, and thus it is likely that some of the discrepancies between the two methods is caused by errors in the traditional technique.

For the CAB450M12XM3 power module, C_{UG} and C_{AG} measurements made with the guard-sink technique agree well with those from the traditional technique. Discrepancies of 3.4 pF (1.9%) and 9.1 pF (3.5%) are observed for C_{UG} and C_{AG}, respectively. However, the traditional technique shows much higher values for C_{LG}, C_{G1G}, and C_{G2G}. This is likely due to parasitic coupling between these terminals and the U and A terminals. In the XM3 internal structure, the L, G_1, and G_2 nodes are not bonded to the ceramic material. Rather, they are elevated above the ceramic and are surrounded by an encapsulant, as shown in Figure 39. These terminals are therefore capacitively coupled to the U/A substrate regions. Even after the wirebonds are severed, this parasitic capacitance forms a shunt path that is similar to C_{OSS} in which current can flow which causes an overestimate of the baseplate capacitance of those regions. For the proposed measurement technique, current that flows through this parasitic capacitance sinks through the guard terminal, and thus does not introduce error. This theory is supported by comparisons of the C_{BP} and C_{total} terms. For the guard-sink technique, the summed baseplate capacitance (435.5 pF) agrees well with the measured total baseplate capacitance (436.1 pF). However, the sum of the individual capacitances for the traditional technique is 474.4 pF, which is much higher than the actual value. Finally, the XM3 power module demonstrates a case in which the model can be simplified when performing EMI analysis. Because the coupling of the L, G_1, and G_2 terminals is 2-3 orders of magnitude smaller than that of the U and A terminals, these values can be omitted from the analysis entirely.

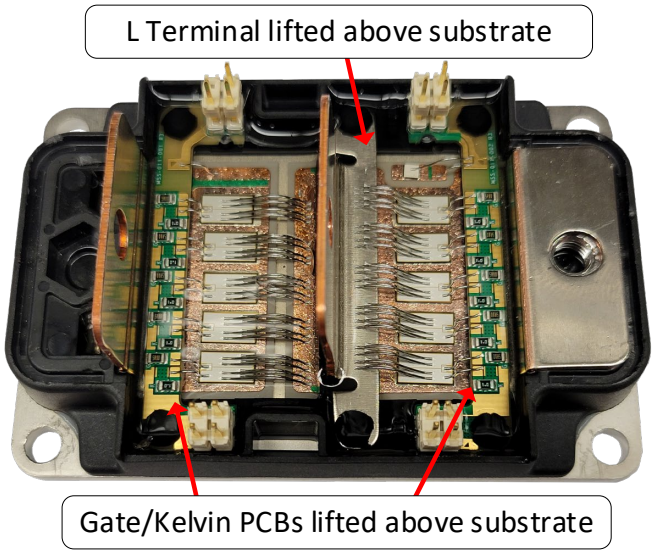

Figure 39: CAB450M12XM3 with the lid removed; annotations describe how several of the XM3 substrate regions lie above the ceramic

From this analysis, several conclusions can be drawn. First, the guard-sink technique agrees well with the traditional approach for half-bridge power modules. However, due to parasitic capacitance between the terminals, the traditional technique overpredicts the baseplate capacitance when the coupling is very small. This is supported by the fact that the guard-sink technique demonstrates greater self-consistency between the total baseplate capacitance measurement and the sum of the individual capacitance measurements. Second, the guard-sink technique is easier to implement, non-destructive, and does not require detailed knowledge of the internal structure. Thus, this technique facilitates baseplate capacitance measurements and provides increased accuracy over the traditional approach.

4.4.2 FM Six-Pack Power Module

Analysis of the CCB021M12FM3 six-pack power module in Figure 36 (c) is more complex than the half-bridge case due to the increased number of individual substrate regions, but the analysis process remains the same. An example measurement for C_{UG} of the FM3 power module using an E4990A impedance analyzer is provided in Figure 40. The positive stimulus lead of the test fixture is connected to the 'U' terminal, and the return lead is attached to the baseplate. Clip lead cables are used to attach the 'G_1', 'G_2', 'G_3', 'A_1', 'A_2', and 'A_3' nodes to the guard terminal of the impedance analyzer. Again, while minimizing the impedance of the guard connections will improve the valid frequency range for measurement, it is not necessary to use low inductance leads and tight measurement loops. For the configuration shown in Figure 40, the baseplate capacitance values were extracted at 10 kHz.

This process was repeated for each of the 13 per-terminal baseplate capacitances described for the six-pack module case. The necessary connection of the stimulus and the guard terminals for each measurement is provided in Table 3. For all measurements, the stimulus return path is connected to the module base. A comparison of the results obtained with this technique and results obtained using the traditional technique is also provided in Table 3. Overall, while the two methods show a similar distribution of the baseplate capacitances, measurements made with the traditional method are all several pF higher than the proposed

method. These differences are likely due to the small parasitic coupling between the substrate regions that introduce error into the traditional technique measurements. These errors become apparent when comparing the measured 'C_{BP}' and summed 'C_{total}' values in Table 3. The guard-sink technique demonstrates a 1.2 pF (0.6%) difference between C_{BP} and C_{total}, while the traditional technique shows a 33.5 pF (15.3%) difference. Thus, the guard-sink technique again shows greater self-consistency than the traditional method and is the more accurate approach. This analysis also shows that the guard-sink technique can be readily applied to more complex power module topologies.

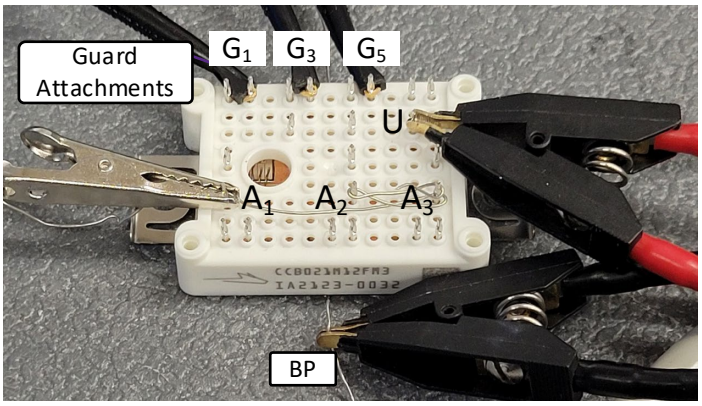

Figure 40: Example measurement of C_{UG} using the proposed measurement technique on a CCB021M12FM3 power module with an E4990A impedance analyzer

Table 3: Measurement Connections and Results for FM Six-Pack Module

Measurement	Stimulus+	Guard(s)	Guard-sink Technique (10 kHz) [pF]	Traditional Technique (10 kHz) [pF]
C_{UG}	U	A_1, A_2, A_3, G_1, G_3, G_5	48.7	51.0
C_{A1G}	A_1	U, G_1, G_2, L_1	24.4	28.1
C_{A2G}	A_2	U, G_3, G_4, L_2	24.9	29.2
C_{A3G}	A_3	U, G_5, G_6, L_3	26.7	30.3
C_{L1G}	L_1	A_1, G_2	12.8	16.5
C_{L2G}	L_2	A_2, G_4	14.5	18.0
C_{L3G}	L_3	A_3, G_6	17.1	19.6
C_{G1G}	G_1	U, A_1	5.6	6.8
C_{G2G}	G_2	A_1, L_1	5.3	7.1
C_{G3G}	G_3	U, A_2	5.6	6.8
C_{G4G}	G_4	A_2, L_2	5.6	7.6
C_{G5G}	G_5	U, A_3	5.9	6.9
C_{G6G}	G_6	A_3, L_3	5.7	7.2
C_{BP}	U, A_{1-3}, L_{1-3}, G_{1-6}	None	201.6	201.6
C_{total}	-	-	202.8	235.1

5. Wolfspeed Module Tabulated Baseplate Capacitances

The guard-sink baseplate capacitance measurement technique has been applied to all current commercial Wolfspeed power modules and is provided in this section for customer use. The values presented represent the values from a typical module, but minor differences may be observed between module samples.

5.1 Half-Bridge and Rectifier Modules

For Wolfspeed half-bridge and rectifier power modules, the equivalent circuit is shown in Figure 41 and the tabulated baseplate capacitances for each module product is provided in Table 4. All values are measured at 10 kHz using a Keysight® E4990A impedance analyzer. The notation for each capacitance is given by the labeled node names in Figure 41 to ground. For example, the baseplate capacitance from DC+ (denoted *U*) to ground (denoted *G*) is given by 'C_{UG}'.

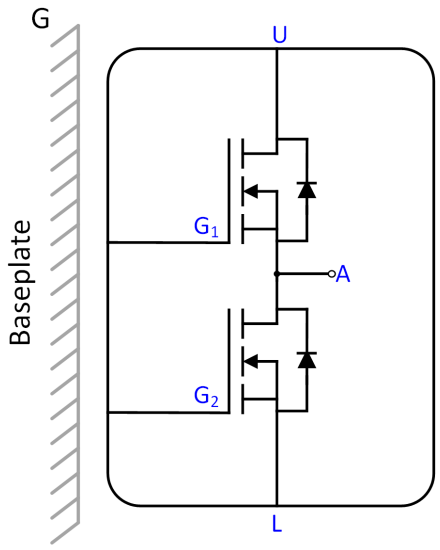

Figure 41: Node description for Half-bridge and rectifier modules

Table 4: Summary of Wolfspeed Power Module Baseplate Capacitances: Half-Bridge

Platform	C_{UG} [pF]	C_{AG} [pF]	C_{LG} [pF]	C_{G1G} [pF]	C_{G2G} [pF]	C_{BP} [pF]
BM	115.1	158.9	52.9	18	37.6	382.9
XM	175	255.4	4.1	0.3	0.7	436.1
HM	315.5	397.9	231.5	2.76	5.6	941.28
HN	317.6	396.3	222.9	0	0	924.07
FM	61.5	85.3	41.9	13.1	12.8	187.8
DM	78.6	91.5	55.8	15.0	15.8	249.2
GM3 (A)	44.5	103.5	50.4	19.7	17.2	198
GM3 (M)	81.3	187.1	90.2	34.2	29.2	354.2
1.2 kV GM4	83	165	81	24	24	375
2.3 kV GM4	50	90	38	10	10	198

5.2 Full-Bridge Modules

For Wolfspeed full-bridge power modules, the equivalent circuit is shown in Figure 42 and the tabulated baseplate capacitances for each module product is provided in Table 5. All values are measured at 10 kHz using an E4990A impedance analyzer. The notation for each capacitance is given by the labeled node names in Figure 42 to ground. For example, the baseplate capacitance from G1 to ground is given by 'C_{G1G}'.

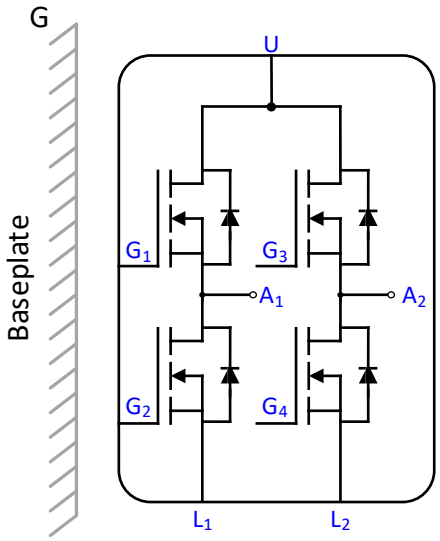

Figure 42: Node description for full-bridge modules

Table 5: Summary of Wolfspeed Power Module Baseplate Capacitances: Full-Bridge

Platform	C_{UG} [pF]	C_{A1G} [pF]	C_{A2G} [pF]	C_{L1G} [pF]	C_{L2G} [pF]	C_{G1G} [pF]	C_{G2G} [pF]	C_{G3G} [pF]	C_{G4G} [pF]	C_{BP} [pF]
FM3	49.6	44.2	41.9	16.1	15.8	9.7	5.2	7.5	5.5	190.1
1.2 kV GM4	92	69	81	36	38	16	13	12	12	364

5.3 Six-Pack Modules

The six-pack modules do not share identical internal topologies, and thus the circuits and measurement results are distinguished in the following results.

5.3.1 FM Modules

For Wolfspeed FM six-pack power modules, the equivalent circuit is shown in Figure 43 and the tabulated baseplate capacitances for each module product is provided in Table 6. All values are measured at 10 kHz using an E4990A impedance analyzer. The notation for each capacitance is given by the labeled node names in Figure 43 to ground. For example, the baseplate capacitance from G1 to ground is given by 'C_{G1G}'.

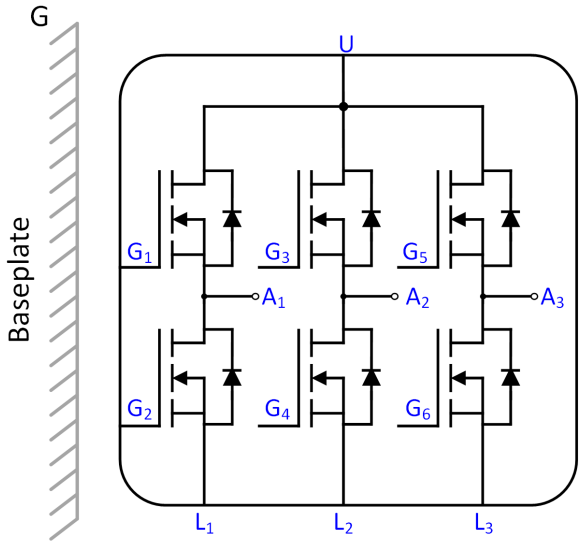

Figure 43: Node description for FM six-pack modules

Table 6: Summary of Wolfspeed Power Module Baseplate Capacitances: FM Six-Pack

Platform	C_{UG} [pF]	C_{A1G} [pF]	C_{A2G} [pF]	C_{A3G} [pF]	C_{L1G} [pF]	C_{L2G} [pF]	C_{L3G} [pF]	C_{G1G} [pF]	C_{G2G} [pF]	C_{G3G} [pF]	C_{G4G} [pF]	C_{G5G} [pF]	C_{G6G} [pF]	C_{BP} [pF]
FM3	48.7	24.4	24.9	26.7	12.8	14.5	17.1	5.6	5.3	5.6	5.6	5.9	5.7	201.6

5.3.2 GM Modules

For Wolfspeed GM six-pack power modules, the equivalent circuit is shown in Figure 44 and the tabulated baseplate capacitances for each module product is provided in Table 7. All values are measured at 10 kHz using an E4990A impedance analyzer. The notation for each capacitance is given by the labeled node names in Figure 44 to ground. For example, the baseplate capacitance from U2 to ground is given by 'C_{U2G}'.

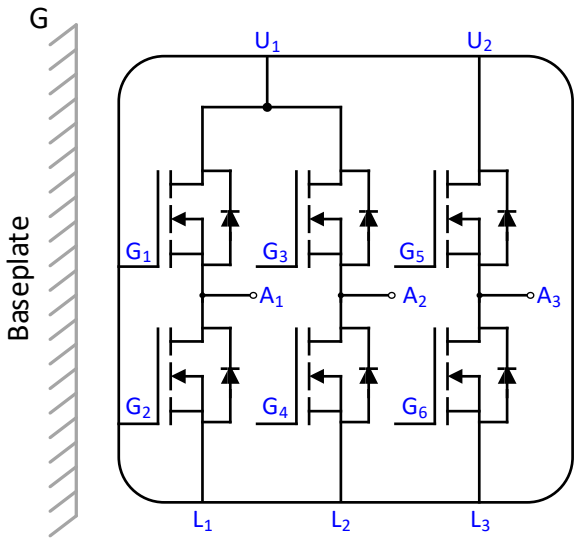

Figure 44: Node description for GM six-pack modules

Table 7: Summary of Wolfspeed Power Module Baseplate Capacitances: GM Six-Pack

Platform	C_{U1G} [pF]	C_{U2G} [pF]	C_{A1G} [pF]	C_{A2G} [pF]	C_{A3G} [pF]	C_{L1G} [pF]	C_{L2G} [pF]	C_{L3G} [pF]	C_{G1G} [pF]	C_{G2G} [pF]	C_{G3G} [pF]	C_{G4G} [pF]	C_{G5G} [pF]	C_{G6G} [pF]	C_{BP} [pF]
GM3	50.4	26.1	52.5	47.8	54.2	19.7	17.2	31.1	8.3	7.7	10.1	9.6	7.8	8.1	343.4

5.3.3 YM Modules

For Wolfspeed YM six-pack power modules, the equivalent circuit is shown in Figure 45 and the tabulated baseplate capacitances for each module product is provided in Table 8Table 8: Summary of Wolfspeed Power Module Baseplate Capacitances: YM Six-Pack. All values are measured at 10 kHz using an E4990A impedance analyzer. The notation for each capacitance is given by the labeled node names in Figure 45 to ground. For example, the baseplate capacitance from U2 to ground is given by 'C_{U2G}'.

The YM module features three parallel half-bridges with identical substrates, therefore $C_{U1G} = C_{U2G} = C_{U3G}$ and so on.

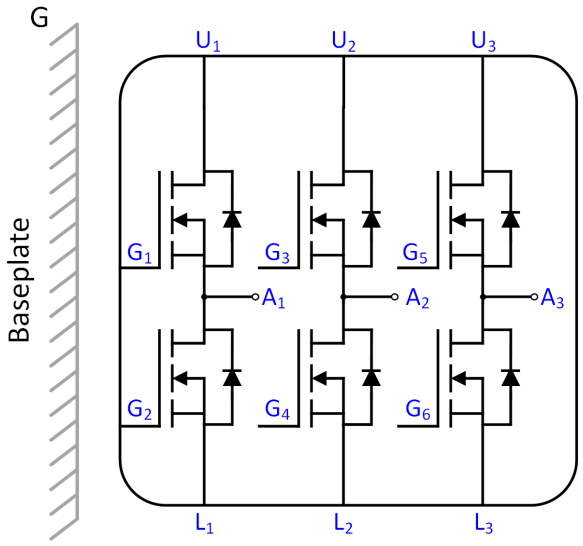

Figure 45: Node description for YM six-pack modules

Table 8: Summary of Wolfspeed Power Module Baseplate Capacitances: YM Six-Pack

Platform	C_{U1G}, C_{U2G}, C_{U3G}, [pF]	C_{A1G}, C_{A2G}, C_{A2G} [pF]	C_{L1G}, C_{L2G}, C_{L2G} [pF]	C_{G1G}, C_{G3G}, C_{G5G} [pF]	C_{G2G}, C_{G4G}, C_{G6G} [pF]	C_{BP} [pF]
YM3	243.1	249.4	62.9	13.3	10.2	583

5.4 Common-Drain T-Type Modules

For Wolfspeed T-Type power modules, the equivalent circuit is shown in Figure 46 and the tabulated baseplate capacitances for each module product is provided in Table 9. All values are measured at 10 kHz using an E4990A impedance analyzer. The notation for each capacitance is given by the labeled node names in Figure 46 to ground. For example, the baseplate capacitance from G11 to ground is given by 'C_{G11G}'.

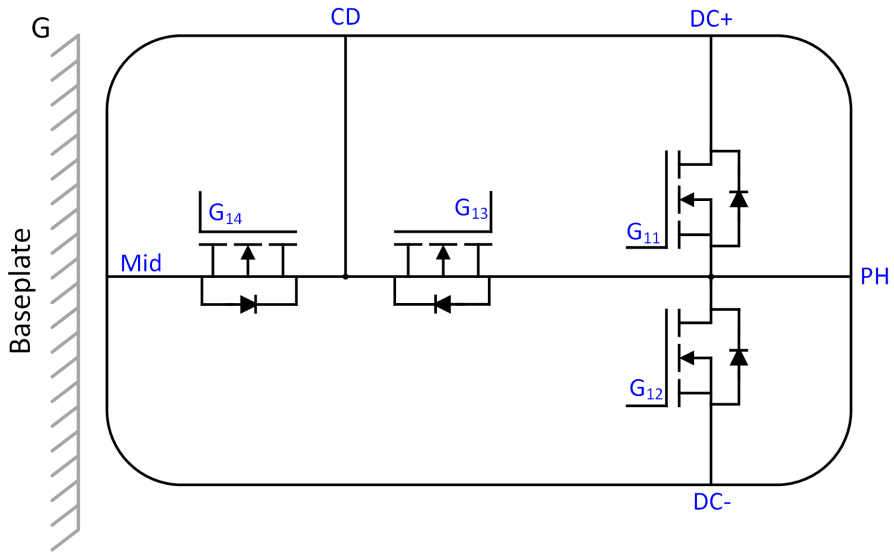

Figure 46: Node description for GM T-Type modules

Table 9: Summary of Wolfspeed Power Module Baseplate Capacitances: T-Type

Platform	C_{DC+G} [pF]	C_{MidG} [pF]	C_{PHG} [pF]	C_{CDG} [pF]	C_{DC-G} [pF]	C_{G11G} [pF]	C_{G12G} [pF]	C_{G13G} [pF]	C_{G14G} [pF]	C_{BP} [pF]
1.2 kV GM4	65	37	121	81	28	10	12	11	10	370

Revision History

Date	Revision	Changes
September 2023	1	Initial release
March 2024	2	Added DM power module baseplate capacitance Updated images and formatting
March 2025	3	Added new Gen4 Wolfpack and YM3 baseplate capacitance values

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