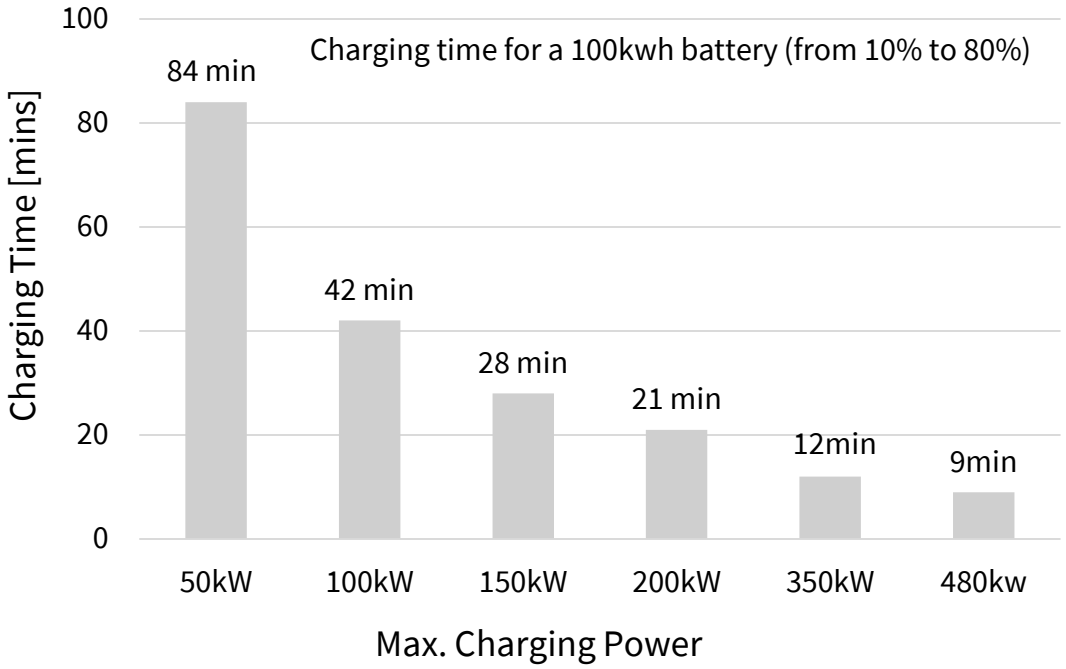
Design Challenges and Considerations of Wolfspeed 60kW LLC Converter

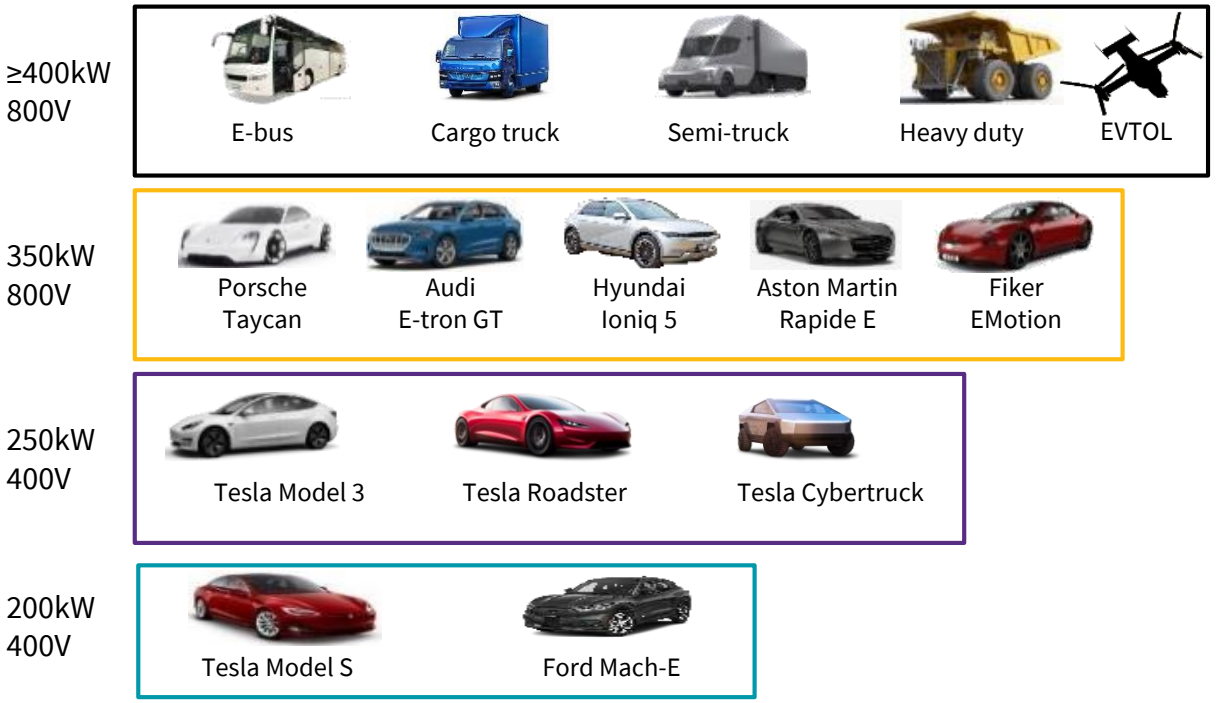
CONTENTS

SPECIFICATIONS AND DESIGN CHALLENGES

TREND FOR EV DC FAST CHARGING: INCREASED POWER AND VOLTAGE

- ## Charging Power vs. Charging Time
  - Max. Charging Power for Selected EV from Major Automakers

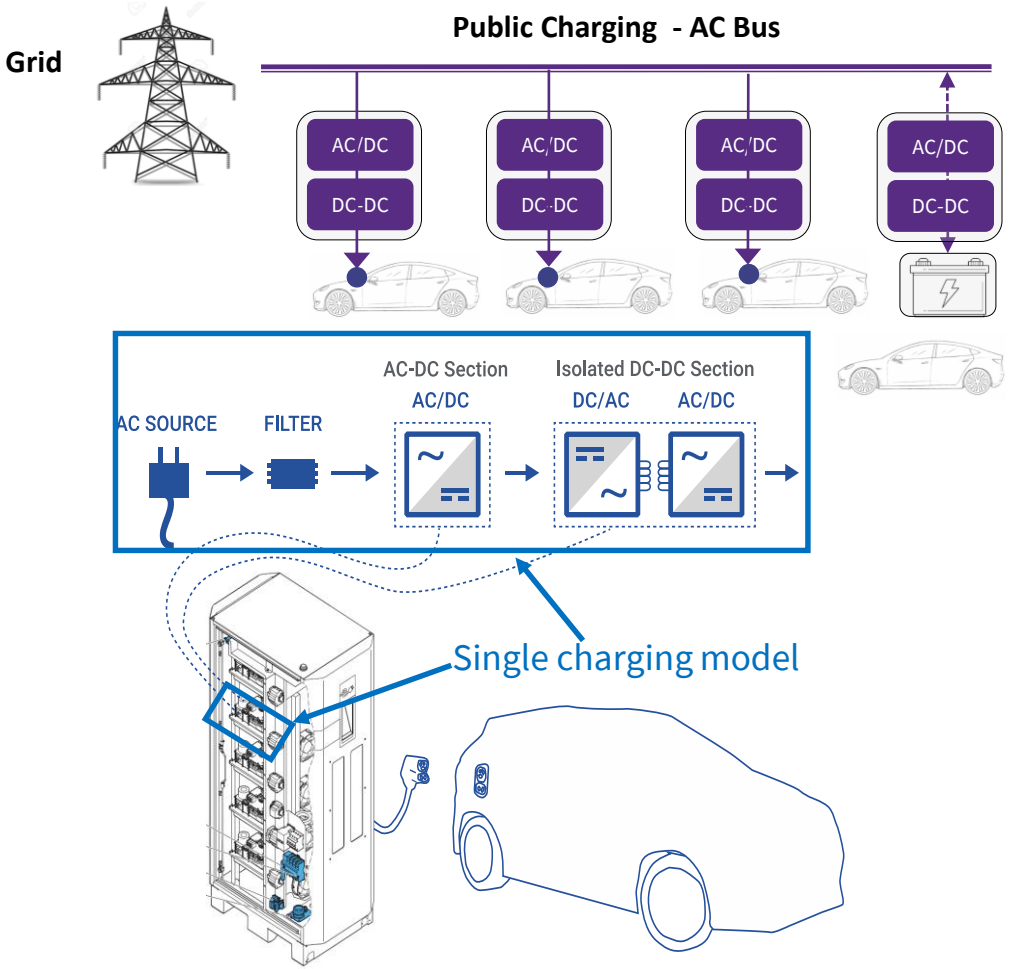


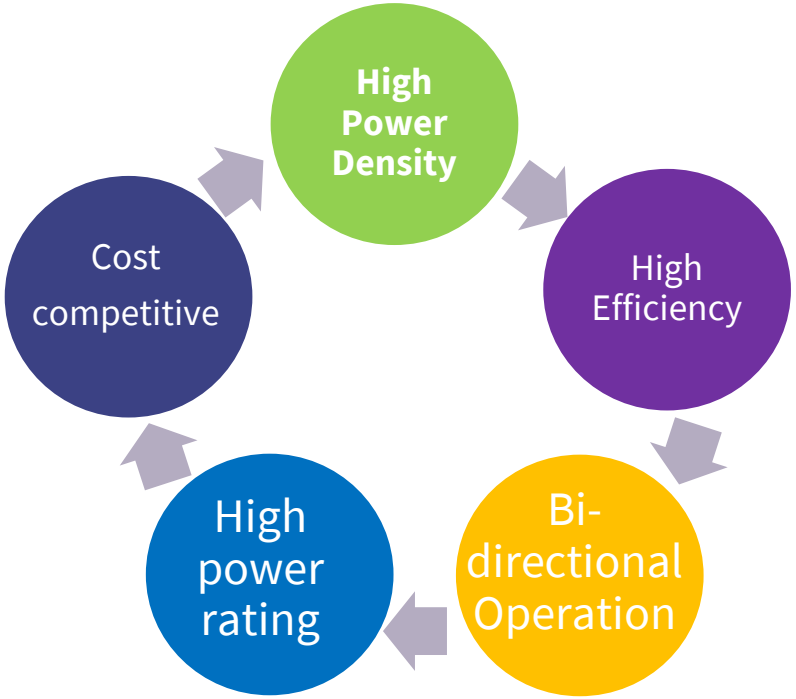


- **EV owners**: Resolve mileage anxiety, better charging experience
- **Automakers:** Selling point for mainstream and high-end cars
- **Charging point operators:** Shorter charging time, higher turn over, more cashflow

Source: Bloomberg New Energy Finance, company press releases, and European Commission, Supercharge. Info.

DC FAST CHARGER – CHALLENGE AND TREND

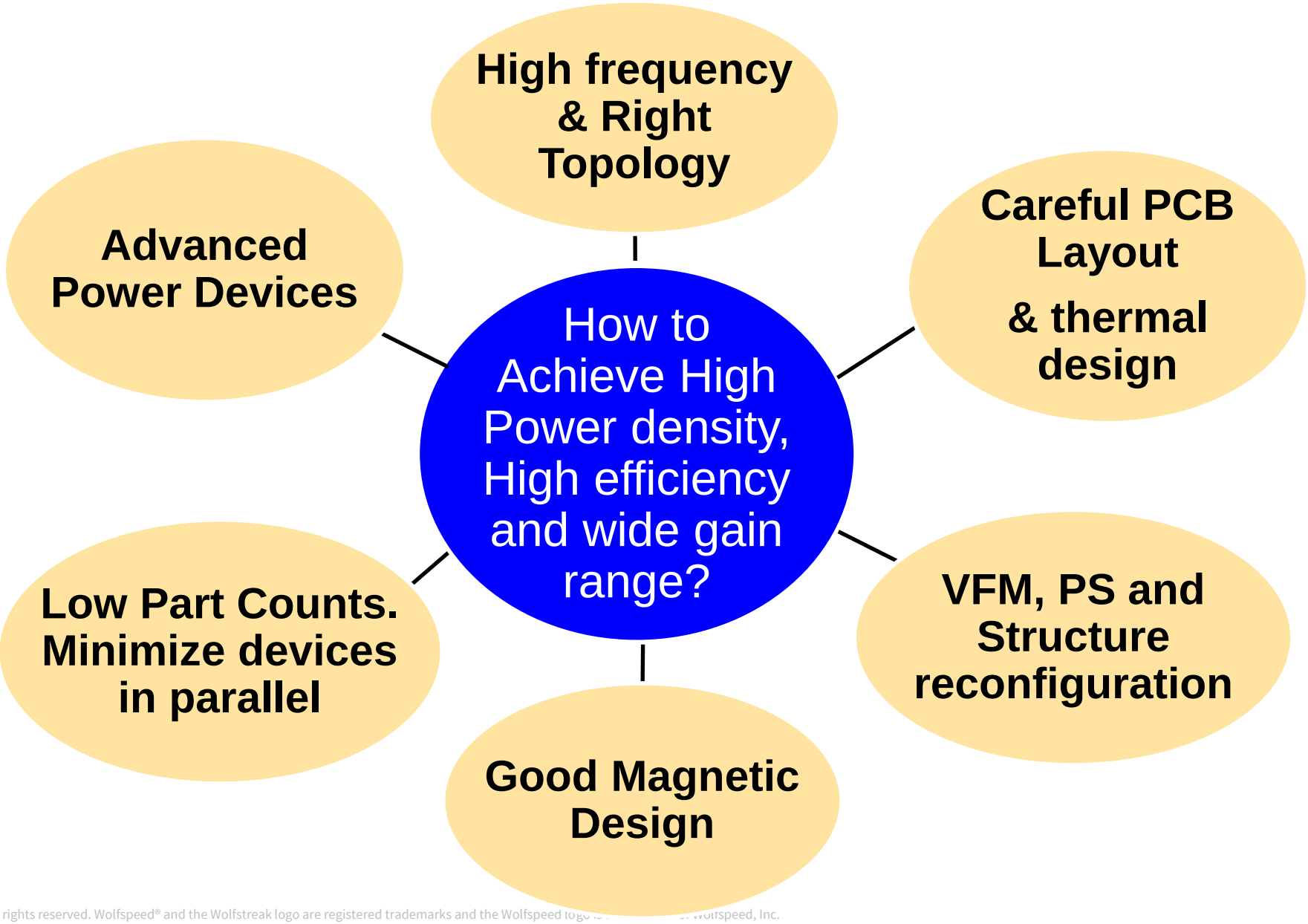




Trend

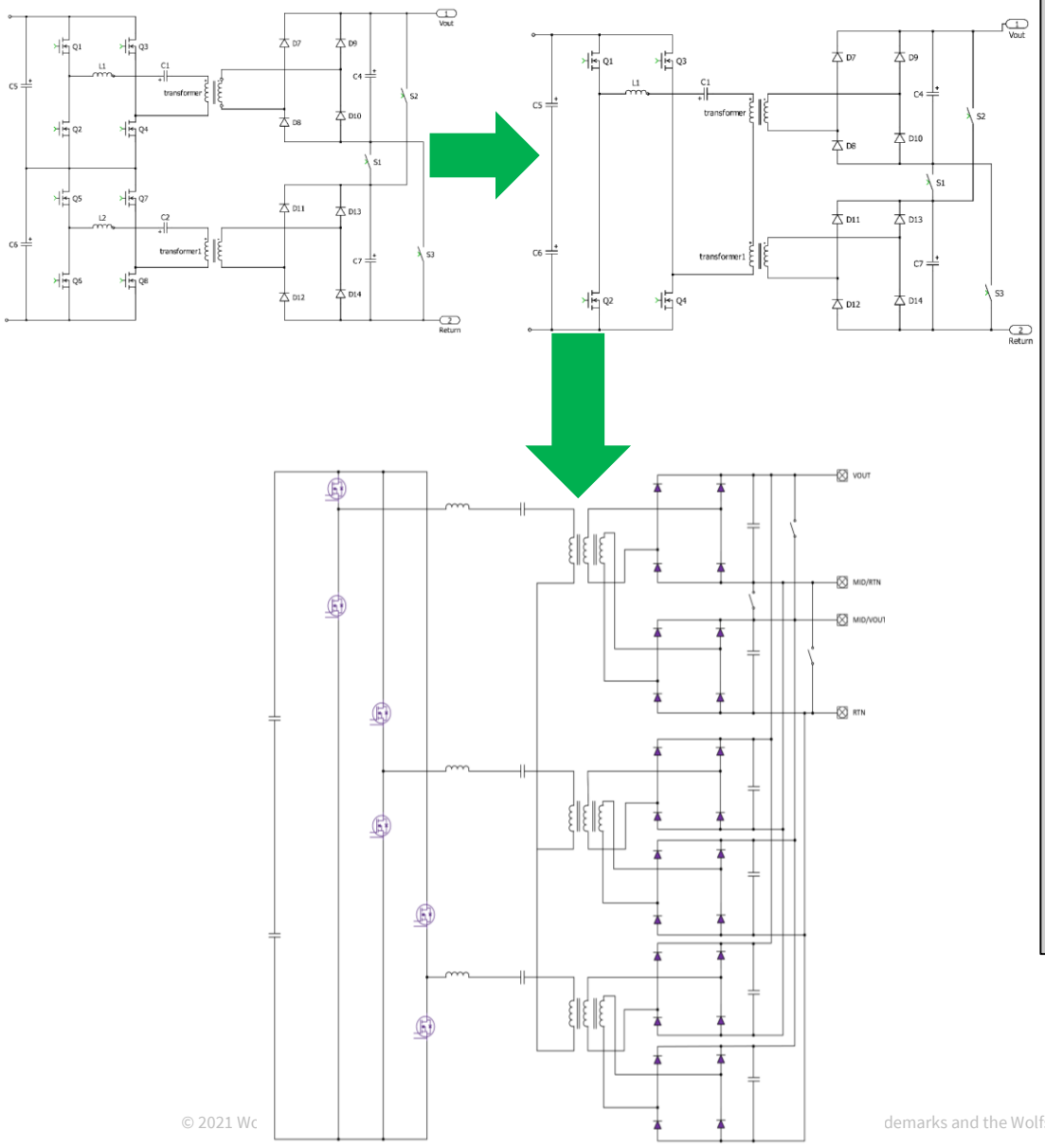
- Very wide output voltage range: 200V-1000V
- High efficiency, high power density and competitive cost
- Increasing power level for each module: 15kW/20kW → 30kW, 40kW and 60kW

HIGH POWER DENSITY, HIGH EFFICIENCY, WIDE VOLTAGE RANGE



TOPOLOGY SELECTION

TOPOLOGY SELECTION : 30KW-60KW BLOCKS | DCDC UNIDIRECTIONAL



Three-Phase LLC

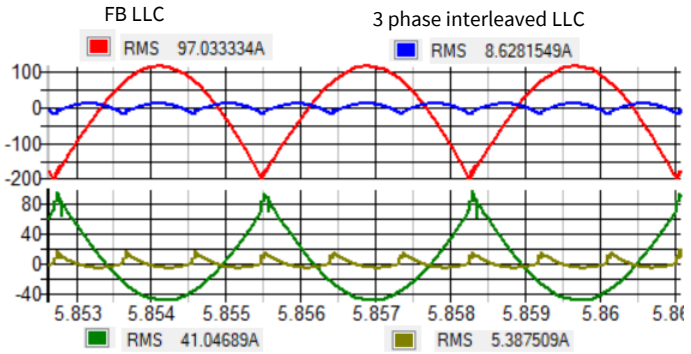
30kW design
- 6x 1200V 40mOhm SiC or
- 6x 1200V 32mOhm SiC

60kW design
- 12x 1200V 40mOhm SiC or
- 12x 1200V 32mOhm SiC

BENEFITS	CHALLENGES
• Low input current ripple |	• Tolerance of resonant C,L and magnetizing Lm can cause unbalanced currents
• **Low output ripple** | **Smaller output Capacitor**	• Complex vector control although three phase analysis applies
• Uniform distribution of Power to Three Phase on Primary	
• Flexible discrete solution with 1x or 2x SiC FET per position	
• **Scalable** to lower phases (shedding) or higher number of phases	

Output ripple current @300V/200A

DC bus ripple current @300V/200A

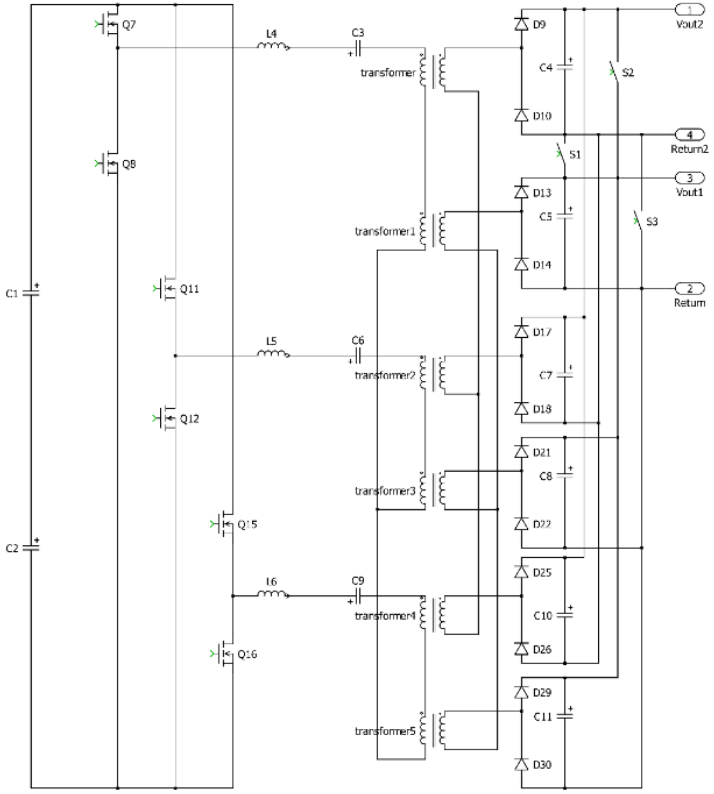


TOPOLOGY SELECTION

A

6 Transformers

Half Bridge for output rectifier

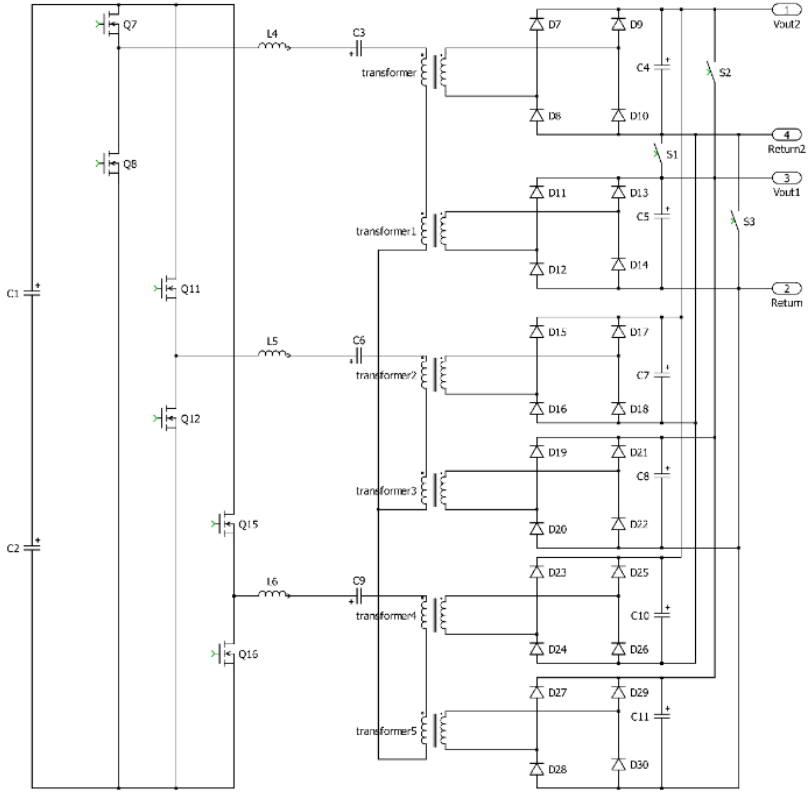


Current sharing concerns on Si output rectifiers in parallel; EMI concern due to large loop

B

6 Transformers

Full Bridge for output rectifier

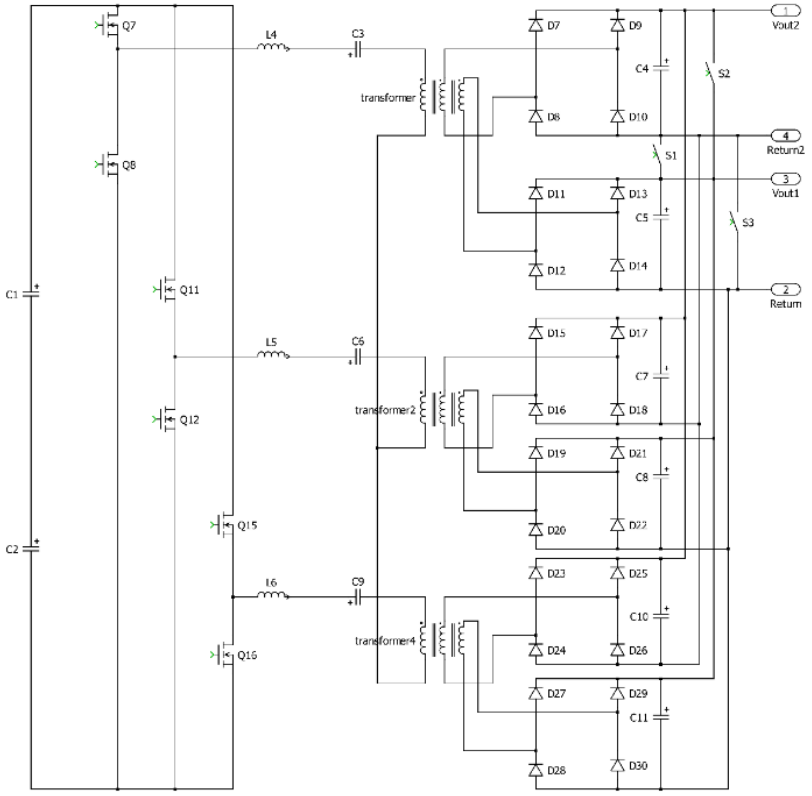


Voltage sharing concerns

C

3 Transformers

Full Bridge for output rectifier



V/I sharing concerns

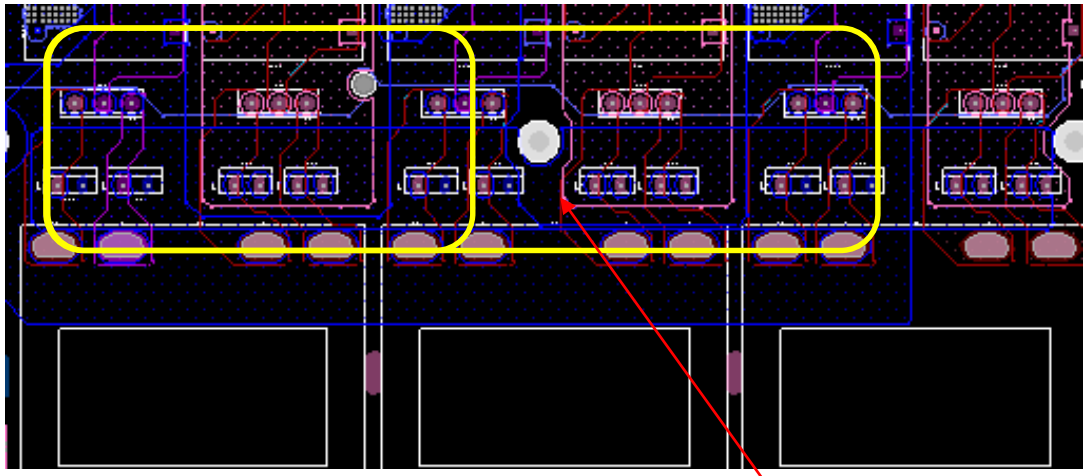
C is selected for 30kW; B will be considered for 60kW

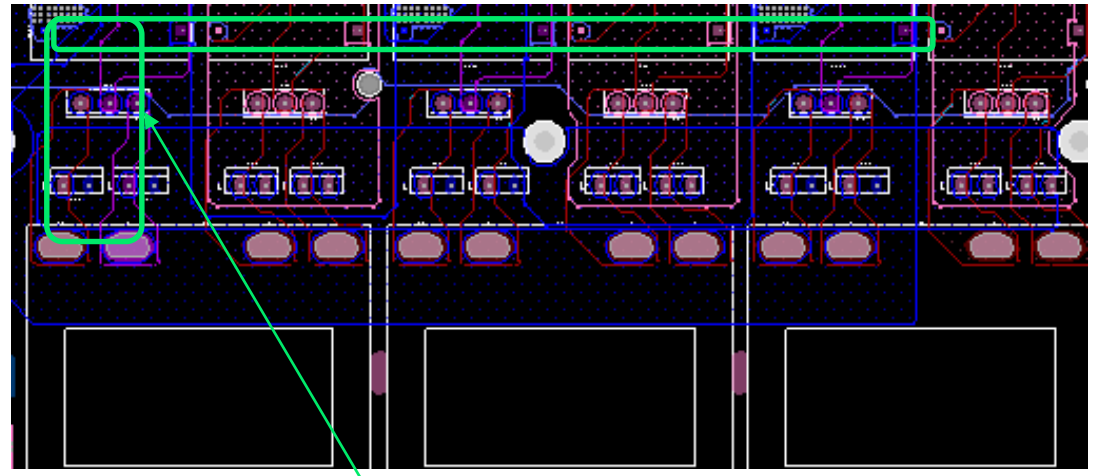
The output rectifier are equivalent to each other. The total current rating of output rectifier are same. Even we see 24 positions in B and C and 12 in A.

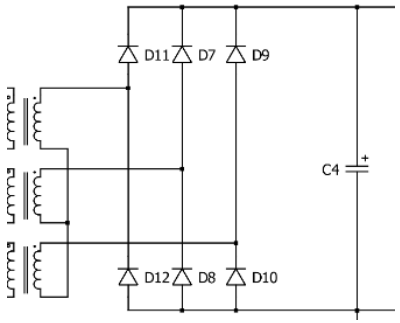
TOPOLOGY SELECTION

3phase output Bridge rectifier

Full Bridge output rectifier

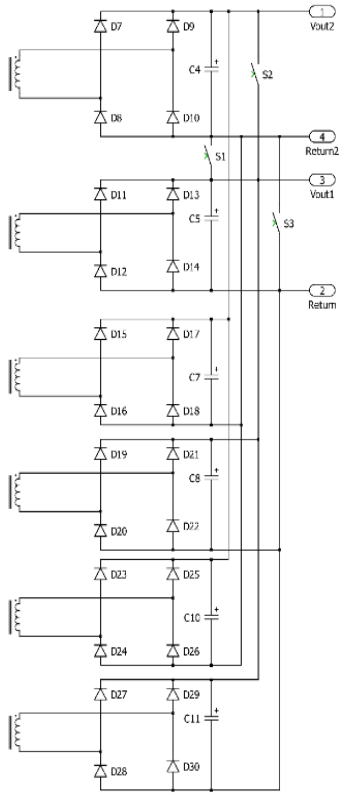






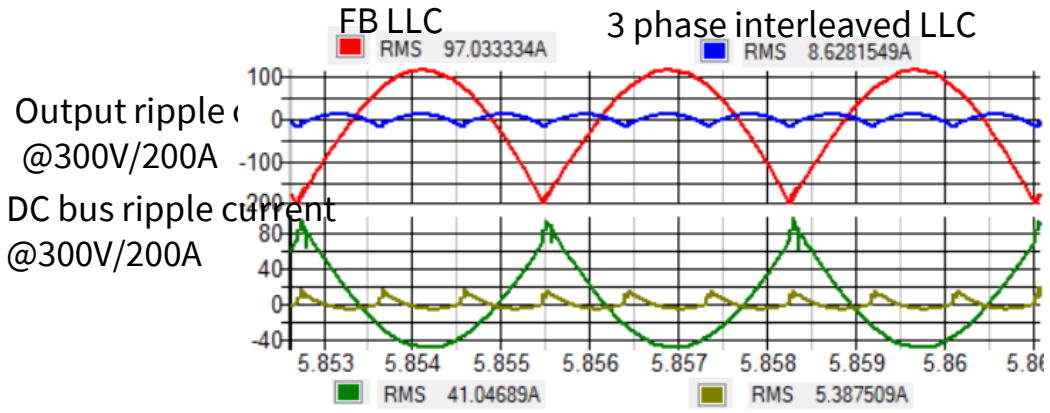
Large loop for di/dt
Magnetic field
to input EMI filters

Small loop for di/dt

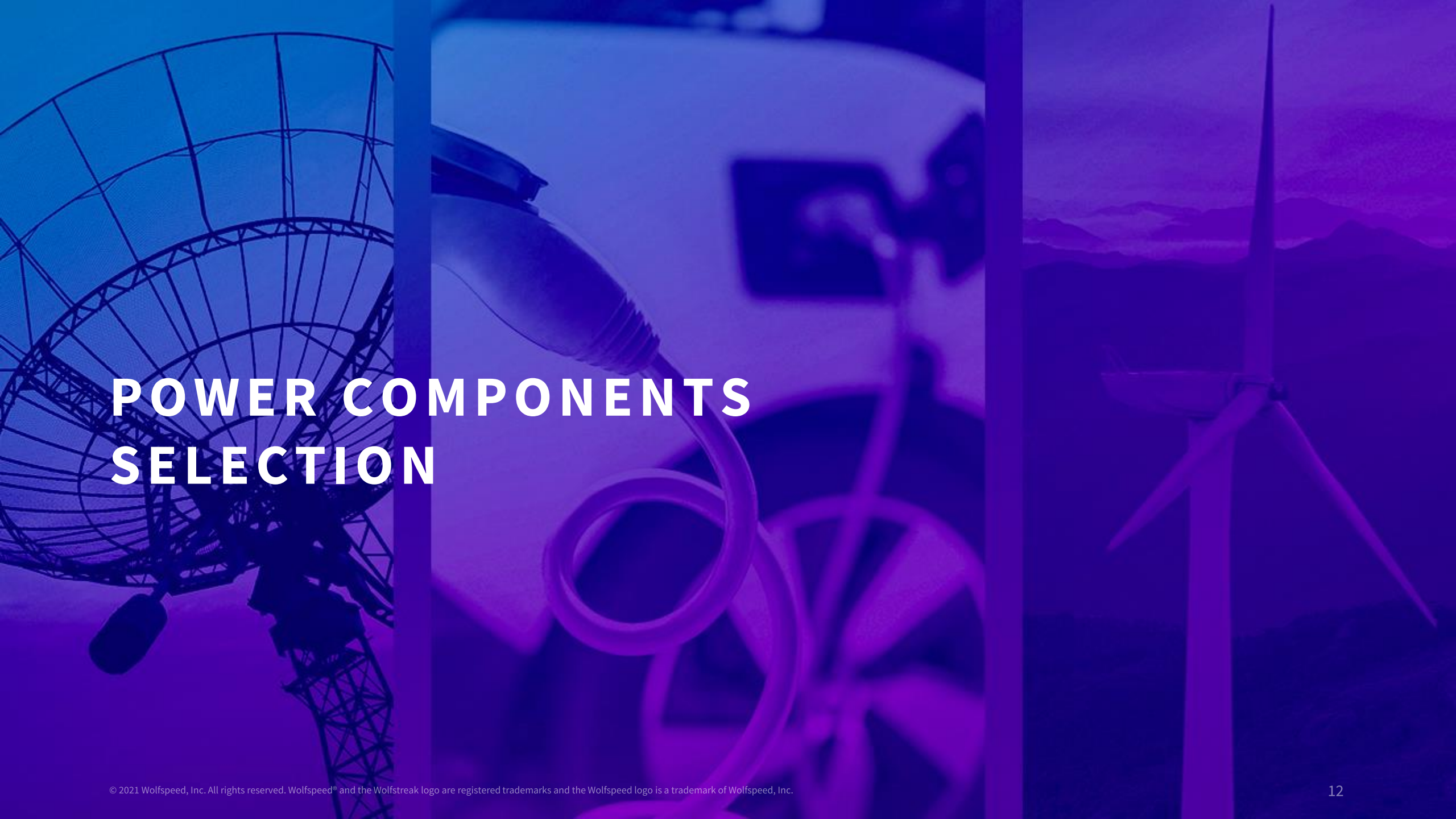


OUTPUT CAPACITOR RIPPLE STRESS AND COMPONENTS SELECTION 60KW

Topology	Condition	Rms current Output	Output Caps	Rms current Input	Input Caps
3 phase Y-FB	300V 200A output	8.6A	630V 3uF *6	8A	1100V 2uF *4
FB-FB	300V 200A output	97A	630V 4.7uF *24	44A	1100V 2uF *14



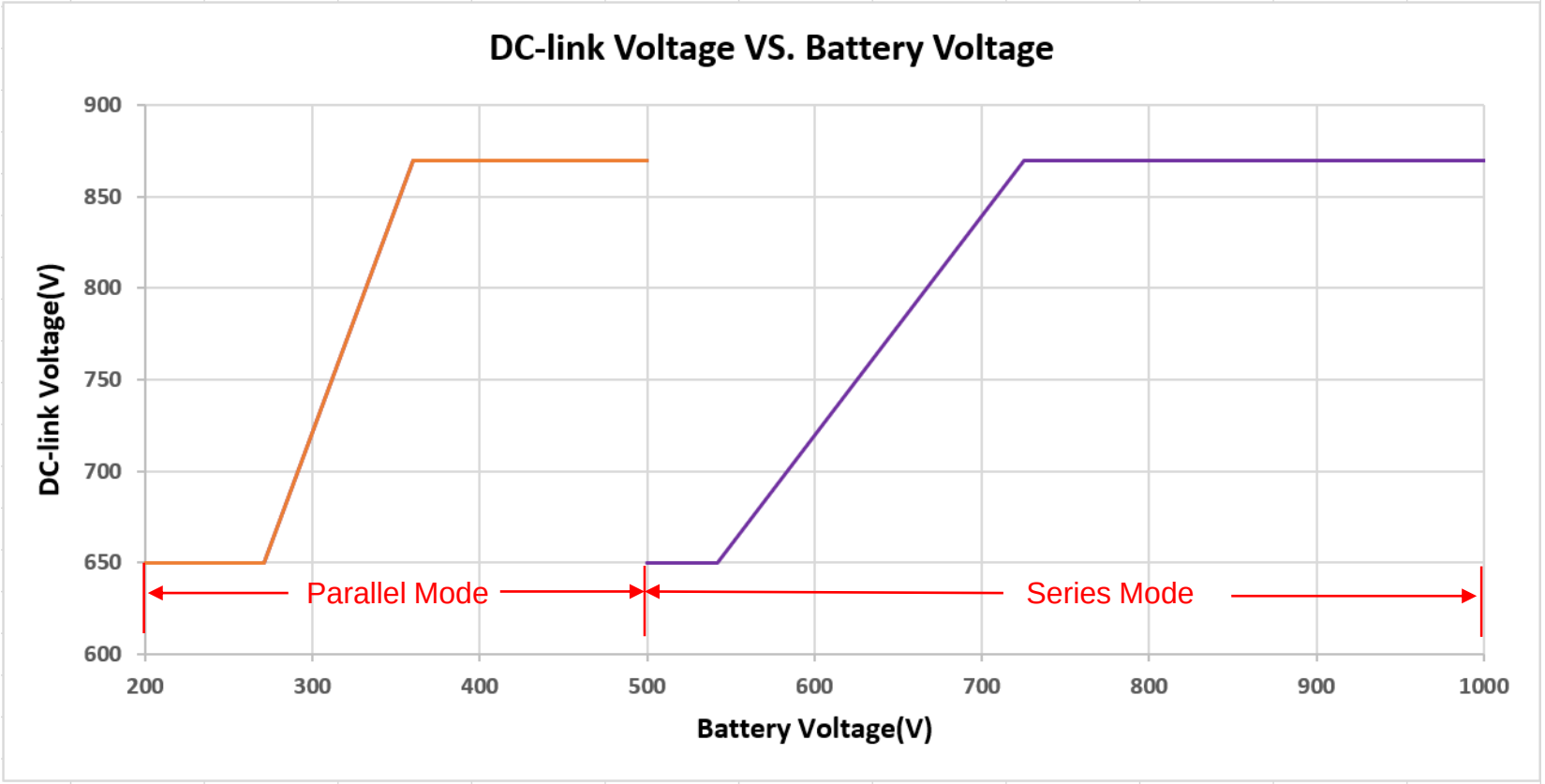
Input & output ripple and the size of filtering caps are much smaller in 3 phase LLC.
It helps to improve the eff and power density.



POWER COMPONENTS SELECTION

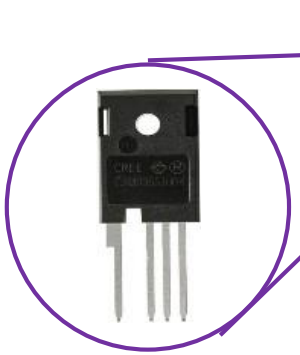
FLEXIBLE DC-LINK CONTROL

Fr=180kHz
Lr=7.5uH
Cr=102nF
Lm=30uH

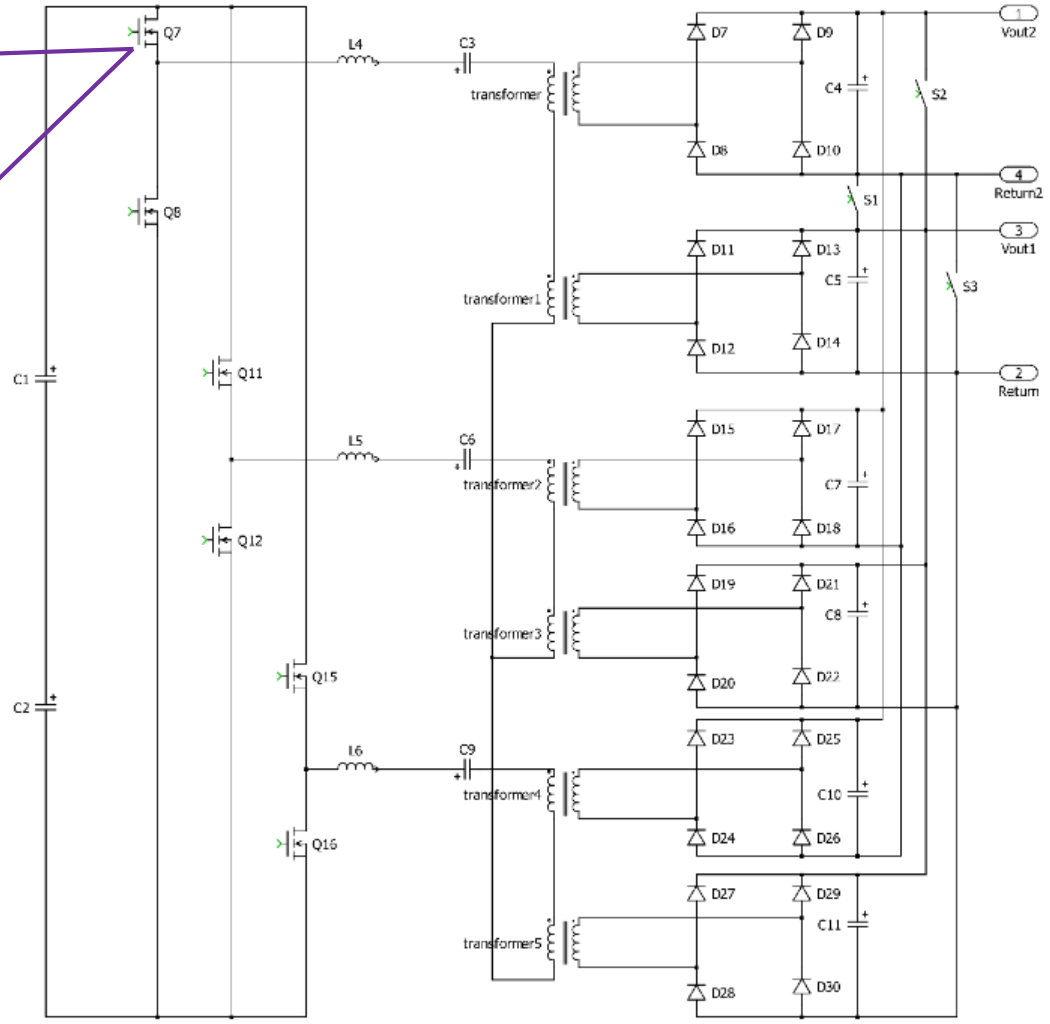


POWER COMPONENTS SELECTION

The DC link voltage is up to 870V. 65A max rms current.
C3M0040120K 1200V 40mohm SiC MOSFET is selected for primary MOSFET of LLC converter based on electrical stress and thermal design. 12 devices provide 60kW output.



2 pcs 1200V 40 mΩ SiC MOSFET



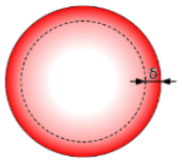
Why SiC?

- ✓ **Fast switching and low switching losses for 1200V device. Enabling high-frequency switching**
- ✓ **Smaller output capacitance, easier to achieve ZVS for LLC resonant converter**
- ✓ **Less temperature dependence of Rdson and low conduction loss at high temperature**
- ✓ **Low reverse recovery body diode enables reliability in case of hard-commutation**

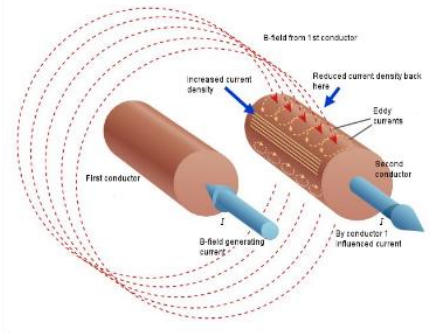
KEY MAGNETICS DESIGN

DESIGN CONSIDERATIONS – POWER TRANSFORMER

Skin Effect



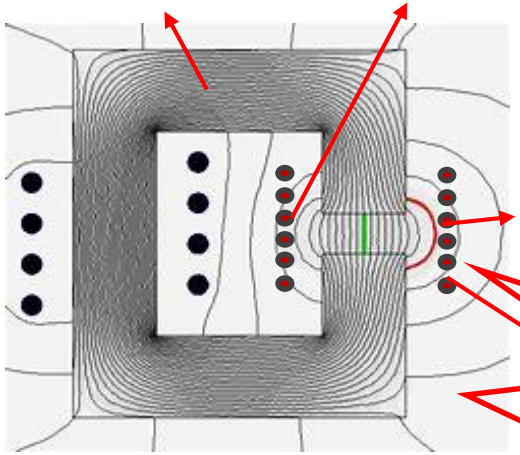
Proximity Effect



- ❑ Wire diameter selection based on frequency
- ❑ Litz wire winding

Core Loss

Thermal Management



Fringing Effect

Extra power loss due to Eddy Current

- ❑ Air Gapped Ferrite Core
- ❑ Good winding design minimizes Eddy current loss
- ❑ Thermal design to cover max & min fs

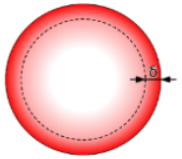
PARAMETERS AND PERFORMANCE COMPARISON– TX CORE MATERIAL

	3C95	3C97	TPW33
ui	3000	3000	3300
Bmax	530mT@ 25 ℃ 410mT@ 100 ℃	550mT@ 25 ℃ 430mT@ 100 ℃	520mT@ 25 ℃ 410mT@ 100 ℃
Pv(200mT/100kHz)	350kW/m3@ 25 ℃ 290kW/m3@ 100 ℃	320kW/m3@ 60 ℃ 380kW/m3@ 140 ℃	380kW/m3@ 25 ℃ 300kW/m3@ 100 ℃
T_range optimized	25 ℃-100 ℃	50 ℃-150 ℃	25 ℃-120 ℃
Frequency Range	<500kHz	<500kHz	<500kHz
Vendor	Ferroxcube	Ferroxcube	TDG

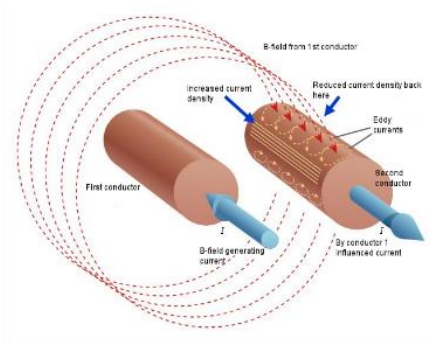
- 3C97 is selected due to its wide temperature range for low power loss.

DESIGN CONSIDERATIONS – RESONANT CHOKE

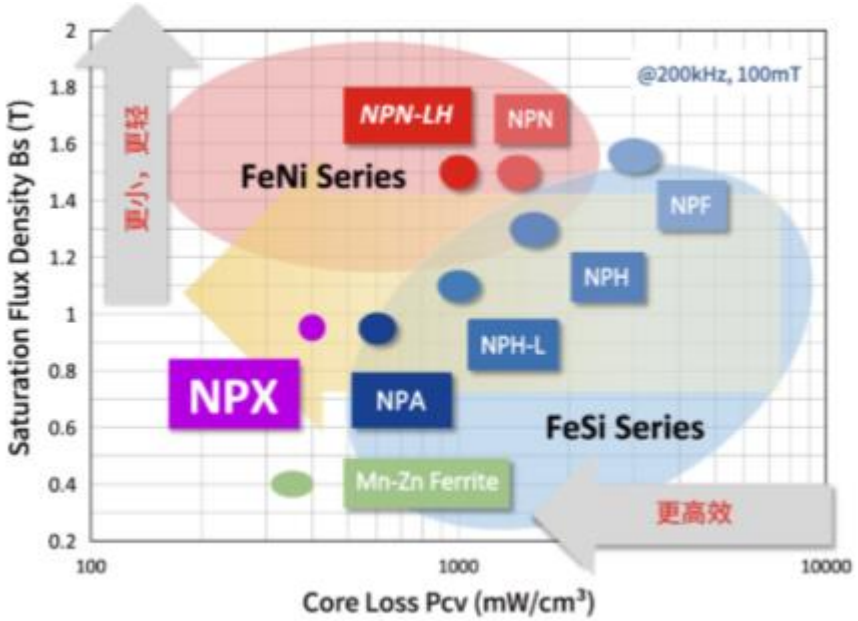
Skin Effect



Proximity Effect



- ❑ Wire diameter selection based on frequency
- ❑ Litz wire winding

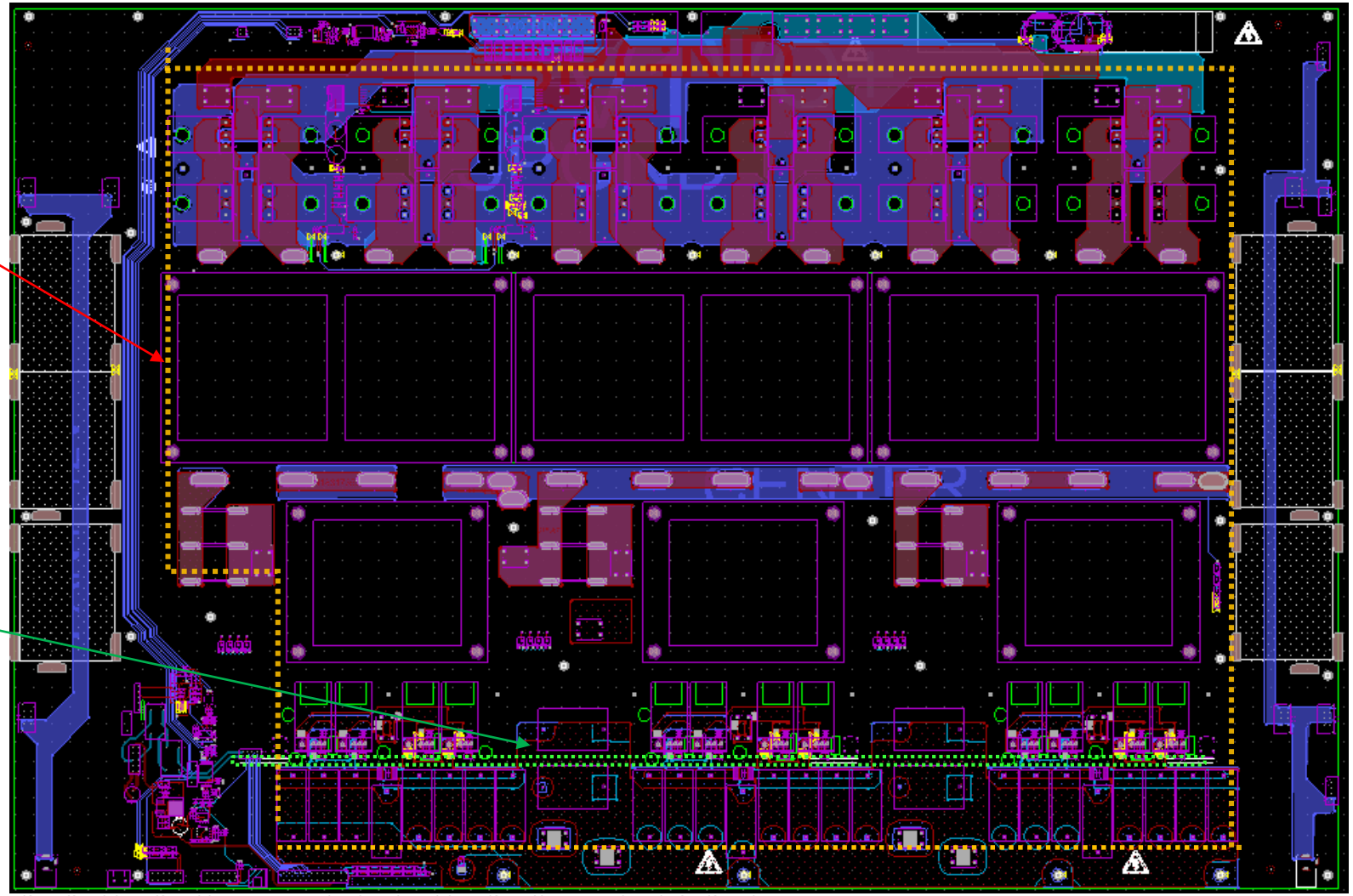


- ❑ NPX Powder Core instead or Air Gapped Ferrite
- ❑ Balance of Core Loss and Winding loss
- ❑ Low thermal resistance at system level

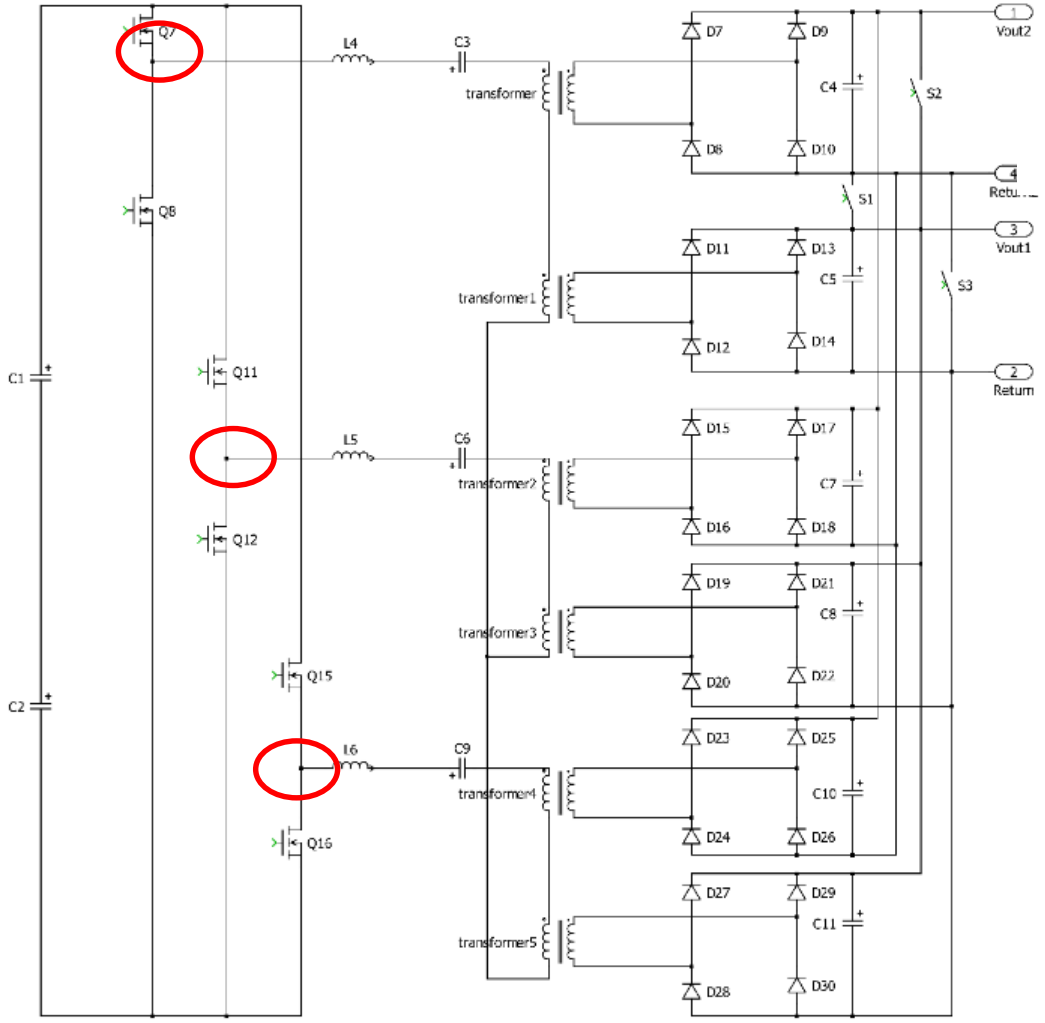
PCB LAYOUT CONSIDERATIONS

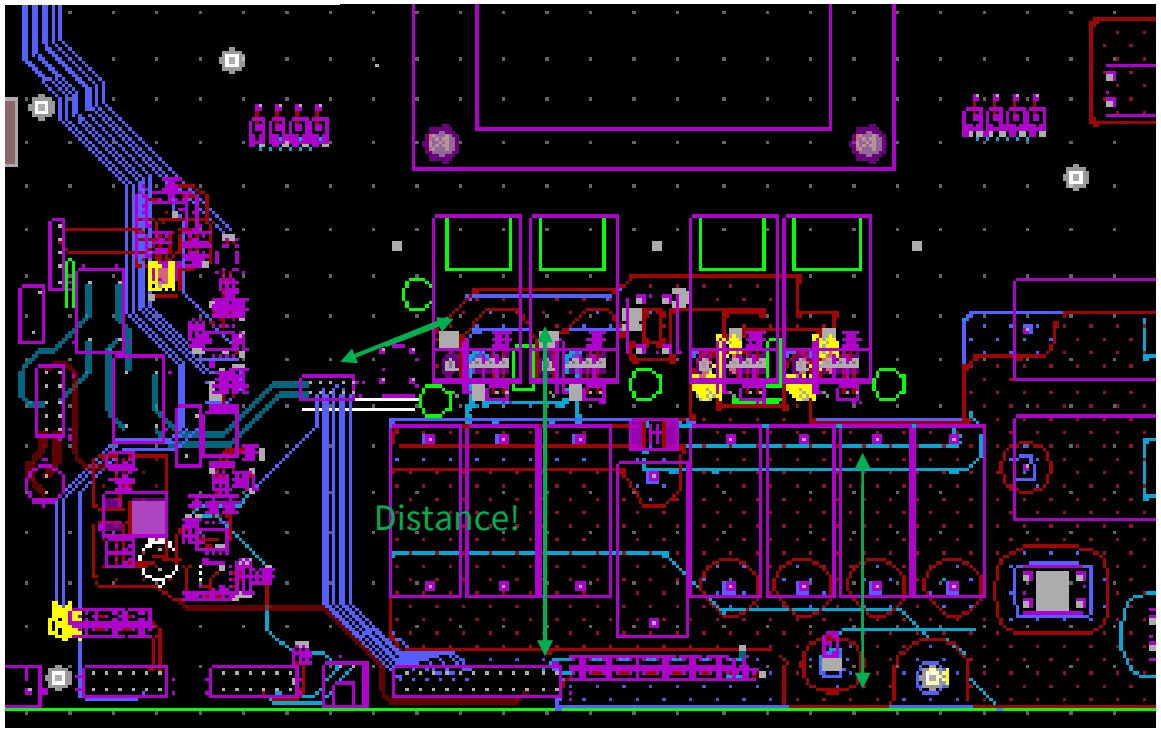
COMPONENTS PLACEMENT

- Avoid overlap between Gate, Gate drive circuit, bias power supply for Gate drive and the drain of the MOSFET.



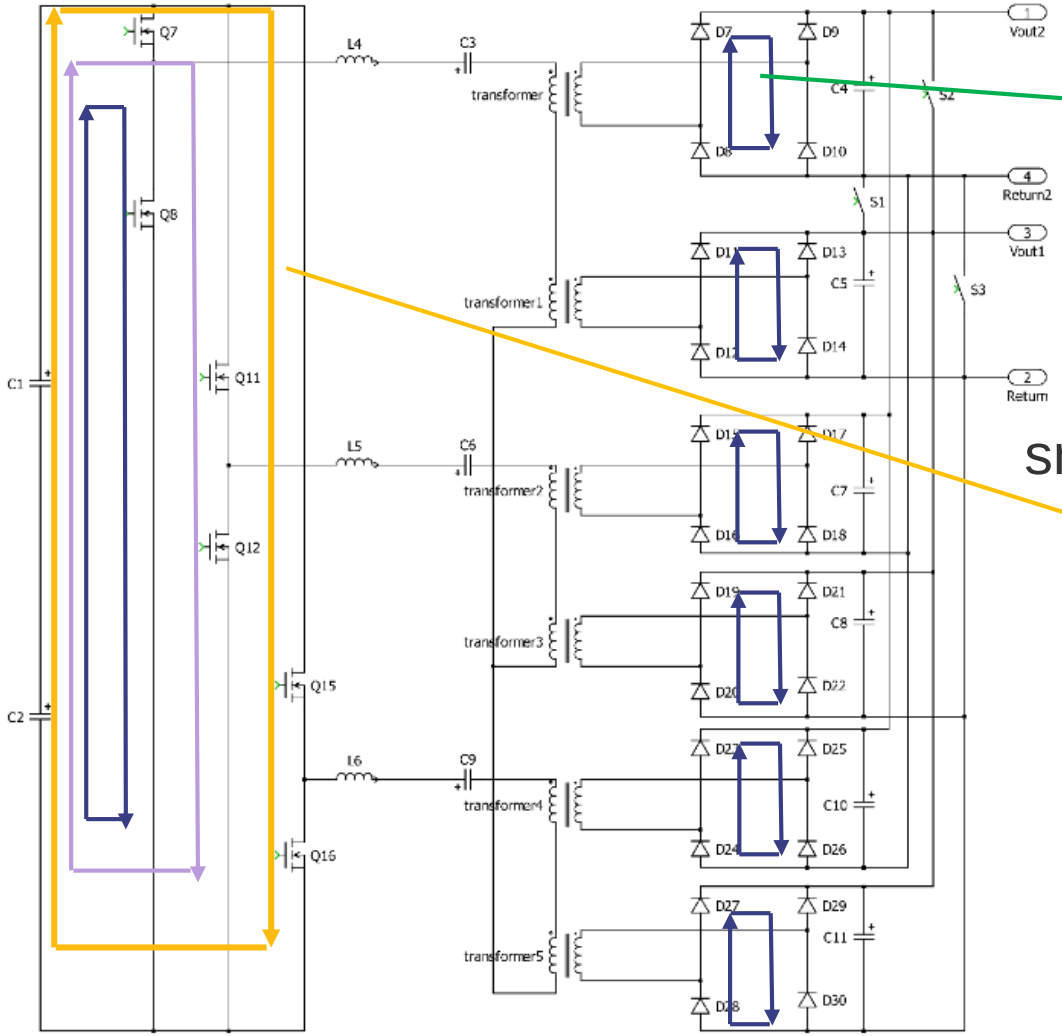
HIGH DV/DT TRACE/NODE



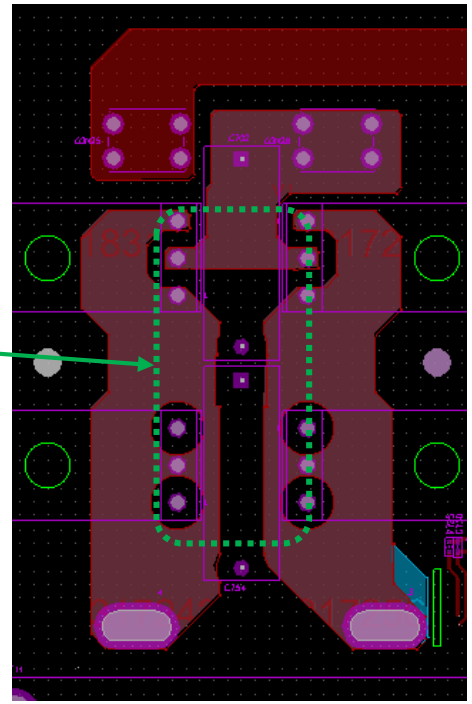


- Keep the sensitive signals far away from the high dV/dt trace/nodes.
- Keep the sensitive signals far away from the high magnetic field such as resonant choke, power transformer.
- Small pad size of Drain nodes to reduce the coupling and parasitic capacitance

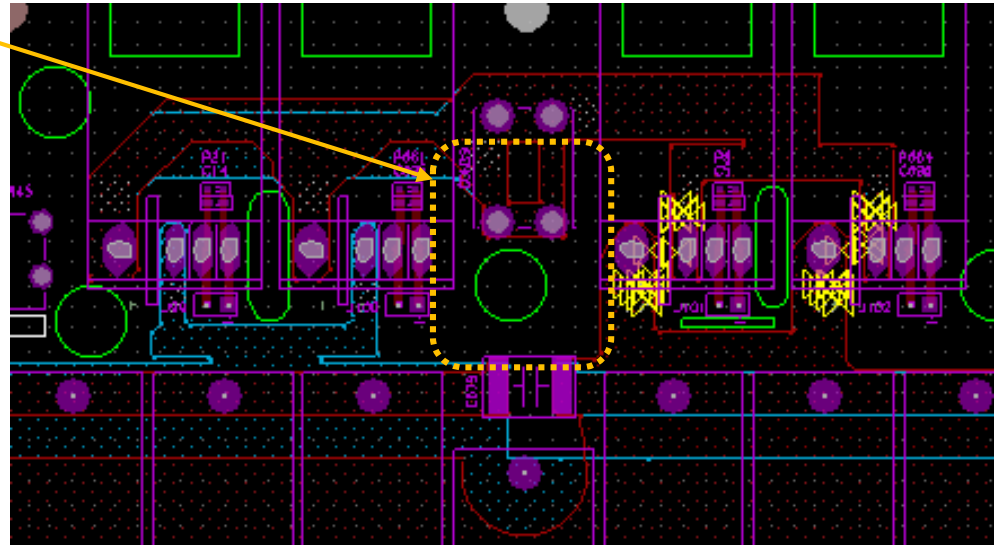
HIGH DI/DT LOOP



small di/dt loop



small di/dt loop

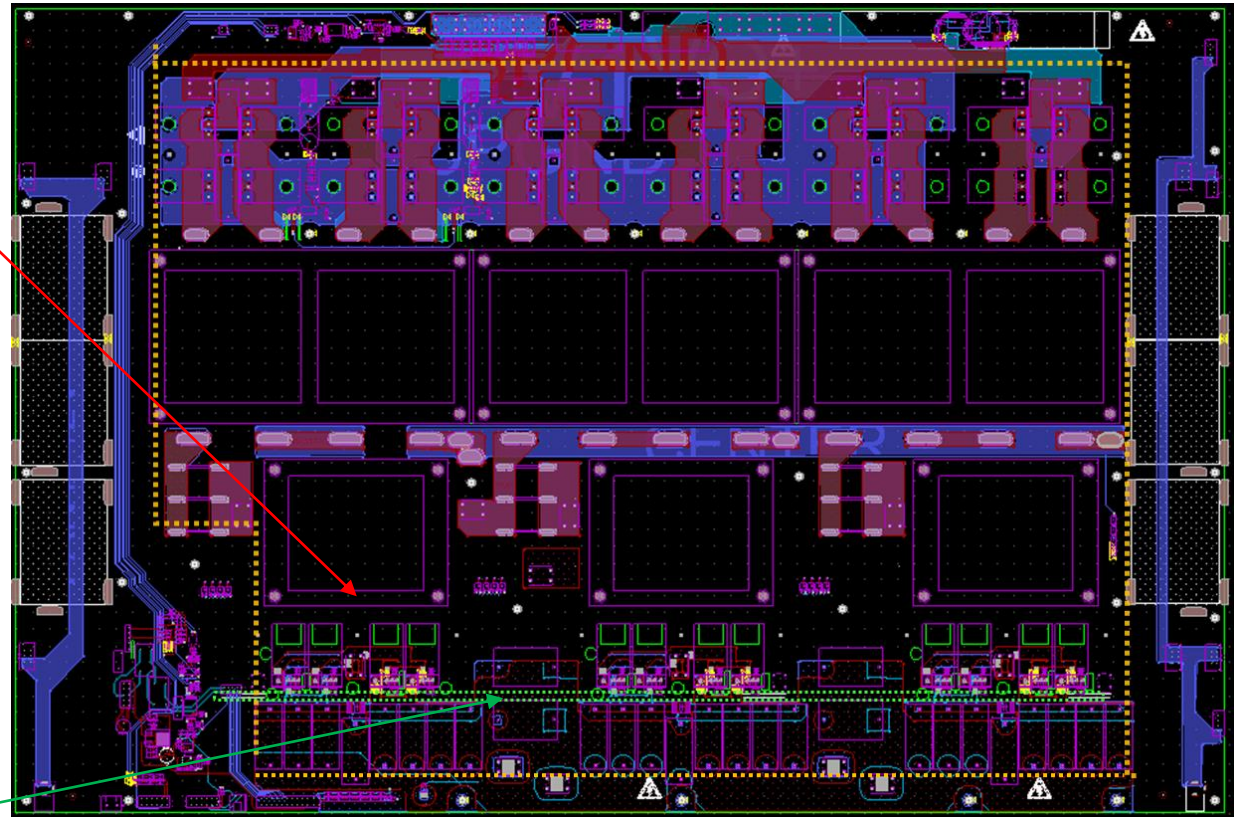


- Place ceramic and film caps as close as possible to minimize the high frequency di/dt loop.
- Proper PCB layout of the power components to minimize the high frequency di/dt loop.

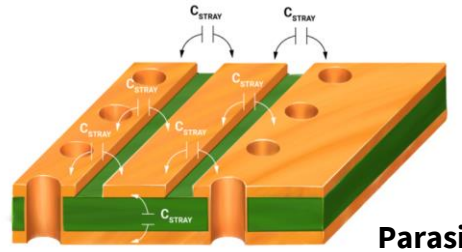
COMPONENTS PLACEMENT

Similar PCB design rules for SiC and Si → Avoid overlap between Gate+Gate-drive-circuit and the drain of MOSFET.

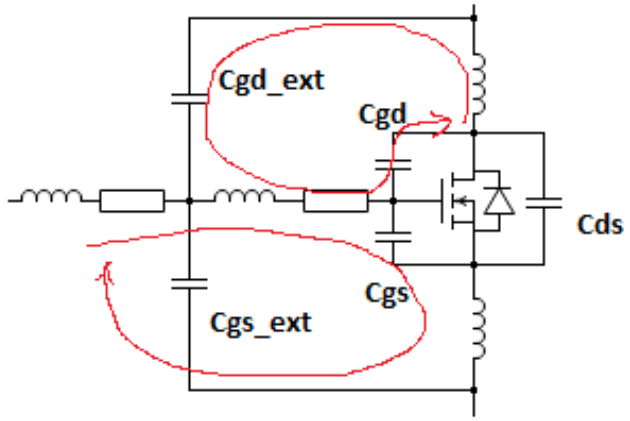
Power loop



Daughter board for Gate drive



Parasitic capacitance on PCB

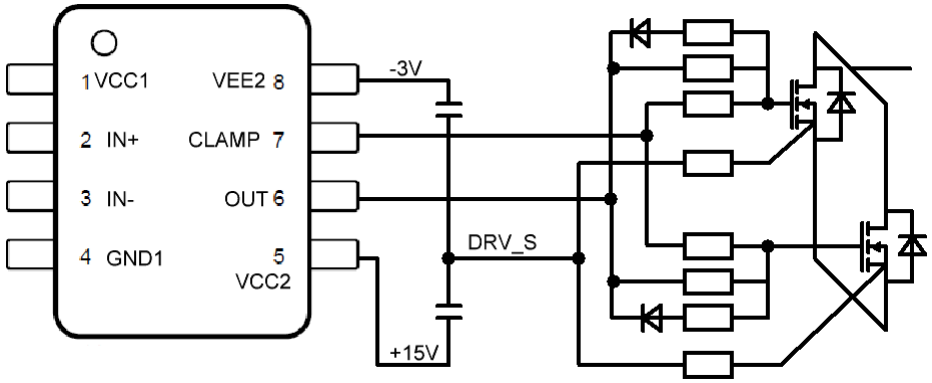


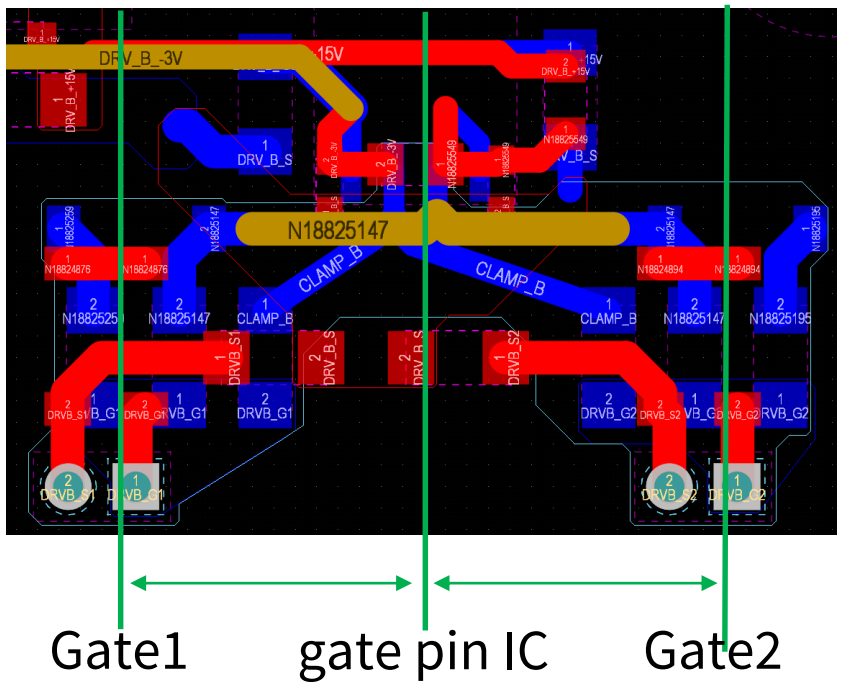
Consequences external Cgd:

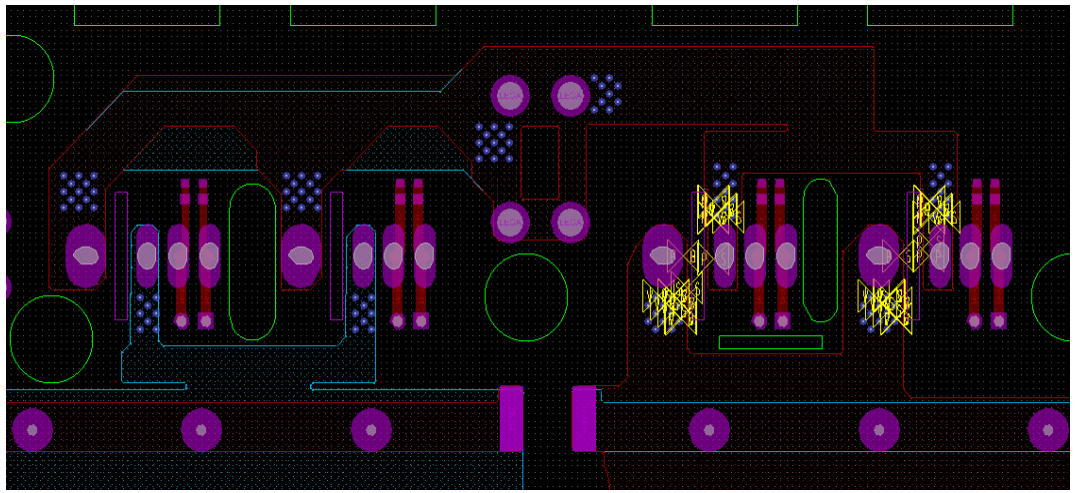
- Not only higher switching loss
- Risk of gate oscillation
- EMI

PCB LAYOUT FOR PARALLELED SIC MOSFET IN 60KW REFERENCE DESIGN

- Minimized the loop of gate drive and active miller clamp
- Symmetrical Gate and return paths
- Have resistors in both Gate and Kelvin-Source and close to the MOSFETs



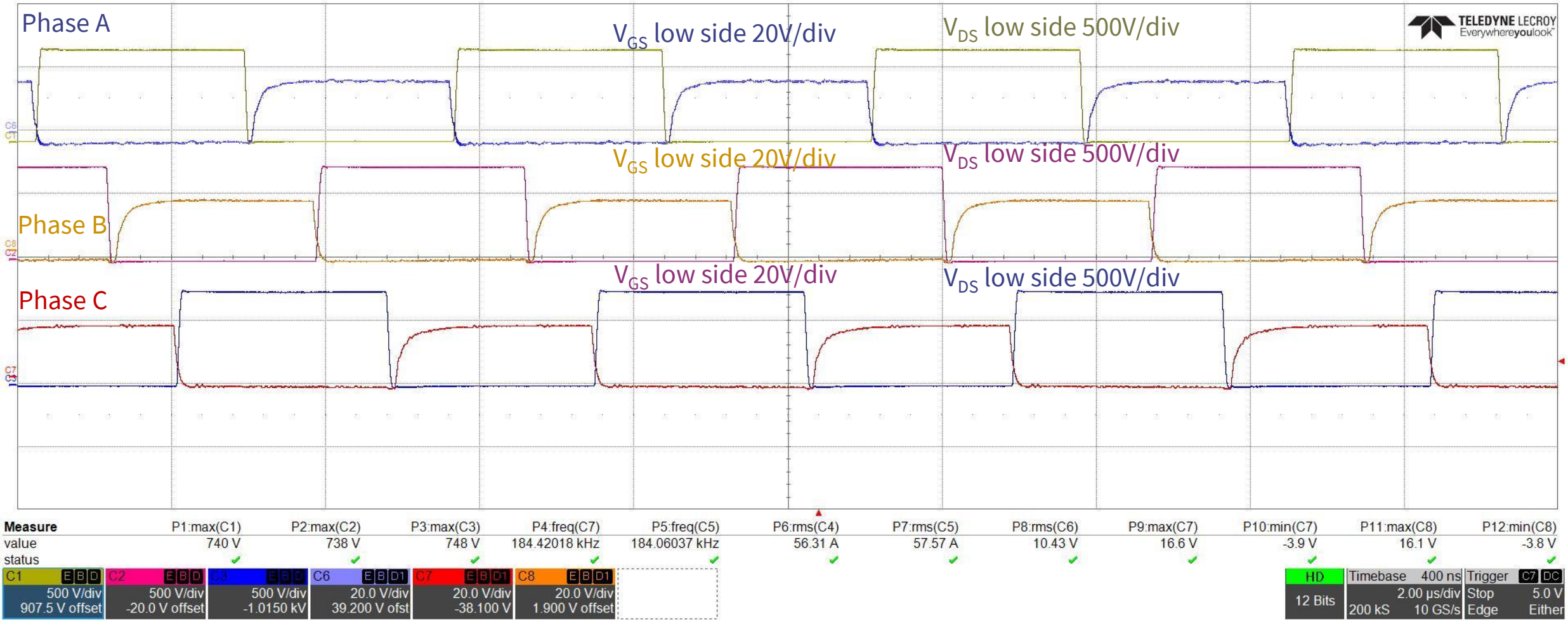




- Add a small inductance to power source pin of the paralleled MOSFET to improve dynamic current sharing.
- Minimize stray inductance at drain

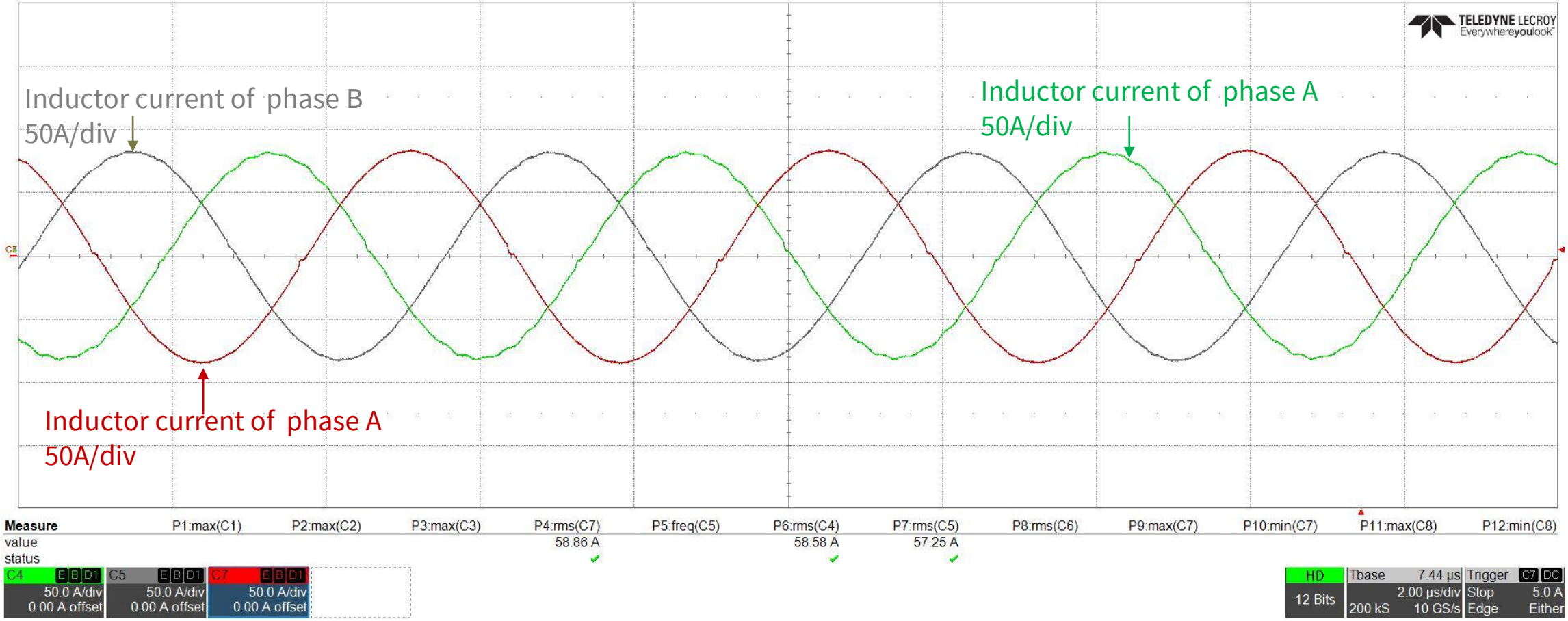
TEST RESULTS

WAVEFORMS - 3PHASE INTERLEAVED – V_{GS} V_{DS}

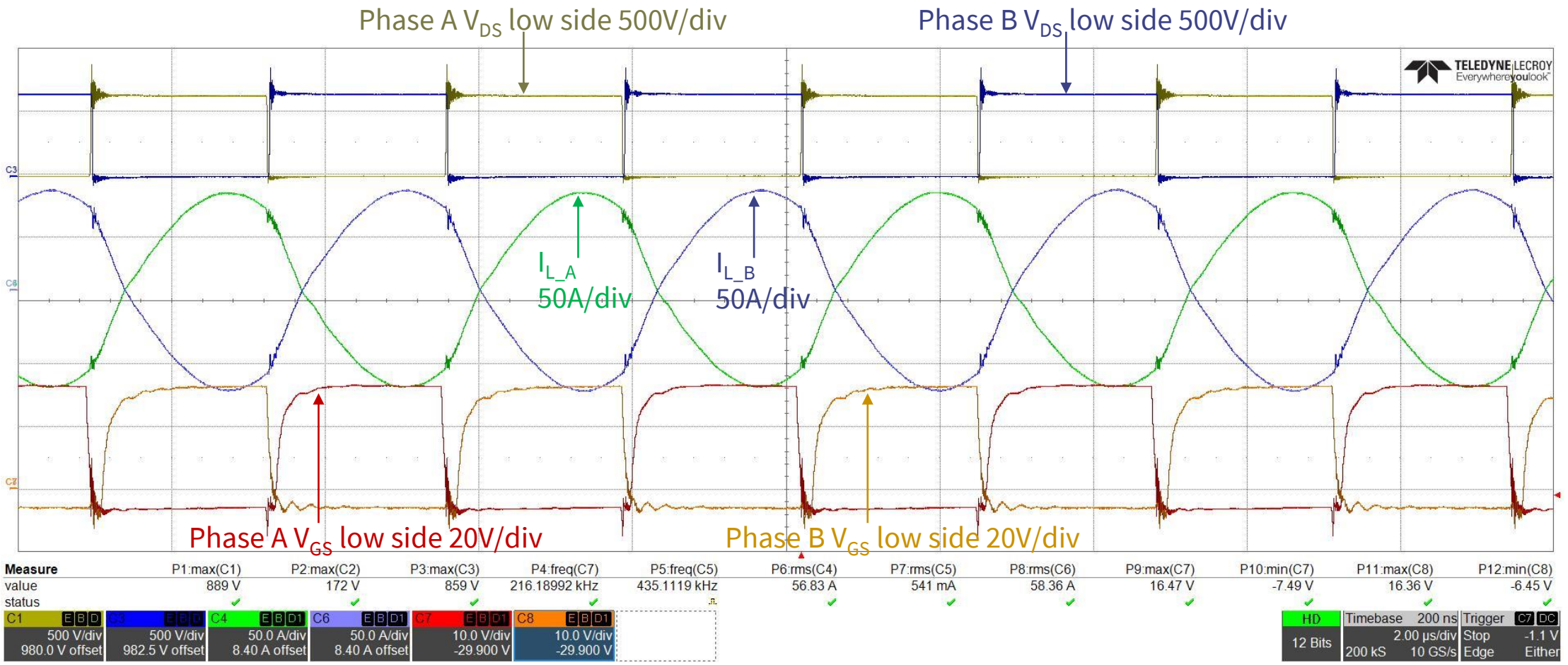


Measure	P1:max(C1)	P2:max(C2)	P3:max(C3)	P4:freq(C7)	P5:freq(C5)	P6:rms(C4)	P7:rms(C5)	P8:rms(C6)	P9:max(C7)	P10:min(C7)	P11:max(C8)	P12:min(C8)
value	740 V	738 V	748 V	184.42018 kHz	184.06037 kHz	56.31 A	57.57 A	10.43 V	16.6 V	-3.9 V	16.1 V	-3.8 V
status	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

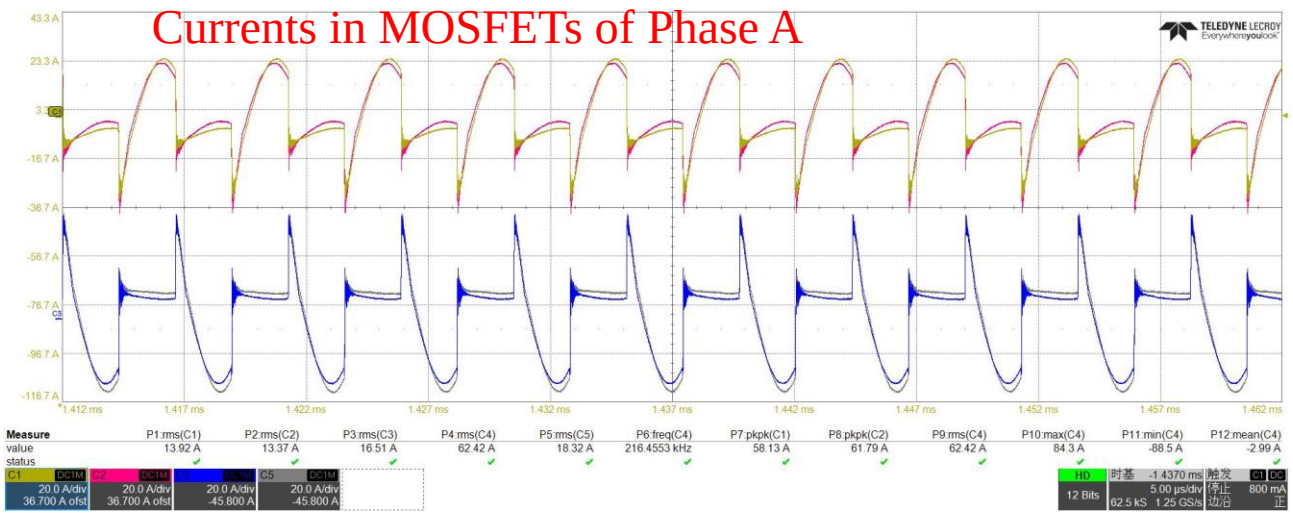
WAVEFORMS - 3PHASE INTERLEAVED – INDUCTOR CURRENT



WAVEFORMS – FULL BRIDGE



200V/26KW– CURRENT SHARING BETWEEN PARALLEL MOSFETS



The current unbalance rate δ is calculated as:

$$\delta = \frac{\Delta I}{I_{avg}} \times 100\%$$

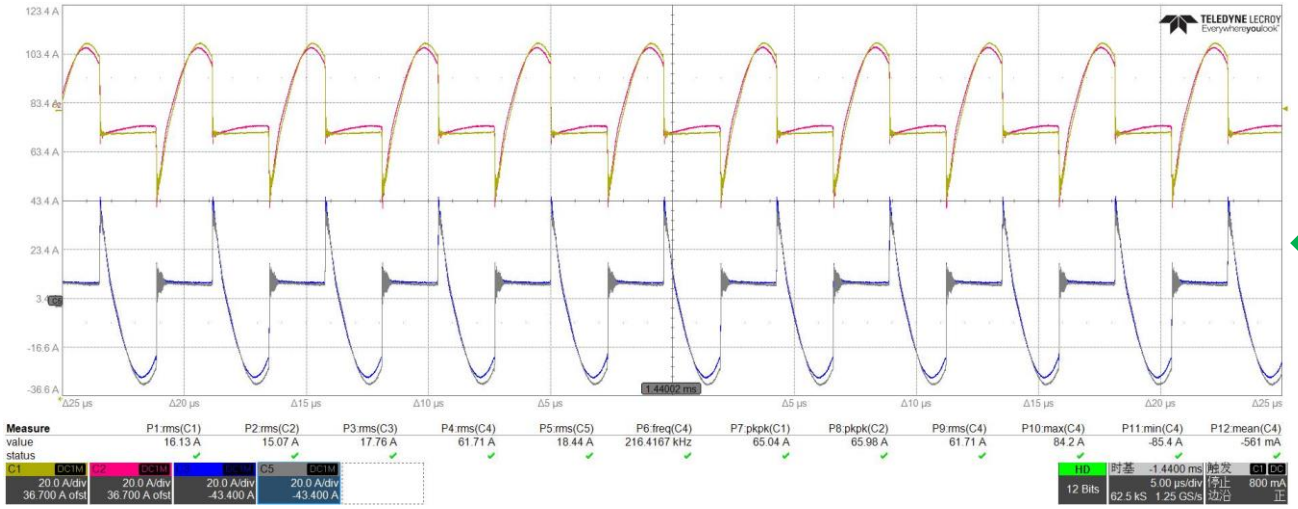
Where:

ΔI —— Current difference between the two parallel MOSFETs

I_{avg} —— Average current of the two parallel MOSFETs

$\delta_{LOW\_A} = 2.02\%$, $\delta_{HIGH\_A} = 5.2\%$

CH1: I_{LOW1} CH2: I_{LOW2} CH3: I_{HIGH1} CH5: I_{HIGH2}

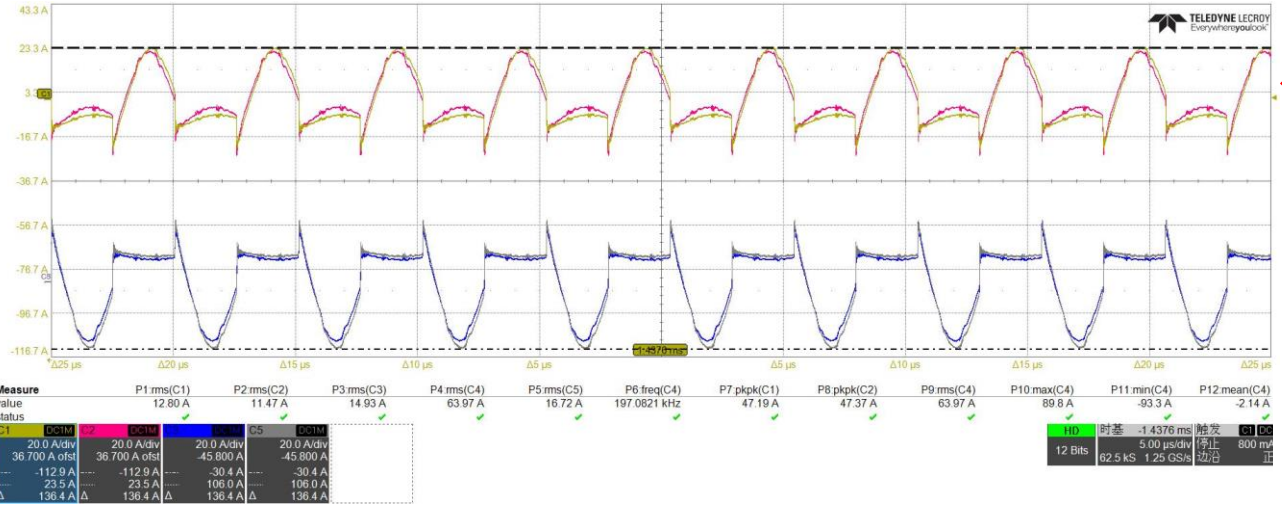


$\delta_{LOW\_B} = 3.4\%$, $\delta_{HIGH\_B} = 1.88\%$

Currents in MOSFETs of Phase B

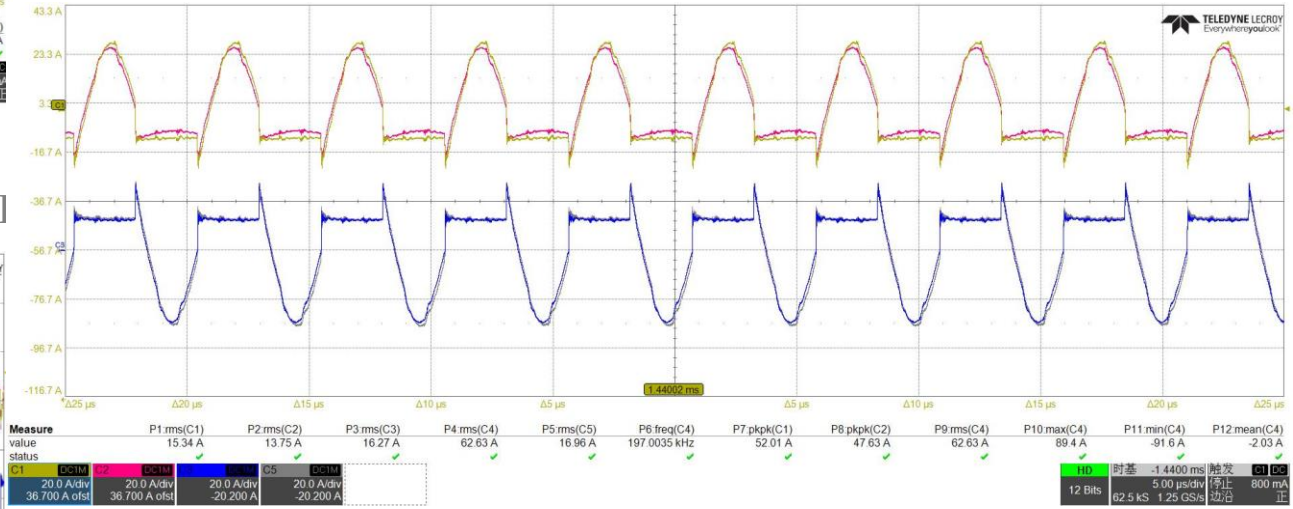
250V/50KW– CURRENT SHARING BETWEEN PARALLEL MOSFETS

Currents in MOSFETs of Phase A

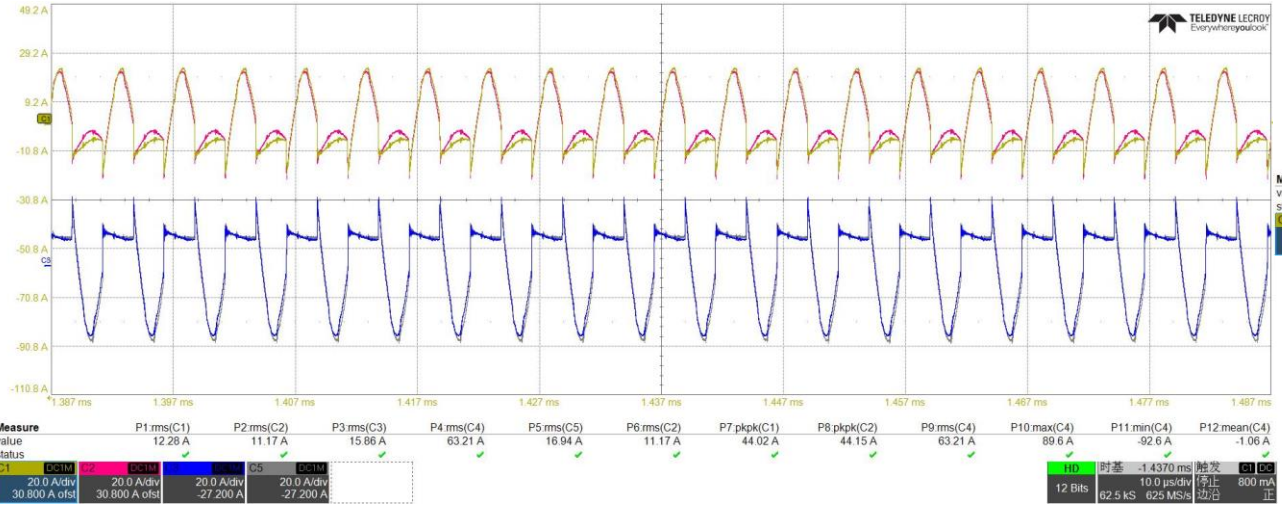


δ_{LOW_A} = 5.48%, δ_{HIGH_A} = 5.66%

δ_{LOW_C} = 5.47%, δ_{HIGH_C} = 2.08%



CH1: I_{LOW1} CH2: I_{LOW2} CH3: I_{HIGH1} CH5: I_{HIGH}

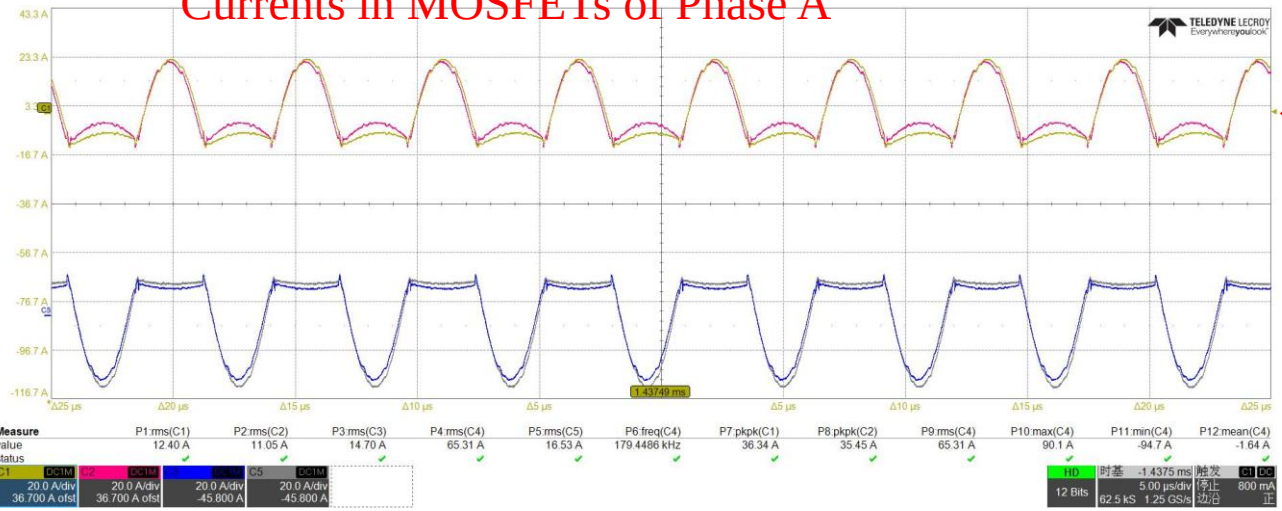


δ_{LOW_B} = 5.2%, δ_{HIGH_B} = 3.17%

Currents in MOSFETs of Phase B

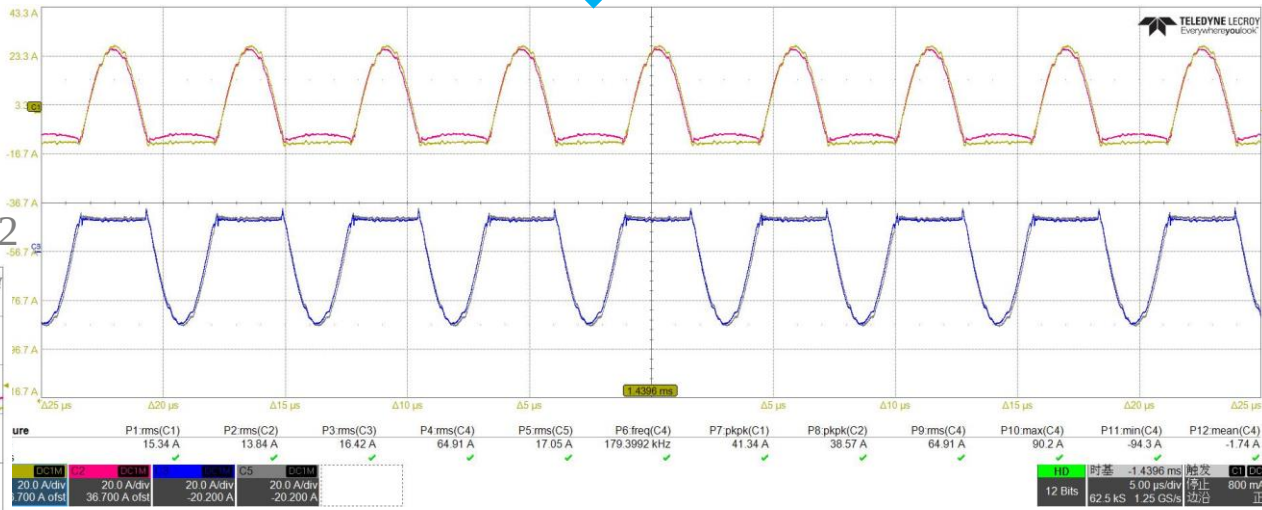
300V/60KW– CURRENT SHARING BETWEEN PARALLEL MOSFETS

Currents in MOSFETs of Phase A

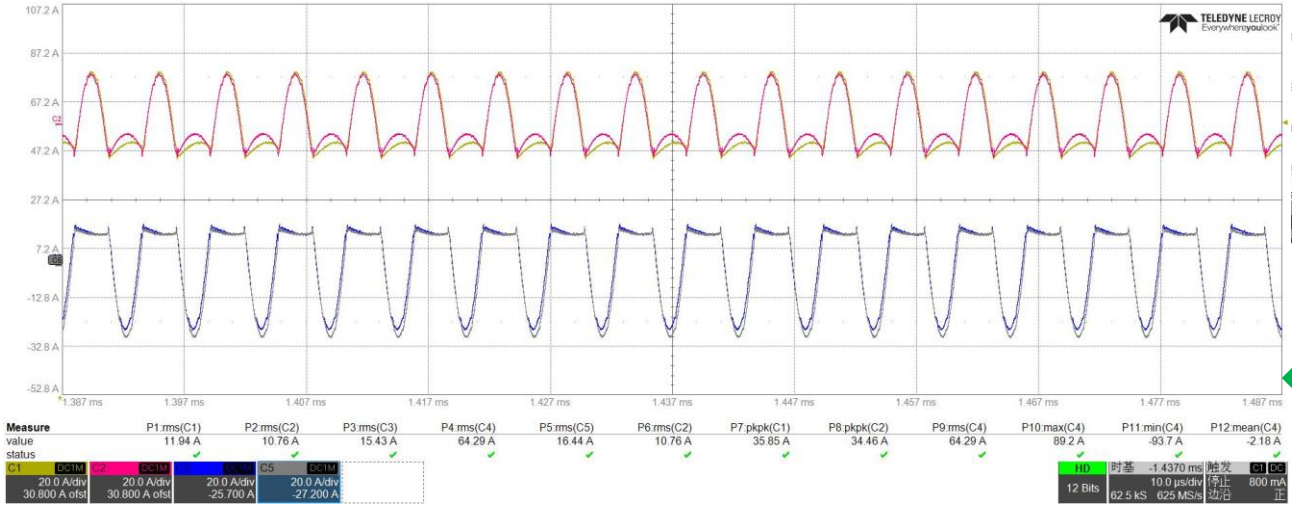


δ_{LOW_A} = 5.76%, δ_{HIGH_A} = 5.86%

δ_{LOW_C} = 5.14%, δ_{HIGH_C} = 1.88%



CH1: I_{LOW1} CH2: I_{LOW2} CH3: I_{HIGH1} CH5: I_{HIGH2}

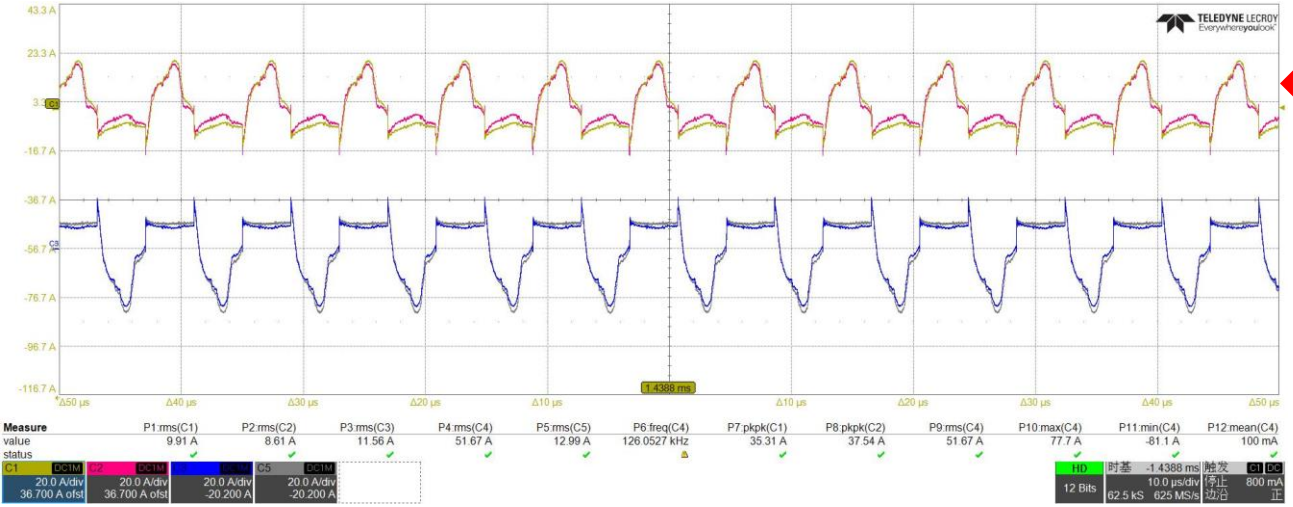


δ_{LOW_B} = 5.21%, δ_{HIGH_B} = 3.15%

Currents in MOSFETs of Phase B

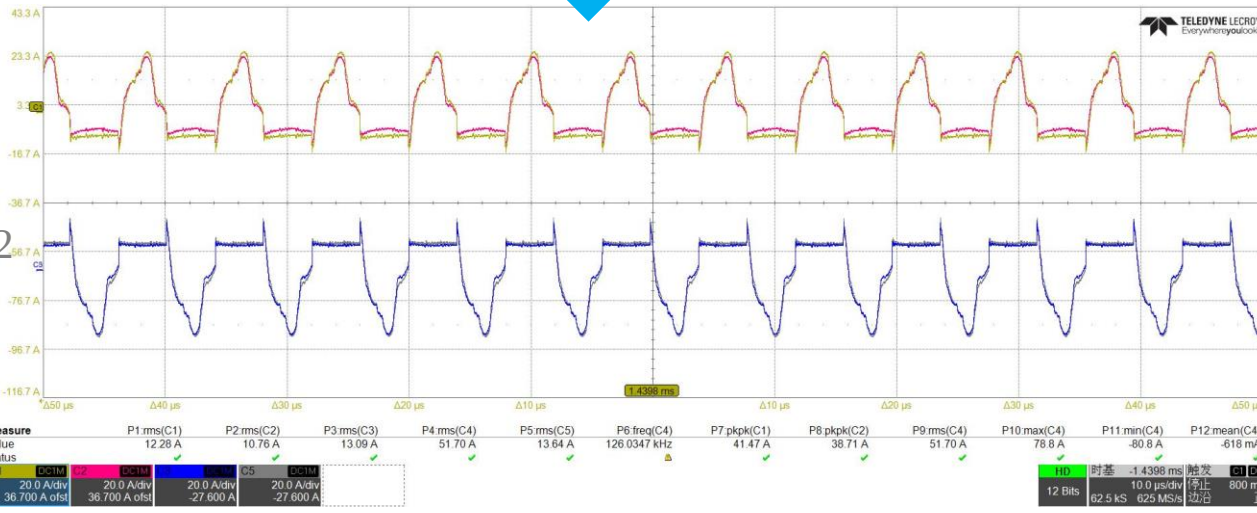
500V/58KW– CURRENT SHARING BETWEEN PARALLEL MOSFETS

Currents in MOSFETs of Phase A

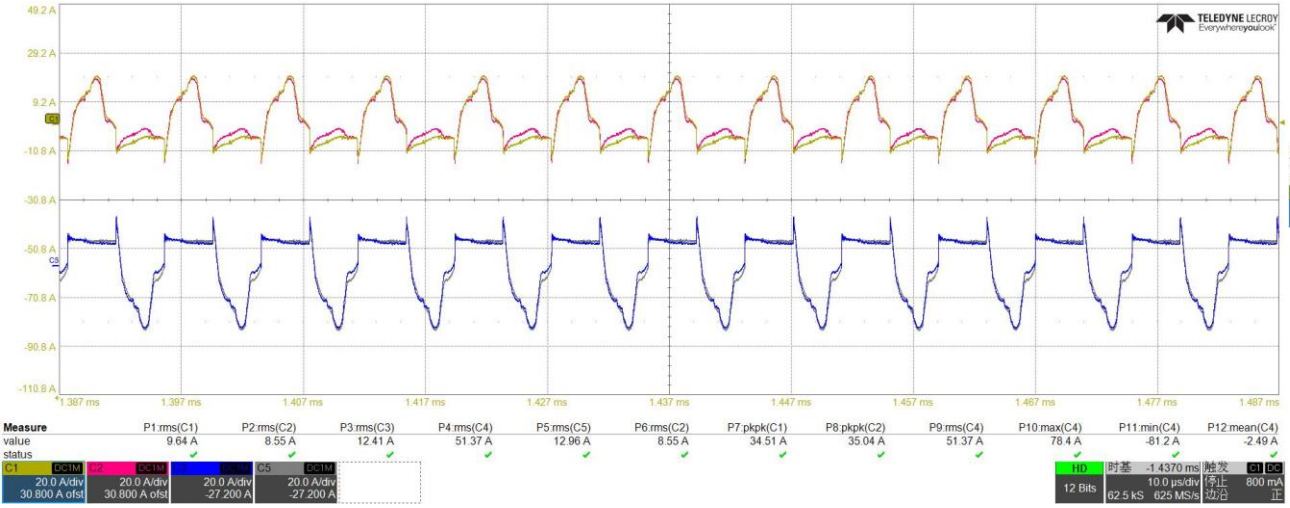


δ_{LOW_A} = 7.02%, δ_{HIGH_A} = 5.82%

δ_{LOW_C} = 6.6%, δ_{HIGH_C} = 2.06%



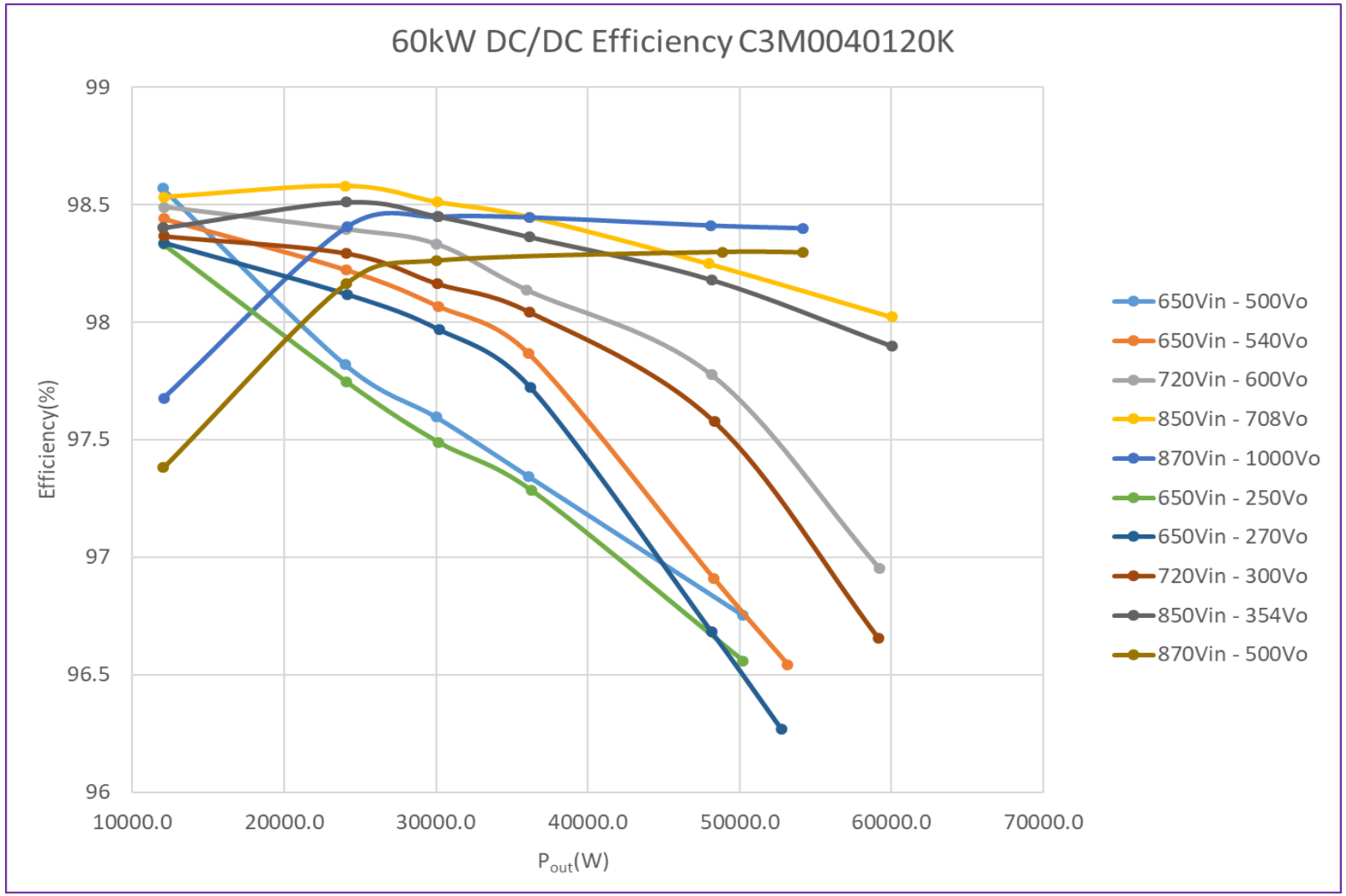
CH1: I_{LOW1} CH2: I_{LOW2} CH3: I_{HIGH1} CH5: I_{HIGH2}



δ_{LOW_B} = 5.99%, δ_{HIGH_B} = 2.17%

Currents in MOSFETs of Phase B

EFFICIENCY TEST RESULT



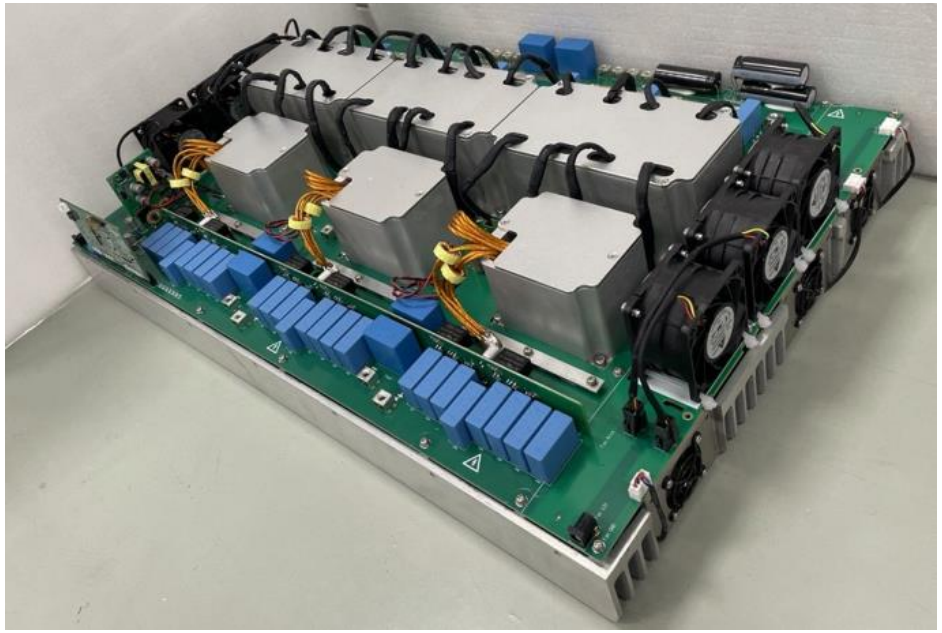
THERMAL RESULTS (TESTED TJ < MAX TJ *0.8 = 140 ℃)

Part Number	Heatsink Temp.	Rth (j-c) (c/w)	Calculated Power Loss (watts)	Case Temp.	Calculated Junction Temp.	Max. Junction Temp.	Comments
720Vdc Input, 300Vdc Output, full load							
C3M0040120K Q23	85	0.46	33.2	96.6	111.9	175 °C	**PASS**
650Vdc Input, 200Vdc Output, full bridge mode							
C3M0040120K Q23	85	0.46	47.5	101.6	123.4	175 °C	**PASS**
870Vdc Input, 500Vdc Output, full load							
C3M0040120K Q23	85	0.46	31	95.8	110.06	175 °C	**PASS**

SUMMARY

The value to get the low power loss from:

- C3M 1200V SiC MOSFET,
- the flexible control scheme
- proper PCB layout



Below design targets are achieved:

✓ Low parts counts, 12 pcs TO-247-4 1200V 40mohm SiC discrete MOSFETs to cover 60kW

✓ High Efficiency up to 98.5% for DC DC converter

✓ Wide battery voltage range 200Vdc-1000Vdc

✓ Good Current Sharing between phases and MOSFETs

THANK YOU

We harness the power of Silicon Carbide to change the world for the better

Wolfspeed® Unleashing the Power of Possibilities™