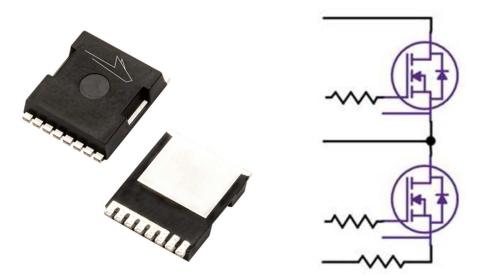


User Guide PRD-06834

# MOD-PWR-MM-...L

# SpeedVal<sup>™</sup> Kit TOLL Power Daughter Card





PRD-06834 REV. 2, March 2024 MOD-PWR-MM-…L SpeedVal<sup>™</sup> KitTOLL Power Daughter Card User Guide

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#### CAUTION

PLEASE CAREFULLY REVIEW THE FOLLOWING PAGE, AS IT CONTAINS IMPORTANT INFORMATION REGARDING THE HAZARDS AND SAFE OPERATING REQUIREMENTS RELATED TO THE HANDLING AND USE OF THIS BOARD.

#### 警告

请认真阅读以下内容,因为其中包含了处理和使用本板子有关的危险和安全操作要求方面的重要信息。

### 警告

ボードの使用、危険の対応、そして安全に操作する要求などの大切な情報を含むので、以下の内容を よく読んでください。

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#### CAUTION

DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE BOARD. THERE CAN BE VERY HIGH VOLTAGES PRESENT ON THIS EVALUATION BOARD WHEN CONNECTED TO AN ELECTRICAL SOURCE, AND SOME COMPONENTS ON THIS BOARD CAN REACH TEMPERATURES ABOVE 50° CELSIUS. FURTHER, THESE CONDITIONS WILL CONTINUE FOR A SHORT TIME AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED.

Please ensure that appropriate safety procedures are followed when operating this board, as any of the following can occur if you handle or use this board without following proper safety precautions:

- Death
- Serious injury
- Electrocution
- Electrical shock
- Electrical burns
- Severe heat burns

You must read this document in its entirety before operating this board. It is not necessary for you to touch the board while it is energized. All test and measurement probes or attachments must be attached before the board is energized. You must never leave this board unattended or handle it when energized, and you must always ensure that all bulk capacitors have completely discharged prior to handling the board. Do not change the devices to be tested until the board is disconnected from the electrical source and the bulk capacitors have fully discharged.

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操作板子时应确保遵守正确的安全规程,否则可能会出现下列危险:

- 死亡
- 严重伤害
- 触电
- 电击
- 电灼伤
- 严重的热烧伤

请在操作本**板子**前完整阅读本**文件。**通电时不必接触板子。在为板子通电**前必**须连接**所有**测试与测量探 针或附件。通电时,禁止使板子处于无人看护状态,或操作板子。必须确保在操作板子前,大容量电容 器释放**了所有**电量。只有在**切**断板子电源,且大容量电容器完全放电后,才可更换待测试器件

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- 死亡
- 重症
- 感電
- 電撃
- 電気の火傷
- 厳しい火傷

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### **1.** Introduction

SpeedVal<sup>™</sup> Kit is a modular evaluation platform enabling engineers to test Wolfspeed<sup>®</sup> SiC devices along with a variety of gate drivers in numerous topologies. The TOLL power daughter card interfaces with one of the Wolfspeed SpeedVal Kit motherboards to enable testing a variety of Wolfspeed SiC MOSFETs in the TOLL package. This power daughter card supports both double pulse testing (DPT) as well as system testing in many common topologies and includes a thermal management system with heatsink and electrical insulator. Test points allow for waveform capture of V<sub>GS</sub>, V<sub>DS</sub>, as well as I<sub>DS</sub>. This power daughter card can be used to:

- Evaluate SiC MOSFET switching performance including measurements of  $E_{ON}$ ,  $E_{OFF}$ , and  $Q_{rr}$
- Evaluate SiC MOSFET thermal performance and efficiency in a power converter

Wolfspeed power daughter cards are available for many of our SiC MOSFETs. This document serves as a guide to all TOLL package daughter cards. The naming convention followed for the SpeedVal Kit power daughter cards is shown in Figure 1.

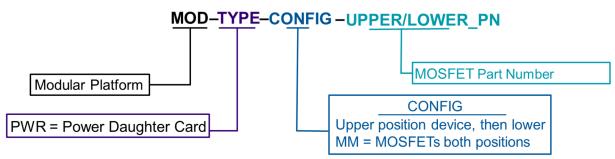


Figure 1: Power Daughter Card Naming Convention

### **1.1 Part Numbers Available**

Power Card Part Number	MOSFET Part Number	<b>Blocking Voltage</b>	$R_{DS(on)} m\Omega$
MOD-PWR-MM-C3M0025065L	C3M0025065L	650	25
MOD-PWR-MM-C3M0045065L	C3M0045065L	650	45
MOD-PWR-MM-C3M0060065L	C3M0060065L	650	60

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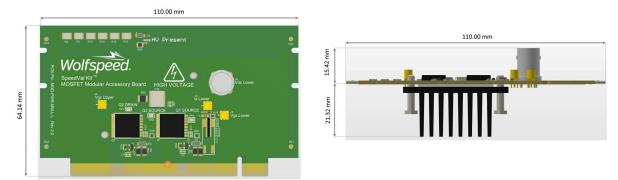
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# 2. Board Overview

### 2.1 Size

The physical dimensions of power daughter card MOD-PWR-MM-...*L* are 110 mm X 64.1 mm, as shown in Figure 2. The depth of the assembly varies depending on the heatsink installed. The power daughter card is a printed circuit board (PCB) with two TOLL package MOSFETs in half-bridge configuration, heatsink (including mounting clips), thermal pad, and hardware accessories.



*Figure 2: Dimensions of the power daughter card: Top view (left) shows the length and width of the board; Side view (right) shows the length and height of the board.* 

### **2.2 Connection**

The power daughter card is an accessory board that plugs into the SpeedVal Kit motherboard. The modularity of the power daughter cards enables the user to quickly switch between different MOSFET  $R_{DS_ON}$  values or even different package types for their design analysis and tests. The daughter card can be mounted on the motherboard as shown in Figure 3.

The power daughter card is connected to the motherboard through a 164-pin connection. The 164 pins are used for various net connections between the two boards. These connections are:

- DC link voltage : +Vbus and -Vbus
- Midpoint or switch node
- Gate and source connections for each device
- Current sense connection
- Thermistor connection
- Miller clamp connections

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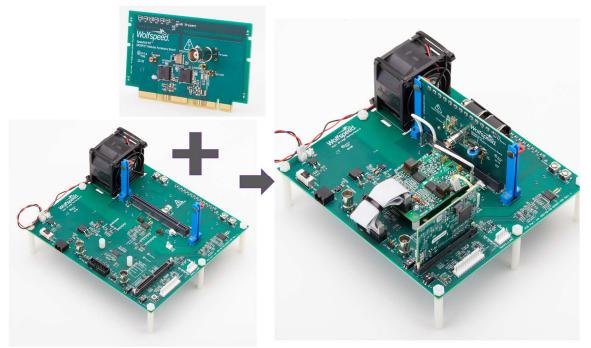


Figure 3: Motherboard and power daughter card assembly

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### **3. Electrical Features**



#### CAUTION

IT IS NOT NECESSARY FOR YOU TO TOUCH THE BOARD WHILE IT IS ENERGIZED. WHEN DEVICES ARE BEING ATTACHED FOR TESTING, THE BOARD MUST BE DISCONNECTED FROM THE ELECTRICAL SOURCE AND ALL BULK CAPACITORS MUST BE FULLY DISCHARGED.

SOME COMPONENTS ON THE BOARD REACH TEMPERATURES ABOVE 50° CELSIUS. THESE CONDITIONS WILL CONTINUE AFTER THE ELECTRICAL SOURCE IS DISCONNECTED UNTIL THE BULK CAPACITORS ARE FULLY DISCHARGED. DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW THE BULK CAPACITORS TO COMPLETELY DISCHARGE PRIOR TO HANDLING THE BOARD.

PLEASE ENSURE THAT APPROPRIATE SAFETY PROCEDURES ARE FOLLOWED WHEN OPERATING THIS BOARD AS SERIOUS INJURY, INCLUDING DEATH BY ELECTROCUTION OR SERIOUS INJURY BY ELECTRICAL SHOCK OR ELECTRICAL BURNS, CAN OCCUR IF YOU DO NOT FOLLOW PROPER SAFETY PRECAUTIONS.

#### 警告

**通**电时不必接触板子。连接器件进行测试时,必须切断板子电源,且大容量电容器必须释放完所有电量。

**板子上一些**组件的温度可能超过 50 摄氏度。移除电源后,上述情况可能会短暂持续,**直至大容量**电容器 完全释放电量。通电时禁止触摸板子,应在大容量电容器完全释放电量后,再操作板子。请确保在操作 板子时已经遵守了正确的安全规程,否则可能会造成严重伤害,包括触电死亡、电击伤害、**或**电灼伤。

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ボードのモジュールの温度は50度以上になるかもしれません。電源を切った後、上記の状況がしばら く持続する可能性がありますので、大容量のコンデンサーで電力を完全に釈放するまで待ってくださ い。通電している時にボードに接触するのは禁止です。大容量のコンデンサーで電力をまだ完全に釈 放していない時、ボードを操作しないでください。

ボードを操作している時、正確な安全ルールを守っているのを確保してください。さもなければ、感 電、電撃、厳しい火傷などの死傷が出る可能性があります。

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Each power daughter card has two devices connected in a half-bridge configuration and various components to support their performance. The values of these components can vary based on the part number of the MOSFET. The power daughter cards are designed to support up to 650 V class MOSFETs. This section discusses various components or PCB features along with their purpose on the daughter card. The various features of the power daughter card are labeled in Figure 4.

### 3.1 High Voltage Indication and Discharge

A series of 6 X 20 kΩ resistors are located on the top of the board, as labeled in Figure 4. The bleeder resistors assist in discharging the DC link voltage upon switching off the input power supply. The board also has an LED indicator, which will turn on to indicate the presence of high voltage on the board.



IMPORTANT NOTE: The bleeder resistors and LEDs should only be used as an indication, not a safety feature. The 'HIGH Voltage Indication LED' in the off state is not an indication of the DC link being completely discharged. For your safety, make sure the system is discharged by measuring with a calibrated instrument rated for at least 1000V before handling the hardware.

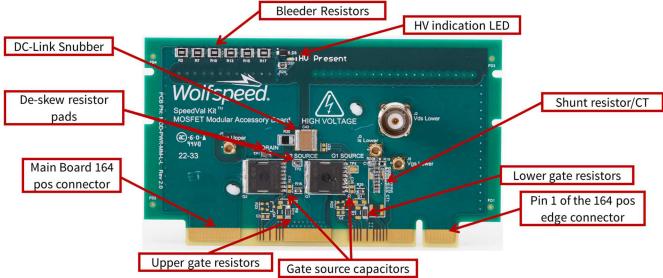


Figure 4: Power daughter card: front view showing various components and features of the board

### 3.2 DC-Link Snubber

A series RC snubber is placed directly across the DC bus on this board. The snubber helps to reduce noise propagating to the DC bus due to switching of the devices. It works by damping the voltage oscillations during switching events without adding to the switching losses of the MOSFETs.

### **3.3 Current Sensing**

The board comes populated with shunt resistors for current measurement. There are eight parallel 0603 resistors to form a low-impedance current shunt. The boards come populated with low resistance values to enable system testing at high power. However, for DPT testing only, the resistors can be replaced with a higher value for more accurate measurements. Details on the current sensing options and best practices are discussed in Section 5.

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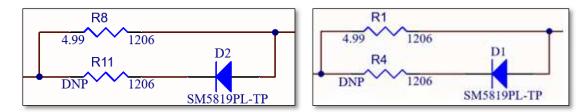
### **3.4 Gate Resistors**

Many gate driver daughter cards come pre-populated with a non-zero gate resistance. The power daughter cards have a pre-populated gate resistor that has been optimized to be the only gate resistance in the circuit. Therefore, it is recommended to replace the gate resistors on the gate driver daughter cards with zero-ohm resistors as many gate driver cards come with a non-zero gate resistor populated. The gate drive path on the power daughter card supports an asymmetrical turn-on/turn-off resistance. There are two gate resistors in 1206 packages. One is connected directly to the gate, while the other is in series with a diode. This allows the user to tune their turn-on and turn-off behavior individually based on the application requirements. The diode is pre-populated to provide a lower turn-off resistance and can be rotated 180° to provide a lower turn-on resistance. The effective value of gate resistance for the upper device is:

- Turn-on: R<sub>g</sub> = R8
- Turn-off: R<sub>g</sub> = R8 || R11

Similarly, for the lower device, the gate resistance is:

- Turn-on: R<sub>g</sub> = R1
- Turn-off: R<sub>g</sub> = R1 || R4



*Figure 5: Asymmetrical Gate resistor configuration: for the upper device(Left) and lower device (right)* 

### 3.5 Gate to Source Capacitor

There is a provision for a 0603 capacitor between the gate and source of each SiC MOSFET. A 1nF capacitor is prepopulated for some of the variants of this board. The added gate to source capacitor slows the di/dt of the MOSFET during turn-on and reduces the impact of the Miller capacitance on the gate during turn-on.

### **3.6 Low Inductance Path for DC Link Connection**

The 164-position edge connector has 82 pins on each side, i.e., the top and bottom of the board. Pins on opposite sides of the board are utilized for the DC link connection to reduce the loop inductance of the DC link path. The high pin count of the connector and the overlapping DC bus layers enables the insertion of a connector between the motherboard and the MOSFETs without compromising the performance of the system by minimizing the parasitic inductance in the switching loop.

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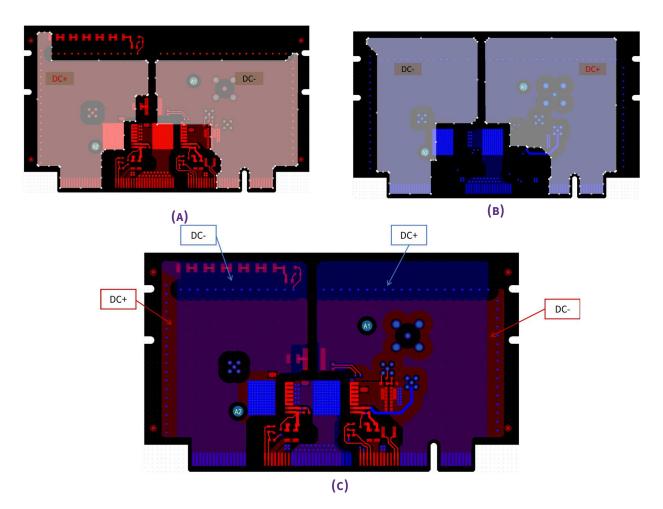


Figure 6: The copper pours for the DC Link connections between the motherboard and power daughter card. These images show how the loop inductance in DC link is reduced.

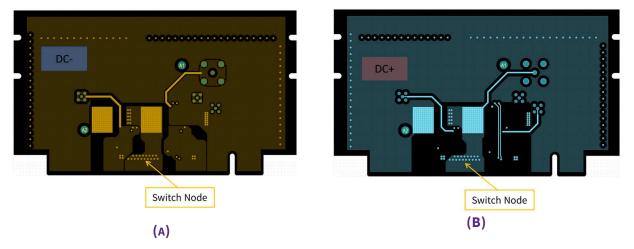


Figure 7: Copper pours for the +/- Vbus in the inner two layers of the pcb to minimize the loop inductance between the connection points on the board.

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### 3.7 De-skew Resistor

Signal propagation delays vary when different probes and connectors are used for voltage and current signals, which can lead to incorrect measurements for switching energy. It is critical that  $V_{DS}$  and  $I_{DS}$  are deskewed (time aligned) before making switching energy measurements. Measuring switching energy without deskewing  $V_{DS}$  and  $I_{DS}$  can result in an error of more than 2X. A low-inductance resistor on the order of approximately 5 Ohms has been found to work well for deskewing and has been included with the motherboard. This resistor can be placed on the sockets shown in Figure 8 on the power daughter card. Please refer to the SpeedVal Kit Motherboard User Guide for more information on the deskewing process and methodology.

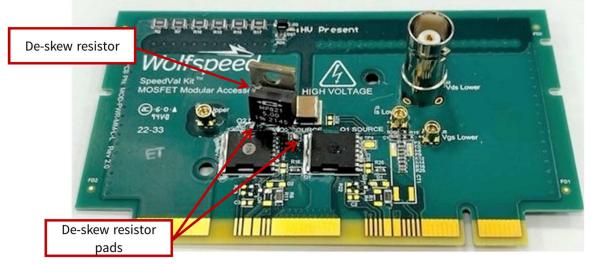


Figure 8: Deskew resistor position on the power TOLL power daughter card

### 3.8 Miller Clamp

A flexible miller clamp circuit is provided on the power daughter card. The cards come with a zero-ohm resistor (R29 and R27) populated to connect the miller clamp signal from the card edge connector directly to the MOSFET gate. This provides compatible gate driver daughter cards with an integrated miller clamp MOSFET the ability to provide a low-impedance path from the gate to the off-state gate bias voltage in order to reduce the impact of dv/dt induced partial turn-on of the MOSFET when the opposite device switches on.

Alternatively, the PCB supports a local miller clamp MOSFET close to the power SiC MOSFET on the power daughter card. To utilize this circuit, the zero-ohm bypass resistor should be depopulated, and the local miller clamp MOSFET (Q3, Q4) a pull-down resistor (R22, R23), and decoupling capacitor (replace R31 and R28 with 0.1uF ceramic capacitor) should be populated. The gate driver daughter card must have the ability to drive an N-channel external miller clamp MOSFET to utilize this approach.

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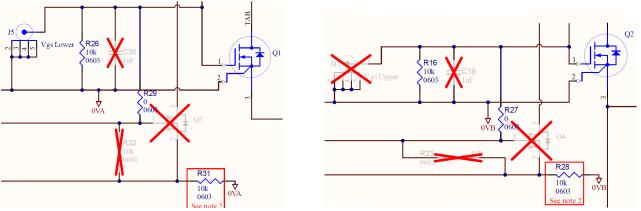


Figure 9: Miller clamp circuits for low-side (left) and high-side (right) MOSFETs

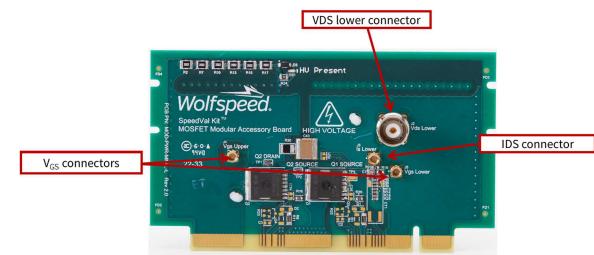


Figure 10: Test points for capturing voltage and current waveforms

Figure 10 shows the various test connectors located on the board. These are:

- **J2:** The drain-source voltage,  $V_{DS}$ , of the lower device can be measured using a BNC connector.
- **J4 and J5:** Two MMCX connectors are provided for measuring the gate-source voltage, V<sub>GS</sub>, waveform of the lower and the upper device respectively.
- **Warning**: Upper V<sub>GS</sub> connector (J4) should only be probed with an isolated probe, otherwise there is potential to damage the probe and the oscilloscope. For this reason, this connector comes unpopulated

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# 4. Test Points



but is included with the daughter card. If an isolated scope probe such as Tektronix, Inc.'s  $IsoVu^{\circ}$  probe is available, then this connector can be installed for capturing  $V_{GS}$  on the upper device.

• **J3:** Another MMCX connector is provided for measuring the drain current  $(I_D)$  through the lower device when using the shunt resistors for current measurements.

# 5. Current sensing

The power daughter cards come populated with shunt resistors (eight paralleled 0603 resistors). This shunt can be optimized for either continuous power testing or DPT switching loss measurements. The power daughter cards come pre-populated with low-resistance shunt resistors optimized for steady-state power testing. The shunt resistors can measure the current waveform for switching energy analysis by replacing the prepopulated values with a higher resistance value to improve signal-to-noise ratio.

For power testing, the shunt resistance is kept to a minimum to keep power dissipation in the shunt within the limits of the packages. This lower shunt resistance displays more ringing and higher measured peak currents at the turn-on switching edge due to noise and parasitic elements in the circuit impacting the signal. Each power daughter card has a small compensation network to mitigate these effects and provide accurate RMS currents, however the waveform behavior at the switching edges will not accurately represent the true current and the switching energy accuracy will not be ideal when using the low resistance shunt values. For this reason, it is recommended to adjust the shunt resistors and filters to be optimized for switching energy measurements when performing DPT. If the shunt is reconfigured for switching energy measurements, the power daughter card cannot be used for power testing until it is reverted to its original state or else damage could occur to the power daughter card and motherboard.

To optimize the shunt for switching energy measurements, the shunt and compensation network should be changed to the circuit shown in Figure 11.

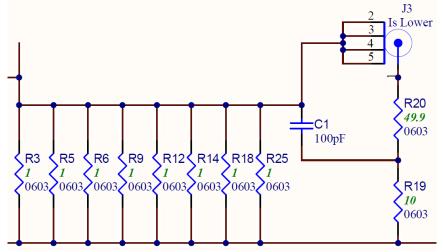


Figure 11: Switching Energy Optimized Shunt

The values shown in Figure 11 are optimized for all variants of the power daughter card for double pulse testing. Figure 12 and Table 2 show the optimized shunt filter values for each variant of the board with different MOSFETs

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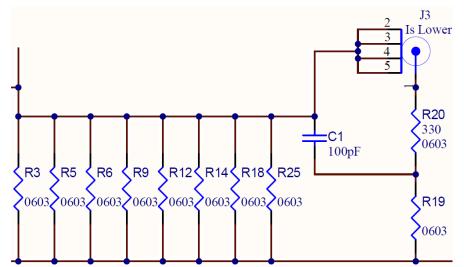


Figure 12: Power testing Optimized Shunt: Resistor values provided in Table 2

Table 2 summarizes different filter configurations that have been used to tune the filter for each MOSFET part number when power testing. The boards come with the correct filter preinstalled.

Power Card Part Number	SHUNT CONFIGURED FOR POWER TESTING			Scope	R33	R34
	Number of resistors	Footprint	Individual	Scaling	(Ω)	(Ω)
	in parallel		resistor value	(A/V)		
MOD-PWR-MM-C3M0025065L	8	0603	40mΩ	200	130	330
MOD-PWR-MM-C3M0045065L	8	0603	40mΩ	200	100	330
MOD-PWR-MM-C3M0060065L	8	0603	80mΩ	100	62	330

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# 6. Thermal management

The devices are attached to a clip-on heatsink on the back side of the board. A thermal interface material (TIM) is applied between each device and the heatsink to provide electrical isolation while maintaining low thermal impedance.

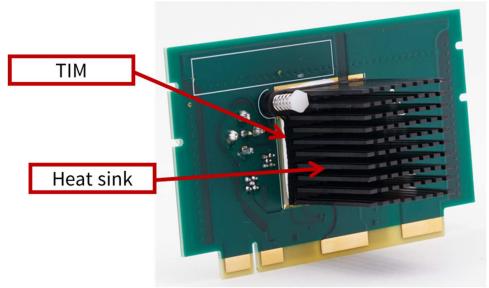


Figure 13: Power daughter card: back view showing devices and thermal management system

The power daughter card is ready for power tests when shipped. For the TOLL package, the devices are mounted on the top of the PCB, and a heatsink is attached to the back side of the PCB. An array of thermal vias conduct heat through the PCB from the drain tab of the devices to the back of the PCB. A layer of Aluminum Nitride (AlN) thermal interface material (TIM) is applied between the PCB and the heatsink. There is a thin layer of nonconductive thermal grease applied to both sides of the AlN TIM to fill any voids. AlN is a good choice for TIM due to its high thermal conductivity and high electrical insulation properties. The heatsink has spring loaded push-pins for good contact between the devices and the PCB.

The TIM can be replaced for experiments; however, it should be noted that the ambient thermal resistance  $(R_{th,CA})$  could change.

Figure 14 illustrates the steps to reassemble the devices and heatsink should the MOSFET(s) or the TIM need to be replaced:

- Step 1: Populate PCB (PN#: MOD-PWR-MM-...L) with components and SMD packages following provided assembly layout drawings
- Step 2: Apply thin layer of thermal grease (~100μm) to bottom side of heat sink (PN#: 960-31-xx-F-AB-0) in a well-controlled manner
- Step 3: Apply thin layer of thermal grease (~100μm) to one side of AlN sheet (PN#: ALN\_32x32x1) in a well-controlled manner
- Step 4: Place AlN (thermal grease side down) onto pad on bottom of PCB

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Step 5: Place heatsink on top of AlN on PCB
 Press heat sink push pins through the mounting holes in PCB to secure to board
 Wipe away any excess thermal grease

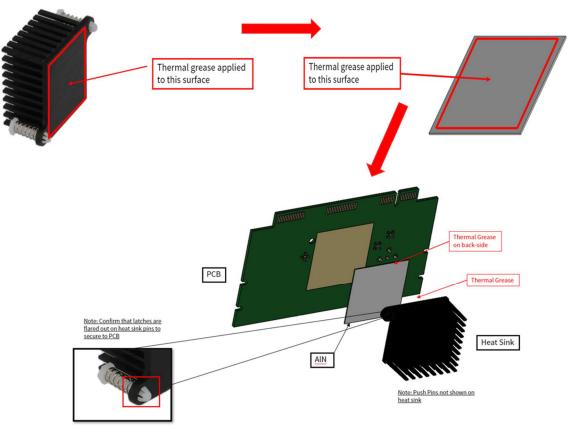


Figure 14: Assembly procedure for MOSFETs and heatsink

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### 7. Revision history

Date	Revision	Changes
December 2022	Rev. 1	1 <sup>st</sup> Issue
March 2024	Rev. 2	Added new parts. Formatting
		and editing changes.

## **8. IMPORTANT NOTES**

#### **Purposes and Use**

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• compliance with applicable regulatory or safety compliance or certification standards that may normally be associated with other products, such as those established by EU Directive 2011/65/EU of the European Parliament and of the Council on 8 June 2011 about the Restriction of Use of Hazardous Substances (or the RoHS 2 Directive) and EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (or WEEE). The board is not a finished end product and therefore may not meet such standards. Users are also responsible for properly disposing of a board's components and materials.

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