Understanding How to Use Ferrite Beads in a SiC Gate Driver Design

Often used with switching transistors and high-power electronics to filter out noise in the power supply lines, ferrite beads employ magnetic materials to produce a lossy inductance when inserted into a circuit. While ferrite beads themselves can be relatively simple in their design (e.g., singular holes, plural holes/turns, toroidal, solenoidal), their applicational design considerations can range in complexity. From power supply filtering and noise suppression on PCBs to common-mode chokes on multiconductor cabling, ferrite beads offer EMC solutions to a wide range of applications.

Understanding basic ferrite bead parameters is pertinent in terms of integrating it into a particular application to suppress EMI. One such application is the installation of a ferrite at the gate of a silicon carbide (SIC) gate driver to dampen any ringing and unwanted resonances. This paper will explore best practices as it relates to the use of ferrite beads in a SiC gate driver design.

The Ferrite Bead: A Bird's-eye View

Commonly used for electromagnetic interference (EMI) suppression, ferrite beads are often small, cylindrically shaped, non-conductive ceramic parts that include a combination of metal oxides such as cobalt, iron, nickel, zinc, or magnesium. When placed along an electrical path, these components are known to remove noise energy by converting it to heat energy.

A ferrite bead, in essence, acts as an RF choke, introducing high-frequency resistance into a circuit without adversely affecting low-frequency performance. The construction of a ferrite can vary from a rod for high-power RF chokes in grounded grid linear amplifiers to a clamp for common-mode suppression on cabling to a bead and SMT component for installation on a PCB.

Materials

Common ferrite cores include manganese zinc (MnZn) and nickel zinc (NiZn) composites. The MnZn typically falls into the 0.1-MHz to 1.5-MHz range, while the highest-frequency performance can be found with the NiZn ferrite materials at about 1 MHz up to 2 GHz due to their higher resistivity compared with the MiZn ferrites.

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Typically, MiZn ferrites exhibit the highest magnetic permeability — a property that refers to the ability of a material to conduct magnetic fields — and therefore can more readily eliminate unwanted EM fields. However, the frequency range, resistivity, temperature stability, and insertion loss can all vary based upon the quality of the fabrication process and the proportions of the various materials used. Ultimately, a designer will need to assess the electrical feasibility of a ferrite bead by understanding the basic EMI sources in a specific application circuit and the range of unwanted frequencies that crop up. Ideally though, the ferrite bead of choice should exhibit the highest resistance in the required bandwidth with undesired oscillations.

Basic Parameters

Datasheets and product descriptions will generally include basic parameters such as impedance at particular frequency points such as 25 MHz or 100 MHz, maximum DC resistance, maximum rated current or power, and bead dimensions such as outer diameter (OD), inner diameter (ID), and length (L). While these parameters grant some insight into the properties of the ferrite materials, it does not provide the more detailed impedance information over the bead's operational frequencies. As stated earlier, this is necessary in order to choose the optimal ferrite bead for a particular noise suppression application.

Generally, ferrite beads involve an increasing impedance (Z), resistance (R), and inductive reactance (X), or permeability, with frequency. After a particular frequency, the reactance begins to decrease while the resistance and impedance both increase. These trends can be observed on what is known as the "ZRX" plot (***Figure 1***), where the impedance-frequency characteristics are more apparent.

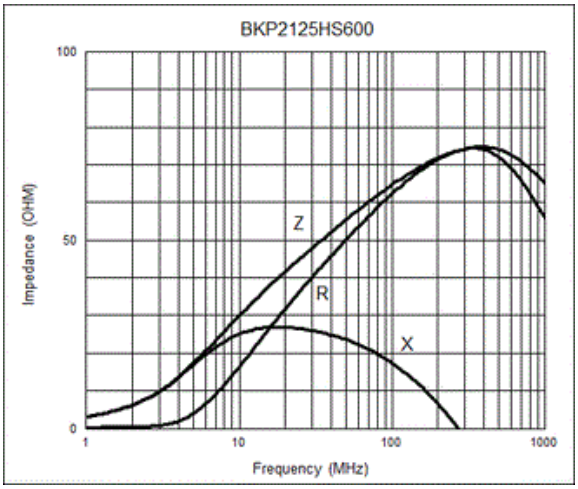

Figure 1: *ZRX curve for the BKP2125HS600 (Source: Taiyo Yuden)*

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Understanding The Ferrite Bead's Frequency Response

Typical ferrite constructions for PCBs include surface mount (SMT) and cylindrically shaped beads with either a singular hole or a plurality of holes such as a binocular core with two through-holes or a multiturn ferrite bead with six through-holes. Typically, the smaller size and large OD-to-ID ratio found in through-hole ferrite beads do not lend themselves toward the application of multiple turns, even with the use of larger-gauge (thinner) wire. However, these smaller dimensions allow for a higher frequency at which self-resonance will occur. And, as with any inductor, a self-resonant frequency will occur, resulting in a high impedance at a specific frequency.

The lumped-element R, L, and C models for ferrite cores vary based upon the material, its dimensions, and the number of turns utilized. The resistance (R) is mostly due to eddy current in the core, while the stray capacitance (C) is distributed from turn to turn and from turn to core. This interwinding capacitance increases with an increase in the number of turns — desirably increasing the impedance at higher frequencies while maintaining a low impedance at low frequencies. This effect can also be accomplished by placing ferrite beads in a line.

The SMT ferrite bead is often fabricated using ceramic processing technology and typically involves the use of embedded electrodes in soft ferrite sheets forming an inductor implemented within a ferrite structure in either a toroidal or solenoidal shape. This way, a higher impedance can be achieved as compared with the through-hole ferrite bead structure. Some frequency responses affect a much sharper impedance at resonance, while wider bandwidth ferrites can exhibit more gentle curves. As with any ferrite bead, it is important to understand the impedance required within the desired frequency band so as to better suppress unwanted noise signals.

For SMT ferrite beads, lumped-element models will include R, L, and C equivalent resistance, wherein the resistive losses are associated mainly with skin effect as well as magnetic losses in the ferrite core. Stray capacitance is distributed within the turn-to-turn capacitance, turn-to-core capacitance, and layer-to-layer capacitance for multilayer coils. This parasitic capacitance acts as a lumped capacitance parallel to the inductor, causing an unavoidable self-resonance. At low frequencies, or before the parallel LC resonance, the inductive characteristic of the SMT ferrite bead is dominant. After self-resonance, the capacitive characteristic becomes dominant due to the magnetic field from the conductor current being confined between the inner conductors, ultimately contributing to a roll-off in impedance.

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Parameters To Consider When Selecting Ferrite Beads

DC Current Rating

The frequency response of a ferrite bead can be altered dramatically when used in a circuit that surpasses the specified DC current rating. As the DC bias increases, the magnetic material approaches saturation and its permeability decreases, causing part (or all) of the signal to fall into the non-linear region of the ferrite. Practically speaking, this causes a noticeable drop in the impedance within its rated bandwidth. This phenomena can drop the impedance up to 10× its nominal value, leaving the distinct possibility for an EMI failure whereby noise cannot be adequately suppressed.

Temperature Dependence

The permeability of ferrite materials also varies as a function of temperature. As stated earlier, the ferrite core converts RF energy into heat, ultimately heating the ferrite material to a point. However, beyond a certain temperature, the magnetic characteristics of the bead are altered, causing a degradation in the permeability, which in turn leads to thermal runaway and part failure.

Ferrite Bead Uses In SiC Gate Driver Circuits

Ferrite beads offer solutions in a broad spectrum of applications. One such application is isolating power planes from power supply noise, with SMT ferrite beads placed close to voltage regulator modules (VRMs). These components can also be leveraged to prevent high-frequency oscillator noise from reaching a load or to dampen ringing on long interconnections between fast logic gates. Depending upon the bandwidth, impedance, and rated current, a variety of ferrite beads can be leveraged to suppress noise/ringing/high-frequency oscillations on a range of components from switching converters to motors. However, the second part of this article focuses on a major contemporary design challenge: the usage of ferrite beads on the gate drive loop to prevent unwanted ringing.

Common Power Switches

Gate drive circuits are leveraged in high-speed switching and power electronics applications in order to both provide voltage isolation between the controlling logic signals and the output power as well as provide independent control for the transistor of choice by supplying the adequate voltages for switching. Typically, wide-bandgap (WBG) semiconductor materials are used, as they can support the high voltage and current ratings required in these applications. Some common transistors substrates include silicon (Si), gallium nitride (GaN), and SiC.

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General SiC MOSFET Gate Driver Parameters		
Parameter	**Description**	**Value**
Supply Voltage Range	The specified +/– gate-source voltage maximum rating (V_{GS}) under transient events (<100 ns) and nominal rating (V_{GS-op}) in recommended operating range.	V_{GS}: –8/+19 V V_{GS-OP}: –4/+15 V
CMTI	Need for high CMTI with smaller external gate resistance (R_G) to maximize efficiency with the high dv/dt (>150 V/ns) generated.	>150 kv/µs
VIORM	Maximum repetitive peak isolation voltage.	>1700 V
Driving Capability	Maximum repetitive peak isolation voltage.	>10 A
Output Pull-Up/Pull-Down $R_{DS(ON)}$	The lower the $R_{DS(ON)}$, the more current the driver can deliver for the same value of R_G.	––
Propagation Delay Time and Channel Mismatch Time	Time it takes for a signal change on the input to be registered at output. Must be kept to a minimum.	<10 ns
Active Miller Clamp	Avoids parasitic turn-on of the transistor due to the Miller capacitor.	––
Fast Short-Circuit Protection	Safe shutdown of transistor, preventing fault currents.	<1.8 µs

Table 1: *Parameters to consider when selecting SiC MOSFET gate drivers*

The Si MOSFETs and insulated-gate bipolar transistors (IGBTs) are typically used, as they offer a wide bandgap and high electric field breakdown voltages with adequate electron mobility for high-speed switching. More recently, SiC MOSFETs have been leveraged in high-power applications for their optimal performance in both power handling and switching speeds.

Brief Overview of SiC Gate Driver Implementation Considerations

In terms of gate drive implementation, there are several considerations for SiC MOSFETs that diverge from the traditional Si transistor — particularly in regard to the faster switching speeds. (***Table 1***) lists some basic parameters to consider when selecting and integrating SiC MOSFET gate drivers into a design.

In general, a good gate driver topology will allow a ±5% tolerance on the specified nominal gate-source voltage (V_{GS-op}), while a tolerance of ±2% is achievable with a tight feedback control — ultimately avoiding the maximum voltage ratings that allow for ringing and overshoots on top of the continuous gate drive voltage. The high dV/dt — the rate of change of voltage over time — found in SiC MOSFETs requires a combination of a lower external gate resistance (R_G) and high common-mode transient immunity (CMTI) to avoid latch-up failures with excessive current running through the transistor.

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The drive capability of the chosen gate driver is critical in that it determines the extent of current that can be pumped into the SiC MOSFET to turn it on as well as current taken out to turn the MOSFET off. In other words, this optimizes the switching speed. Additional protective circuitry is also necessary in order to ensure robust performance of the entire system.

As shown in (***Figure 2***), there are several potential solutions in order to properly implement a gate driver circuit, including:

- Placing the gate driver close as close to the MOSFET as is possible
- Optimizing the switching speed to be mindful of dV/dt
- Minimizing the gate loop inductance with a symmetrical PCB layout
- Placing a small capacitor between the gate and the source
- Keeping the power traces away from the gate loop
- Placing a ferrite bead in series with the gate

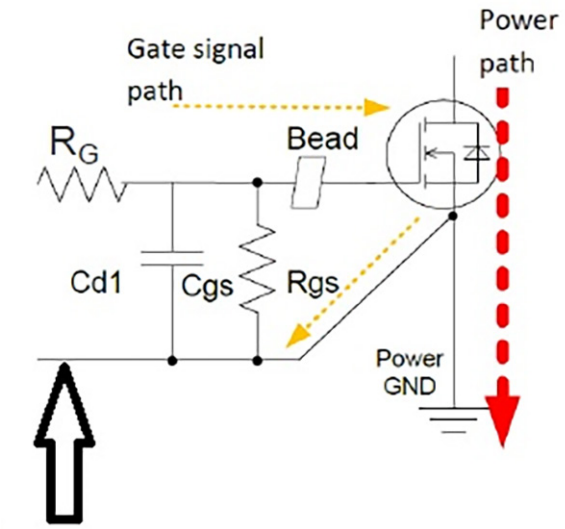

Figure 2: *Placing a ferrite bead at the gate leg reduces voltage spikes and ringing on the gate.*

While all of the above are important to consider when implementing a SiC gate driver circuit, the next section focuses on the dampening effects of the ferrite bead used at the gate.

Parasitic Oscillation and the Choice of Ferrite

In configurations featuring a high-side MOSFET and a low-side MOSFET (e.g., H-bridge, three-phase bridge), the high-side MOSFET can turn on faultily when the low-side transistor exhibits parasitic oscillations, causing overvoltage transients on the gate and potential hardware failure.

The SiC MOSFETs are particularly susceptible to these oscillation conditions due to the high dV/dt — the quick change in drain-source voltage during a switching transient induces a current in the low-side MOSFET to flow from the drain, through the gate-to-drain capacitance, to the gate circuitry. And when the gate-source voltage is higher than the threshold voltage during the rise time of the high-side transistor, the low-side MOSFET will undesirably turn on.[1] This is particularly troublesome with high-power devices, as these parasitic resonances can couple to a positive feedback loop that can potentially sustain or amplify the oscillations.

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Increasing the gate resistance (R_G) is typically sufficient at suppressing these resonances; however, that comes with the tradeoff of slowing down the switching speeds. Because parasitic oscillations from these circuits typically fall within the 50-MHz to 200-MHz range, the use of a ferrite bead of 30-Ω to 40-Ω impedance at 25 MHz to 100 MHz in frequency with a maximum drive current of no more than 2 A to 3 A is often sufficient in dampening the ringing in SiC gate drivers without negatively impacting switching performance. When used in series with a small R_G, there is a drop in parasitic oscillation while minimizing switching losses.

Choosing The Right Ferrite Bead For Sic Gate Drivers

Understanding a high impedance within the bandwidth at which undesired high-frequency noise occurs is particularly important to adequately suppressing the noise without affecting the low-frequency performance of a device. Furthermore, understanding the ferrite bead's frequency response (ZRX curve) and how it may change with respect to the number of turns, number of beads, dimensions, layout, current rating, or temperature can be illuminating in the design process.

Generally, the ferrite bead will function optimally only within its specified current rating where low-frequency performance and switching performance will likely be degraded if the ferrite bead is driven beyond its maximum ratings. And, as with most electronic circuitry, temperature fluctuations/extremes can adversely affect performance, so working within the specified temperature ratings is key to predictable performance.

In some applications, multiple ferrite beads can be used; however, this is often unnecessary and an overly tedious process, particularly in regard to installing ferrite beads in the gate leg of SiC gate drivers. For this application in particular, SMT NiZn beads would often be leveraged for their performance well into the VHF band without adding extra wiring and parasitics that could potentially make EMI worse.

Ultimately, understanding the design considerations of ferrite beads can demystify the process of integrating a ferrite bead into a circuit.

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References

1. Gachovska, Tanya K., Hudgins, Jerry L., “SiC and GaN Power Semiconductor Devices,” Power Electronics Handbook. Elsevier Science, 2017. 140–145.
2. Dodge, Jonathan, “Eliminating Parasitic Oscillation between Parallel MOSFETs,” Advanced Power technology. Application Note, APT-0402 Rev A. 2004.

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