Demystifying PCB Layout Methodologies for SiC Gate Drivers

When designing the printed circuit board (PCB) layout for any high-power or high-voltage system, the gate drive circuitry can be particularly susceptible to parasitic impedances and signals. Silicon carbide (SiC) gate drivers require even closer attention to the details due to voltage and current slew rates that are typically much faster than with silicon. Following specific PCB design guidelines can help mitigate these common pitfalls and eliminate failures in the lab or in the field.

Benefits and considerations of SiC power circuits

SiC power electronics have the major advantage of high switching frequency along with reduced conduction losses, higher efficiency, and simpler heat management systems. When compared with Si-based converters, these benefits allow SiC power systems to optimize performance in applications that require high power density, like solar power inverters, energy storage systems (ESS), uninterruptible power supplies (UPS), and electric vehicles. However, the high voltage slew rates (dv/dt) and current slew rates (di/dt) inherent to SiC power devices make these circuits more sensitive to crosstalk and false turn-on, as well as to parasitic resonances and electromagnetic interference (EMI), than with their silicon counterparts. (Figure 1).

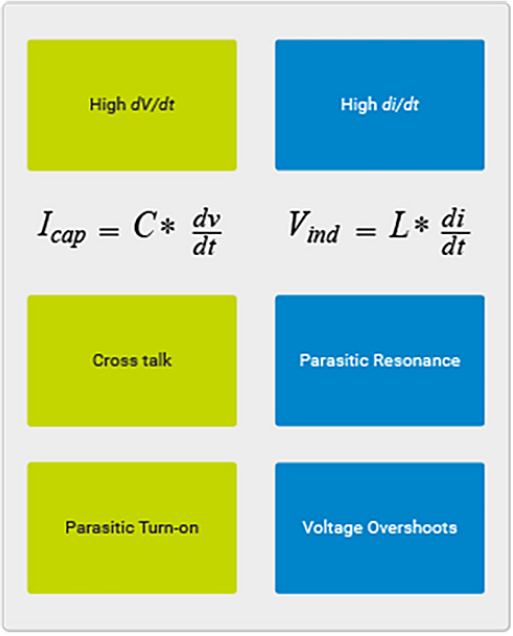

Figure 1: *Summary of the effects of high voltage and current slew rates.*

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When paralleling power MOSFETs, the designer must pay even closer attention to minimizing these effects, as an unequal current distribution between devices may impact performance. For instance, adding one more device in parallel doubles the di/dt during switching transients, potentially resulting in much larger voltage overshoots. Moreover, any parasitic inductances can yield resonances that couple with feedback mechanisms that only worsen current imbalance. In these cases, PCB designers have to pay special attention to mitigating parasitic inductance.

The negative effects of board parasitics on SiC circuits

Parasitic inductance and capacitance found in SiC circuits

To begin, SiC MOSFETs have the desirable quality of inherently low parasitic capacitances (C_{GD}, C_{DS}, C_{GS}). This allows for the high switching frequencies that help enable high-power-density designs. However, this benefit does come with a general susceptibility to resonances from parasitic inductances that inevitably occur within layout. The parasitic inductances themselves can be found within the gate loop (L_{GS}) and power loop (L_{DS}) of the application circuit as well as a common source inductance (L_{CS}). As stated earlier, these inductances stem from long trace lengths and between the device leads themselves.

The gate loop inductance can add ringing on the gate voltage, which, in turn, increases turn-on delay and, in some cases, causes oscillations ringing in the drain-source voltage of the MOSFET. Generally, the gate loop inductance is minimized to avoid spurious operation of the MOSFET, but the effect of this parasitic inductance is the least severe of the three main sources of parasitic inductances.

The power loop inductance, sometimes known as the switching loop inductance, is generally responsible for the overshoot voltage across the device, which yields high switching losses. The common source inductance can create a voltage feedback to the gate drive during switching transients, counteracting change in gate voltage and slowing down the drain current, thereby dramatically increasing the switching losses at turn-on and turn-off.[1] Moreover, a small parasitic L_{CS} mismatch between parallel devices can cause a current imbalance during switching transients, amplifying the effect of negative gate voltage feedback.

It is impossible to completely eliminate all parasitic inductances and capacitances when designing a PCB; however, some commonly-used techniques can help minimize them.

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Addressing SiC gate driver layout challenges

Keeping the power traces away from the gate loop

Typically, the power loop is routed on a single PCB layer often known as the “lateral power loop,” while the first inner layer serves as a “shield layer” that reduces the impact of the field generated within the power loop by the high switching frequency (***Figure 2***). The pulsating current within the power loop induces a current and magnetic field within the shield layer that cancels out the one found in the power loop. Ultimately, this yields a drop in parasitic inductance due to an effective reduction of the contained area within the power loop and gate-drive loop.

Minimize distance between gate driver and MOSFET

Any gate loop inductance will resonate with the input capacitance and cause oscillations in the gate-source voltage, leading to ringing in the drain-source voltage. Placing the gate driver in close proximity to the SiC MOSFET minimizes gate loop inductance with minimal trace lengths. Moreover, this practice also helps maintain a constant value for the common source inductance between designs for paralleled MOSFETs.

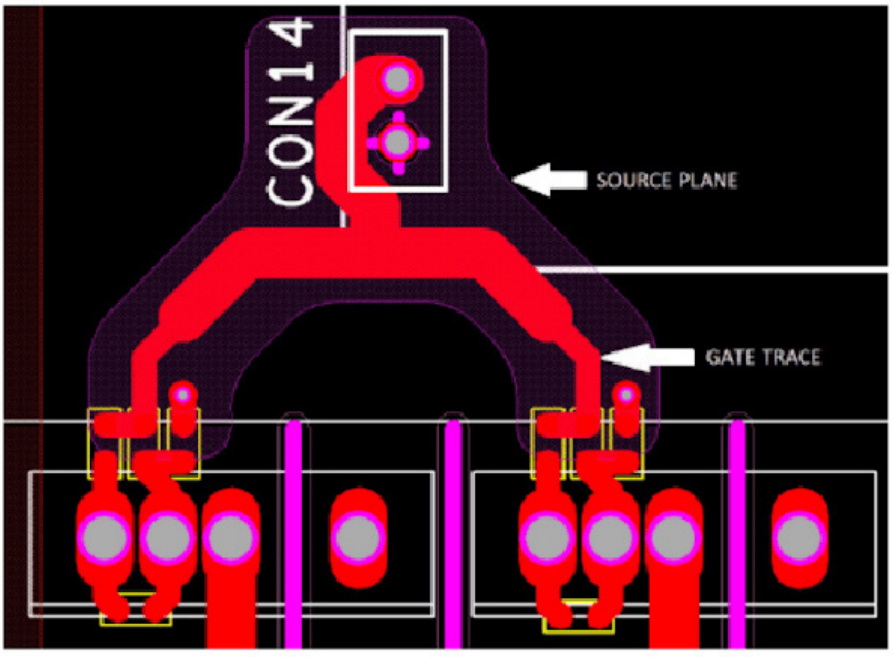

Figure 2: *Reducing the effect of parasitic inductance can be accomplished by cancelling out the magnetic fields in current loop paths and implementing symmetrical trace layout*

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Maintain PCB layout symmetry with minimal trace lengths

It is critical to minimize the circumference of the high-frequency gate loop and power loop so as to reduce the voltage overshoot and any EMI that may be caused by that overshoot. This is particularly important with parallel devices, as the parasitic inductances are inherently higher. As shown in (***Figure 2***) a symmetrical gate drive path for parallel MOSFETs allows a more even current distribution.

Place small capacitor between the gate and the source

As with Si-based circuits, placing a decoupling capacitor between the gate and the source minimizes the gate voltage spike induced by transient signals. The capacitor provides a low-impedance path for the gate-drive current, reducing the rise in V_{GS}. However, this does increase switching losses by slowing down the gate drive signal, so the value of C_{GS} should be adjusted to balance losses with transient immunity.

Add an EMI filter or snubber

Effective EMI suppression can be accomplished by the addition of components such as an RC snubber or a ferrite bead. An RC snubber connected along the DC bus (between the drain and source) absorbs parasitic ringing or voltage overshoots at the drain. A ferrite bead with high resistance and low inductance at high frequencies placed in series with the gate is effective at suppressing parasitic resonances at the gate. This parasitic oscillation is induced from drain-to-source voltage transients that build up a voltage on the gate circuitry, potentially causing a resonance between the capacitance and parasitic inductance (LC tank) at the gate leg. A ferrite bead dampens this oscillation without negatively impacting switching performance.

The additional care needed for SiC-based layout

Layout methodologies for SiC-based power electronics are, in many ways, similar to Si-based circuits. Taking extra care with these layout practices ultimately mitigates the challenges of fast-switching power devices, enabling designers to enjoy all the benefits of silicon carbide in their power supply applications.

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References

1. Z. Chen, D. Boroyevich and R. Burgos, "*Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics*," The 2010 International Power Electronics Conference - ECCE ASIA -, Sapporo, 2010, pp. 164-169, doi: 10.1109/IPEC.2010.5543851

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