Handling Heat with Surface-Mount Power Devices

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As the demand for smaller, faster, cheaper microelectronics pushes devices to operate at higher performance levels, thermal management has become a critical requirement for power electronics, including power supplies, inverters, fast chargers, and motor control.

Through experimentation, the authors examine two thermal management solutions — thermal vias and embedded aluminum nitride (AlN) — and give recommendations on when to use which solution.

A 6.6-kW bidirectional on-board electric vehicle charger reference design demonstrates the suitability of the proposed thermal management solution.

Thermal Management Challenges & Solutions

As electronics applications continue their march toward higher performance from smaller equipment size, so do components toward higher power density. This, in turn, means that our applications generate more heat than ever before. Uncontrolled or poorly managed heat is one of the main causes of electronic system failures, making design time and effort to achieve good thermal management well-spent.

The primary objective of thermal management is to dissipate heat as quickly and efficiently as possible. There are three main ways to transfer heat away from an electronic component: conduction to the PCB, convection into the immediate environment, and radiation to another surface. For many applications, conduction is the most effective and realistic method available to the designer.

Impact of SMDs on thermal management

The use of surface-mount devices (SMDs), which is common for power applications, may help reduce size and make manufacturing automation easier to achieve, but it presents a challenge to thermal management.

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Commonly used printed circuit (PC) laminates (like the glass-reinforced epoxy material FR4), which offer good electrical insulation, are also good thermal insulators. Add to that the demand for SiC-based power devices to increase power density, and the need for carefully considering heat transfer options becomes more important. The high thermal conductivity of a SiC substrate efficiently transfers heat to thermal pads and to the PCB, where it faces high thermal resistance.

The most cost-effective method of overcoming the low thermal conductivity of the PCB laminate is to use thermal-via arrays for low-power applications. But determining the array pattern to maximize thermal performance is not a trivial task.

Much of the available literature[1][2][3] discusses placement of thermal vias directly underneath the thermal source. However, placing copper-plated thermal vias on the PC board results in yet another challenge,[1] as shown in (***Figure 1***). With the thermal vias under the solder pad of devices, solder flows or "wicks" into vias during the reflow process. This causes voids at solder joints, adversely affecting their reliability and lifetime.

Figure 1: *Solder voiding due to wicking of solder into copper-plated thermal via under the device*

This problem can be avoided by filling the vias with thermally conductive material, such as a resin or copper. Whatever technique is used to fill the vias, it calls for additional material as well as processing. This adds to the cost of manufacturing.

Another method of overcoming the laminate's low thermal conductivity is to use an insulated metal substrate (IMS) base.[4] IMS is widely used with PCBs for high-brightness (HB) LED lighting, but for multi-layered PCB designs, constructions are complex, requiring resin-coated foil or film and thermally conductive pre-pegs. Yet again, this adds to the cost of manufacturing.

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A more recent option available to PCB designers is the use of embedded ceramic. The poor electrical conductivity but good thermal conductivity of the embedded layer opens it up to high-power-density applications.

To aid the designer in choosing the right thermal strategy, a study — discussed subsequently — was conducted to find recommendations on the use of thermal vias and embedded AlN ceramic.

Thermal Vias Fit Low-Power Applications

For this study, information from research and manufacturer literature[2][3] was used to select a 0.3-mm diameter for the thermal-via hole size and 1 mm for their center-to-center separation in the array.

Because thermal vias under devices cause solder wicking, we arranged the vias around the SMD, as shown in (***Figure 2***). With the hole size and center-to-center distance already selected, we only needed to decide how many rows of thermal vias to place on each side of the device.

Different array patterns were selected and simulated to find the best pattern for thermal conductivity in terms of thermal impedance — how many vias in X and Y directions will give the optimum thermal results. To verify the simulation, PCBs with different thermal-via arrangements were fabricated and the thermal impedance measured.

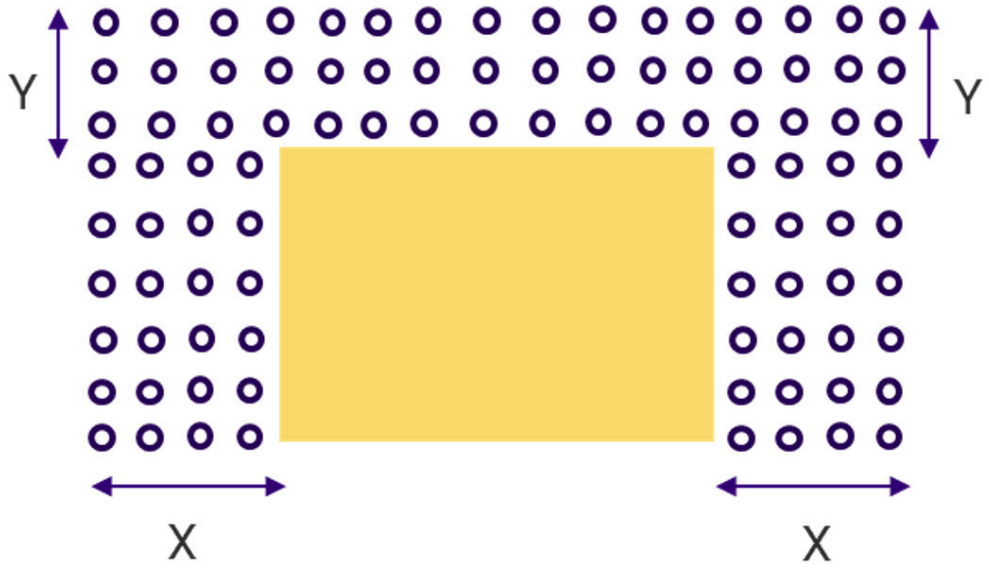

Figure 2: *Thermal-via pattern around the device pad*

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The simulation targeted a seven-lead D2PAK SiC MOSFET. We modeled the device and used a PCB with two copper layers. The copper-layer thickness was ~60 mm and the overall thickness of the PCB was 1.6 mm.

The three selected via patterns considered are shown in (***Figure 3***).

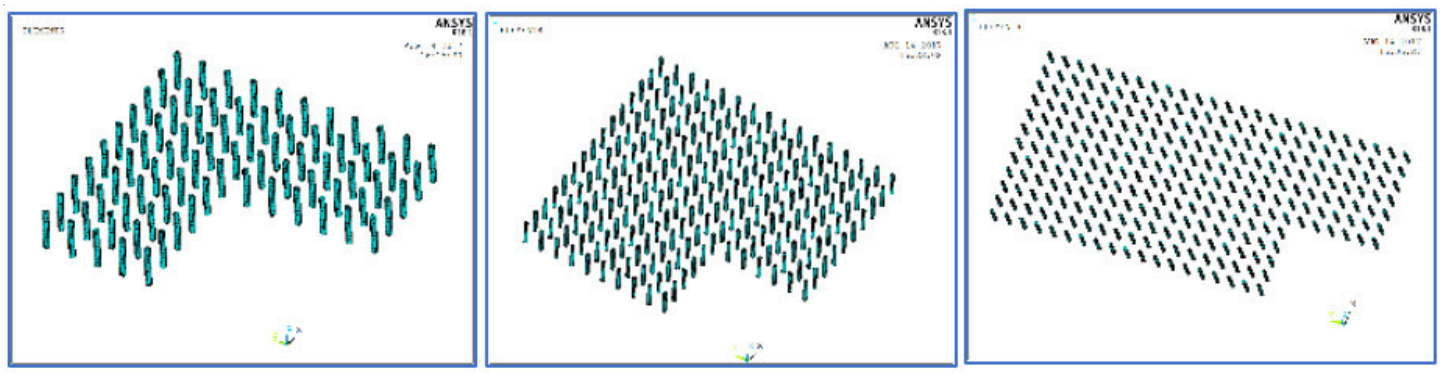

Figure 3: Because patterns are symmetrical, half of each array is shown above. Vias are arranged in five and 10 rows on the three sides of the device in Models A and B, respectively. In Model C, vias fill the entire 1 × 1-inch copper area.

Consider the wide range of materials used by the available thermal management options as well as their widely ranging thermal conductivities and physical characteristics (***Table 1***). The values in the table were used for the simulations.

Materials	Thermal Conductivity (W/m·K)	Specific Heat (J/kg·K)	Density (kg/m^3)
SiC	4,900	750	3.1e3
Solder	50	167	8.4e3
Copper	386	380	8.954e3
Molding Compound	0.99	820	1,980
FR4	0.3	950	1.8e3
Air	0.0257	100.5	1.205
AlN	170	740	3,260

Table 1: *Materials properties for static thermal simulations*

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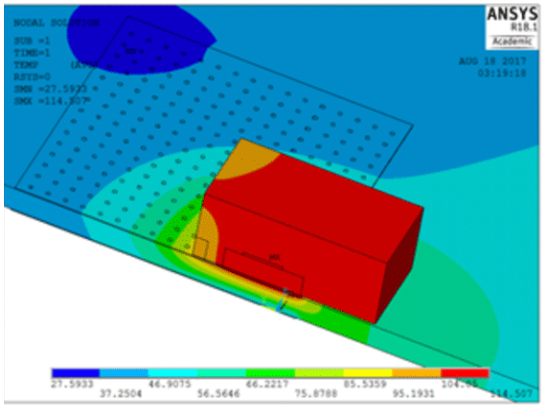
Heat-spread simulations

The simulation boundary condition was fixed with the bottom convection coefficient 1,200 W/m^{2}K. The loss of the power device was 6 W. The simulation of heat spread for Model B is shown as an example in (***Figure 4***). The results of the simulation are shown in the table on the right.



Case	Θjunction-case °C/W	Θsolder °C/W	Θboard °C/W
A	0.51	0.02	3.92
B	0.51	0.02	3.62
C	0.51	0.02	3.92

Figure 4: *Temperature distribution in the simulation for model B (left) and simulation results (right)*

The simulation results show Θboard, the thermal impedance of the PCB board through thermal vias. They reveal that the heat spread was up to the 10th via with a significant fall after the sixth via. It was found that the heat does not spread to all vias, implying that simply adding vias does not help manage heat.

Verification

All models were then fabricated, and the thermal resistance of the PCBs measured experimentally to verify the simulations. The measured results of Θboard were all found to be close to 4°C/W and within reasonable range of simulations, considering experimental variations and uncontrollable factors.

Recommendations for using thermal vias

The simulation and experimental results show that thermal vias present an expected high thermal impedance, making them suitable only for low-power applications. We recommend the following for thermal-via array design:

1. Avoid placing vias under the MOSFET drain tab to prevent solder wicking through them.
2. While a via diameter of 0.3 mm with 1-mm center-to-center distance in the array is recommended, manufacturing capabilities can vary them.

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3. Thermal via with 35-µm copper plating achieves good thermal performance with limited cost escalation in fabrication.
4. Vias evenly distributed in all three directions contribute more to reducing thermal impedance and improving thermal performance compared with the larger 1-inch square array.
5. Heat spreading through thermal-via arrays is limited to 10 mm from the edges of the device. An array of at least five vias extending from each edge of the device is recommended, but more than 10 vias in each direction is not useful.

Embedded AlN Handles High-Power Requirements

For high-power applications, like electric vehicle (EV) on-board and off-board battery chargers, the use of thermal vias is impractical for dissipating heat because of the limited impact on thermal impedance. Because the IMS approach has also been ruled out for such applications — while single-sided PCB designs could have reliability issues because they require control signals to come from another PCB through connectors, the more exotic workarounds for multi-layer designs add to complexity and manufacturing costs — we examined the AlN approach.

AlN is a unique ceramic material in that it offers high thermal conductivity along with high electrical resistivity. However, it is not toxic like beryllium oxide (BeO) or difficult to produce like cubic boron nitride (c-BN),[5] the other ceramics that possess high thermal conductivity.

Like other ceramics, it offers additional benefits like rigidity, resistance to chemicals, and no water absorption. Regular multi-layer PCB design can be employed for complex circuitry with AlN, and it is already used today for HB LED,[6] laser, and high-current switch applications. However, no studies have reported its use in high-power applications.

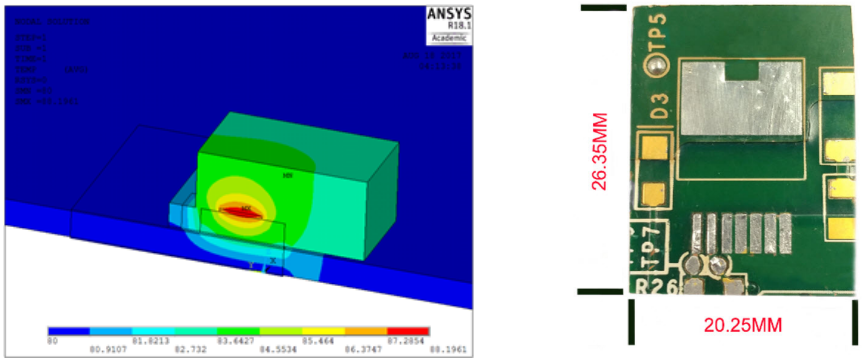

Figure 5: *The thermal simulation (left) of the PCB with embedded AlN shows heat transference to the bottom of the PCB without significant spread. The AlN block is under the landing pad of the power device in the prototype (right).*

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Simulating a PCB with AlN is similar to the modeling of the thermal-via PCBs earlier. The only difference is that embedded thermal conductive AlN blocks are placed between the top and bottom copper pads on PCBs. The AlN block chosen is 6.5 × 10.5 mm, with a thickness of 1.6 mm.

Thermal performance of embedded AlN-embedded PCB

The simulation shows no heat spread (***Figure 5***) and the heat being transferred directly to the bottom of the PCB. The simulation results show that the AlN block offers a thermal impedance of just 0.21oC/W. Verification by lab testing a prototype confirms the low thermal impedance at 0.23°C/W.

Compare this with the 4°C/W obtained for the PCB using thermal vias, and it becomes clear that embedded AlN blocks offer far superior thermal management for high-power applications.

Thermal management on a 6.6-kW charger

Because the embedded-AlN solution can be integrated with regular multi-layered PCBs, its high thermal conductivity and electrical isolation combine to allow an increase in power density much better than IMS solutions.

To demonstrate this capability beyond simulations in a real-world application, a 6.6-kW bidirectional EV on-board charger was designed using the AlN-embedded PCB technology.[7] It successfully provides good thermal management with peak system efficiency >96.5%.

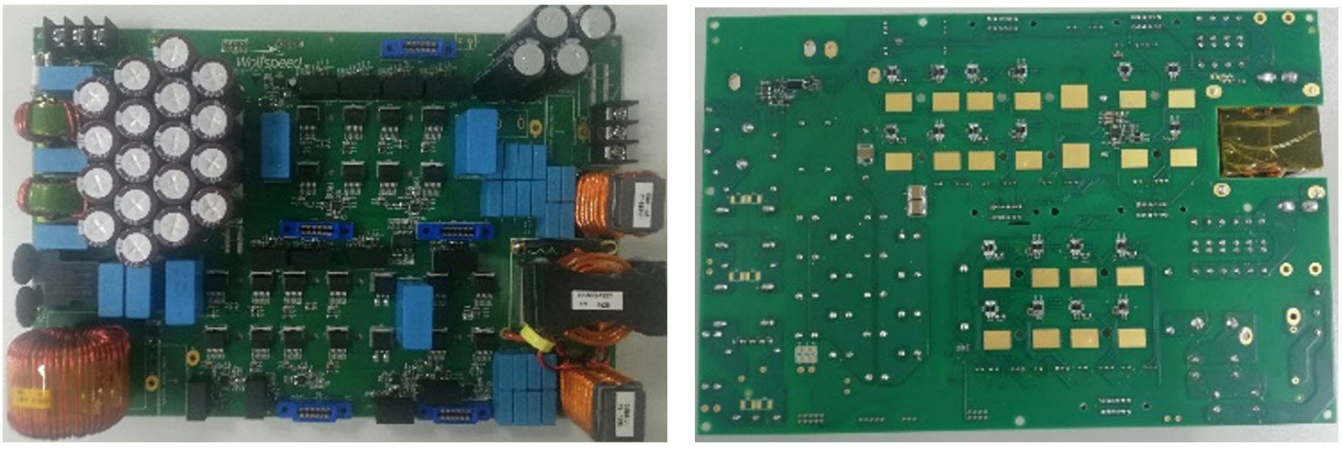

Figure 6: *A 6.6-kW EV on-board charger reference design using a surface-mount SiC MOSFET package on an embedded-AlN PCB*

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