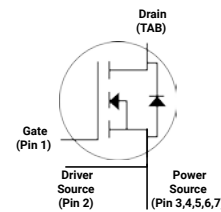


C3M0350120J

Silicon Carbide Power MOSFET C3M™ MOSFET Technology
N-Channel Enhancement Mode

Features

- 3rd generation Silicon Carbide (SiC) MOSFET technology
- Low impedance package with driver source pin
- 7mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant



Wolfspeed, Inc. is in the process of rebranding its products and related materials pursuant to the entity name change from Cree, Inc. to Wolfspeed, Inc. During this transition period, products received may be marked with either the Cree name and/or logo or the Wolfspeed name and/or logo.

Part Number	Package	Marking
C3M0350120J	TO 263-7	C3M0350120J

Typical Applications

- Renewable energy
- High voltage DC/DC converters
- Switch Mode Power Supplies
- UPS

Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1200	v	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			7.2	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 150^\circ\text{C}$	Fig. 19
				5		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 150^\circ\text{C}$	Note 2
Pulsed Drain Current	I_{DM}			20		t_{Pmax} limited by T_{Jmax} $V_{GS} = 15\text{V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			40.8	W	$T_c = 25^\circ\text{C}, T_J = 150^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-55 to +150	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design



Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6	V	$V_{DS} = V_{GS}, I_D = 1 \text{ mA}$	Fig. 11
		—	2.0	—		$V_{DS} = V_{GS}, I_D = 1 \text{ mA}, T_J = 150^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}	—	1	50	μA	$V_{DS} = 1200 \text{ V}, V_{GS} = 0 \text{ V}$	
Gate-Source Leakage Current	I_{GSS}	—	10	250	nA	$V_{GS} = 15 \text{ V}, V_{DS} = 0 \text{ V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$	—	350	455	m Ω	$V_{GS} = 15 \text{ V}, I_D = 3.6 \text{ A}$	Fig. 4, 5, 6
		—	525	—		$V_{GS} = 15 \text{ V}, I_D = 3.6 \text{ A}, T_J = 150^\circ\text{C}$	
Transconductance	g_{fs}	—	2.9	—	S	$V_{DS} = 20 \text{ V}, I_{DS} = 3.6 \text{ A}$	Fig. 7
		—	2.6	—		$V_{DS} = 20 \text{ V}, I_{DS} = 3.6 \text{ A}, T_J = 150^\circ\text{C}$	
Input Capacitance	C_{iss}	—	345	—	pF	$V_{GS} = 0 \text{ V}, V_{DS} = 1000 \text{ V}$ $f = 1 \text{ Mhz}$ $V_{AC} = 25 \text{ mV}$	Fig. 17, 18
Output Capacitance	C_{oss}	—	20	—			
Reverse Transfer Capacitance	C_{rss}	—	3.4	—			
Output Capacitance Stored Energy	E_{oss}	—	10.6	—	μJ	$V_{GS} = 0 \text{ V}, V_{DS} = 1000 \text{ V}$ $f = 1 \text{ Mhz}$ $V_{AC} = 25 \text{ mV}$	Fig. 16
Turn-On Switching Energy (Body Diode FWD)	E_{on}	—	46	—			
Turn Off Switching Energy (Body Diode FWD)	E_{off}	—	8	—	μJ	$V_{DS} = 800 \text{ V}, V_{GS} = -4 \text{ V}/15 \text{ V}, I_D = 3.6 \text{ A},$ $R_{G(ext)} = 2.5 \Omega, L = 716 \mu\text{H}$	Fig. 26, 29
Turn-On Delay Time	$t_{d(on)}$	—	6	—			
Rise Time	t_r	—	7	—	ns	$V_{DD} = 800 \text{ V}, V_{GS} = -4 \text{ V}/15 \text{ V}$ $I_D = 3.6 \text{ A}, R_{G(ext)} = 0 \Omega,$ Timing relative to V_{DS} Inductive load	Fig. 27, 28, 29
Turn-Off Delay Time	$t_{d(off)}$	—	9	—			
Fall Time	t_f	—	11	—			
Internal Gate Resistance	$R_{G(int)}$	—	7	—	Ω	$f = 1 \text{ MHz}, V_{AC} = 25 \text{ mV}$	
Gate to Source Charge	Q_{gs}	—	5.1	—	nC	$V_{DS} = 800 \text{ V}, V_{GS} = -4 \text{ V}/15 \text{ V}$ $I_D = 3.6 \text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—	4.6	—			
Total Gate Charge	Q_g	—	13	—			

Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	V_{SD}	4.5	—	V	$V_{GS} = -4 \text{ V}, I_{SD} = 1.8 \text{ A}$	Fig. 8, 9, 10
		4.0	—		$V_{GS} = -4 \text{ V}, I_{SD} = 1.8 \text{ A}, T_J = 150^\circ\text{C}$	
Continuous Diode Forward Current	I_S	—	7.3	A	$V_{GS} = -4 \text{ V}$	
Diode Pulse Current	$I_{S, pulsed}$	—	20		$V_{GS} = -4 \text{ V},$ pulse width t_p limited by T_{jmax}	
Reverse Recover Time	t_{rr}	5	—	nS	$V_{GS} = -4 \text{ V}, I_{SD} = 3.6 \text{ A}, V_R = 800 \text{ V}$ $di/dt = 3550 \text{ A}/\mu\text{s}, T_J = 150^\circ\text{C}$	Fig. 29
Reverse Recovery Charge	Q_{rr}	23	—	nC		
Peak Reverse Recovery Current	I_{rrm}	8	—	A		

Thermal Characteristics

Parameter	Symbol	Typ	Unit	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.9	$^\circ\text{C}/\text{W}$	Fig. 21



Typical Performance

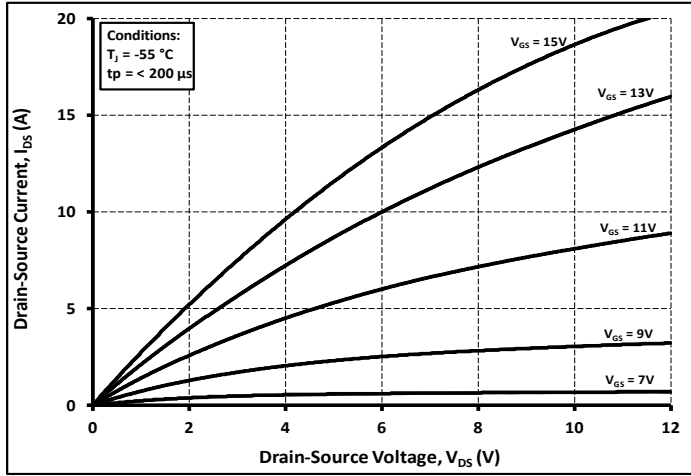


Figure 1. Output Characteristics $T_j = -55^\circ\text{C}$

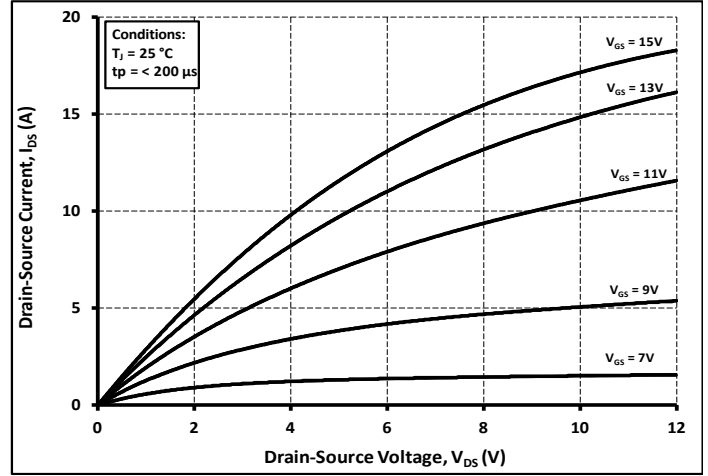


Figure 2. Output Characteristics $T_j = 25^\circ\text{C}$

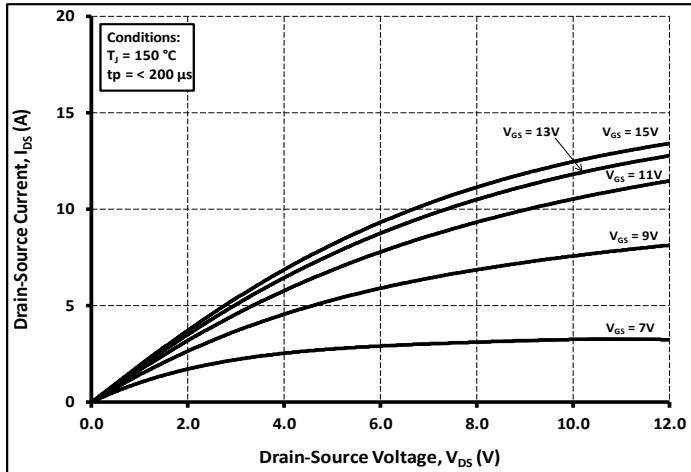


Figure 3. Output Characteristics $T_j = 150^\circ\text{C}$

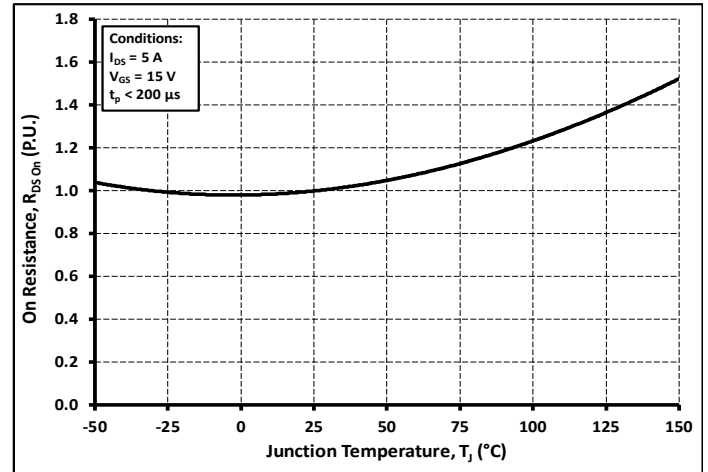


Figure 4. Normalized On-Resistance vs. Temperature

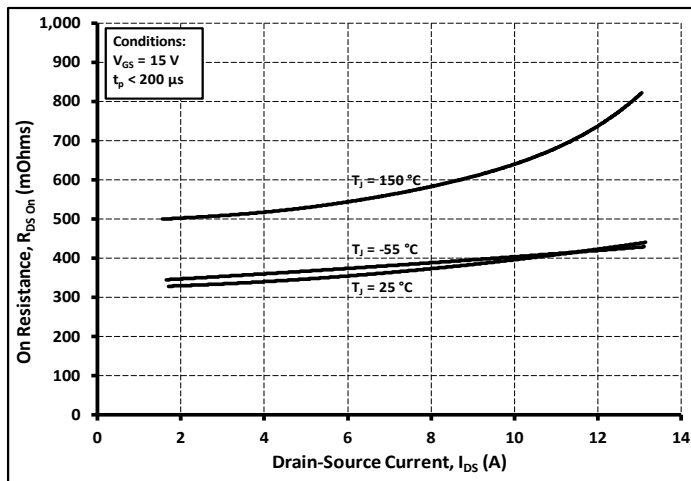


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

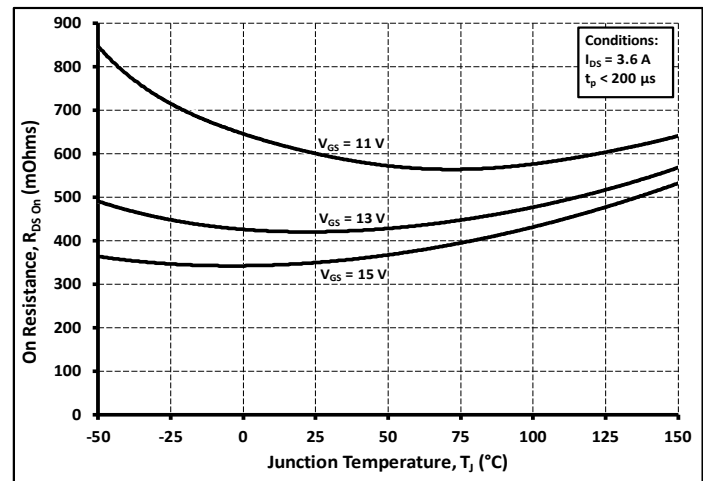


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

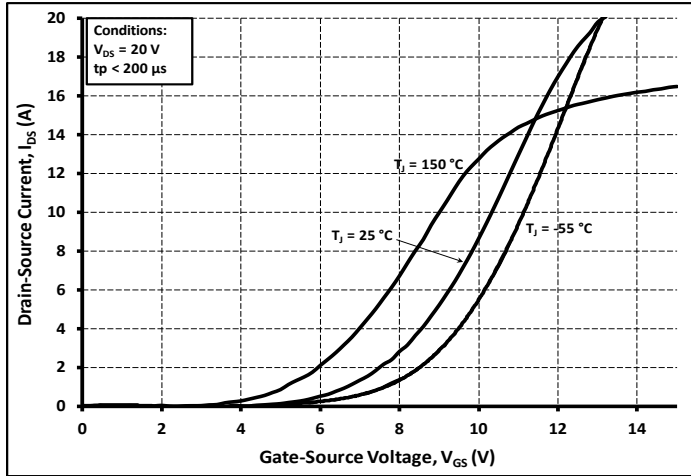


Figure 7. Transfer Characteristic for Various Junction Temperatures

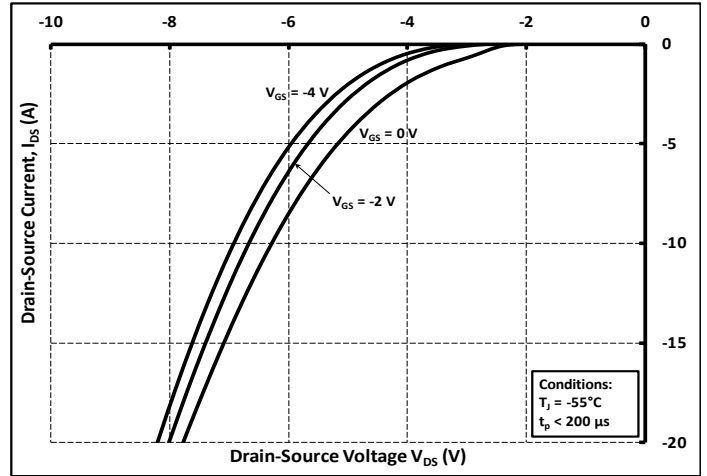


Figure 8. Body Diode Characteristic at -55°C

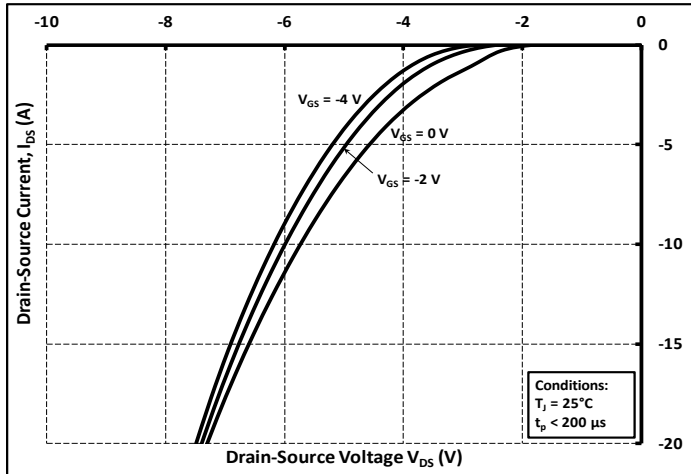


Figure 9. Body Diode Characteristic at 25°C

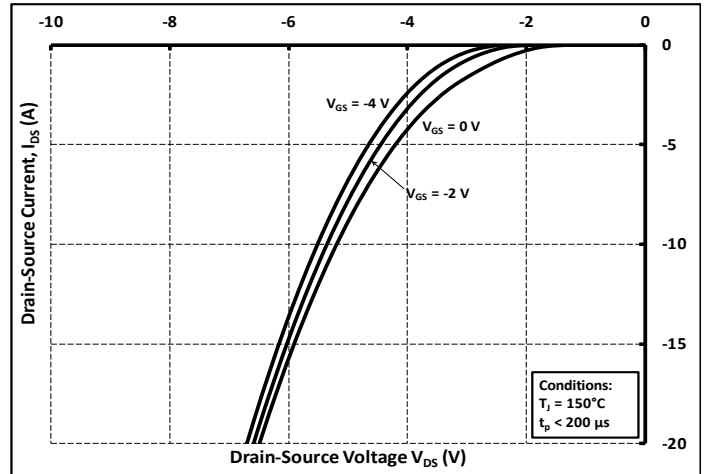


Figure 10. Body Diode Characteristic at 150°C

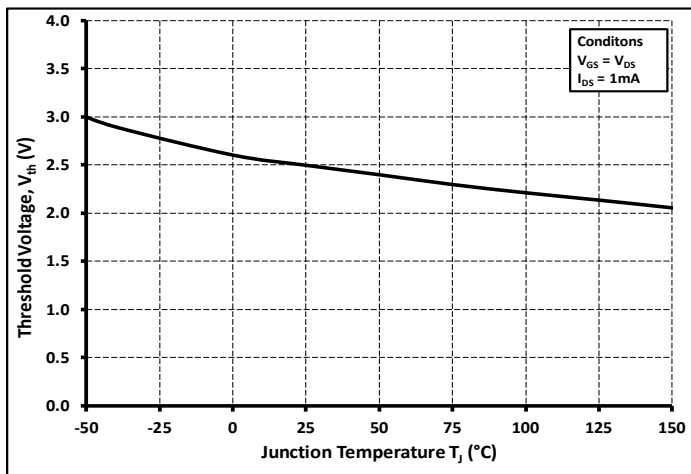


Figure 11. Threshold Voltage vs. Temperature

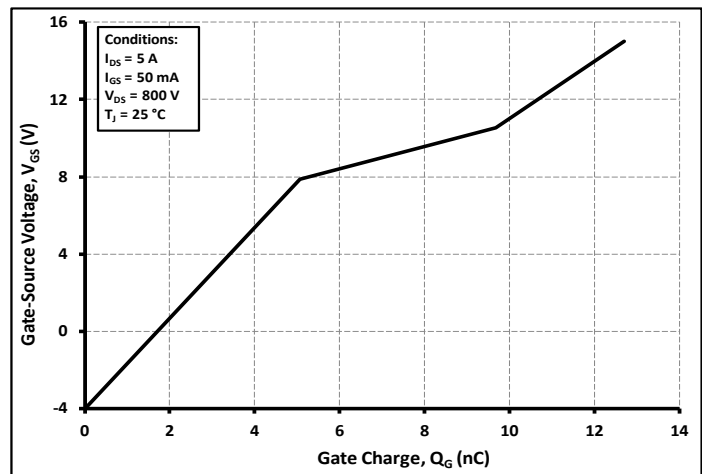


Figure 12. Gate Charge Characteristics



Typical Performance

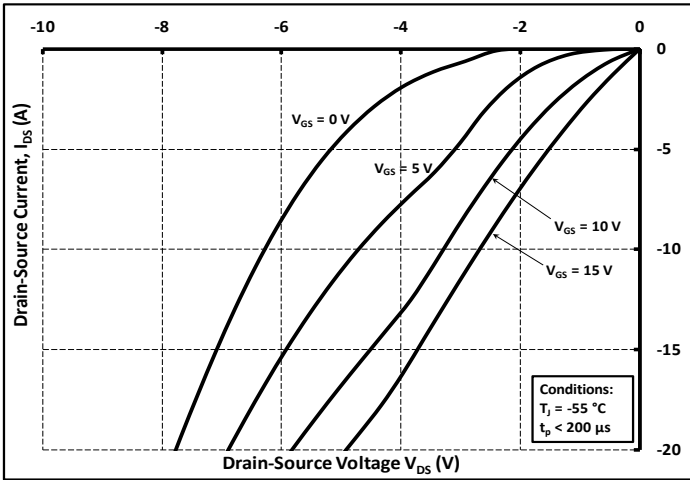


Figure 13. 3rd Quadrant Characteristic at -55°C

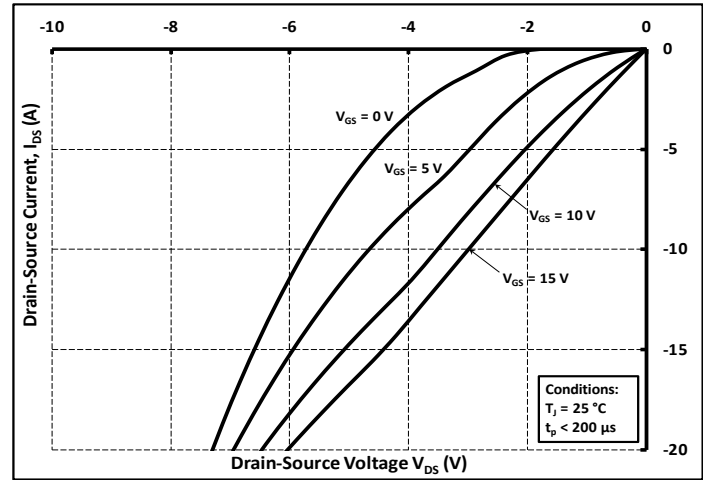


Figure 14. 3rd Quadrant Characteristic at 25°C

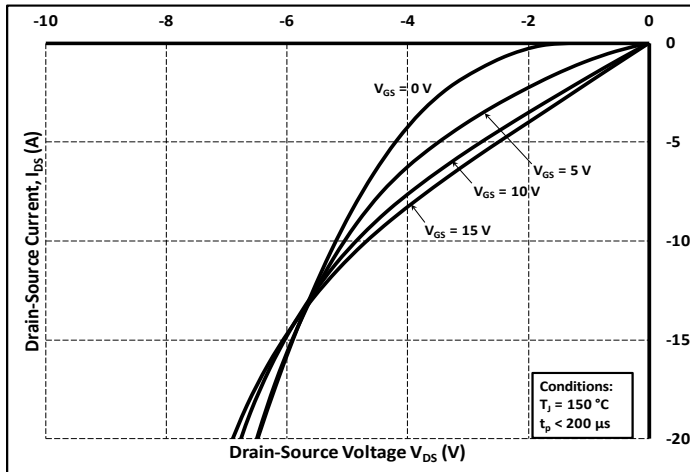


Figure 15. 3rd Quadrant Characteristic at 150°C

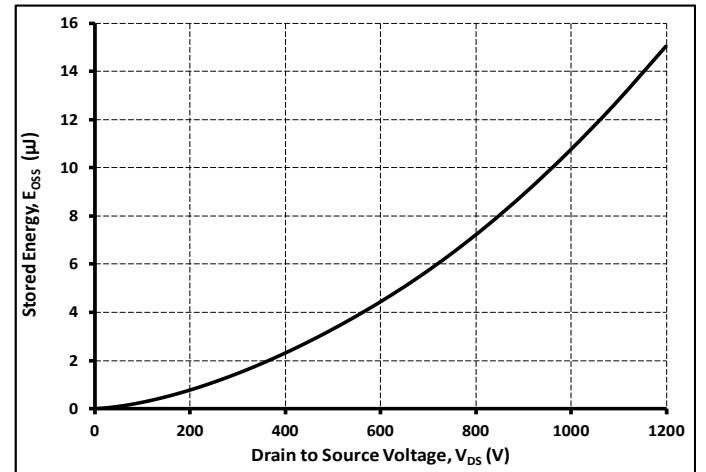


Figure 16. Output Capacitor Stored Energy

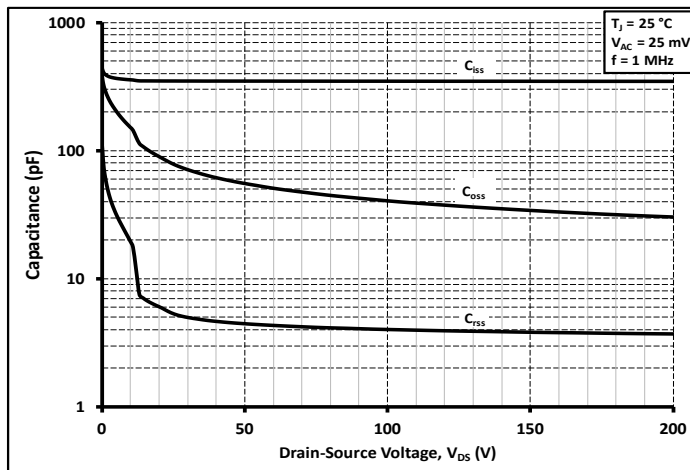


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

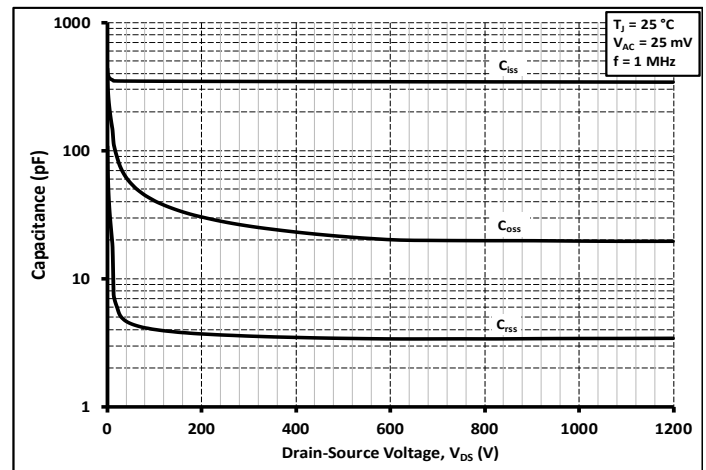


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1000 V)

Typical Performance

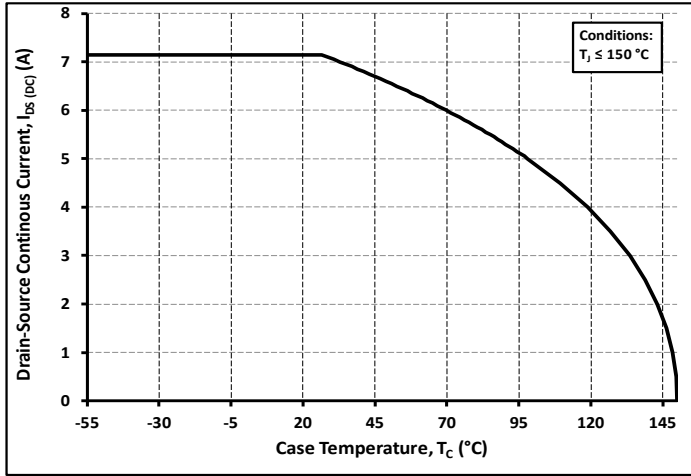


Figure 19. Continuous Drain Current Derating vs. Case Temperature

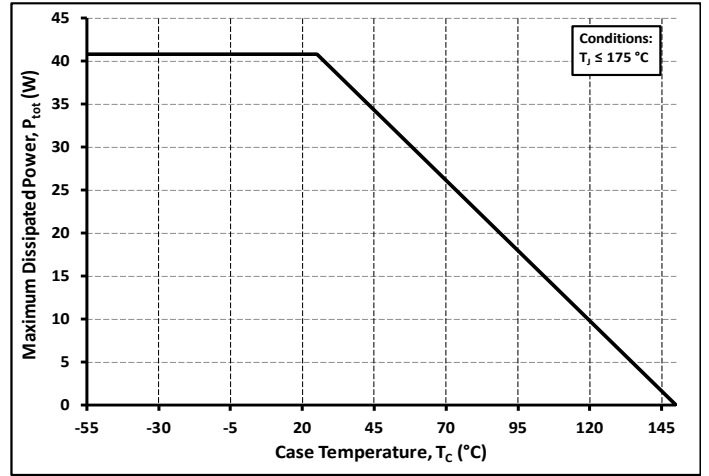


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

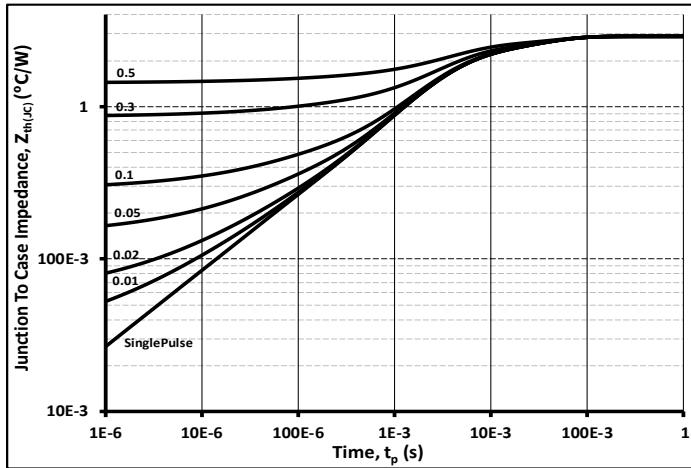


Figure 21. Transient Thermal Impedance (Junction - Case)

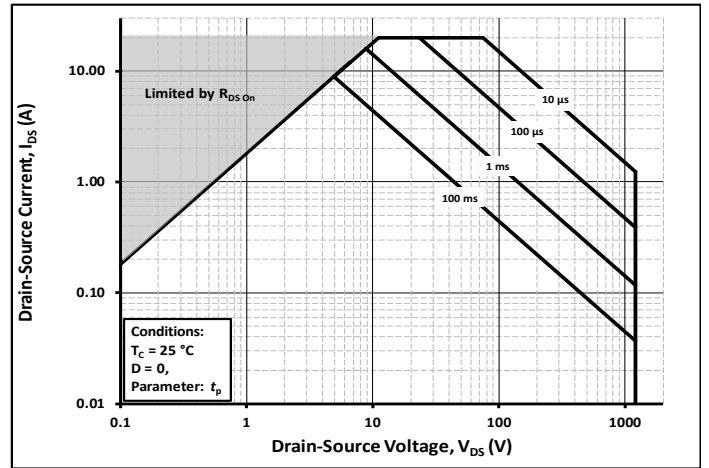


Figure 22. Safe Operating Area

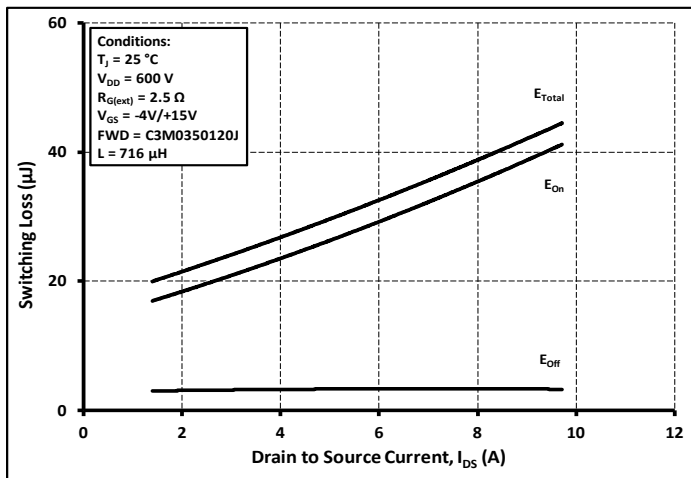


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 600\text{ V}$)

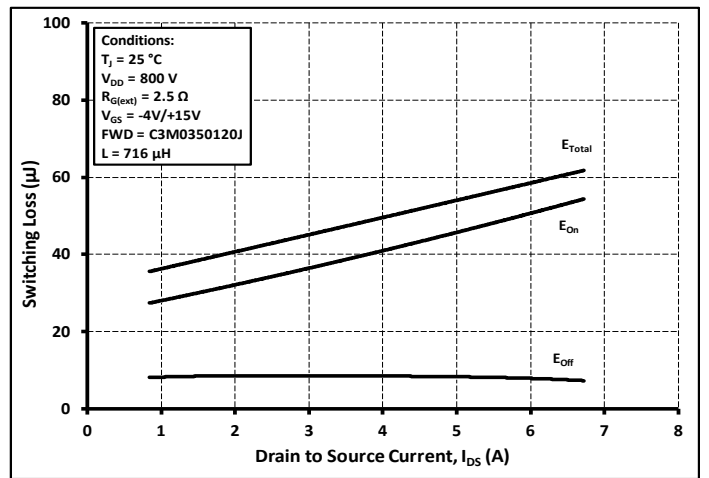


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 800\text{ V}$)



Typical Performance

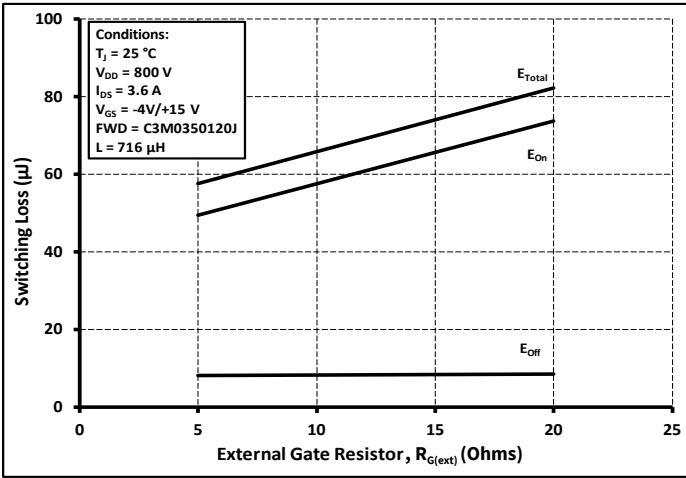


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

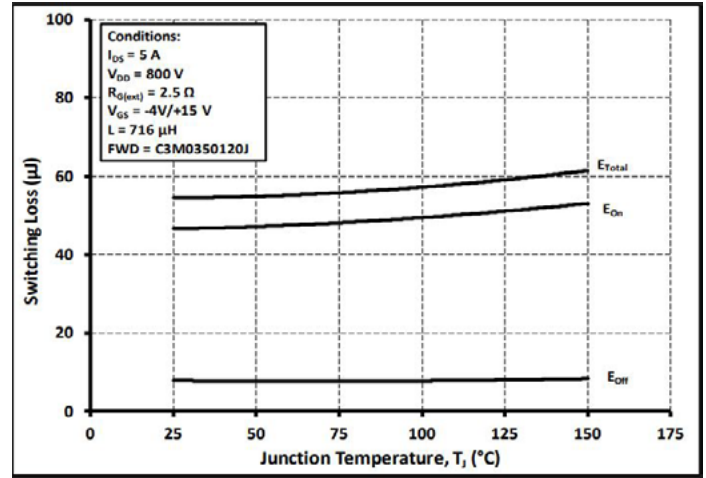


Figure 26. Clamped Inductive Switching Energy vs. Temperature

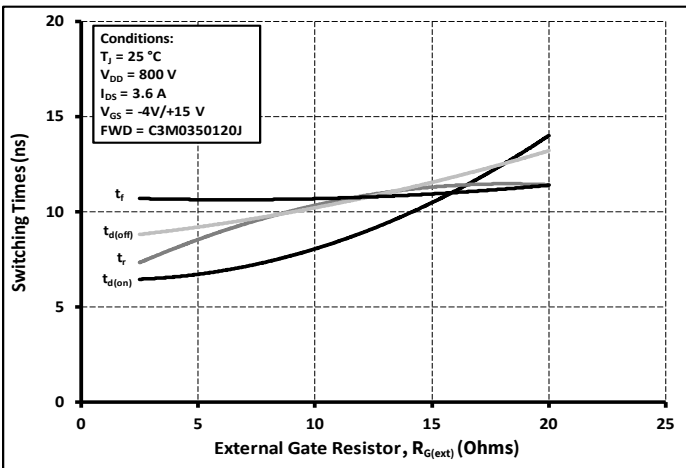


Figure 27. Switching Times vs. $R_{G(ext)}$

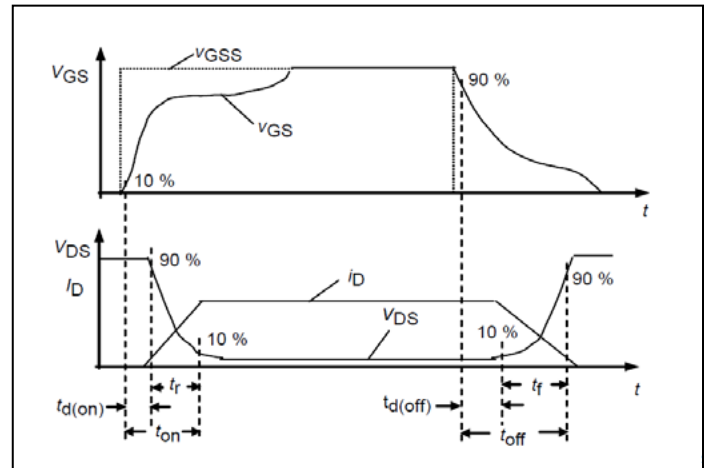


Figure 28. Switching Times Definition

Test Circuit Schematic

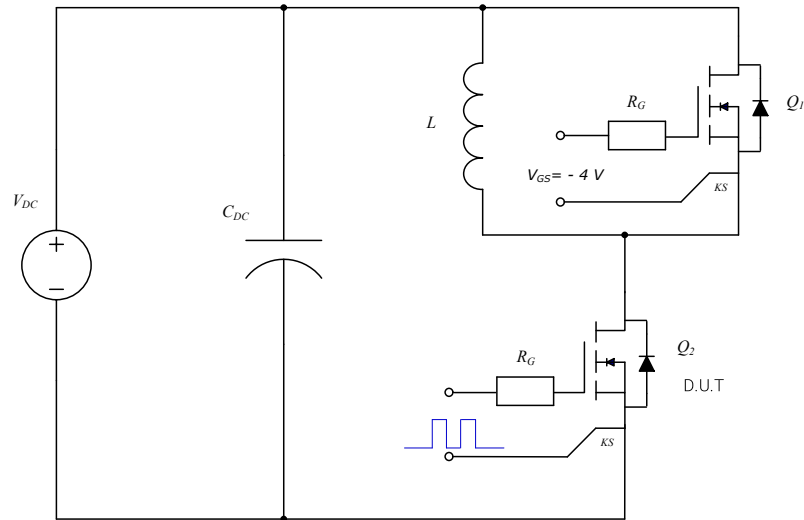


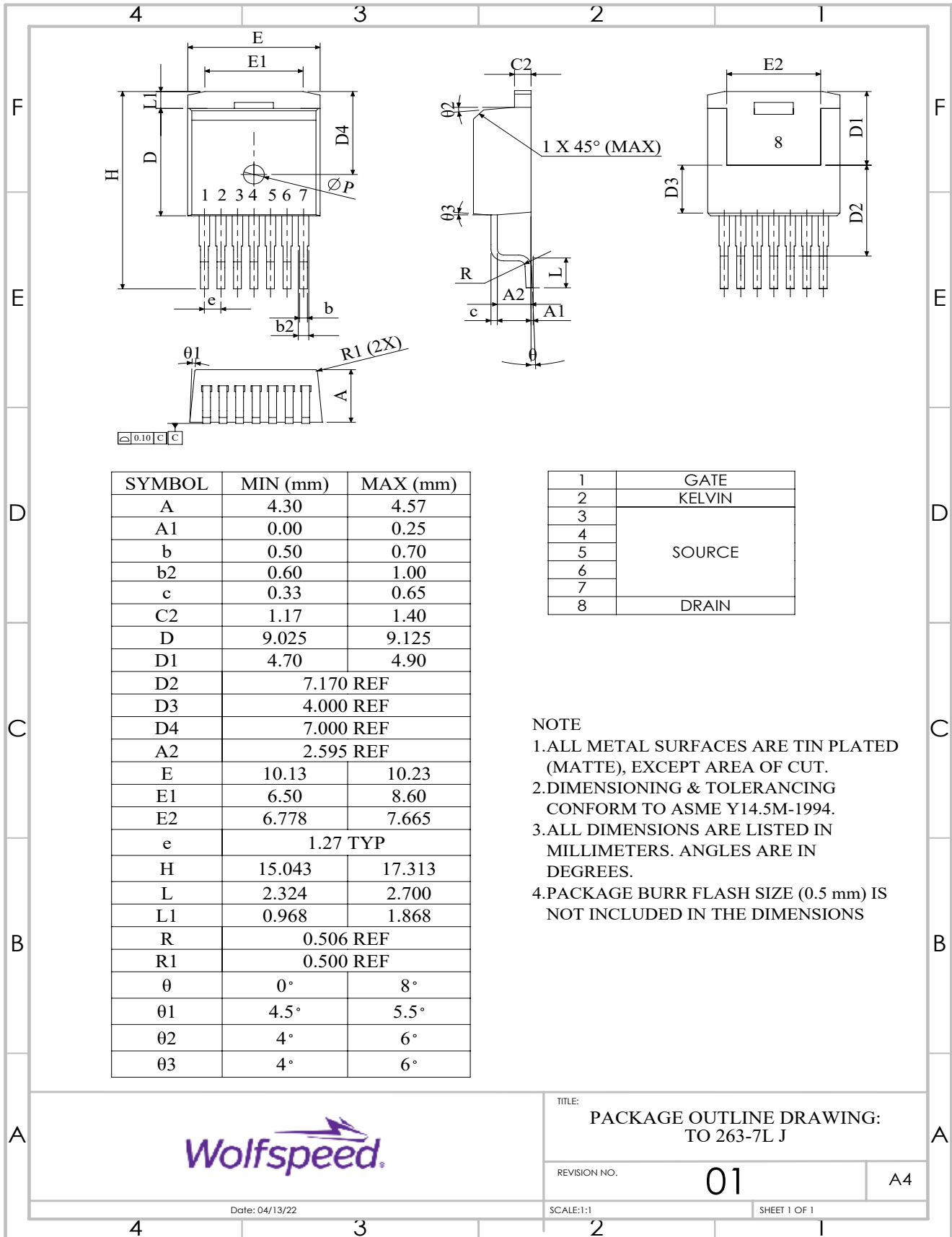
Figure 29. Clamped Inductive Switching Waveform Test Circuit

Note:

Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.



Package Dimensions – Package 7L D2PAK



NOTE
 1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
 2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
 3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
 4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS



TITLE:
**PACKAGE OUTLINE DRAWING:
 TO 263-7L J**

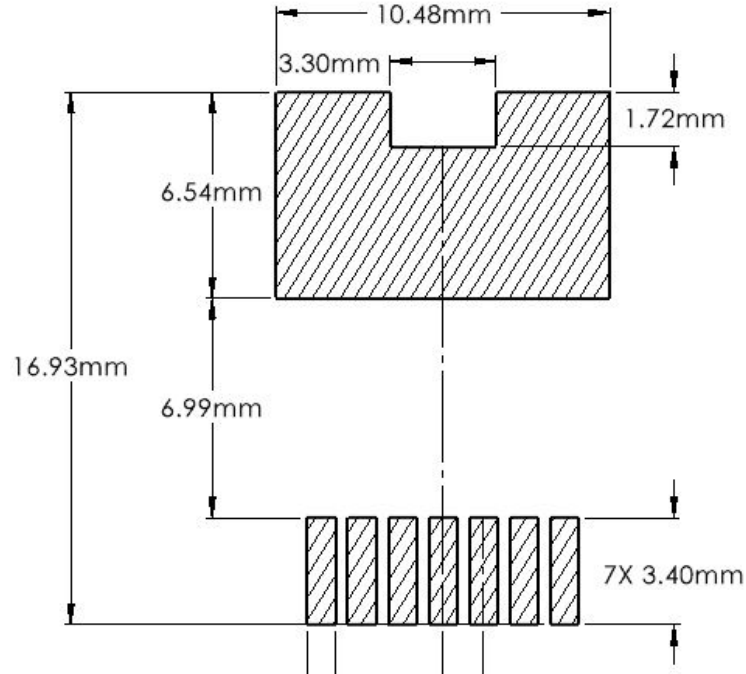
REVISION NO. **01** A4

SCALE: 1:1 SHEET 1 OF 1

Date: 04/13/22



Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
A	March-2020	N/A
2	January-2024	Updated Wolfspeed branding, package drawing, package image, solder pad layout, added Rev history, Table 1 layout revised
3	December - 2024	Legal Disclaimer Updated

Related Links

- [SiC MOSFET Isolated Gate Driver reference design](#)
- [SiC MOSFET Evaluation Board](#)



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